

# A DC-DC Boost Converter with a Wide Input Range and High Voltage Gain for Fuel Cell Vehicles

Yun Zhang, *Senior Member, IEEE*, Heyu Liu, Jing Li, *Member, IEEE*, Mark Sumner, *Senior Member, IEEE*, and Changliang Xia, *Senior Member, IEEE*

**Abstract**—In fuel cell vehicles, the output voltage of the fuel cell source is typically much lower than the voltage required by the DC bus and also this output voltage drops significantly as the output current increases. In order to match the output voltage of the fuel cell source to the DC bus voltage, a new DC-DC boost converter with a wide input range and high voltage gain is proposed to act as the required power interface, which reduces voltage stress across the power devices and operates with an acceptable conversion efficiency. A prototype rated at 300W/400V has been developed and the maximum efficiency of the proposed converter was measured as 95.01% at 300W. Experimental results are presented to validate the effectiveness of the proposed converter.

**Index Terms**—Boost DC-DC converter, Fuel cell Vehicles, High voltage-gain, Switched-capacitor, Wide input range.

## I. INTRODUCTION

As nonrenewable resources such as oil, gas and coal become scarce, more and more research is focused on the problem of high energy usage and society's dependence on fossil fuels [1]-[3]. Additionally, the number of automobiles continues to increase in most countries, causing a significant rise in air pollution. Vehicles powered by fuel cell sources may help to reduce transport's dependence on oil, and reduce polluting emissions [4]. The fuel cells can utilize hydrogen or natural gas, to achieve a high energy density and can potentially generate "clean" electricity with high efficiency. However, unlike batteries which have a fairly constant output voltage, the output voltage of fuel cells drops significantly with an increase of output current [5]-[7]. Hence, a step-up DC-DC converter with a wide range of voltage-gain is essential to interface between the low voltage fuel-cell source and the high voltage DC bus of the motor drive inverter. The conventional DC-DC Boost converter

is one of the most commonly used topologies for stepping up voltage. In theory, when the duty cycle approaches unity, the conventional boost converter can achieve a high voltage gain [8]. However, it is difficult to implement a high voltage gain (e.g. more than 6), due to the existence of parasitic elements (stray inductance, capacitance) and the extreme duty cycle required. In addition, the power semiconductors suffer from a high voltage stress - the DC bus voltage.

In order to obtain a DC-DC Boost converter with a high voltage gain and a low voltage stress, many different topologies have been proposed by researchers [9]. These converters can be divided into two types: isolated and non-isolated converters. Isolated converters are widely used in many applications, and an arbitrarily high voltage-gain can be theoretically achieved by increasing the turns ratio of the transformer employed [10]. However, there are many situations where galvanic isolation is unnecessary, and the snubber circuit required in an isolated topology will increase the complexity of the converter design [11]-[12]. Compared with isolated converters, the cost and magnetic losses of non-isolated converters are lower. A high voltage-gain can be achieved by introducing a coupled inductor to topology e.g. [13], and the converter can maintain a low device voltage stress. However a large number of inductors is required leading to an increased volume, a higher cost, and a reduced efficiency [14]. Non-coupled inductor based converters can also be used to obtain a high voltage-gain reducing the number of magnetic devices. The conventional quadratic DC-DC boost converter in [15] can obtain a high voltage-gain, but the voltage stress across the high side power semiconductors is as high as the output-voltage. To solve this problem, the switched-capacitor (SC) configurations introduced in [16], and [17] are able to obtain a high voltage gain, but they cannot achieve flexible voltage regulation unless they are combined with other DC-DC converters [18]. A topology called the "switched-capacitor-based active-network" (SC-ANC) is presented in [19]; the voltage stress across the power semiconductors can be reduced by half, and the voltages across the output capacitors can also balance themselves naturally. However, the power switches may see a large voltage spike as a result of the leakage inductance of the circuit. The switched-capacitor circuit was studied in [20]: it achieves flexible voltage regulation by combining it with other DC-DC converters, however the difference in potential between the ground points of the input voltage source side and the load side is a high frequency PWM voltage, because instead of a common ground structure, there is a diode located between the ground points of the input voltage source side and the load side. As a result, it may introduce issues associated with  $du/dt$  and these may limit its applications [21]-[22].

Manuscript received June 8, 2018; accepted July 17, 2018. This work was supported in part by the National Natural Science Foundation of China under Grants 51577130 and 51207104, and in part by the Research Program of Application Foundation and Advanced Technology of Tianjin China under Grant 15JCQNJC03900.

Y. Zhang, and H. Liu are with the School of Electrical and Information Engineering, Tianjin University, Nankai, Tianjin, China (e-mail: zhangy@tju.edu.cn; henry\_liu1994@163.com).

J. Li is with the Department of Electrical and Electronic Engineering, University of Nottingham Ningbo China, Ningbo, China (email: jing.li@nottingham.edu.cn).

C. Xia is with the School of Electrical and Information Engineering, Tianjin University, Tianjin 300072, China, and also with the Tianjin Engineering Center of Electric Machine System Design and Control, Tianjin Polytechnic University, Tianjin 300387, China (e-mail: motor@tju.edu.cn).

M. Sumner is with the Department of Electrical and Electronic Engineering, University of Nottingham, Nottingham, England, U.K (e-mail: mark.sumner@nottingham.ac.uk).

The Z source DC-DC Boost converter has the potential for a high voltage gain. A Z source DC-DC converter with a cascaded switched-capacitor has been presented in [23]. This topology can improve the voltage gain of the Z source DC-DC Boost converter by using the voltage multiplier function of the switched-capacitor. However, the drawbacks of the converter are obvious, such as the penalty of the discontinuous input current and the different ground points between the input voltage source side and the load side. Moreover, the power semiconductors will see a high voltage stress when the duty cycle approaches zero. In a similar way, switched-inductor (SL) techniques can also be used in dc-dc converters to achieve a high voltage gain as presented in [24], and [25], but they often need large numbers of inductors. Therefore, the volume and cost of these converters will be increased.

To address these issues, a new non-isolated high ratio step-up dc-dc converter is proposed in this paper, which has the following features:

- 1) It reduces the voltage stress across the power devices and has a common ground between the input and output sides.
- 2) The two power switches turn on and off simultaneously. As a result, the control of the converter is simple, and power switches with low on-state resistance can be employed.
- 3) The system operates with a high voltage gain and a wide input voltage range and does not use any extreme values for its duty cycle.

This paper is organized as follows: In Section II, the configuration and operating principles of the proposed converter are presented. The voltage gain is analyzed in Section III. In Section IV, the voltage and current stresses are calculated. The design of the components is presented in Section V and in Section VI, the dynamic modeling is established. Experimental results and analysis are presented in Section VII to validate the features of the proposed converter.

## II. OPERATING PRINCIPLES OF PROPOSED CONVERTER

### A. Configuration of the proposed converter

The high voltage gain DC-DC Boost converter is shown in Fig. 1. It comprises two active power switches ( $Q_1$  and  $Q_2$ ), five power diodes ( $D_3$ - $D_7$ ), two inductors ( $L_1$  and  $L_2$ ) and five capacitors ( $C_1$ - $C_5$ ). The fuel-cell source  $U_{in}$  and the inductor  $L_1$  are connected in series to charge capacitors  $C_1$  and  $C_2$  in parallel. Inductor  $L_2$  is another energy storage component which is used to realize a high voltage gain. The ladder type voltage multiplier (capacitors  $C_3$ - $C_5$  and diodes  $D_5$ - $D_7$ ) can improve the voltage-gain further and reduces the voltage stress across the power semiconductors on the high voltage side.

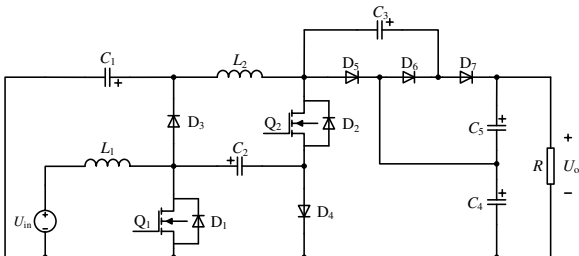


Fig. 1 Topology of proposed converter.

### B. Operating principles of the Proposed Converter

The gate signals of the two power switches ( $Q_1$ ,  $Q_2$ ) are identical -  $Q_1$  and  $Q_2$  are turned on and off simultaneously. Therefore, there are two switching states in each switching period, which are shown in Fig. 2.

**1) Switching state I.** As shown in Fig. 2(a),  $Q_1$  and  $Q_2$  turn on,  $L_1$  is charged by the DC source  $U_{in}$  (i.e.  $U_{in}$ - $L_1$ - $Q_1$ ), and  $L_2$  is charged by  $C_1$  and  $C_2$  in series (i.e.  $C_1$ - $L_2$ - $Q_2$ - $C_2$ - $Q_1$ ). Meanwhile,  $C_3$  is charged by  $C_2$  and  $C_4$  in series (i.e.  $C_4$ - $D_6$ - $C_3$ - $Q_2$ - $C_2$ - $Q_1$ ).

**2) Switching state II.** As shown in Fig. 2(b),  $Q_1$  and  $Q_2$  turn off,  $C_1$  and  $C_2$  are charged in parallel by the DC source and  $L_1$  (i.e.  $U_{in}$ - $L_1$ - $D_3$ - $C_1$ , and  $U_{in}$ - $L_1$ - $C_2$ - $D_4$ ). At the same time,  $C_4$  is charged by the DC source,  $L_1$ , and  $L_2$  in series (i.e.  $U_{in}$ - $L_1$ - $D_3$ - $L_2$ - $D_5$ - $C_4$ ). In addition,  $C_4$  and  $C_5$  are charged by the DC source,  $L_1$ ,  $L_2$ , and  $C_3$  (i.e.  $U_{in}$ - $L_1$ - $D_3$ - $L_2$ - $C_3$ - $D_7$ - $C_5$ - $C_4$ ), as well as through the load  $R$ . The output-voltage  $U_o$  is equal to the total voltages across  $C_4$  and  $C_5$ .

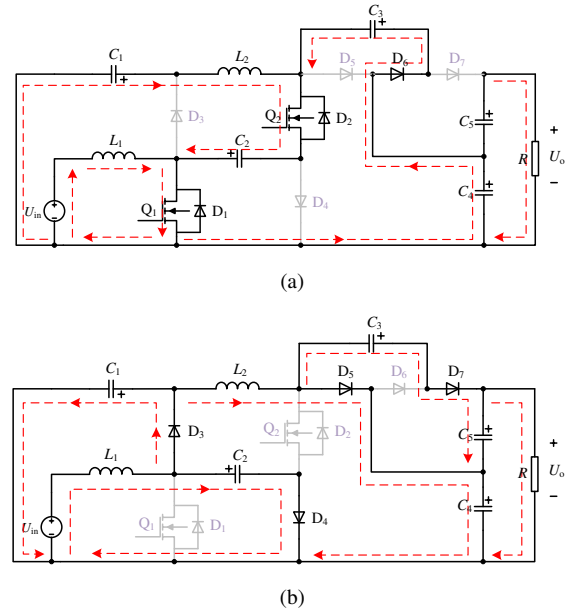


Fig. 2 Switching states of the proposed converter. (a) Switching state I. (b) Switching state II.

According to the key operating waveforms of the proposed converter shown in Fig. 3, the inductor currents  $i_{L1}$  and  $i_{L2}$  have the same energy transfer process. When  $S=1$ , power switches  $Q_1$ ,  $Q_2$  and diode  $D_6$  are turned on. The current  $i_{Q1}$  increases linearly while  $i_{Q2}$  and  $i_{D6}$  decreases linearly. The output capacitor current  $i_{C5}$  is negative which means  $C_5$  is discharged. When  $S=0$ , power switches  $Q_1$ ,  $Q_2$  and diode  $D_6$  are turned off. The currents  $i_{D5}$  and  $i_{C5}$  decrease linearly. The capacitor voltage fluctuations reflect the charging and discharging processes. It can be seen from the capacitor voltages  $U_{C2}$  and  $U_{C3}$  that capacitors  $C_2$  and  $C_3$  have the opposite charging and discharging states.

## III. STEADY-STATE VOLTAGE GAIN ANALYSIS

If the switching period for the power switches is  $T$ , then,  $dT$  is the on-state period, and  $(1-d)T$  is the off-state period, where  $d$  is the duty cycle of the power switches. It is assumed that the capacitor voltage and the inductor current are constant during

each switching period, and the forward voltage drop and the on-state resistance of the power semiconductors are ignored.

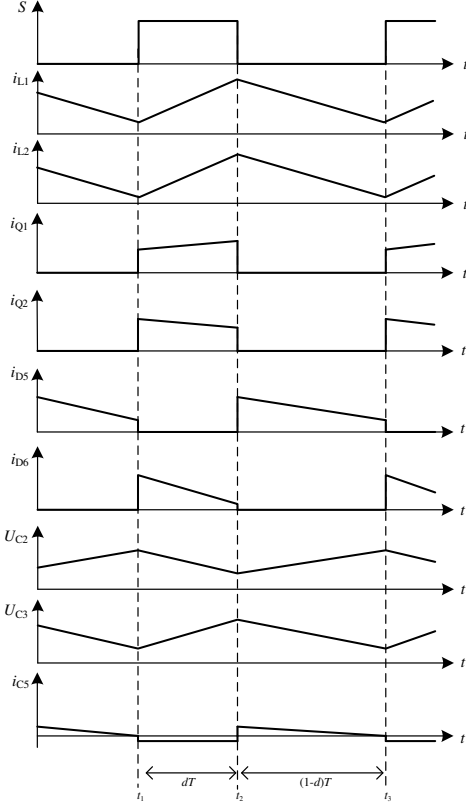


Fig. 3 Key operating waveforms of the proposed converter.

(1) can be derived according to the volt-second balance principle for inductors  $L_1$  and  $L_2$ :

$$\begin{cases} U_{in} \times dT + (U_{in} - U_{C2}) \times (1-d)T = 0 \\ (U_{C1} + U_{C2}) \times dT + (U_{C2} - U_{C4}) \times (1-d)T = 0 \end{cases} \quad (1)$$

The voltage relationship between the output and capacitor voltages can be found, in terms of the two switching states which are shown in Fig. 2:

$$\begin{cases} U_{C1} = U_{C2} \\ U_{C3} = U_{C5} = U_{C2} + U_{C4} \\ U_o = U_{C4} + U_{C5} \end{cases} \quad (2)$$

As a result, the output voltage  $U_o$  can be obtained from (1) and (2) as follows:

$$U_o = \frac{3+d}{(1-d)^2} U_{in} = M \times U_{in} \quad (3)$$

where  $M$  is the conversion ratio, i.e. the voltage gain. (3) shows that the proposed converter can theoretically obtain a high and wide voltage gain range. The voltage gain as a function of the duty cycle for the proposed converter has been compared to the converters in [23] and [26]-[28] and these are shown in Fig. 4. It can be concluded that the voltage gain of the proposed converter is higher than the converters in [26]-[28], especially when  $d > 0.2$ . Although the converter in [23] has a better voltage gain curve, the low conversion efficiency and the non-common ground will cause more power losses and increased  $du/dt$  issues, which will be analyzed in Table III. Considering the voltage

gain, the efficiency and the common ground together, the proposed converter in this paper has the advantages of a high and wide voltage gain range, an acceptable conversion efficiency, and a common ground.

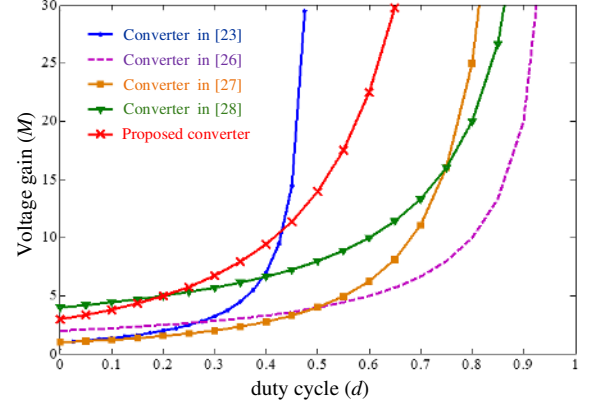


Fig. 4 Comparisons of voltage gain as a function of the duty cycle for different converter topologies.

#### IV. ANALYSIS OF COMPONENT ELECTRICAL STRESS

##### A. Voltage Stress Analysis

According to the analysis of each of the operation states in Fig. 2 and the voltage gain in (3), the voltage stresses across the power devices can be deduced as shown in Table I.

TABLE I  
Voltage stresses across the power devices.

Component	$Q_1$	$Q_2$	$D_3$	$D_4$
Voltage stress	$\frac{1-d}{3+d} U_o$	$\frac{1+d}{3+d} U_o$	$\frac{1-d}{3+d} U_o$	$\frac{1-d}{3+d} U_o$
Component	$D_5$	$D_6$	$D_7$	$C_1$
Voltage stress	$\frac{2}{3+d} U_o$	$\frac{2}{3+d} U_o$	$\frac{2}{3+d} U_o$	$\frac{1-d}{3+d} U_o$
Component	$C_2$	$C_3$	$C_4$	$C_5$
Voltage stress	$\frac{1-d}{3+d} U_o$	$\frac{2}{3+d} U_o$	$\frac{1+d}{3+d} U_o$	$\frac{2}{3+d} U_o$

Therefore, the voltage stresses across the active power switches  $Q_1$  and  $Q_2$  are less than half of the output voltage  $U_o$ . For diodes  $D_3$  and  $D_4$ , the voltage stresses are less than one third of  $U_o$ , whilst the voltage stresses across  $D_5$ - $D_7$  are less than two thirds of  $U_o$ , as well as the voltage stresses across capacitors  $C_1$ - $C_5$ . The voltage stresses across  $C_1$  and  $C_2$  are less than one third of  $U_o$ . The voltage stress across  $C_4$  is less than half of the output high voltage  $U_o$ , whilst the voltage stresses across  $C_3$  and  $C_5$  are less than two thirds of  $U_o$ .

##### B. Current Stress Analysis

Using the current analysis in Fig. 2 and Kirchhoff's current laws (KCL), the current stresses across the power devices can also be obtained as shown in Table II.

The current stresses across the power devices are related to the operating duty cycle  $d$  (usually between 0.2 and 0.4). For instance, the maximum current stress across active power switch  $Q_2$  is  $7.5I_o$ . Therefore, it can be used as a reference in the component parameters design section. Note also that the current

stresses across  $Q_1$ - $D_7$  are mean values, the current stresses across capacitors  $C_1$ - $C_5$  are root mean square values.

TABLE II  
Current stresses across the power devices.

Component	$Q_1$	$Q_2$	$D_3$	$D_4$
Current stress	$\frac{1+3d-d^2-d^3}{d(1-d)^2} I_o$	$\frac{1+d}{d(1-d)} I_o$	$\frac{2}{(1-d)^2} I_o$	$\frac{1+d}{(1-d)^2} I_o$
Component	$D_5$	$D_6$	$D_7$	$C_1$
Current stress	$\frac{1}{1-d} I_o$	$\frac{1}{d} I_o$	$\frac{1}{1-d} I_o$	$\frac{\sqrt{4d-4d^2}}{(1-d)^2} I_o$
Component	$C_2$	$C_3$	$C_4$	$C_5$
Current stress	$\frac{1+d}{\sqrt{d(1-d)^3}} I_o$	$\frac{1}{\sqrt{d(1-d)}} I_o$	$\frac{1+d}{\sqrt{d(1-d)}} I_o$	$\sqrt{\frac{d}{1-d}} I_o$

The comparison of the proposed converter with other existing high voltage gain DC-DC Boost converters is shown in Table III. It can be seen that the proposed converter achieves a high and wide voltage gain range by increasing the number of diodes by a small amount. The converter in [23] can achieve a high voltage gain when the duty cycle approaches 0.5, but the converter will suffer from a high voltage stress which is almost equal to the output voltage when the duty cycle  $d$  is close to zero. In addition, the converter in [23] has a poor efficiency compared to the other converters. Compared with the converters in [26] and [27], the proposed converter is more suitable for applications requiring a large step-up ratio. Considering the selection of the power switches, the converter in [27] will have its maximum device voltage stress (which is higher than half of the output voltage) when  $d \neq 0.5$ , whereas the maximum voltage stress across the power switches is less than half of the output voltage in the proposed converter. Considering the selection of the diodes, the maximum voltage stress across the diodes for the proposed converter is lower than that of the converters in [26] and [27]. Although the converter in [28] has the advantage of the lower

voltage stress, it does not have a common ground between the input and the output sides and this may cause additional  $du/dt$  issues.

## V. COMPONENT PARAMETERS DESIGN

### A. Design of the power switches and diodes

The design of the power switches and diodes should refer to the most severe conditions that the semiconductor devices will operate in. Assuming that the maximum required voltage gain is 10 and the load power is 400W, the duty cycle  $d$  and the output current  $I_o$  can be obtained as follows:

$$\begin{cases} d = 0.42 \\ U_o = 400V \\ I_o = 1A \end{cases} \quad (4)$$

It can be deduced from Table I and Table II that the maximum mean voltage stresses across  $Q_1$  and  $Q_2$  are 70V and 166V respectively, and the maximum mean current stresses on  $Q_1$  and  $Q_2$  are 16.5A and 6.2A respectively. Similarly, it can be derived from Table I and Table II that the maximum mean voltage stress across  $D_3$  and  $D_4$  is 70V, which is equal to that of  $Q_1$ . In addition, the maximum mean current stress on  $D_3$  and  $D_4$  is 5.8A, and the maximum mean voltage and current stresses on  $D_5$ - $D_7$  are 234V and 1.9A, respectively.

### B. Design of the inductors and capacitors

Assuming that the maximum required current ripple in the inductors is  $\Delta I_L$ , the inductances can be calculated when  $L$  is in the charging state as given in (5):

$$L = u_L \frac{dt}{di_L} \quad (5)$$

where  $di_L = \Delta I_L$ ,  $dt = d \times T = d/f_s$  ( $f_s$  is the switching frequency). The inductances of  $L_1$  and  $L_2$  can be derived as (6):

TABLE III  
Comparisons among the proposed converter and other high voltage gain converters.

Topology	Converter in [23]	Converter in [26]	Converter in [27]	Converter in [28]	Proposed converter
Number of power switches	1	1	2	2	2
Number of diodes	3	2	2	4	5
Number of inductors	3	2	2	2	2
Number of capacitors	5	3	2	4	5
Voltage-gain	$(1+d)/(1-2d)$	$2/(1-d)$	$1/(1-d)^2$	$4/(1-d)$	$(3+d)/(1-d)^2$
Maximum voltage stress across power switches	$U_o/(1+d)$	$U_o$	$dU_o$ or $(1-d)U_o$	$U_o/4$	$(1+d)U_o/(3+d)$
Maximum voltage stress across diodes	$U_o/(1+d)$	$U_o$	$U_o$	$U_o/2$	$2U_o/(3+d)$
Common ground	No	Yes	Yes	No	Yes
Conversion efficiency	50.2%~80.4%	88%~95%	88%~93%	94.32%~96.05%	90.06%~95.01%

$$\begin{cases} L_1 = \frac{d \times U_{in}}{\Delta I_{L1} \times f_s} \\ L_2 = \frac{4d \times U_{in}}{(1-d)^2 \times \Delta I_{L2} \times f_s} \end{cases} \quad (6)$$

If it is assumed that the maximum acceptable voltage ripple across the capacitor is  $\Delta U_C$ , the capacitances of the five capacitors in the proposed converter can be calculated as (7):

$$C = i_c \frac{dt}{du_c} \quad (7)$$

where  $dt=d \times T=df_s$ ,  $i_c$  is the corresponding current flowing through the capacitor,  $C$  is the capacitance, and  $du_c = \Delta U_C$ . The capacitances of the five capacitors can be calculated as (8):

$$\begin{cases} C_1 = \frac{2d \times I_o}{(1-d) \times \Delta U_{C1} \times f_s} \\ C_2 = \frac{(1+d) \times I_o}{(1-d) \times \Delta U_{C2} \times f_s} \\ C_3 = \frac{I_o}{\Delta U_{C3} \times f_s} \\ C_4 = \frac{(1+d) \times I_o}{\Delta U_{C4} \times f_s} \\ C_5 = \frac{d \times I_o}{\Delta U_{C5} \times f_s} \end{cases} \quad (8)$$

## VI. DYNAMIC MODELING

It is assumed that the power semiconductors, inductors, and capacitors are analyzed for operation under ideal conditions. The average model and the small-signal model can be obtained by using the state-space averaging method [29]-[31]. The capacitances are set such that  $C_1=C_2=C_3=C_4=C_5=C$  to simplify the analysis. The inductances are defined as  $L_1$  and  $L_2$ , the load resistance is  $R$ , and  $u_{in}(t)$ ,  $u_c(t)$  and  $d$  are the input variable, the output variable and the control variable, respectively.  $i_{L1}(t)$ ,  $i_{L2}(t)$ ,  $u_{C1}(t)$ ,  $u_{C2}(t)$ ,  $u_{C3}(t)$ ,  $u_{C4}(t)$ , and  $u_{C5}(t)$  are the state variables. According to Fig. 2(a),  $C_2$ ,  $C_3$  and  $C_4$  are connected in series in the loop circuit when  $Q_1$  and  $Q_2$  turn on. It means the sum of voltages across  $C_2$ ,  $C_3$  and  $C_4$  is 0. There is an invalid state variable ( $u_{C2}(t)+u_{C3}(t)+u_{C4}(t)=0$ , i.e. there are only two independent variables) in this loop circuit. By including the equivalent series resistance (e.g.  $r_1=r=0.1\Omega$ ) in the same loop circuit, the coupling between  $C_2$ ,  $C_3$  and  $C_4$  can be removed to avoid the invalid state variable. Similarly, as shown in Fig. 2(b),  $C_1$  and  $C_2$  are connected in parallel when  $Q_1$  and  $Q_2$  turn off, and this means the voltages across  $C_1$  and  $C_2$  should be equal, i.e. there is another invalid state variable. The coupling relationship between  $C_1$  and  $C_2$  can also be removed to avoid the invalid state variable ( $u_{C1}(t)+u_{C2}(t)=0$ ), by including the equivalent series resistance (e.g.  $r_2=r=0.1\Omega$ ) in the loop circuits.

When  $S=1$ , the on-state period is  $d \times T$ , and the state space

average model can be obtained as (9):

$$\begin{bmatrix} \frac{di_{L1}(t)}{dt} \\ \frac{di_{L2}(t)}{dt} \\ \frac{du_{C1}(t)}{dt} \\ \frac{du_{C2}(t)}{dt} \\ \frac{du_{C3}(t)}{dt} \\ \frac{du_{C4}(t)}{dt} \\ \frac{du_{C5}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{r}{L_2} & \frac{1}{L_2} & \frac{1}{L_2} & 0 & 0 & 0 \\ 0 & -\frac{1}{C} & 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{C} & 0 & -\frac{1}{Cr} & \frac{1}{Cr} & -\frac{1}{Cr} & 0 \\ 0 & 0 & 0 & \frac{1}{Cr} & -\frac{1}{Cr} & \frac{1}{Cr} & 0 \\ 0 & 0 & 0 & -\frac{1}{Cr} & \frac{1}{Cr} & -\frac{R+r}{CR} & -\frac{1}{CR} \\ 0 & 0 & 0 & 0 & 0 & -\frac{1}{CR} & -\frac{1}{CR} \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ u_{C1}(t) \\ u_{C2}(t) \\ u_{C3}(t) \\ u_{C4}(t) \\ u_{C5}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} u_m(t) \quad (9)$$

$$u_e(t) = [0 \ 0 \ 0 \ 0 \ 0 \ 1 \ 1][i_{L1}(t) \ i_{L2}(t) \ u_{C1}(t) \ u_{C2}(t) \ u_{C3}(t) \ u_{C4}(t) \ u_{C5}(t)]^T$$

When  $S=0$ , the off-state period is  $(1-d) \times T$ , and the state space average model can be written as (10):

$$\begin{bmatrix} \frac{di_{L1}(t)}{dt} \\ \frac{di_{L2}(t)}{dt} \\ \frac{du_{C1}(t)}{dt} \\ \frac{du_{C2}(t)}{dt} \\ \frac{du_{C3}(t)}{dt} \\ \frac{du_{C4}(t)}{dt} \\ \frac{du_{C5}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & -\frac{1}{L_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_2} & 0 & -\frac{1}{L_2} & 0 \\ 0 & 0 & -\frac{1}{Cr} & \frac{1}{Cr} & 0 & 0 & 0 \\ \frac{1}{C} & -\frac{1}{C} & \frac{1}{Cr} & -\frac{1}{Cr} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{1}{Cr} & 0 & \frac{1}{Cr} \\ 0 & \frac{1}{C} & 0 & 0 & 0 & -\frac{1}{CR} & -\frac{1}{CR} \\ 0 & 0 & 0 & 0 & \frac{1}{Cr} & \frac{1}{CR} & -\frac{R+r}{CR} \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ u_{C1}(t) \\ u_{C2}(t) \\ u_{C3}(t) \\ u_{C4}(t) \\ u_{C5}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} u_m(t) \quad (10)$$

$$u_e(t) = [0 \ 0 \ 0 \ 0 \ 0 \ 1 \ 1][i_{L1}(t) \ i_{L2}(t) \ u_{C1}(t) \ u_{C2}(t) \ u_{C3}(t) \ u_{C4}(t) \ u_{C5}(t)]^T$$

Combining (9) with (10), the average model of the converter can be obtained as (11):

$$\begin{bmatrix} \frac{di_{L1}(t)}{dt} \\ \frac{di_{L2}(t)}{dt} \\ \frac{du_{C1}(t)}{dt} \\ \frac{du_{C2}(t)}{dt} \\ \frac{du_{C3}(t)}{dt} \\ \frac{du_{C4}(t)}{dt} \\ \frac{du_{C5}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \frac{d-1}{L_1} & 0 & 0 & 0 \\ 0 & -\frac{rd}{L_2} & \frac{d}{L_2} & \frac{1}{L_2} & 0 & \frac{d-1}{L_2} & 0 \\ 0 & -\frac{d}{C} & \frac{d-1}{Cr} & \frac{1-d}{Cr} & 0 & 0 & 0 \\ \frac{1-d}{C} & -\frac{1}{C} & \frac{1-d}{Cr} & -\frac{1}{Cr} & \frac{d}{Cr} & -\frac{d}{Cr} & 0 \\ 0 & 0 & 0 & \frac{d}{Cr} & -\frac{1}{Cr} & \frac{d}{Cr} & \frac{1-d}{Cr} \\ 0 & \frac{1-d}{C} & 0 & -\frac{d}{Cr} & \frac{d}{Cr} & [-\frac{1}{CR} - \frac{d}{Cr}] & -\frac{1}{CR} \\ 0 & 0 & 0 & 0 & \frac{1-d}{Cr} & -\frac{1}{CR} & [-\frac{d}{Cr} - \frac{R+r}{CR}] \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ u_{C1}(t) \\ u_{C2}(t) \\ u_{C3}(t) \\ u_{C4}(t) \\ u_{C5}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} u_m(t) \quad (11)$$

$$u_e(t) = [0 \ 0 \ 0 \ 0 \ 0 \ 1 \ 1][i_{L1}(t) \ i_{L2}(t) \ u_{C1}(t) \ u_{C2}(t) \ u_{C3}(t) \ u_{C4}(t) \ u_{C5}(t)]^T$$

The state variables, the input variable, the output variable and the control variable can be described by the small-signal disturbance variables as (12):

$$\begin{cases} \hat{i}_{L1}(t) = I_{L1} + \hat{i}_{L1}(t) \\ \hat{i}_{L2}(t) = I_{L2} + \hat{i}_{L2}(t) \\ \hat{u}_{C1}(t) = U_{C1} + \hat{u}_{C1}(t) \\ \hat{u}_{C2}(t) = U_{C2} + \hat{u}_{C2}(t) \\ \hat{u}_{C3}(t) = U_{C3} + \hat{u}_{C3}(t) \\ \hat{u}_{C4}(t) = U_{C4} + \hat{u}_{C4}(t) \\ \hat{u}_{C5}(t) = U_{C5} + \hat{u}_{C5}(t) \\ \hat{u}_{in}(t) = U_{in} + \hat{u}_{in}(t) \\ \hat{u}_o(t) = U_o + \hat{u}_o(t) \\ \hat{d} = D + \hat{d} \end{cases} \quad (12)$$

where  $I_{L1}$ ,  $I_{L2}$ ,  $U_{C1}$ ,  $U_{C2}$ ,  $U_{C3}$ ,  $U_{C4}$ ,  $U_{C5}$ ,  $U_{in}$ ,  $U_o$  and  $D$  are the steady state components, and  $\hat{i}_{L1}(t)$ ,  $\hat{i}_{L2}(t)$ ,  $\hat{u}_{C1}(t)$ ,  $\hat{u}_{C2}(t)$ ,  $\hat{u}_{C3}(t)$ ,  $\hat{u}_{C4}(t)$ ,  $\hat{u}_{C5}(t)$ ,  $\hat{u}_{in}(t)$ ,  $\hat{u}_o(t)$  and  $\hat{d}$  are the corresponding small-signal disturbance variables. Therefore, from (11) and (12), the small-signal model of the converter can

be written as (13):

$$\begin{aligned}
 & \begin{bmatrix} \frac{d\hat{i}_{L1}(t)}{dt} \\ \frac{d\hat{i}_{L2}(t)}{dt} \\ \frac{d\hat{u}_{C1}(t)}{dt} \\ \frac{d\hat{u}_{C2}(t)}{dt} \\ \frac{d\hat{u}_{C3}(t)}{dt} \\ \frac{d\hat{u}_{Cs}(t)}{dt} \\ \frac{d\hat{u}_{Cs}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \frac{d-1}{L_1} & 0 & 0 & 0 \\ 0 & -\frac{rd}{L_2} & \frac{d}{L_2} & \frac{1}{L_2} & 0 & \frac{d-1}{L_2} & 0 \\ 0 & -\frac{d}{C} & \frac{d-1}{Cr} & \frac{1-d}{Cr} & 0 & 0 & 0 \\ \frac{1-d}{C} & -\frac{1}{C} & \frac{1-d}{Cr} & -\frac{1}{Cr} & \frac{d}{Cr} & -\frac{d}{Cr} & 0 \\ 0 & 0 & 0 & \frac{d}{Cr} & -\frac{1}{Cr} & \frac{d}{Cr} & \frac{1-d}{Cr} \\ 0 & \frac{1-d}{C} & 0 & -\frac{d}{Cr} & \frac{d}{Cr} & [-\frac{1}{Cr} \frac{d}{Cr}] & -\frac{1}{Cr} \\ 0 & 0 & 0 & 0 & \frac{1-d}{Cr} & -\frac{1}{Cr} & \frac{d}{Cr} - \frac{R+r}{Cr} \end{bmatrix} \begin{bmatrix} \hat{i}_{L1}(t) \\ \hat{i}_{L2}(t) \\ \hat{u}_{C1}(t) \\ \hat{u}_{C2}(t) \\ \hat{u}_{C3}(t) \\ \hat{u}_{Cs}(t) \\ \hat{u}_{Cs}(t) \end{bmatrix} \\
 & + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \hat{u}_{in}(t) + \begin{bmatrix} 0 & 0 & 0 & \frac{1}{L_1} & 0 & 0 & 0 \\ 0 & -\frac{r}{L_2} & \frac{1}{L_2} & 0 & 0 & \frac{1}{L_2} & 0 \\ 0 & -\frac{1}{C} & \frac{1}{Cr} & -\frac{1}{Cr} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{Cr} & 0 & \frac{1}{Cr} & -\frac{1}{Cr} \\ 0 & -\frac{1}{C} & 0 & -\frac{1}{Cr} & \frac{1}{Cr} & \frac{1}{Cr} & 0 \\ 0 & 0 & 0 & 0 & -\frac{1}{Cr} & 0 & \frac{1}{Cr} \end{bmatrix} \begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ U_{C1} \\ U_{C2} \\ U_{C3} \\ U_{Cs} \\ U_{Cs} \end{bmatrix} \hat{d} \\
 & \hat{u}_{in}(t) = [0 \ 0 \ 0 \ 0 \ 0 \ 1 \ 1] \begin{bmatrix} \hat{i}_{L1}(t) \\ \hat{i}_{L2}(t) \\ \hat{u}_{C1}(t) \\ \hat{u}_{C2}(t) \\ \hat{u}_{C3}(t) \\ \hat{u}_{Cs}(t) \\ \hat{u}_{Cs}(t) \end{bmatrix}^T
 \end{aligned} \quad (13)$$

Using (13) and the experimental parameters shown in Table IV, when the duty cycle  $d=0.4$ , the control-to-output transfer function can be transformed from the time domain to the complex frequency domain as (14):

$$G_{u,d}(s) = \frac{\hat{u}_o(s)}{\hat{d}(s)} \Big|_{\hat{u}_{in}(s)=0} = \frac{-5.7 \times 10^{-20} s^6 - 7.1 \times 10^{-15} s^5 - 1.6 \times 10^{-10} s^4 + 5.9 \times 10^{-7} s^3 + 0.01 \times 10^{-2} s^2 - 0.04 s + 14000}{1.69 \times 10^{-23} s^7 + 3.91 \times 10^{-20} s^6 + 2.67 \times 10^{-15} s^5 + 5.16 \times 10^{-11} s^4 + 1.08 \times 10^{-6} s^3 + 1.73 \times 10^{-3} s^2 + 2.78 \times 10^{-3} s + 9.34} \quad (14)$$

And the zero-pole modeling of the control-to-output transfer function can be obtained as (15):

$$G_{ZPK}(s) = \frac{-3.4 \times 10^5 \times (s + 9.2 \times 10^4) \times (s + 3.2 \times 10^4) \times (s + 8.5 \times 10^3) \times (s - 8.8 \times 10^3) \times (s^2 - 53s + 1.1 \times 10^6)}{(s + 1.2 \times 10^5) \times (s + 7.7 \times 10^4) \times (s + 3.2 \times 10^4) \times (s^2 + 13s + 5.5 \times 10^4) \times (s^2 + 22s + 3.3 \times 10^6)} \quad (15)$$

It is usually necessary to reduce the order of the dynamic model (keeping a reasonable approximation) to simplify further analysis. Therefore, (15) can be reduced to be (16) from the seventh to the fifth order by appropriate pole-zero cancellation.

$$G_{ZPK}(s) = \frac{-3.4 \times 10^5 \times (s + 8.5 \times 10^3) \times (s - 8.8 \times 10^3) \times (s^2 - 53s + 1.1 \times 10^6)}{(s + 1.2 \times 10^5) \times (s^2 + 13s + 5.5 \times 10^4) \times (s^2 + 22s + 3.3 \times 10^6)} \quad (16)$$

The Bode diagram of the proposed converter is shown in Fig. 5. It can be seen that the curves of the original and the simplified model are approximately the same. In order to achieve stable operation, a voltage loop PI controller needs to be designed and this is now described.

Based on (16), the voltage loop control scheme for the proposed converter can be obtained as shown in Fig. 6.  $G_{ZPK}(s)$  is the transfer function of the converter,  $G_c(s)$  is the voltage controller transfer function (i.e. a PI controller) as shown in (17), and  $H(s)$  is the feedback transfer function. Therefore, the voltage controller can be designed for the proposed converter to achieve suitable static and dynamic performances.

$$G_c(s) = K_p + K_i \frac{1}{s} \quad (17)$$

For this work  $K_p=0.0013$ , and  $K_i=0.00033$ .

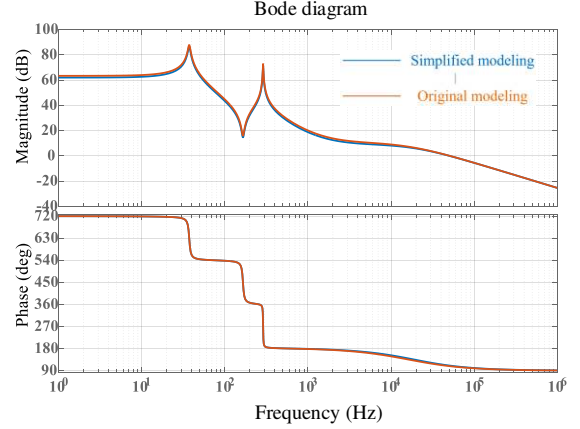


Fig. 5 Bode diagram of proposed converter.

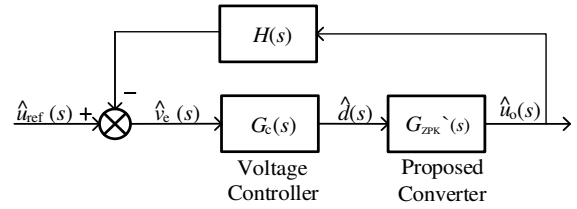


Fig. 6 Voltage loop control scheme for the proposed converter.

Using this voltage loop PI controller, the bode diagram of proposed converter voltage loop is shown in Fig. 7. It can be seen that the phase margin is 50.4 degrees (i.e. greater than 0) when the gain is 0 dB, and therefore the converter can theoretically achieve stable operation.

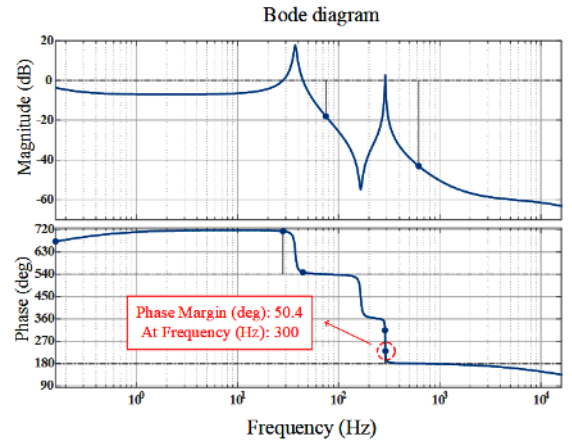


Fig. 7 Bode diagram of proposed converter voltage control loop.

## VII. EXPERIMENTAL RESULTS AND ANALYSIS

In order to validate the feasibility and effectiveness of the proposed converter, a 300W experimental prototype has been developed as shown in Fig. 8. The parameters of the experimental converter are listed in TABLE IV. An adjustable dc source with a range of  $U_{in}=40V \sim 120V$  is used to emulate the fuel cell stack source. The voltage loop of the converter is controlled by a TMS320F28335 DSP controller. Hybrid power switches (MOSFETs IRFP250N and IXTH88N30P) are employed in the low and the high voltage sides, respectively.

DSEC60-03A diodes are used on the low voltage side and DPF60IM400HB diodes are used on the high voltage side. In addition, the switching frequency is 20 kHz, the inductors are  $L_1=330\mu\text{H}$  and  $L_2=1\text{mH}$  respectively (the inductances are increased to keep the current continuous), the electrolytic capacitances are  $C_1=C_2=540\mu\text{F}$ , and the film capacitances are  $C_3=C_5=20\mu\text{F}$ ,  $C_4=40\mu\text{F}$ . The input voltage  $U_{in}$  is variable from 40V to 80V, the reference output voltage is 400V, and the load resistance is  $R=533\Omega$  (i.e. the rated power=300W).

TABLE IV  
Experimental parameters.

Component	parameter	Cost
Input voltage ( $U_{in}$ )	40~80V	
Output voltage ( $U_o$ )	400V	
Rated power	300W	
Switching frequency ( $f_s$ )	20kHz	
Power switch $Q_1$	IRFP250N	\$2.43
Power switch $Q_2$	IXTH88N30P	\$10.48
Diode $D_3/ D_4$	DSEC60-03A	\$2.53×2
Diode $D_5/ D_6/ D_7$	DPF60IM400HB	\$3.47×3
Electrolytic capacitor $C_1/ C_2$	540 $\mu\text{F}$	\$0.95×4
Film capacitor $C_3/ C_5$	20 $\mu\text{F}$	\$3.8×2
Film capacitor $C_4$	40 $\mu\text{F}$	\$6.32
Inductor $L_1$	330 $\mu\text{H}$	\$6.8
Inductor $L_2$	1mH	\$7.28
Other cost (PCB, heat sink, power supply etc.):		\$30
Total cost:		\$90

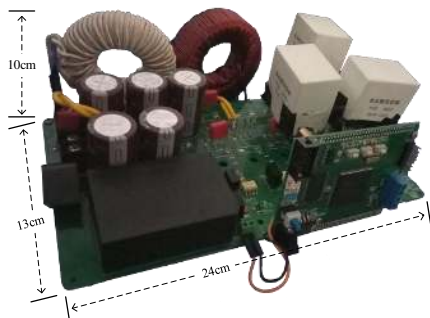
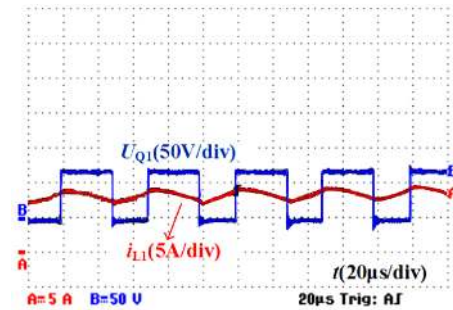


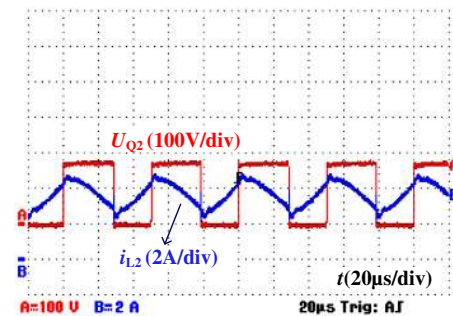
Fig. 8 Experimental prototype.

The voltage stresses across  $Q_1$  and  $Q_2$  and the inductor current  $i_{L1}$  in the steady state are shown in Fig. 9, when  $U_{in}=40\text{V}$ , and  $U_o=400\text{V}$ . From Fig. 9(a), it is clear that when  $U_{Q1}=0$ ,  $i_{L1}$  increases linearly. When  $U_{Q1}\approx 65\text{V}$ ,  $i_{L1}$  decreases linearly. The average value of  $i_{L1}$  is about 8A while the ripple rate is about 12.5%. Similarly, Fig. 9(b) shows that the inductor current  $i_{L2}$  has the same trend as  $i_{L1}$ : the average value of  $i_{L2}$  is approximately 3.5A, and the voltage stress across  $Q_2$  is 165V, which is less than half of the output-voltage (400V). The input-voltage and the output-voltage are shown in Fig. 10 where the voltage-gain is 10, and it can be seen that the proposed converter can achieve a high voltage gain. Fig. 10(a) shows the simulated result and Fig. 10(b) shows the experimental result. Furthermore, according to Fig. 10(a), the duty cycle  $d$  in the simulation is 0.42. Thus, the duty cycle  $d$  in the experimental result is also approximately 0.42 - a good correlation. The voltage stresses across the low voltage diodes  $D_3$  and  $D_4$  are shown in Fig. 11. It is clear that the voltage

stresses across  $D_3$  and  $D_4$  are low - the same as  $U_{Q1}$ . The voltage stress across the high side diodes, and the output voltage are shown in Fig. 12. It can be seen that all the voltage stresses across the high side diodes  $D_5$ - $D_7$  are equal, and are about half of the output voltage.

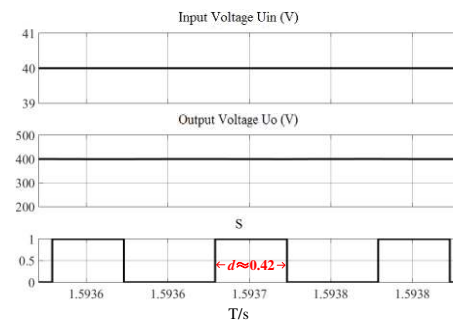


(a)

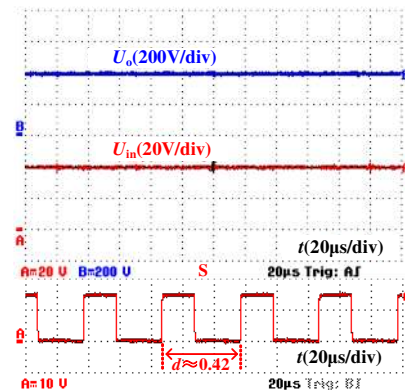


(b)

Fig. 9 Inductor currents and voltage stresses across power switches. (a) Inductor current  $i_{L1}$  and voltage stress  $U_{Q1}$ . (b) Inductor current  $i_{L2}$  and voltage stress  $U_{Q2}$ .



(a)



(b)

Fig. 10 Input-voltage  $U_{in}$  and output-voltage  $U_o$  when voltage-gain is 10. (a) Simulated. (b) Measured.

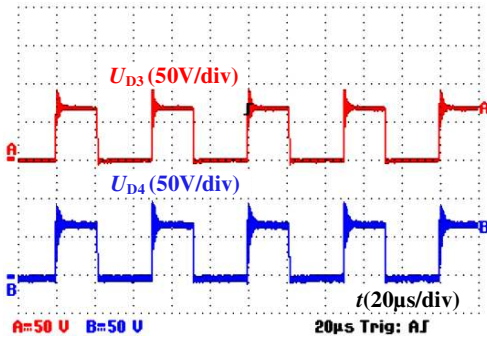


Fig. 11 Voltage stresses across low voltage diodes  $D_3$  and  $D_4$ .

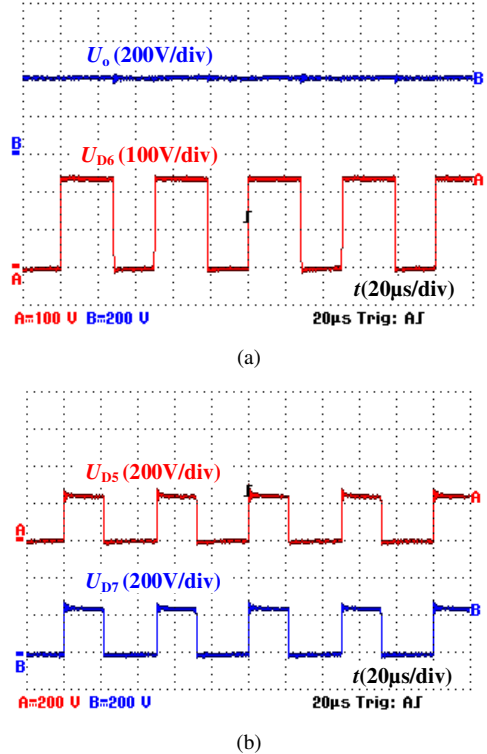


Fig. 12 Voltage stresses across high side diodes and output voltage. (a) Voltage stress across  $D_6$  and output-voltage  $U_o$ . (b) Voltage stresses across  $D_5$  and  $D_7$ .

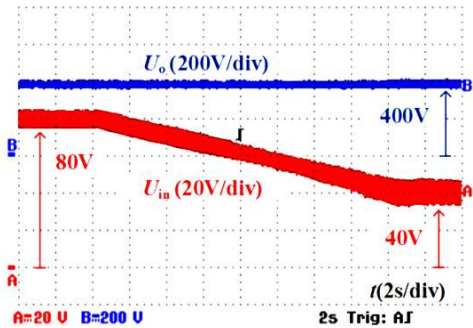


Fig. 13 The output-voltage  $U_o$  with the input-voltage  $U_{in}$  changed from 80V to 40V in dynamic state.

The voltage loop control maintains the output-voltage at 400V in the steady state. In addition, the output voltage can still be kept at 400V even when the input voltage changes significantly, which can be seen in Fig. 13, where the input voltage is changed from 80V to 40V over 16 seconds and the output voltage stays at approximately 400V (i.e. a voltage-gain

increase from 5 to 10). Therefore, the proposed converter can realize a high step-up ratio and a wide step-up voltage gain range during dynamic operation with a variable input voltage.

The conversion ratio is an important parameter which reflects the actual operating performance of the converter. Based on (3), Fig. 14 shows the gain curves derived from theory and from the experimental measurements. Neglecting the parasitic impedances, the theoretical curve is calculated using (3) and is in general higher than the experimentally measured curve for different duty cycles (0.2-0.5). The measured gain curve has a good match with the theoretical curve, which shows the practicability of the proposed converter from an experimental perspective.

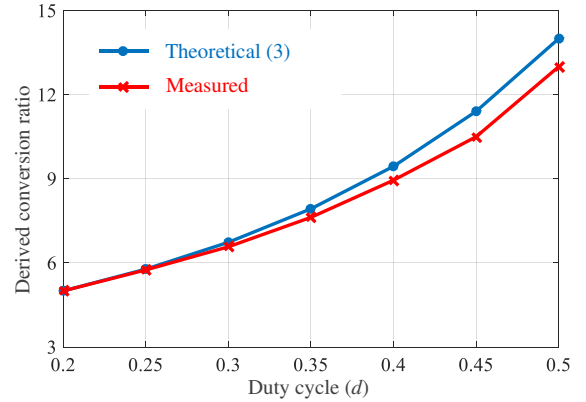


Fig. 14 The derived conversion ratio against the duty cycle under two different conditions.

The efficiency measured by a Power Analyzer (Yokogawa-WT3000) with different voltage-gains is shown in Fig. 15: the output voltage is  $U_o=400V$ , and the output power  $P_o$  varies from 200W to 400W. The maximum efficiency is 95.01%, when  $U_{in}=80V$ , and  $P_o=300W$ , i.e. the voltage-gain is 5. The minimum efficiency is 90.06%, when  $U_{in}=40V$ , and  $P_o=400W$ , i.e. the voltage-gain is 10. The efficiency decreases as the voltage gain increases, because the increase in input current causes larger switching losses.

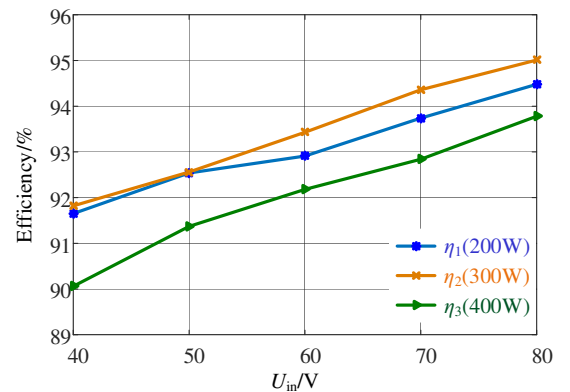


Fig. 15 Measured efficiency of the proposed converter when  $U_o=400V$ , and  $P_o=200W-400W$ .

The calculated loss distribution [32] for the experimental system for  $U_{in}=40V$ ,  $U_o=400V$ , and  $P_o=300W$  are shown in Fig. 16. The total losses of the proposed converter are 24.6W. The turn-on and turn-off (switching) losses of the power switches  $Q_1$  and  $Q_2$  (i.e.  $P_2=7.36W$ ) account for 30% of the



total losses. The conduction losses of all diodes  $D_3$ - $D_7$  (i.e.  $P_D=3.97\text{W}$ ) account for 16% of the total losses, which is nearly equal to the conduction loss of power switches  $Q_1$  and  $Q_2$  (i.e.  $P_Q=3.9\text{W}$ ). In addition to the conduction losses of the semiconductors, the copper losses  $P_{Cu}$  of inductors  $L_1$  and  $L_2$  are  $4.07\text{W}$ , which account for 16% of the total losses. The core losses of inductors  $L_1$  and  $L_2$  (i.e.  $P_{Fe}=4.36\text{W}$ ) account for 18% of the total losses. The capacitor losses of  $C_1$ - $C_5$  are  $P_C=0.94\text{W}$ , which account for 4% of the total losses.

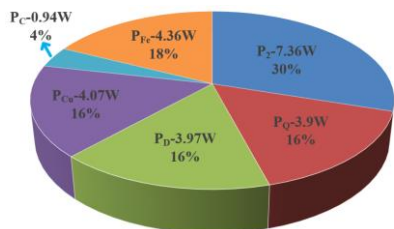


Fig. 16 Calculated loss distributions for experiment under  $U_{in}=40\text{V}$ ,  $U_o=400\text{V}$ , and  $P_o=300\text{W}$  ( $P_2$ : turn-on and turn-off losses of  $Q_1$ - $Q_2$ ,  $P_Q$ : conduction losses of  $Q_1$ - $Q_2$ ,  $P_D$ : conduction losses of  $D_3$ - $D_7$ ,  $P_{Cu}$ : copper losses of  $L_1$  and  $L_2$ ,  $P_C$ : capacitor losses of  $C_1$ - $C_5$ , and  $P_{Fe}$ : core losses of  $L_1$  and  $L_2$ ).

## VIII. CONCLUSION

A high voltage gain DC-DC Boost converter with a wide input range, continuous input current and common ground points between the input side and the load side has been proposed in this paper. The voltage stress across the main power switches is lower than half of the output voltage. In addition, the proposed converter can keep the output voltage at  $400\text{V}$  using a voltage control loop, when the input voltage changes from  $80\text{V}$  to  $40\text{V}$ . Therefore, it is suitable for the power interface between a fuel cell source and the DC bus for the motor drive in fuel cell vehicles.

## REFERENCES

- [1] B. Zeng, J. Zhang, X. Yang, J. Wang, J. Dong, and Y. Zhang, "Integrated planning for transition to low-carbon distribution system with renewable energy generation and demand response," *IEEE Trans. Power Syst.*, vol. 29, no. 3, pp. 1153–1165, May 2014.
- [2] H. Rudnick, R. Palma-Behnke, A. Rudnick, and C. Benavides, "Restless Waters: Fossil Fuel Emissions Conditioning a Reduction in Hydroelectric Resources in Chile," *IEEE Power Energy Mag.*, vol. 12, no. 5, pp. 50–60, Aug. 2014.
- [3] J. Parikh, and K. Parikh, "Growing Pains: Meeting India's Energy Needs in the Face of Limited Fossil Fuels," *IEEE Power Energy Mag.*, vol. 10, no. 3, pp. 59–66, Apr. 2012.
- [4] A. Emadi, and S. S. Williamson, "Fuel Cell Vehicles: Opportunities and Challenges," in *Proc. IEEE Power Eng. Soc. General Meeting*, Denver, CO, Jun. 2004, pp. 1640–1645.
- [5] M. Shen, A. Joseph, J. Wang, F.Z. Peng, and D. J. Adams, "Comparison of Traditional Inverters and Z-Source Inverter for Fuel Cell Vehicles," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1453–1463, Jul. 2007.
- [6] G. Su, and L. Tang, "A reduced-part, triple-voltage DC-DC converter for EV/HEV power management," *IEEE Trans. Power Electron.*, vol. 24, no. 10, pp. 2406–2410, Oct. 2009.
- [7] Y. Zhang, C. Fu, M. Sumner, and P. Wang, "A Wide Input-Voltage Range Quasi-Z Source Boost DC-DC Converter with High Voltage-Gain for Fuel Cell Vehicles," *IEEE Trans. Ind. Electron.*, in press.
- [8] G. Dotelli, R. Ferrero, P. G. Stampino, S. Latorrata, and S. Toscani, "PEM fuel cell drying and flooding diagnosis with signals injected by a power converter," *IEEE Trans. Instrum. Meas.*, vol. 64, no. 8, pp. 2064–2071, Aug. 2015.

- [9] Q. Zhao, F. C. Lee, "High-efficiency high step-up dc-dc converters," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 65–73, Jan. 2003.
- [10] F. L. Tofoli, D. de Castro Pereira, W. J. de Paula, and D. de Sousa Oliveira Junior, "Survey on non-isolated high-voltage step-up DC-DC topologies based on the boost converter," *IET Power Electron.*, vol. 8, no. 10, pp. 2044–2057, 2015.
- [11] J. H. Lee, T. J. Liang, and J. F. Chen, "Isolated coupled-inductor integrated DC-DC converter with nondissipative snubber for solar energy applications," *IEEE Trans. Ind. Electron.*, vol. 61, no. 7, pp. 3337–3348, Jul. 2014.
- [12] W. H. Li, X. N. He, "Review of Nonisolated High-Step-Up DC/DC Converters in Photovoltaic Grid-Connected Applications," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1239–1250, Apr. 2011.
- [13] P. Sadat, and K. Abbaszadeh, "A Single-Switch High Step-Up DC-DC Converter Based on Quadratic Boost," *IEEE Trans. Ind. Electron.*, vol. 63, no. 12, pp. 2959–2968, Dec. 2016.
- [14] H. Choi, M. Ciobotaru, M. Jang, and V. G. Agelidis, "Performance of medium-voltage DC-bus PV system architecture utilizing high-gain DCDC converter," *IEEE Trans. Sustain. Energy*, vol. 6, no. 2, pp. 464–473, Apr. 2015.
- [15] J. Leyva-Ramos, M. G. Ortiz-Lopez, L. H. Diaz-Saldierna, and J. A. Morales-Saldana, "Switching regulator using a quadratic boost converter for wide dc conversion ratios," *IET Power Electron.*, vol. 2, no. 5, pp. 605–613, Sep. 2009.
- [16] B. Axelrod, Y. Berkovich and A. Ioinovici, "Switched -capacitor/switched-inductor structures for getting transformerless hybrid DC-DC PWM converters," *IEEE Trans. Circuits Syst. I Reg. Papers*, vol. 55, no. 2, pp. 687–696, Mar. 2008.
- [17] A. Ioinovici, "Switched-capacitor power electronics circuits," *IEEE Circuits Syst. Mag.*, vol. 1, no. 4, pp. 37–42, Sep. 2001.
- [18] G. Wu, X. Ruan, and Z. Ye, "Nonisolated high step-up dc-dc converters adopting switched-capacitor cell," *IEEE Trans. Ind. Electron.*, vol. 61, no. 1, pp. 383–393, Jan. 2015.
- [19] Y. Tang, T. Wang, and Y. He, "A switched-capacitor-based active-network converter with high voltage gain," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2959–2968, Jun. 2014.
- [20] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Transformerless DC-DC converters with a very high DC line-to-load voltage ratio," *J. Circuits, Syst. Comput.*, vol. 13, no. 3, pp. 467–475, Jun. 2004.
- [21] Patidar, K., Umarikar, A.C., "High step-up pulse-width modulation dc-dc converter based on quasi-Z-source topology," *IET Power Electron.*, vol. 8, no. 4, pp. 477–488, 2015.
- [22] Y. Zhang, J. Shi, L. Zhou, J. Li, M. Sumner, P. Wang, and C. Xia, "Wide Input-Voltage Range Boost Three-Level DC-DC Converter with Quasi-Z Source for Fuel Cell Vehicles," *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 6728–6738, Sep. 2017.
- [23] Y. Shindo et al., "Z-source DC-DC converter with cascade switched capacitor," in *Proc. 37th Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, 2011, pp. 1665–1670.
- [24] G. Zhang, B. Zhang, Z. Li, D. Qiu, L. Yang, and W. A. Halang, "A 3-Z-network boost converter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 1, pp. 278–288, Jan. 2015.
- [25] M. Zhu, K. Yu and F. L. Luo "Switched-inductor Z-source inverter," *IEEE Trans. Power Electron.*, vol. 25, no. 8, pp. 2150–2158, Aug. 2010.
- [26] M. Prudente, L. L. Pfitscher, G. Emmendoerfer, E. F. Romaneli and R. Gules, "Voltage Multiplier Cells Applied to Non-Isolated DC-DC Converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 871–887, Mar. 2008.
- [27] Y. R. Novaes, A. Rufer, and I. Barbi, "A new quadratic, three-level, dc/dc converter suitable for fuel cell applications," in *Proc. Power Convers. Conf.*, Nagoya, Japan, 2007, pp. 601–607.
- [28] C. T. Pan, C. F. Chuang, and C. C. Chu, "A novel transformer-less adaptable voltage quadrupler DC converter with low switch voltage stress," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4787–4796, Sep. 2014.
- [29] O. Cornea, GD. Andreescu, N. Muntean, and D. Hulea, "Bidirectional Power Flow Control in a DC Microgrid through a Switched-Capacitor Cell Hybrid DC-DC Converter," *IEEE Trans. Ind. Electron.*, vol. 64, no. 4, pp. 3012–3022, Apr. 2017.
- [30] E. Ferro, VM. Brea, P. López, and D. Cabello, "Dynamic Model of

Switched-Capacitor DC–DC Converters in the Slow-Switching Limit Including Charge Reusing,” *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5293–5311, Jul. 2017.

- [31] Y. Liu, H. Abu-Rub, and B. Ge, “Front-End Isolated Quasi-Z-Source DC–DC Converter Modules in Series for High-Power Photovoltaic Systems—Part II: Control, Dynamic Model, and Downscaled Verification,” *IEEE Trans. Ind. Electron.*, vol. 64, no. 1, pp. 359–368, Jan. 2017.
- [32] Y. Zhang, Y. Gao, L. Zhou, and M. Sumner, “A Switched-Capacitor Bidirectional DC-DC Converter with Wide Voltage Gain Range for Electric Vehicles with Hybrid Energy Sources,” *IEEE Trans. Power Electron.*, in press.



**Yun Zhang** (M'13-SM'18) was born in Jiangsu, China, in 1980. He received the B.S. and M.S. degrees in electrical engineering from the Harbin University of Science and Technology, Harbin, China, in 2003 and 2006, respectively, and the Ph.D. degree in electrical engineering from the Harbin Institute of Technology, Harbin, China, in 2010.

In 2010, he joined the Tianjin University, Tianjin, China, as a Lecturer in the School of Electrical and Information Engineering, where he is currently an Associate Professor. From December 2016 to

December 2017, he was an Academic Visitor with the Power Electronics, Machines and Control (PEMC) Group at the University of Nottingham, Nottingham, U.K.. His current research interests include topologies, modulation, and control strategies of power converters for electric vehicles and microgrids.

Dr. Zhang is an Associate Editor of the JOURNAL OF POWER ELECTRONICS.



**Heyu Liu** was born in Shandong, China. He received his B.S. degree in Qingdao University of Technology, Qingdao, Shandong, China, in 2016. He started pursuing his M.S. degree in Electrical Engineering from the Tianjin University, Tianjin, China, in 2016.

His current research interests include DC-DC converters, and energy management of electric vehicles.



**Jing Li** (M'15) received the B.Eng. (Hons.) and M.Sc. (Distinction) degrees both in control science and engineering from the Beijing Institute of Technology, Beijing, China, in 1999, and 2002, respectively, and the Ph.D. degree in electrical engineering from the University of Nottingham, Nottingham, U.K., in 2010.

She was a Research Fellow with the Power Electronic, Machine and Control Group, University of Nottingham. She is currently a Lecturer at the Department of Electrical and Electronic Engineering, University of Nottingham, Ningbo, China. Her

research interests include condition monitoring for motor drive systems and power distribution systems and advanced control and design of motor drive systems.



**Mark Sumner** (SM'05) received the B.Eng. degree in electrical and electronic engineering from Leeds University, Leeds, U.K., in 1986, and the Ph.D. degree in induction motor drives from the University of Nottingham, Nottingham, U.K., in 1992.

He was with Rolls Royce, Ltd., Ansty, U.K. He was a Research Assistant with the University of Nottingham, where he became a Lecturer in October 1992, and is currently a Professor of electrical energy systems. His research interests include control of

power electronic systems including sensorless motor drives, diagnostics and prognostics for drive systems, power electronics for enhanced power quality, and novel power system fault location strategies.



**Changliang Xia** (SM'12) was born in Tianjin, China, in 1968. He received the B.S. degree from Tianjin University, China, in 1990, and the M.S. and Ph.D. degrees from Zhejiang University, China, in 1993 and 1995 respectively, all in electrical engineering.

He is currently an Academician with the Chinese Academy of Engineering. He is also a Professor and the Head of Engineering Center of Electric Machine System Design and Control,

Tianjin, China. His research interests include electrical machines, power electronics, and their control systems.