DC-DC Converter-Aware Power Management for Battery-Operated Embedded Systems

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ABSTRACT

Most digital systems are equipped with DC-DC converters to supply various levels of voltages from batteries to logic devices. DC-DC converters maintain legal voltage ranges regardless of the load current variation as well as battery voltage drop. Although the efficiency of DC-DC converters is changed by the output voltage level and the load current, most existing power management techniques simply ignore the efficiency variation of DC-DC converters. However, without a careful consideration of the efficiency variation of DC-DC converters, finding a true optimal power management will be impossible. In this work, we solve the problem of energy minimization with the consideration of the characteristics of power consumption of DC-DC converter. Specifically, the contributions of our work are: (1) We analyze the effects of the efficiency variation of DC-DC converters on a single task execution in DVS (dynamic voltage scaling) scheme, and propose a technique, called DC_DVS, of DC-DC converter-aware energy-minimal DVS; (2) DC_DVS is then extended to combine the effects of DC-DC converters with the procedures of general DVS techniques with multiple tasks; (3) Conversely, we propose a technique, called DC_CONF, of generating a DC-DC converter that is best suited, in terms of total energy efficiency, to the intended application, and (4) finally, we complete our integrated framework DC-lp, which is based on DC_DVS and DC_CONF, that attempts to solve the DC-DC converter configuration selection problem and the DVS problem simultaneously. To show the effectiveness of the proposed techniques, a set of experimental results is provided. In summary, it is shown that DC-lp is able to save 16.0%∼22.1% of energy on the average, which otherwise was dissipated in the previous power management schemes with no consideration of DC-DC converter efficiency variation.

Categories and Subject Descriptors: B.8.2 [PERFORMANCE AND RELIABILITY]: Performance Analysis and Design Aids, C.4 [PERFORMANCE OF SYSTEMS]

General Terms: Design, Performance

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1. INTRODUCTION

Almost all modern digital systems are supplied with power through DC-DC converters as high-performance CMOS devices are optimized to specific supply voltage ranges. DC-DC converters are generally classified into two types: linear voltage regulators and switching voltage regulators, according to the circuit implementation. However, the power dissipation in both types of voltage conversion is unavoidable, and directly affects the lifetime of battery in the whole system. Fig. 1 shows the path of current flow through DC-DC converter from battery. It is reported that there is always a non-trivial power loss in the converter, the amount of which is 10%∼40% of the total energy consumed in the system.

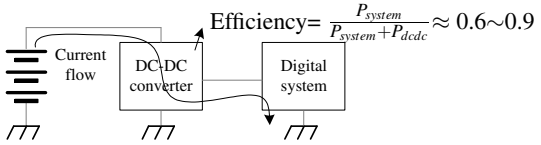

Figure 1: A typical current flow path from battery: a non-trivial power loss in DC-DC converter, resulting in short battery life despite of low-power dissipation in the digital system.

It is generally known that switching regulators expose better power efficiency than linear regulators, but linear regulators are much cheaper in implementation and invoke lower noise than switching regulator. For this reason, switching regulators are mostly used for low power and/or high current application except some cases, in which low noise or low cost is required. There are several works which have addressed the problem of increasing power efficiency of switching DC-DC converters. Notable works are those in [1], focusing on more efficient circuit configurations, those in [2], focusing on circuit modifications, and those in [1], investigating the sources of power loss in DC-DC converters and the power dissipation model in terms of input/output characteristics and converter parameters. The work in [3] proposed a methodology for cycle-accurate simulation of performance and energy consumption in an embedded system with a DC-DC converter and pointed out that the energy loss in a DC-DC converter took a significant fraction of the total energy consumption.

On the other side, so far a lot of power management techniques on saving energy in embedded system design are proposed. Nevertheless, almost all of them do not seriously take into account the efficiency of DC-DC converters, simply assuming DC-DC converter power efficiency as a constant value [4]. If the amount of power dissipation of a DC-DC converter were constant over the entire operating range, we could ignore its effect on the total energy consumption of the system. However, in reality, the efficiency of a DC-DC converter has a close correlation with the level of output

voltage and the values of load current it produces. Consequently, when a power management scheme with the capability of varying voltage (*e.g.*, dynamic voltage scaling (DVS)) is implemented in an embedded system, it is also very important and necessary to properly schedule the output voltage of the DC-DC converter, so that overall energy consumption of the system including that in the DC-DC converter is to be minimized. Note that in case of a switching regulator, in addition to the output voltage, its power efficiency is affected by the load current as well. The key concern of our work is: Even though an effective power management scheme can reduce the power consumption of a device to a large extent, it does not always mean that it also reduces the power consumption of a DC-DC converter minimally, in some cases operating very inefficiently, resulting in poor battery life enhancement. Consequently, it is quite necessary to solve the two problems, namely the problem of (output) voltage scaling of a DC-DC converter, and the problem of voltage scaling that is applied to the devices other than the DC-DC converter in an integrated fashion, so that the total energy consumption is globally minimized.

It is accepted that dynamic voltage scaling (DVS) is one of the most effective and well-studied power management techniques. Under the assumption of a dynamically continuously variable voltage processor, there are optimal algorithms for finding a schedule of non-periodic tasks and voltage scaling to the tasks [5], and a voltage scaling with fixed priority schedule for periodic tasks [6]. Essentially, most studies suggested DVS algorithms based on dynamic or static priorities. They are differentiated by how slacks are estimated and what slack distribution schemes are used [7]. Some DVS schemes adjust the supply voltage within an individual task boundary (*i.e.*, intra-task), not on task-by-task basis [8]. In [9], practical DVS schemes with the consideration of discrete supply voltage and non-uniform load capacitances were suggested. However, it should be noted that none of the DVS schemes mentioned above, even their significance in saving energy, do not take into account the output voltage scaling of a DC-DC converter and thus the load current variation. Finally, the output voltage and load current variations due to DVS will cause efficiency variation of the DC-DC converter. To overcome this limitation of the previous power management techniques, we first address the problem of so called DC-DC converter-aware power management. Specifically, we approach the problem in two aspects, in which the two subproblems in (1) and (2) in the following to cover the core parts of the problem of DC-DC converter-aware power management: (*1. Converter-aware voltage scaling problem*) For a given single task with execution cycles and a deadline, we derive the power consumption model of a DC-DC converter by analyzing how the power consumption is related to the output voltage, and propose a solid voltage scaling technique[1] that minimizes the total sum of the energy consumed by the execution of the task and the energy dissipated by the DC-DC converter. The proposed technique is then simply, yet effectively, extended to handle multiple tasks; (*2. Application-driven converter optimization problem*) Conversely to the problem solved in (1), we propose a solution to the problem of finding a configuration of a DC-DC converter that is best suited for the application to be executed in the system in terms of minimizing total energy consumption.

Section 2 briefly summarizes the function of DC-DC converters as a background knowledge, followed by a modeling of power consumption of the converters and a derivation of power equations. In Section 3, we present an integrated DC-DC converter-aware energy minimization algorithm, which essentially solves two core problems namely *converter-aware voltage scaling problem* and *application-driven converter optimization problem*. Section 4 provides a set of experimental results to show how much the proposed techniques are effective. Finally, concluding remarks of the work are given in Section 5.

[1]Note that our proposed voltage scaling technique is flexible enough to be easily modified to fit into most of the known DVS methods.

2. DC-DC CONVERTERS

2.1 Voltage regulation

The divergence of digital devices and technology innovation make it hard to use a single supply voltage to all devices or even to an individual device. Since all supply voltages to the devices are generally received from a single battery source, the voltage regulators (DC-DC converters) control the supply voltage for each device, as indicated in Fig. 2, which shows a simplified power supply network for battery-operated embedded systems.

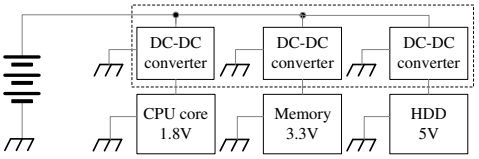

Figure 2: DC-DC converters generate different supply voltages to CPU, Memory, and HDD devices from a single battery.

The primary role of a DC-DC converter is to generate a regulated power source. Unlike passive components, logic devices do not draw constant current from a power supply. The power supply current rapidly changes according to the changes of its internal states. An unregulated power supply may induce IR drop corresponding to the load current, whereas a regulated power supply keeps the same output voltage regardless of the load current variation. Note that IR drop is caused by non-zero resistance of power supply. Thus, even though we use a single power supply voltage, a DC-DC converter for voltage regulation is required.

2.2 Switching regulator basics

In our work, we focus on minimizing the power dissipation of switching regulator, which is mostly used a switching-mode of DC-DC converters in low power applications. A switching regulator is a circuit that uses an inductor, a transformer or a capacitor as an energy-storage element to transfer energy from a power source to a system. The amount of power dissipated by voltage conversion in a switching regulator is relatively low, mainly due to the use of low-resistance switches and energy storage elements, while the amount of power dissipated in a linear regulator, as opposed to the switching regulator, is rather high, mainly from the fact that the power efficiency of a linear regulator is upper-bounded by the value of output voltage divided by the input voltage. In addition, switching regulators can step up (*i.e.*, boost), step down (*i.e.*, buck), and invert input voltage with a simple modification of the converter topology, unlike linear regulators. A switching regulator contains a circuit, positioned on the path between the external power supply and the energy-storage element to control switches.

2.3 Modeling of power dissipation in DC-DC converters

To clarify the focus of the context, we assume a step-down converter which has two same types of switches and is controlled by fixed switching frequency, without loss of generality. Under the assumption, we adopt the power loss model introduced in [1] to describe the energy consumption of a DC-DC converter according to the load current. We do not use this model as it is, but make a simplified version, which considers many manufacture-related parameters as constants, as follows:

$$P_{DC}(I,W) = (\frac{c_1}{W} + c_2)I^2 + c_3W + c_4, \text{ when } I \neq 0,$$
$$P_{DC}(I,W) = 0, \text{ otherwise} \quad (1)$$

where I is the load current, W is a DC-DC converter configuration parameter which controls a tradeoff between load independent power consumption and load dependent power consumption (*e.g.* the gate width of MOSFET switches in Kursun's loss model[1]), and $c_1, \cdots, c_4$ are constants. If $I = 0$, we can consider $P_{DC}(I,W)$

as zero because many DC-DC converters enter the shutdown state with very little power loss when there is no load current.

Fig. 3 shows the relation between the converter's energy efficiency and the converter configuration parameter W. We can see that the energy efficiency of a DC-DC converter increases as W becomes large at heavy load, or W becomes small at light load. The curves in Fig. 3 clearly show that W is a key parameter that characterizes the power consumption of various capacities of DC-DC converters.

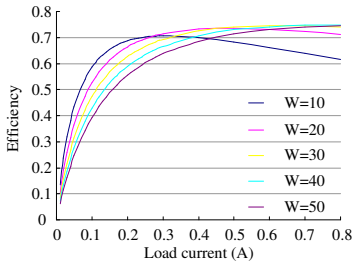

Figure 3: The energy efficiency of DC-DC converter with a set of different values of parameter W.

3. DC-DC CONVERTER-AWARE ENERGY MANAGEMENT TECHNIQUES

3.1 The proposed algorithm: an overview

Solving the problem of determining a configuration of a DC-DC converter and a DVS result that lead to a minimal energy consumption, is a quite complex problem, as it shall be hinted in the following subsections. To make the problem easily tractable to solve in a systematic way, we propose a simple, but solid framework, called DC-lp, of converter-aware energy minimization algorithm. DC-lp essentially combines two core techniques: DC_DVS (Section 3.2) and DC_CONF (Section 3.3); The objective of DC_DVS is to refine the DVS result by considering the energy efficiency of the DC-DC converter to be used, while the objective of DC_CONF to refine the configuration of the DC-DC converter (*i.e.*, determining an optimal value of parameter W) according to the update of the DVS result. Fig. 4 shows the flow of the integrated algorithm. Initially, we are given a DVS result A for input tasks, and a converter configuration B. Then, the two steps in Fig. 4 are performed iteratively until there is no further reduction in total energy consumption: (Step 1) DC_DVS is applied to A by using B to produce a new DVS result A'; (Step 2) DC_CONF is applied to A' to produce a new configuration B'.

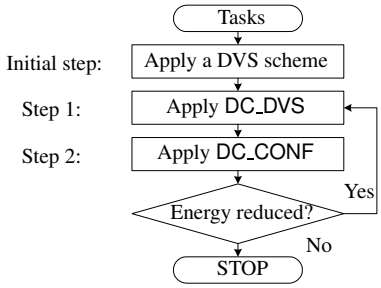

Figure 4: The flow of our proposed iterative algorithm DC-lp.

The following subsections describe the two steps, each of which solves the DC-DC converter related energy minimization problems: (Step 1) converter-aware voltage scaling problem, which determines task and voltage scheduling that minimizes the total energy consumption of system including that in the DC-DC converter and (Step 2) application-driven DC-DC converter optimization problem which finds the best energy-efficient configuration of the DC-DC converter for the application.

3.2 Converter-aware voltage scaling technique

It is a well-known fact [10] that the amount of the CPU power, P_i, and energy consumption, E_i, for task J_i, in CMOS circuits (by simply assuming a fixed supply voltage for the task) is computed by:

$$P_i = C_i \cdot V_i^2 \cdot f, \qquad E_i = R_i \cdot C_i \cdot V_i^2 \tag{2}$$

where C_i is the average switched capacitance per clock cycle for the task, f is the operating frequency, V_i is the supply voltage used for the execution of the task, and R_i is the total number of cycles required for the execution of task J_i.

However, the supply voltage scaling incurs one critical penalty: The voltage reduction increases circuit delay, which is approximately linearly proportional to the supply voltage, since the circuit delay, T_d, is expressed as ([10]):

$$T_d = \frac{C_L V_i}{\mu C_{ox}(D/L)(V_i - V_t)^{\alpha}} \tag{3}$$

where C_L represents the total node capacitance, μ is the mobility, C_{ox} is the oxide capacitance, V_t is the threshold voltage, V_i is the supply voltage to the task, α is a constant satisfying $1 < \alpha < 2$, and D and L represent the width and length of transistors, respectively.

An instance of a task scheduling and a voltage allocation problem in a system consists of a set $\mathcal{J} = \{J_1, J_2, \cdots, J_N\}$ of tasks (or jobs) and a variable voltage range $[V_{min}, V_{max}]$ where N represents the number of tasks. We denote $f(V)$ to be the clock speed corresponding to the voltage V.

Each task $J_i \in \mathcal{J}$ is associated with the following parameters:

- a_i : the arrival time of J_i.
- d_i : the deadline of J_i ($a_i \leq d_i$),
- R_i : the number of processor cycles required to complete J_i,

Since the supply voltage directly determines the processor's clock frequency (as implied in Eq. 3), it is often convenient to think of the energy consumption as a function of the clock frequency. Let $f_i(t)$ be the clock frequency assigned to task J_i at time t, and $P_i(f_i(t))$ be the energy consumed in task J_i during a period of unit time, starting at t. Then, the total energy consumed by a voltage scaling, $\mathcal{A}_i$, for task J_i is given by ([5])

$$E(\mathcal{A}_i) = \int_{t_{i,1}}^{t_{i,2}} P_i(f_i(t))dt \tag{4}$$

where $t_{i,1}$ and $t_{i,2}$ are the start and ending times of the execution of task J_i. Thus, the total CPU energy consumption, E_{CPU}, excluding that in DC-DC converter for N tasks $(J_1, J_2, \cdots, J_N)$ is

$$E_{CPU} = \sum_{i=1}^{N} \int_{t_{i,1}}^{t_{i,2}} P_i(f_i(t))dt. \tag{5}$$

Then, from Eqs. 5 and 1, the total energy consumption including that in a DC-DC converter for the tasks is computed by

$$E_{tot} = E_{CPU} + \sum_{i=1}^{N} \int_{t_{i,1}}^{t_{i,2}} P_{DC}dt. \tag{6}$$

Note that the values of a_i, d_i, and R_i are given for task J_i, and the values of $s_i(t)$ and $P_i(f_i(t))$ vary according to the dynamic scaling of voltages to J_i, and, thus, directly affect the amount of energy consumption. A schedule of tasks is referred to as a *feasible schedule* if all the timing constraints of the tasks are satisfied. We assume that tasks can be preempted. Then, the task scheduling and voltage scaling problem is:

Problem 1: *Given an instance of tasks, a DC-DC converter, and a voltage range of a processor, find a feasible task schedule and voltage scaling to tasks that minimizes the quantity of E_{tot} in Eq. 6.*

To reduce the complexity of the problem, we first propose a technique for solving a restricted version of Problem 1, and then extend it to fully solve Problem 1.

• **Solution to Problem 1 with a single task**: We derive, from Eqs. 1 and 2, a total power equation in terms of supply voltage variable only: For a system with dynamic voltage scaling, the maximum operating frequency is proportional to the operating voltage. That is, $f = \alpha V$ where α is a system-dependent constant, and thus $P = C\alpha V^3$. Furthermore, since power consumption can also be expressed as a product of load current and supply voltage (*i.e.*, $P = VI$), we have

$$I = C \cdot \alpha \cdot V^2. \tag{7}$$

From Eqs. 7 and 1 with a fixed value of W, we can express the total power consumption, P_{tot}, including that in the DC-DC converter as

$$P_{tot}(V) = P_{CPU}(V) + P_{DC}(V) = C \cdot \alpha \cdot V^3 + (\frac{c_1}{W} + c_2) \cdot C^2 \cdot \alpha^2 \cdot V^4 + c_3 \cdot W + c_4. \tag{8}$$

For a task with execution time of T and deadline of D, the quantity of E_{tot} for the execution of the task can be obtained by simply multiplying the total power consumption, $P_{tot}(V)$, by the execution time because the power loss of the DC-DC converter in standby state is negligible:

$$E_{tot}(V) = \int_0^D P_{tot}(V)dt = \int_0^T P_{tot}(V)dt = T \cdot P_{tot}(V).$$

Then, applying $T = \frac{R}{f} = \frac{R}{\alpha V}$ (R is the number of cycles for given task) to $E_{tot}(V)$ gives

$$E_{tot}(V) = R \cdot C \cdot V^2 + (\frac{c_1}{W} + c_2) \cdot R \cdot C^2 \cdot \alpha \cdot V^3 + (R \cdot c_3 \cdot W + R \cdot c_4) \frac{1}{\alpha V}. \tag{9}$$

The last term in Eq. 9 indicates that the total energy consumption is not a monotonic increasing function of the output voltage. This means that using the lowest feasible voltage (or frequency) for a task does not always lead to minimal total energy consumption. Fig. 5 shows the curve of $E_{tot}(V)$ for a DC-DC converter. The curve clearly indicates that the optimal voltage for $E_{tot}(V)$ is not always the lowest feasible voltage.

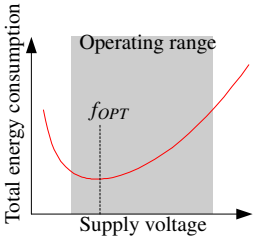

Figure 5: Total energy consumption over supply voltage (V∝ CPU clock frequency).

Fig. 6 summarizes our procedure of DC-DC converter-aware energy optimal dynamic voltage scaling, called DC_DVS-1, to the problem 1 with a single task. DC_DVS-1 simply checks if the value of f_{OPT} of Eq. 9 is in the feasible frequency range $[f_{min}, f_{max}]$ of processor, and set the energy minimal frequency accordingly.

• **Solution to Problem 1 with multiple tasks**: There can be two directions to solve Problem 1 with multiple tasks. One is a generic technique that is applicable to a broad class of DVS methods. The other is a fine-tuned technique only applicable to a specific DVS

DC_DVS-1: DC-DC converter-aware DVS for a single task
Input: A task, DC-DC-converter, and processor with operating frequency range $[f_{min}, f_{max}]$.
Output: Frequency f that minimizes $E_{tot}(V(f))$.
• Derive f_{OPT} from Eq. 9;
case
$f_{OPT} < f_{min}$: $f = f_{min}$;
$f_{OPT} > f_{max}$: $f = f_{max}$;
otherwise: $f = f_{OPT}$;
endcase;
return f;

Figure 6: A summary of the proposed algorithm for Problem 1 with a single task.

method. Since we are interested in the problem of integrating the efficiency variation of a DC-DC converter into the existing DVS methods, we choose the former direction. Specifically, for any (existing) DVS method with no consideration of power minimization in the DC-DC converter, our devised technique is the one that attempts to improve the quality of results produced by the method by reflecting the power consumption in a DC-DC converter. The idea of our proposed technique, called DC_DVS-m, is to decompose the schedule of tasks into task basis and apply DC_DVS-1 in Fig. 6 to each of decomposed schedules to further reduce the total energy consumption of the task. Let E_i^{before} and E_i^{after} be the quantities of E_{tot} in Eq. 9 of task i, before and after the application of DC_DVS-1 to task i. Then, the total amount of energy saving ΔE_{tot} by DC_DVS-m over that of an existing DVS method is:

$$\Delta E_{tot} = \sum_{task\ i} (E_i^{before} - E_i^{after}). \tag{10}$$

Note that the value of ΔE_{tot} is always positive because for every i, $E_i^{before} - E_i^{after} > 0$. Fig. 7 summarizes the procedure of DC_DVS-m. DC_DVS-m preserves the schedule of tasks that is produced by the input DVS method. It only updates frequency (*i.e.*, supply voltage) to each task. If the schedule of a task spans more than one time interval, the intervals are merged to be one time interval and DC_DVS-m is applied to the interval. The assignment $[a_i, d_i] = |s|$ in Fig. 7 performs such merge of time intervals. After when DC_DVS-1 is applied to each task, the merged interval is restored to the original intervals.

DC_DVS-m: DC-DC converter-aware DVS for multiple tasks
Input: Tasks, DVS scheme, DC-DC-converter, and processor with operating frequency range $[f_{min}, f_{max}]$.
Output: Frequency f_i to each task i that minimizes $E_{tot}(V(f))$.
• Apply the DVS scheme to the input tasks and produce schedule S and voltage scaling to tasks;
foreach (schedule s of task i) // s: (start-time, end-time)
• Apply DC_DVS-1 to task i with $[a_i, d_i] = |s|$ and produce f_i;
endfor;
return (f_i to each task, S);

Figure 7: A summary of the proposed algorithm for Problem 1 with multiple tasks.

3.3 Application-driven converter optimization technique

The problem of implementing a DC-DC converter that consumes the least energy consumption under the application of DVS is not simple since there could be various parameters, possibly, some of which are conflict each other. However, as mentioned in Section 2.3, one of the most critically impacting parameters on the variation of energy consumption is parameter W in Eq. 1 that controls the tradeoff between load independent power and load dependent power in a significant way. (Fig. 8 shows two different energy

curves that are extracted from experimentation for two different values of parameter W of a DC-DC converter.) In this section, we show how the parameter W can be optimized to minimize the total energy consumption of a system. Note that our optimization procedure is general in that it is applicable to any of the parameters only if the energy consumption can be expressed in terms of the parameter.

The derived form of energy model in terms of parameter W and applied voltage V is that in Eq. 9:

$$E_{tot}(V,W) = R\cdot C\cdot V^2 + (\frac{c_1}{W}+c_2)\cdot R\cdot C^2\cdot\alpha\cdot V^3 + (R\cdot c_3\cdot W + R\cdot c_4)\frac{1}{\alpha V}. \quad (11)$$

The last two terms represent the amount of energy consumption in the converter itself while the first term represents the amount of CPU energy consumed in a task. Note that W in the converter design should be constrained to be a value in $[W_{min}, W_{max}]$. Even though it is not so difficult to find energy-optimal values of W and V from Eq. 11 for a 'single' task in a specific application, in a practical point of view, it would be hard to find optimal values for 'multiple' tasks. Since solving the problem using a complex mathematical tool would be a very time consuming process, we simplify the problem in a way to find the best value of W after the application of DVS, independently of the DC-DC converter. In other word, for a given DVS result, we want to find a value of W in $[W_{min}, W_{max}]$ that minimizes the total amount of energy consumption of the system. Precisely, let $v_1, v_2, \cdots v_k$ be the voltages used to a (scheduled) sequence of unit times of execution of multiple tasks produced by a DVS scheme, and $E_{tot}(v_i, W)$ be the total energy consumption in the corresponding time using voltage v_i, then the total energy can be expressed, in terms of variable W only, as follows:

$$\begin{aligned} E_{tot} &= E_{tot}(v_1,W) + \cdots + E_{tot}(v_k,W) \\ &= r_1\cdot C\cdot v_1^2 + \cdots + r_k\cdot C\cdot v_k^2 \\ &\quad + (\tfrac{c_1}{W}+c_2)\cdot r_1\cdot C^2\cdot\alpha\cdot v_1^3 + (r_1\cdot c_3\cdot W + r_1\cdot c_4)\tfrac{1}{\alpha v_1} \\ &\quad \cdots \\ &\quad + (\tfrac{c_1}{W}+c_2)\cdot r_k\cdot C^2\cdot\alpha\cdot v_k^3 + (r_k\cdot c_3\cdot W + r_k\cdot c_4)\tfrac{1}{\alpha v_k} \\ &= \gamma_1\cdot W + \gamma_2\cdot\tfrac{1}{W} + \gamma_3 \end{aligned} \quad (12)$$

where γ_1, γ_2, and γ_3 are constants. Note that Eq. 12 is convex with respect to W. Consequently, to determine an energy-optimal value of W in $[W_{min}, W_{max}]$, the proposed solution, called DC_CONF, first derives a W value, w_{OPT}, that leads to a minimum quantity of E_{tot}, and simply checks whether w_{OPT} is in the range of $[W_{min}, W_{max}]$, and set the energy minimal value of W accordingly, as shown in Fig. 9.

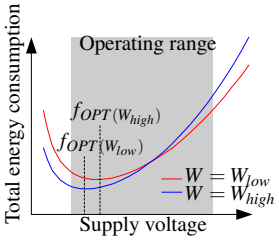

Figure 8: Total energy consumption over W.

4. EXPERIMENTAL RESULTS

We implemented our proposed DC-DC converter-aware power management techniques in C++ and tested on a set of multimedia benchmark designs in [8][11][12]. The evaluation was conducted in two-fold: (1) For a given configuration of a DC-DC converter, a task set, and a voltage range, we want to know how much DC_DVS (*i.e.*, Figs. 6 and 7) effectively performs voltage scaling to tasks to reduce the energy consumption including that in the DC-DC converter; (2) For a range of the value of W of the DC-DC converter,

DC_CONF: Energy-minimal DC-DC converter configuration
Input: DVS voltage result for multiple tasks,
parameter W's range of converter $[W_{min}, W_{max}]$.
Output: Value w of W that minimizes E_{tot} under $[W_{min}, W_{max}]$.
• Solve equation of E_{tot} to find w_{OPT};
case
$w_{OPT} < w_{min}$: $w = w_{min}$;
$w_{OPT} > w_{max}$: $w = w_{max}$;
otherwise: $w = w_{OPT}$;
endcase;
return w;

Figure 9: A summary of the proposed algorithm for finding an energy-minimal configuration of a DC-DC converter.

a task set, and voltage range, we want to know how much DC-lp (*i.e.*, Fig. 4) effectively determines the converter configuration and voltage scaling to tasks to reduce total energy consumption.

• **Assessing the effectiveness of** DC_DVS: We tested DC_DVS on a number of real-time task sets from a videophone application (VP) [8], an Avionics application (AVN) [11] and a Computerized Numerical Control machine controller application (CNC) [12]. To evaluate $E_{tot}(V,W)$ in Eq. 11, we used a typical values for constants c_1, c_2, c_3 and c_4, namely $c_1 = 11$, $c_2 = 0.12$, $c_3 = 0.004$ and $c_4 = 0.075$, which are determined by reflecting the power loss of a real DC-DC converter [13] when $W = 30$ and representing the power loss of various DC-DC converters in the range of $W = 10$ to 50. The voltage range the processor can scale is set to $[0.6V, 1.8V]$ using 400MHz and 0.5A as the clock frequency and current at $1.8V$, respectively. For a fixed configuration of the DC-DC converter (*i.e.*, $W = 20, 30, 40$ and 50), Table 1 summarizes the comparisons of the amounts of energy consumed by the scheme (NO_DVS) that always applies the fastest clock frequency to every task, the scheme (DVS_ONLY in [5]) that performs an energy-optimal voltage scaling without consideration of the energy consumption in the DC-DC converter, and our DC-DC converter-aware scheme (DC_DVS). Note that MPEG is a single task and the rest of the designs are multiple tasks. Thus, DC_DVS-1 is applied to MPEG and DC_DVS-m is applied to the rest. The deadline column indicates that each design is tested three times with the normal deadline D, a reduced deadline from D, and an extended deadline from D. The deadlines of designs AVN and CNC could not be reduced to 50% in experiment because of infeasible schedule even using the highest voltage, thus reduced to 10% and 40%, respectively. In summary, DC_DVS is able to reduce the total energy consumption up to 15.5% further compared to the DC-DC converter-unaware conventional optimal DVS techniques for four different configurations of DC-DC converters.

• **Assessing the effectiveness of** DC-lp: On the other hand, Table 2 shows comparisons of energy consumption by NO_DVS and DVS_ONLY with two fixed values of W, *i.e.*, $W = 30$ and $W = 40$, and DC-lp with $[W_{min}, W_{max}]$ = [10, 50]. The comparisons reveal that DC-lp performs well both of the voltage scaling and the selection of converter configuration to save the total energy consumption, resulting in 16.0% energy reduction for $W = 30$ and 22.1% energy reduction for $W = 40$ over that by DVS_ONLY, which strongly implies that the problem of selecting converter configuration that is best suited for the target application program is as much important as the problem of voltage scaling to reduce energy consumption.

5. CONCLUSION

It is known that a DC-DC converter is an essential component for voltage scaling, and 10%∼40% of total energy consumed in the whole system is due to the converter itself. In that respect, in this paper, we proposed an effective approach to the problem of integrating the effects and optimization of a DC-DC converter into a well-known DVS scope. Specifically, we proposed a DC-DC converter-aware low-power DVS technique, DC-lp, in which two core subproblems, *DC-DC converter-aware energy-minimal DVS*

Design	deadline constraint	Normalized energy consumption with W=**20** NO_DVS	DVS_ONLY	DC_DVS	red. over DVS_ONLY	Normalized energy consumption with W=**30** NO_DVS	DVS_ONLY	DC_DVS	red. over DVS_ONLY
MPEG	D	1	0.467	0.442	5.4%	1	0.567	0.515	9.2%
	D×0.5	1	0.455	0.455	0%	1	0.518	0.518	0%
	D×1.5	1	0.467	0.442	5.4%	1	0.567	0.515	9.2%
VP	D	1	0.457	0.442	5.4%	1	0.567	0.515	9.2%
	D×0.5	1	0.461	0.461	0%	1	0.521	0.521	0%
	D×1.5	1	0.457	0.442	5.4%	1	0.567	0.515	9.2%
AVN	D	1	0.765	0.765	0%	1	0.785	0.785	0%
	D×0.9	1	0.907	0.907	0%	1	0.914	0.914	0%
	D×1.5	1	0.485	0.485	0%	1	0.539	0.539	0%
CNC	D	1	0.460	0.460	0%	1	0.523	0.523	0%
	D×0.6	1	0.748	0.748	0%	1	0.769	0.769	0%
	D×1.5	1	0.462	0.442	4.3%	1	0.557	0.515	7.7%
Design	deadline constraint	Normalized energy consumption with W=**40** NO_DVS	DVS_ONLY	DC_DVS	red. over DVS_ONLY	Normalized energy consumption with W=**50** NO_DVS	DVS_ONLY	DC_DVS	red. over DVS_ONLY
MPEG	D	1	0.655	0.573	12.5%	1	0.737	0.622	15.5%
	D×0.5	1	0.573	0.573	0%	1	0.624	0.622	0.2%
	D×1.5	1	0.655	0.573	12.5%	1	0.737	0.622	15.5%
VP	D	1	0.655	0.573	12.5%	1	0.737	0.622	15.5%
	D×0.5	1	0.574	0.574	0%	1	0.622	0.622	0%
	D×1.5	1	0.655	0.573	12.5%	1	0.737	0.622	15.5%
AVN	D	1	0.800	0.800	0%	1	0.814	0.814	0%
	D×0.9	1	0.920	0.920	0%	1	0.925	0.925	0%
	D×1.5	1	0.585	0.585	0%	1	0.627	0.627	0%
CNC	D	1	0.579	0.578	0.2%	1	0.630	0.625	0.8%
	D×0.6	1	0.787	0.787	0%	1	0.803	0.803	0%
	D×1.5	1	0.643	0.573	10.8%	1	0.721	0.622	13.6%

Table 1: Comparisons of energy consumed by no DVS scheme (NO_DVS), DC-DC converter-unaware DVS scheme (DVS_ONLY) and our DC-DC converter-aware DVS technique (DC_DVS) for benchmark programs where W represents the configuration parameter of the DC-DC converter used.

Design	Normalized energy consumption $W = 30$ NO_DVS	DVS_ONLY	W=**[10,50]** DC-lp	red. over DVS_ONLY	$W = 40$ NO_DVS	DVS_ONLY	W=**[10,50]** DC-lp	red. over DVS_ONLY
MPEG	1	0.567	0.369	34.8%	1	0.655	0.364	44.4%
VP	1	0.567	0.369	34.8%	1	0.655	0.364	44.4%
AVN	1	0.785	0.769	2.0%	1	0.800	0.758	5.3%
CNC	1	0.523	0.410	21.7%	1	0.579	0.404	30.2%
AVN (D× 0.9)	1	0.914	0.909	0.6%	1	0.920	0.896	2.6%
CNC (D× 0.6)	1	0.769	0.751	2.4%	1	0.787	0.741	5.9%
Average				**16.0**%				**22.1**%

Table 2: Comparisons of energy consumed by no DVS scheme (NO_DVS), DC-DC converter-unaware DVS scheme (DVS_ONLY) and our integrated converter-aware DVS (DC-lp) to show how much effectively DC-lp finds energy-efficient configurations of DC-DC converters for each of the tested benchmark programs.

problem and *converter configuration selection problem*, were effectively solved and integrated. In the mean time, the experimental results showed that DC-lp was able to restore over 16.0%∼22.1% of energy loss on the average over that by a DC-DC converter-unaware DVS method. By this, we have a strong belief that a DC-DC converter-aware power management scheme is very necessary and valuable to the embedded system design equipped with variable voltage processors.

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