

DC/DC Converter for Helicopter Starter/Generator

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Master's Thesis

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Abstract

The use of power electronics DC/DC converters in aircraft has increased due to the state-of-art converters developments. However, the volume, efficiency and mass of such converters are critical issues. Each component of the DC/DC converters contributes to the total mass of the system. By designing each component, optimized to have small volume, high efficiency and small mass, the total system can have small volume, small mass and high efficiency.

This master project explores design optimization of dual active bridge (DAB) DC/DC converter components: the capacitors, the cooling system and the transformer. Different types of capacitors are compared in terms of mass, volume and loss for the input and output capacitors. After selecting the types of capacitors, the number, volume and mass of the input and output filter capacitors are optimized by interleaving two and three dual active bridge DC/DC converters. The thermal resistance of external cooling system for the selected switches is optimized by a trade-off between the junction temperature of the switches and the losses induced. The transformer is optimized by an evolutionary algorithm, particle swarm optimization, for volume, power loss and required maximum allowable thermal resistance for cooling.

The three interleaved DAB is found to be attractive in terms of less capacitor number which leads to a small volume and mass. It is also found to be attractive in terms of thermal management of the transformers designed using the particle swarm optimization. This decreases the volume of cooling systems needed for the transformer. Interleaved three DAB is selected as best in terms of volume, mass and thermal management.

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Chapter 1

Introduction

1.1 Background

The increased need for bidirectional power transfer for different application in vehicles, renewable energy and motor drives has attracted power engineers in designing low volume, low mass and high efficiency power electronics circuits. As the practical interest of the aviation industry to make airplanes more electric/all electric has increased, power electronics is playing a major role. The current challenges of using more electric in the aviation industry are the replacement the conventional methods of power transfer methods: hydraulic, mechanical, and pneumatic, with a comparable volume and mass of electrical power transfer methods and the generation of electrical power[1]. Currently due to the increase in energy density of storage devices and the state-of-art converter types, the conventional methods of energy transfer in aircrafts are being replaced by power electronics converters[2].

One of the applications of power converters is in Integrated Starter/Generator (ISG). It is the use of a single AC machine as both a starter and generator, in automotive and aircraft applications where efficiency increment, space and weight reduction is of critical importance [48]. Figure 1.1 shows the block diagram of the system needed for ISG power processing. The DC/DC converter is for boosting the battery voltage and the inverter converts the boosted voltage in to AC.

The DC/DC converter should have the capability of bidirectional power flow. It should convert the low voltage at the terminal of the battery into high voltage at the terminal of the inverter. When the power transfer is from the battery to the ISG (which is defined as motor mode), the voltage raise steps down the current drawn by the ISG. The inverter changes the stepped-up voltage in to a three phase AC voltage required by the ISG. During the power flow from the ISG to the battery (which is called Generator mode), the inverter changes the AC voltage from the terminal of the ISG to DC voltage at the terminal of the DC/Converter. The battery is charged from the stepped down voltage by DC/DC converter.

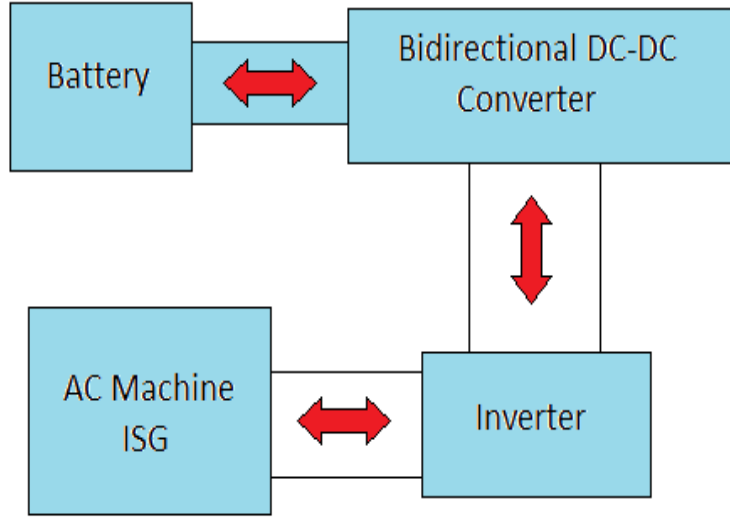


Figure 1.1: Bidirectional DC-DC converter in Integrated Starter/Generator system

1.2 Specification of the investigated converter

The specifications of the bidirectional DC/DC converters investigated in this work have been described as follows. The DC/DC converter comprises of a high voltage (HV) port with the terminal voltage, V_0 (270V maximum value) and a low voltage (LV) port with the terminal voltage , V_i ($13V \leq V_i \leq 28V$). A nominal output power, P_O , of 12kW is required within the specified voltage range in generator mode. Table 1.1 shows the specification. Figure 1.2 shows the power specification graphically. The positive 5 pulses show transient power consumption during motoring for starting the ISG and the constant negative power shows the battery charging power during generating.

Table 1.1: Specification of the DC/DC converter to be investigated

Input Voltage(V)	$13 \leq V_i \leq 28$
Output Voltage(V)	$V_0 \leq 270(\text{Maximum})$
Nominal Power(Kw)	12 (Generating)
Power Peaks(Kw)	23 (20 sec) + 23 (15 sec) + 23 (20 sec) 23 (15 sec) + 23 (20 sec) (Motoring)
Frequency(KHz)	25

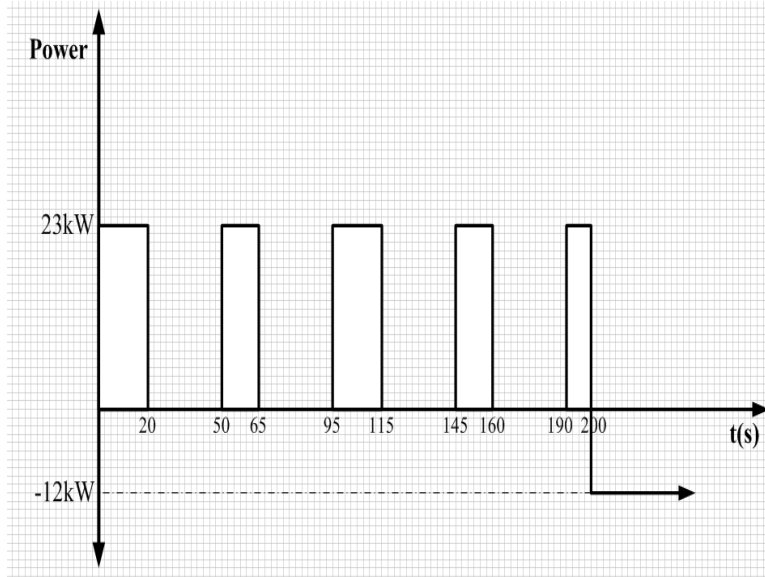


Figure 1.2: Power requirements of ISG

1.3 Objectives and New Contribution of the work

The objective of this work is to select a converter topology which is suitable to fulfill the requirements specified. Furthermore, the selected converter topology is optimized to get a high converter efficiency, low volume and low mass. The works can be explained as follows:

1. A brief overview on bidirectional DC/DC converter topologies, including a comparison of the different converters that are suitable to fulfill the given specifications.
2. Making a pre-selection of circuits (investigate limited number of circuits)
3. Making a design of each of these circuits by doing design optimization on volume, mass and efficiency
4. Comparing designs with respect to performance criteria (weight, volume, efficiency)

The new contribution of this work is

1. Optimizing the required transformer dimensions by an evolutionary algorithm called Particle Swarm Optimization. It is a trade-off optimization between the volume and power loss of a transformer.
2. Determining the number of switches per heatsink with respect to volume and mass of heatsink designed.

1.4 Delimitations

This project is completely theoretical. The proposed setup has not been build and tested. All calculations are based on information given from the manufacturers of the different components. The control system for the converter has not been considered as well.

1.5 Chapter Overview

Chapter 2 is the literature review. It is a brief overview of different bidirectional DC/DC converters. The merits and demerits of different BDCs is explained. It also selects the Dual Active Bridge(DAB) for further investigation based on the requirements specified.

Chapter 3 explains theoretical principles of the a single DAB. It formulates the RMS and average currents of the switches and transformer. It discusses the need of interleaving of 2 and 3 DAB converters. It also shows the relationship between reactive and active power and calculates losses and optimizes heatsink for the switches selected. The design of heatsink optimization is the use of one or two or four switches per heatsink and the heatsink with minimum volume is taken.

Chapter 4 is about optimizing transformer dimensions. It uses an evolutionary algorithm called particle swarm optimization. It discusses a trade-off between the volume,power loss and the heatsink thermal resistance of the transformer. Based on the outputs of the optimization, it selects the core surface area for external cooling system to be attached.

Chapter 5 is conclusion of the work and proposes future works.

Appendices includes results of different repetitive works and datasheets of components selected.

Chapter 2

Related Works

This chapter discusses the overview of different bidirectional DC/DC converters. It also selects one circuit that is suitable for the specifications and objectives described in chapter 1 for further investigation.

The need of bidirectional energy transfer in high-power applications have drawn the use of bidirectional DC-DC converters (BDC). The application of BDC are in uninterruptible power supplies, motor drives, renewable energy storages and full cell energy storages. Different applications use different BDCs. They are classified into two main types, Non-isolated BDC and Isolated BDC.

2.1 Non-Isolated Bidirectional DC-DC converters

The most common non-isolated BDC is the combination of conventional boost and buck converters as shown in figure 2.1[4]. This type of BDC is preferable in high-power application where the main concern is weight and size like in aircraft.

The advantages of non-isolated buck-boost BDC is

1. It is transformer-less which decreases loss and weight [4]
2. The presence of inductor in the Low-voltage side is advantageous for application where lower ripple currents is needed, like in application of batteries.[3].

The disadvantages of non-isolated BDC are

1. When the voltage ratio is high, it becomes impractical [4]
2. There is no galvanic isolation which is necessary for personnel safety, noise reduction and correct operation of protection systems.

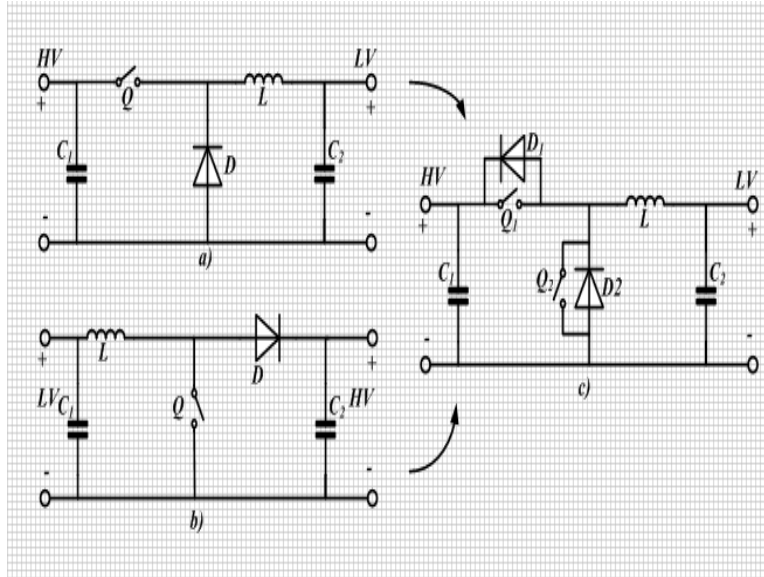


Figure 2.1: Conventional buck-boost converter a) Buck converter b) Boost converter c) Buck-boost converter

2.2 Isolated Bidirectional DC-DC converters

For isolated BDC, an additional transformer is needed which increases the weight and loss of the systems. However, in systems where a high-voltage step-up is a must, isolated BDC are the best choices. There are many types of isolated BDC available for different applications.

2.2.1 Fly-back Converter

Flyback converter is mainly used in lower power application [7]. The advantages of flyback converters are

1. Smaller number of passive and active components
2. Smaller size when it is used in discontinuous conduction mode

The disadvantages are

1. Higher switch voltage stress
2. Only half of the core B-H can be used due to unipolar magnetizing current
3. Low power applications

2.2.2 Dual Active Bridge Converter

It is initially proposed by [13]. There are three types of Dual Active Bridge (DAB) converters: Single phase DAB, three phase DAB and Half Dual Bridge(HDB).

2.2.2.1 Single Phase Dual Active Bridge Converter

It has two voltage sourced full bridge circuits on both the high-voltage and low-voltage side coupled by high-frequency(HF) transformer[13]. It has the following advantages

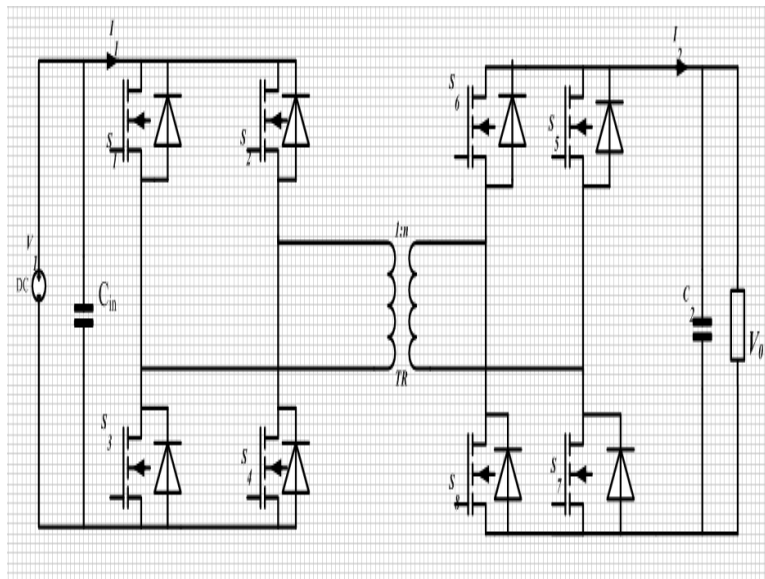


Figure 2.2: Bidirectional Single Phase Dual Active Bridge Converter

1. Low number of passive components
2. Evenly shared currents in the switches
3. Inherent Zero Voltage Switching
4. High power capability [14]
5. Different kinds of modulation techniques possible

It has the following disadvantages

1. Inductor current depends on the input and output voltage ratio
2. High Circulating current

2.2.2.2 Three Phase DAB Converter

Figure 2.3 shows the three phase DAB circuit[13]. It has the following advantages

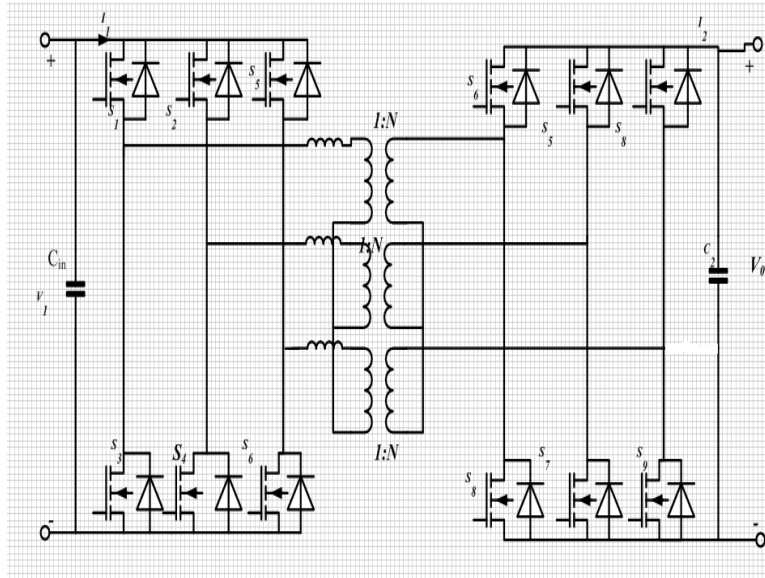


Figure 2.3: Three Phase Dual Active Bridge Converter Topology

1. Low total transformer VA ratings compared to single DAB
2. Low switch VA ratings compared to Single DAB
3. Low magnetic energy storage capability
4. Low RMS capacitors current

And it has the following disadvantages

1. High number of active switches
2. Only conventional modulation scheme is possible
3. Difficulty in achieving the required leakage inductance for peak power transfer which leads to an additional inductor.

2.2.2.3 Dual Half Bridge

It is proposed by [17]. It contains one half bridge in each HV and LV side as shown in figure 2.4. It has the following advantages

1. Low number of switches

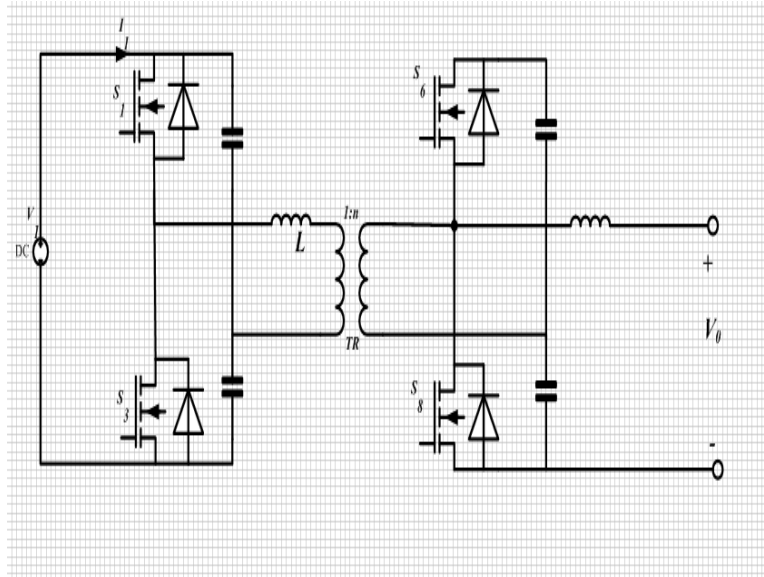


Figure 2.4: Single Phase Dual Half Bridge Converter Topology

2. Same VA ratings of switches as single DAB with conventional phase shift modulation.

However, it has the following disadvantages

1. Unequal RMS switch currents and high blocking voltage
2. LV side capacitor has high RMS current
3. Additional inductor increases the size

2.2.3 Full-bridge Converters

Figure 2.5 shows full-bridge BDC[9]. It has a voltage sourced full bridge on the high-voltage side and a current sourced full bridge on the low-voltage side. Energy transfer is controlled by the Duty cycle. The advantages are

1. Lower capacitor rms current compared to DAB [8]
2. High voltage side zero voltage switching and low voltage side zero current switching is possible[8].

The disadvantages are

1. Transformer turns ratio are limited due to the duty cycle [8]
2. Higher VA ratings of switches compared to DAB

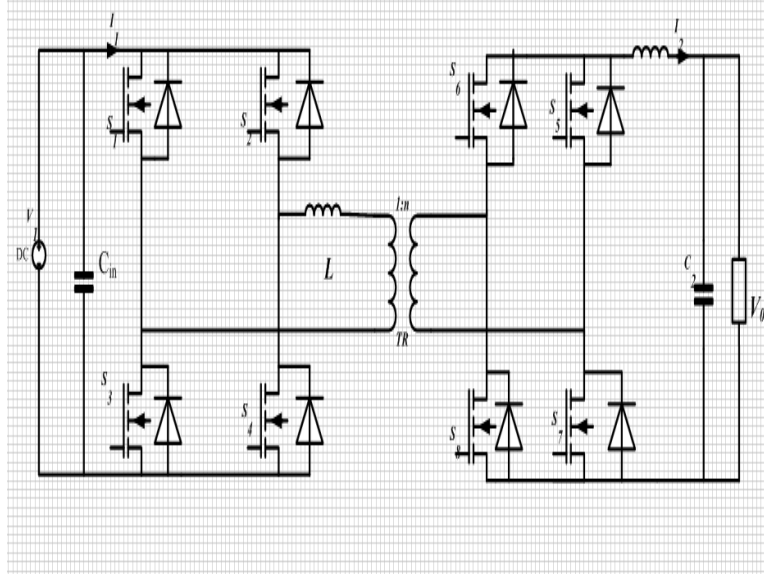


Figure 2.5: Full-bridge Bidirectional Converter Topology

3. Additional volume for the inductor
4. Snubber circuit may be necessary to avoid a spike due to the transformer stray inductance [8]

2.3 Topology Selection

Comparing the above discussed BDCs, for low volume, low weight, high efficiency and complexity of the circuits at high-power requirement, a single phase DAB is found to be very attractive. It has low switch count. The energy transfer inductance can be included in the transformer's leakage inductance which decreases the volume and avoids an additional requirements of inductor. It also has high voltage step up capability.

There are different types of single DAB topologies. They vary on their modulation techniques, interleaving methodologies and soft switching capabilities. A short overview of the different kinds of the single DAB modulation techniques will be presented which address all those features and selected a single DAB with the best feature for the given specifications and objectives.

2.3.1 Single DAB Modulation Techniques

Depending on the specification of the DAB, a zero voltage switching mechanism can be implemented effectively. The type of the switching mechanism depends on voltage ratios of the input and output, and the variation of the load [14].

2.3.1.1 Conventional Phase Shift Modulation

It is the most common modulation technique which operates with a constant switching frequency and maximum duty cycle of both full bridges. The power transfer solely depends on the phase shift between the two full bridges[16]. Its main advantage is simplicity of power transfer which can be controlled using the phase shift. Its disadvantage is its limited operating range with inherent soft switching capability [15]and large rms current in the transformer leakage inductance which makes it unsuitable modulation technique in wide voltage ranges and wide load variations[16].

2.3.1.2 Alternative Modulation Techniques

With the conventional mechanism limited operating ranges, other alternative mechanism of modulation are implemented with the capability of wide range operation and zero current switching on the low voltage switches. Some are based on the operation of one duty cycle principle(1-D), keeping one full bridge at $D = 0.5$, and varying the duty ratio of the second full bridge[10]. This improves the efficiency of the DAB.

2-D operation principles are implemented with a better efficiency comparing to 1-D and conventional modulation techniques. It has wide operating range of voltage and load capability with zero voltage switching as opposed to the conventional[15]. The common 2-D optimization mechanisms are Triangular Current Mode Operation and Trapezoidal Current Mode Operation[11].

Triangular Current Mode Operation enables the zero current switching in the LV side. It has a very high rms current reduction compared to conventional but within the limited power level. Trapezoidal Current mode Operation eliminates the limitation of power level in Triangular current Mode Operation[8].

In [19] the combination of Conventional, Triangular and Trapezoidal mechanisms are used since they each are more efficient in some ranges. The advantage of Alternative modulation mechanism is higher efficiency for wide range input and output voltages and load variations. However, these two types of modulation techniques introduce control complexity compared to conventional phase shift mechanism.

2.3.1.3 Selection of Modulation Techniques

The inverter at the output of the DC/DC converter in figure 1.1 can be used easily to control the output voltage in such a way that the high voltage transferred to the primary is equal to the low voltage when the power transfer is from the generator to the battery. This makes the use of the conventional modulation method preferable as this method has inherent zero voltage switching in all ranges of the duty cycle with a fixed load requirement at steady state. This leads to a higher efficiency and less control complexity compared to the alternative modulation techniques.

2.3.2 Interleaving of Converters

The use of a number of converters in parallel sharing same input and output in high power converter application is called interleaving.

Recently, due to the need of high power application demands in automobiles and aircrafts, the use of cellular architecture to construct a single large converter system is becoming more general approach[43]. Each converter shares a fraction of the total power. The advantages of using interleaving mechanism is

1. The failure of a single converter does not compromise the system failure. This increases the reliability of the converters.
2. A large degree of input and output ripple cancellation in the input and output waveforms. The waveforms of each converter in the interleaved system can be displaced in phase over a switching period. This leads to harmonic cancellation among the interleaved converters and leads to a low ripple amplitude and high ripple frequency in the input and output waveforms. For N converters in parallel, interleaving increases the fundamental frequency by N and decreases the ripple amplitude by $\frac{1}{N}$ in the input and output capacitors[44].
3. The decrease of capacitance value and rms ripple current decreases the expected number, volume and mass of the input and output filter capacitors in high current and high power applications.

2.3.2.1 Low Voltage Side interleaving

For high-power application where a very high current is expected in the low voltage side, a number of converters in the low voltage side interleaved is proposed in [8]. In figure 2.6, two full bridges are interleaved in the low-voltage side. It decreases the ripple current in the input capacitor.

It uses a single transformer. However, the attainment of leakage inductance and design of transformer is complex. Hence, an external inductor can be introduced for transferring the required power.

2.3.2.2 Low-Voltage and High Voltage side interleaving

A number of DABs can be interleaved either in Parallel Input and Parallel Output (PIPO) configuration or Parallel Input and Series Output(PISO) configuration as shown in figure 2.7[21].

PIPO is mainly used when the low-voltage and low-voltage have high current requirements. This decreases the ripple rms current in the input and output capacitors. It also increases the fundamental frequency of the input and output waveforms by a factor of the number of DABs interleaved. This decreases the value of input and output capacitance which results in a less number of capacitors.

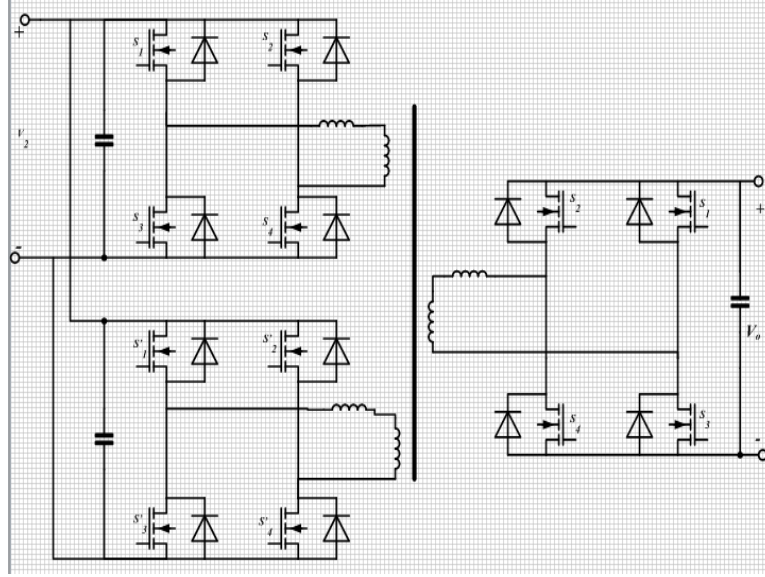
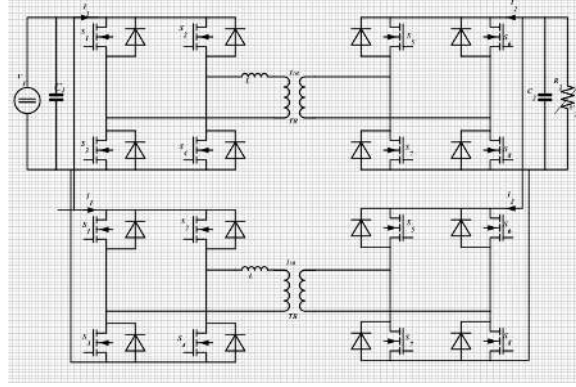


Figure 2.6: Two full-bridges interleaved in the low-voltage side

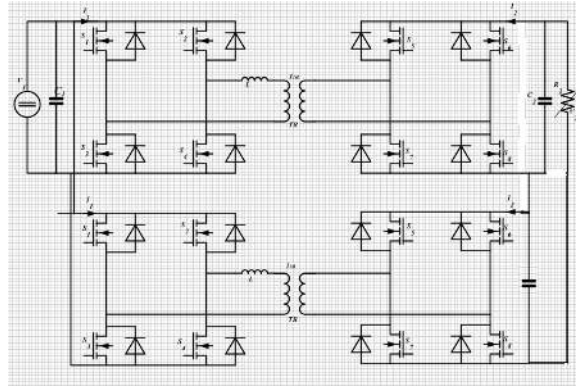
PISO is mainly used when a high voltage is required in the high-voltage side with a very low-current. It has same effect as PIPO in fundamental frequency increment.

In PIPO and PISO, each interleaved converter type can be designed with a desired level of power. However, most of the time, load is shared among all interleaved converters equally.

Due to the high-power requirement and relatively low voltage of the high-voltage side of the specification, a relatively high current in both high-voltage and low-voltage sides is expected. Therefore, PIPO is selected for further investigation in this master project. The number of topologies to be investigated are a single DAB, two PIPO interleaved DABs and three PIPO interleaved DABs.



(a)



(b)

Figure 2.7: Interleaving a number of DABs in the low-voltage and high-voltage sides a) Parallel Input and Parallel Output circuit configuration for two DABs b) Parallel Input and Series Output configuration for two DABs

2.4 Conclusion

The dual active bridge with phase shift modulation is selected for further investigation. Moreover, two and three interleaved dual active bridges will be compared to a single dual active bridge to see which one of the three has low mass, low volume and high efficiency.

Basically the three phase DAB and three interleaved DABs are the same except that the former uses one core of transformer for the three phase and the latter uses three different transformer cores for each interleaved DABs. The difference between the two circuit configuration is that the easiness of attaining the inductance required for transferring power in transformer core. Due to the low value of inductance needed for transferring power in DABs, including the inductance in the leakage inductance of the three phase transformer of three phase DAB is difficult [13]. However, including the small value of inductance accurately to the needed value is easy in each single phase of the three interleaved DABs. This is why three interleaved DAB is selected over three phase DAB.

Chapter 3

Steady State Operation of Dual Active bridge

This chapter deals with steady state analysis of a single DAB and the selection of capacitor, switches and designing of heatsinks with fan for cooling . First, the waveforms and RMS currents of each active and passive devices will be formulated to calculate the rating of each device. Different operating points of the DAB that decreases the volume, mass and loss of the whole DC/DC converters will be analyzed.

After calculating the rating of the input and output filter capacitors, different types of capacitors are compared with respect volume, mass and losses. The mass, volume and loss for single, two interleaved and three interleaved DAB will also be compared and the best one will be determined.

The selection of transistor types for the primary and secondary full bridges based on the estimated rms currents and input and output voltages is done. For each selected transistor type, the selection of junction temperature has huge effect on the mass and volume of the cooling system and the loss of the switches. The junction temperature determines the on-resistance of the switches. The on-resistance also determines the selected switches losses. A trade-off between the junction temperature and the maximum allowable thermal resistance of the heatsink for the switches is optimized to have a small volume, low mass and high efficiency. At last, junction temperatures and thermal resistance values that develop low volume, low mass heatsinks and high efficiency are selected.

After selecting the heatsinks' maximum allowable thermal resistance, optimized mechanical design of heatsinks with fans to have high cooling system power density is implemented.

The single phase DAB shown in 3.1 is selected as the best for the application which was originally proposed in [[13], [14]]. It consists of two full bridges coupled via transformer. Both bridges generate a square wave voltage at the terminals of the transformer. Its steady state analysis is presented assuming it works in phase shift modulation where both the full bridge are at 50% duty cycle. The high voltage side is transferred to the primary low side voltage that is $V_o' = \frac{V_o}{n}$, where n is the turns ratio of the transformer. The transformer's leakage inductance stores and transfers the power. The amount of power transfer depends on the phase shift between the two full bridges.

Power is transferred from the leading to the lagging bridge.

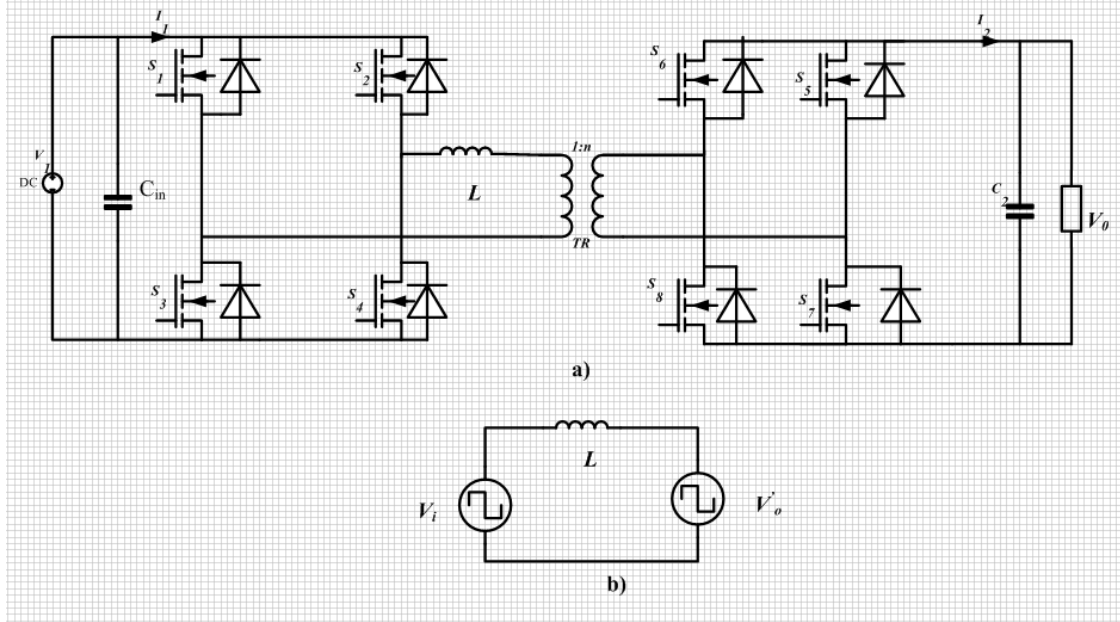


Figure 3.1: a) Dual Active Bridge b) Equivalent circuit of the Dual Active Bridge transferred to primary

For simple analysis, the following assumptions are made.

1. All losses are neglected
2. Magnetizing inductance is neglected
3. All variables and parameters are transferred to the low voltage side and
4. The voltages are constant

3.1 DAB leakage Inductance and power transfer

The relationship between the leakage inductance and power transfer will be developed. There are several mechanisms of modulation techniques in DAB[[13]]. The so-called phase shift modulation method is used to analyze the DAB to find the waveforms shown in figure 3.2. The phase shift between the waveforms generated by the full bridges is φ . At steady state, the leakage current has the waveform shown in figure 3.2d.

when $0 \leq \theta \leq \varphi$,

$$i_L(\theta) = i_L(0) + \frac{V_i(1 + M)\theta}{\omega L} \quad (3.1)$$

where $i_L(\theta)$ is the instantaneous inductor current, V_i is the input voltage, θ is rad, L is the leakage inductance, $M = \frac{V_o'}{V_i}$ and V_o' is the secondary voltage transferred to primary.

When $\varphi \leq \theta \leq \pi$, the instantaneous current is given by

$$i_L(\theta) = i_L(\varphi) + \frac{V_i(1-M)}{\omega L}(\theta - \varphi) \quad (3.2)$$

At steady state, $i_L(0) = -i_L(\pi)$ in figure 3.2d which leads to

$$i_L(0) = \frac{V_i(1-M)}{2\omega L}(\pi M - 2M\varphi - \pi) \quad (3.3)$$

The output power for the ideal DAB is found to be as [13]

$$P_O = V_i I_i = V_O I_O = \frac{V_i^2 M \varphi}{\omega L} \left(1 - \frac{|\varphi|}{\pi}\right) \quad (3.4)$$

where $-\pi \leq \varphi \leq \pi$ and $P_O \geq 0$ if the power transfer is from primary to secondary ($0 \leq \varphi \leq \pi$) and $P_O \leq 0$ if the power transfer is from secondary to primary ($-\pi \leq \varphi \leq 0$).

The power transfer is maximum at $\varphi = \pm \frac{\pi}{2}$ and is given by 3.5

$$P_{MAX} = \frac{V_i^2 M \pi}{4\omega L} \quad (3.5)$$

Although the operation for $|\varphi| > \frac{\pi}{2}$ is possible, to avoid excessive reactive current which causes high conduction losses, the phase shift, $|\varphi|$, should be less than $\frac{\pi}{2}$. From equation (3.4) the relationship between power flow and φ is given in figure 3.3 for $M = 1$.

In figure 3.2d, the transformer peak current is dependent on the value of M . Moreover, the peak current of the input and output current waveforms shown in 3.2e and 3.2f are also dependent on the value of M . For M equals to one, the peak value is smaller than for M greater or less than one. The peak current specifies the transformer, the input and output filter capacitors and the switches peak current capability. Therefore, making the voltage ratio equals to one always makes the peak current capability of the switches, transformer and capacitors less. This decreases the number of transistors and the input and output filter capacitors to be used.

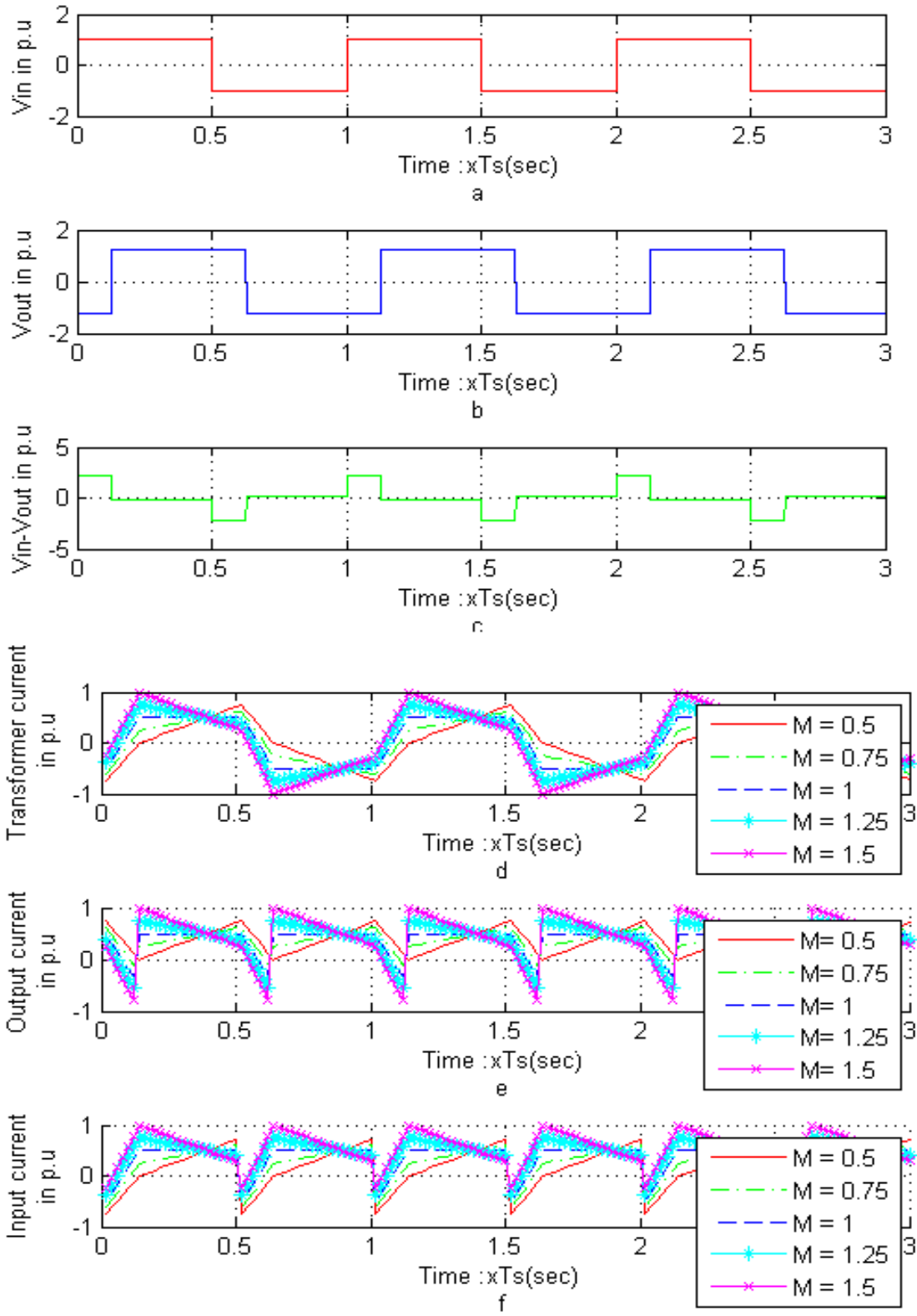


Figure 3.2: Waveforms of single phase DAB for different values of $M = \frac{V_o'}{V_i}$. T_s is the period.

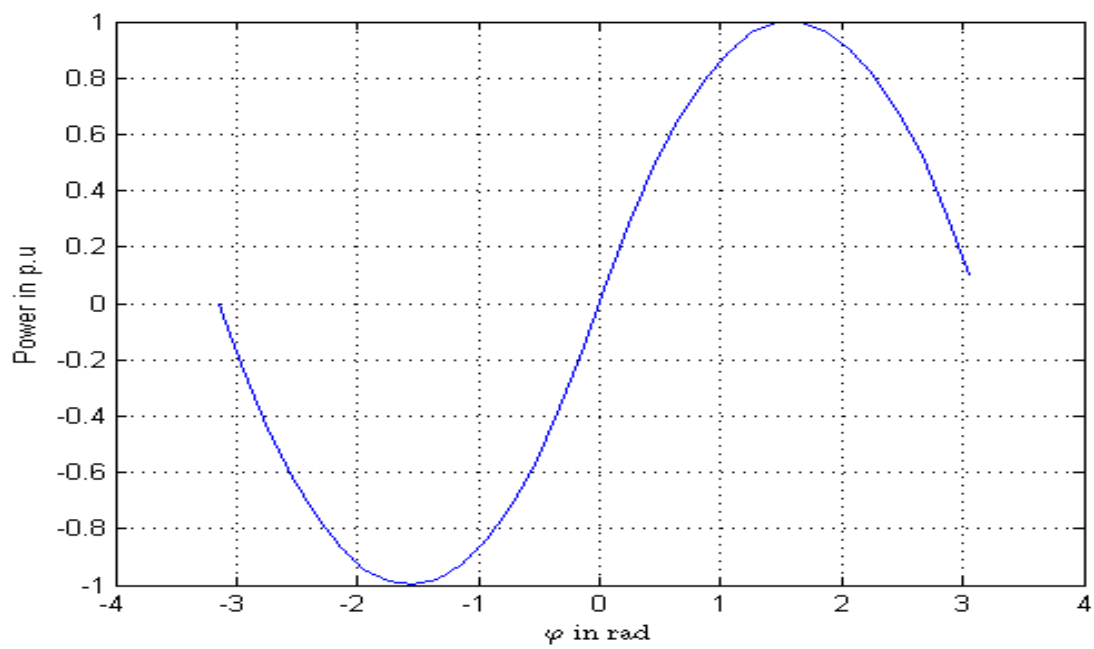


Figure 3.3: Power transfer in pu as a function of phase angle, φ

3.2 RMS current of DAB

The current waveforms for each time interval will be described with respect to the corresponding conducting switches. These piecewise equations will be used to derive the RMS and average currents flowing through each active and passive devices, which will be subsequently used to define their required current rating. The currents within each of the respective devices are derived under the assumption of lossless components. The rms currents and voltages will be used to define the ratings of each device.

The phase shift between V_i and V_o' is φ and can be expressed in the time domain as $\frac{dT_s}{2}$ where T_s is the switching period and d is the duty cycle which is described as $\frac{\varphi}{\pi}$. The piecewise linear waveform of the leakage inductance current, $i_L(t)$, is shown in figure 3.4.

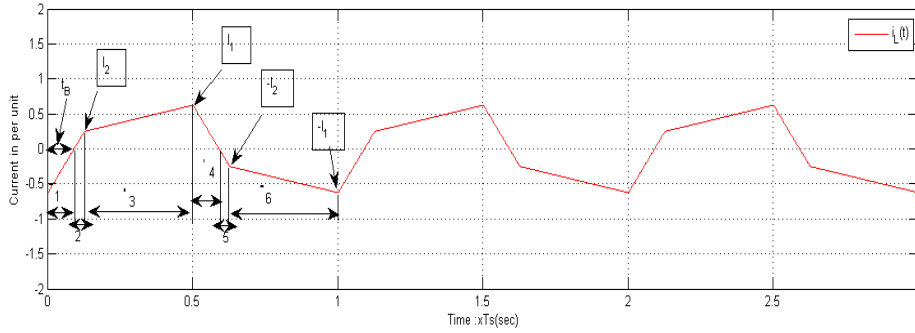


Figure 3.4: Transformer Current waveform for $M < 1$

The triggered and conducting devices of the DAB are listed in table 3.1 for each region shown in figure 3.4. The numeric subscripts in table 3.1 are used to indicate which respective transistor or diode is being considered in figure 3.1. The current directions for each region in table 3.1 are

Table 3.1: Conducting devices in the six regions a period of the leakage inductance current

Region	Conducting Devices	Triggered Devices
1	D_1, D_4, D_2', D_3'	T_1, T_4, T_2', T_3'
2	T_1, T_4, T_2', T_3'	T_1, T_4, T_2', T_3'
3	T_1, T_4, D_1', D_4'	T_1, T_4, T_1', T_4'
4	D_2, D_3, D_1', D_4'	T_2, T_3, T_1', T_4'
5	T_2, T_3, T_1', T_4'	T_2, T_3, T_1', T_4'
6	T_2, T_3, D_2', D_3'	T_2, T_3, T_1', T_4'

shown in figure 3.5.

When $0 \leq t \leq \frac{dT_s}{2}$,

$$V_i + V_o' = L \frac{I_1 + I_2}{d \frac{T_s}{2}} \quad (3.6)$$

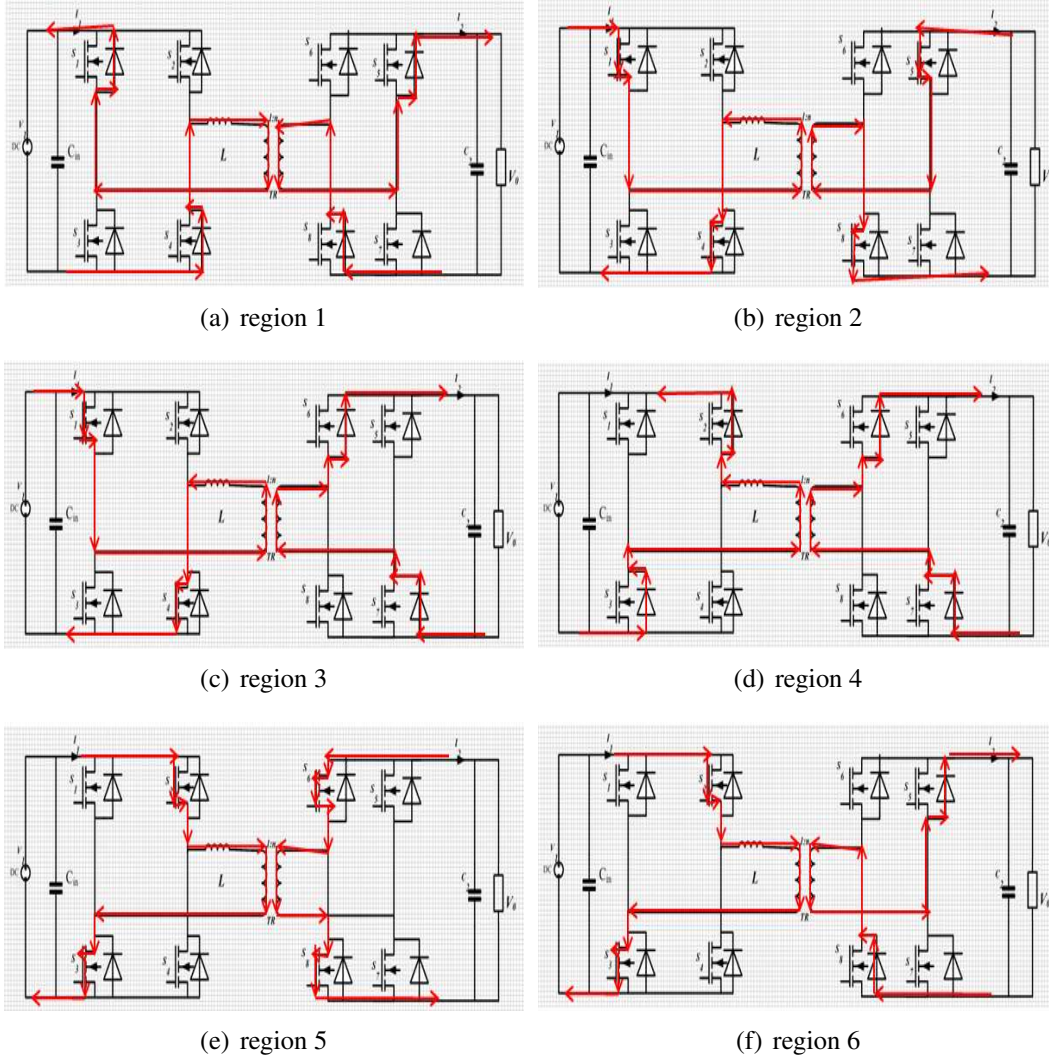


Figure 3.5: Current directions of the dual active bridge for phase shift modulation for the six steps listed in table 3.1

where I_1 is the primary transformer current at $\frac{dT_s}{2}$, I_2 is the primary transformer current at $\frac{T_s}{2}$. And when $\frac{dT_s}{2} \leq t \leq \frac{T_s}{2}$,

$$V_i - V_o' = L \frac{I_1 - I_2}{d\frac{T_s}{2}} \quad (3.7)$$

where t_B is the time the current takes to go to zero from the initial value shown in figure 3.4. Using equations (3.6) and (3.7), the values of I_1 , I_2 and t_B in figure 3.4 are

$$\begin{aligned}
I_1 &= \frac{T_s}{4L} (2V_O' d + V_i - V_O') \\
I_2 &= \frac{T_s}{4L} (2V_i d - V_i + V_O') \\
t_B &= \frac{T_s}{2} \left(\frac{2V_O' d + V_i - V_O'}{2(V_O' + V_i)} \right)
\end{aligned} \tag{3.8}$$

The value of the peak current of a DAB is not only dependent on the value of input and output voltages, but also on the phase shift, φ . For equal input and output voltage values transferred to the primary, doubling the phase shift, doubles the peak current. Therefore, when choosing the value of phase shift range, considerations should be given to the peak current value.

Assuming the power is transferred from the primary, low-voltage side to the secondary, high-voltage side, equations (3.8) can be used to determine the RMS value of the transformer current, as referred to primary. The LV and HV rms currents of each device are listed in table 3.2, where $I_r = I_1 - I_2$ and the average currents are listed in table 3.3[18]. These formula are used to calculate the losses in the devices.

Table 3.2: RMS current of Devices In LV and HV sides[[18]]

Devices	Devices RMS current
Transformer($I_{L_{rms}}$)	$\sqrt{\frac{2}{T_s} \left(\frac{I_2^2}{3} (d \frac{T_s}{2} - t_B) + (\frac{T_s}{2} - \frac{dT_s}{2}) (I_2^2 + \frac{I_r^2}{3} + I_2 I_r) + \frac{I_1^2 t_B}{3} \right)}$
LV side Switches	$\sqrt{\frac{1}{T_s} \left((\frac{T_s}{2} - \frac{dT_s}{2}) (I_2^2 + \frac{I_r^2}{3} + I_2 I_r) + \frac{I_1^2 t_B}{3} \right)}$
LV side diodes	$\sqrt{\frac{1}{T_s} \left(\frac{I_2^2}{3} (\frac{dT_s}{2} - t_B) \right)}$
HV side switches	$\sqrt{\frac{1}{T_s} \left(\frac{I_1^2 t_B}{3} \right)}$
HV side Diodes	$\sqrt{\frac{1}{T_s} \left(\frac{I_2^2}{3} (d \frac{T_s}{2} - t_B) + (\frac{T_s}{2} - \frac{dT_s}{2}) (I_2^2 + \frac{I_r^2}{3} + I_2 I_r) \right)}$

When the power transfer is from the high-voltage side to the low-voltage side, the RMS and average current equations of diodes and switches should be interchanged in the LV and HV sides respectively [18].

For a given duty cycle and leakage inductance, the values of rms current in table 3.2 and average current in table 3.3 depends on the values of I_1 and I_2 . Both values are dependent on M . For constant input and output voltages, leakage inductance and duty cycle, the rms and average currents are minimum at $M = 1$. The values of M determines the rms and average currents through the switches and their anti-parallel diodes. The rms and average currents determine the losses. Therefore, designing the DAB to have M equal to one would decrease the losses and decreases the cooling system accordingly.

Table 3.3: Average current of Devices In LV and HV sides referred to primary [[18]]

Devices	Devices Average current
LV side Switches	$\frac{\frac{1}{2}(I_2+I_1)\left(\frac{T_s}{2}-d\frac{T_s}{2}\right)+\frac{1}{2}I_1t_B}{T_s}$
LV side diodes	$\frac{\frac{1}{2}I_2\left(d\frac{T_s}{2}-t_B\right)}{T_s}$
HV side switches	$\frac{\frac{1}{2}I_1t_B}{T_s}$
HV side Diodes	$\frac{\frac{1}{2}I_2\left(d\frac{T_s}{2}-t_B\right)+\frac{1}{2}(I_2+I_1)\left(\frac{T_s}{2}-d\frac{T_s}{2}\right)}{T_s}$

3.3 Zero Voltage Switching of Phase Shift Modulated DAB

This section shows the relationship between the duty ratio, d , and voltage ratio, M , in order to get a zero voltage switching in phase shift modulation. Zero voltage switching(ZVS) is switching of a transistor when the voltage across the device is zero. In phase shift modulated DAB, ZVS is acquired if the anti-parallel diode of a switch is conducting when the transistor is triggered. In phase shifted modulation DAB, for the anti-parallel diode to conduct while the switches are triggered, I_1 and I_2 in figure 3.4 has to be positive for switches 1 and 4 or negative for switches 2 and 3. Solving (3.8) gives the following boundary conditions for soft switching:

$$\begin{aligned} d &\geq \frac{(M-1)}{2M}, \text{ if } M > 1 \\ d &\geq \frac{1-M}{2}, \text{ if } M < 1 \end{aligned} \quad (3.9)$$

Attaining inherent zero voltage switching in all ranges of of the duty cycle decreases the switches losses considerably. This decrease in loss has two main advantage. The first one is that the efficiency increases. The second one is that due to the loss reduction, the volume and mass of the cooling system decreases. For $M = 1$, zero voltage switching for any angle $\varphi = d\pi$ is fulfilled as can be seen in Figure 3.6. If the voltage gain between the input and output voltage is 2, the phase shift has to be at least 0.25 to have zero voltage switching in phase shift modulation. As can be seen from figure 3.6, as the duty cycle decreases so does the zero voltage switching range of the allowable voltage range. This shows phase shift modulation is ideally suited for small variation in voltages and loads.

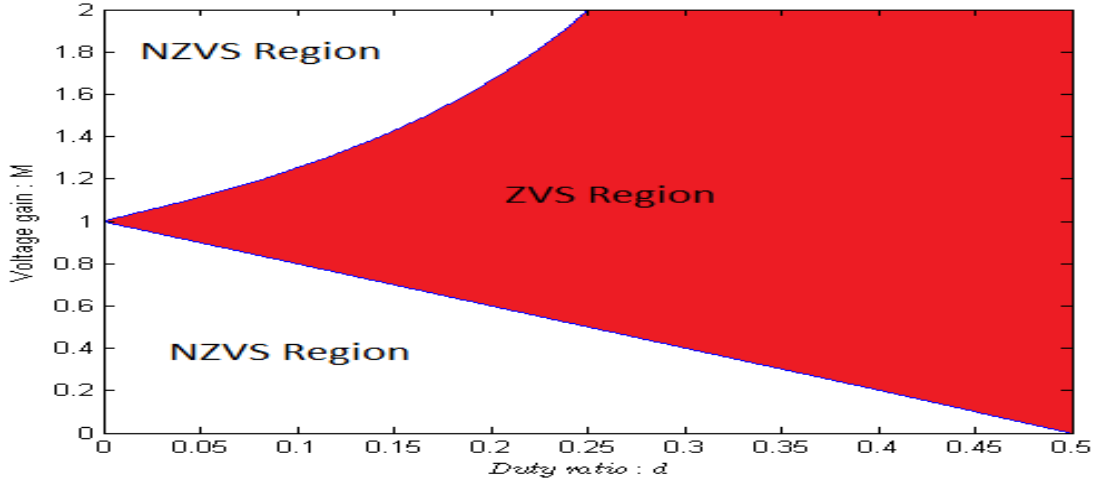


Figure 3.6: Soft Switching Boundaries

3.4 Transformer Apparent Power

The transformer apparent power is [13]

$$VA_T = \frac{1}{2}(V_i I_i + V'_O I'_O) = 0.5V_i(M + 1)I_i \quad (3.10)$$

Where VA_T is apparent power of the transformer, subscript T stands for transformer, $V'_O = MV_i$ is the secondary voltage transferred to primary. $I_i = I'_O$ as the magnetizing current is assumed zero. Assuming equation 3.5 as base unit, the output power in base unit is

$$P_{opu} = 4Md(1 - d) \quad (3.11)$$

and the VA_T in base unit is

$$VA_{Tpu} = \frac{(M + 1)I_{L_{rms}}4FL}{V_i} \quad (3.12)$$

where $I_{L_{rms}}$ is the rms transformer current calculated using equation in Table 3.2 and F is the switching frequency. The VA rating of the transformer is dependent on the voltage gain and rms transformer current where the transformer current is mainly dependent on the phase shift, φ , and voltage ratio, M , as shown in figure 3.7. When the phase shift is zero, the VA value of the transformer is nonzero for all values of the voltage ratio except for $M = 1$ even though there is no real power transfer. As the voltage ratio and phase shift increase, the VA of the transformer increases.

One possible solution for decreasing the apparent power is decreasing the circulating current of the DAB by decreasing the phase shift. However, in low values of the phase shift, controlling the DAB becomes difficult as it is very sensitive to change in phase shift. Small increase in phase shift increase the power transfer by very high value as shown in figure 3.3. So when choosing the range of phase shift, circulating current and controllability have to be considered. The range between 15° and 45° is normally a good range for both conditions[15].

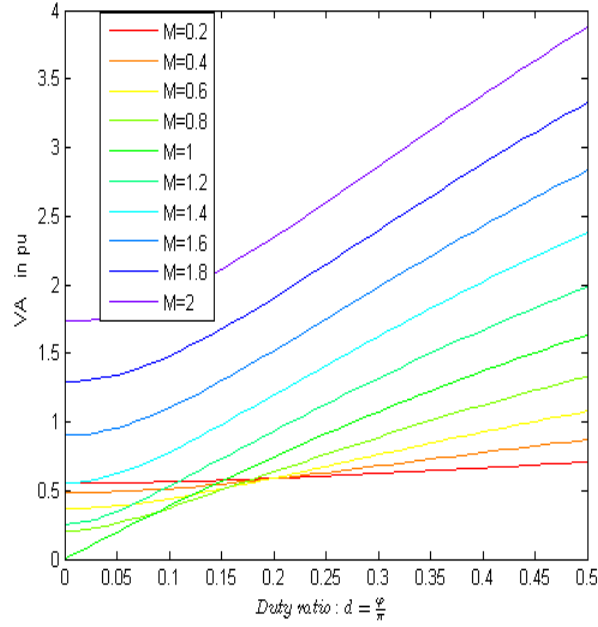


Figure 3.7: VA of Transformer as a function of duty ratio, $d = \frac{\varphi}{\pi}$ for different values of M . [13]

The relationship between real power and apparent power of the transformer is shown in figure 3.8. This helps to calculate the utilization factor of the transformer. For the power per unit between one and zero, the VA of the transformer per unit for $M = 1$ is less than any other M value. This means for a given real power transfer at $M = 1$, the transformer has small mass and volume than designed at other M values. At power per unit of 0.4, for $M = 2$, the VA per unit is greater than 2. However, for $M=1$, the VA per unit is less than 0.5. This means the VA rating of the transformer designed at $M = 2$ is $4 (\frac{2}{0.5})$ of the VA rating of the transformer designed at $M = 1$ for transferring same amount of real power. Therefore, the transformer size at $M = 2$ is expected to be bigger in volume, mass and loss. This shows that depending the range of controllability or maximum power transfer, various design points can be taken [12].

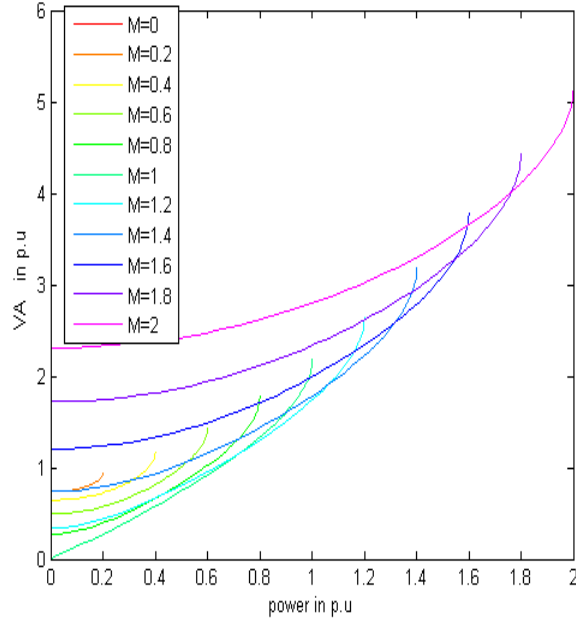


Figure 3.8: $V A_{pu}$ of transformer as a function of P_{opu} . [13]

3.5 Interleaving

Interleaving in high power application is defined as the use of a number of converters in parallel sharing same input and output in order to realize a desired power level. The various advantages of interleaved converters, phase displacement amount the converters and their associated impacts on ripple current will be discussed in this section.

Recently, due to the need of high power application demands in automobiles and aircrafts, the use of cellular architecture to construct a single large converter system is becoming a more general approach [43]. Each converter shares a fraction of the total power. The advantages of using interleaving mechanism is

1. The failure of a single converter does not compromise the system failure. This increases the reliability of the system
2. A large degree of input and output ripple cancellation in the input and output waveforms. The waveforms of each converter in the interleaved system can be displaced in phase over a switching period - phase displacement. This leads to harmonic cancellation among the interleaved converters and leads to a low ripple amplitude and high ripple frequency in the input and output waveforms. For N converters in parallel, interleaving increases the fundamental frequency by N and decreases the ripple amplitude by $\frac{1}{N}$ in the input and output capacitors[44].

3.5.1 Determining Interleaving Angles of DABs

For interleaved DABs, the best displacement phase between the DABs that decrease the magnitude of input and output capacitor ripple currents and increase the ripple current frequency should be determined. Matlab code is, therefore, developed to determine the phase displacement between the DABs that leads to maximum decrease in the ripple RMS currents through the input and output capacitors for two and three interleaved DABs. Figure 3.9 shows the per unit value of currents in varying the phase shifts from 0 to 180 degrees among the DABs. It shows that 90° and 60° or 120° are the phase shifts which result in the lowest rms ripple currents for two and three interleaved DABs in input and output capacitors respectively. This decreases the volume, mass, loss and required capacitance which are quantitatively discussed in section 3.6.2.

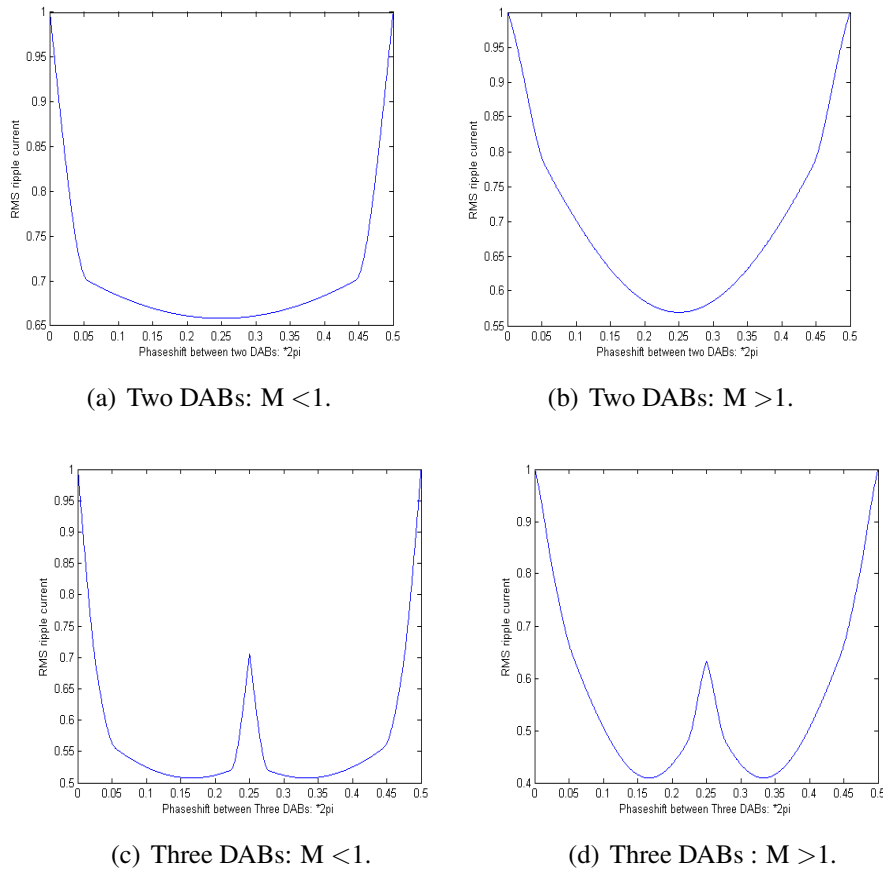


Figure 3.9: Rms ripple current in a capacitor as a function of the phase displacement a) For the two and three interleaved DABs at

The graphs in figure 3.9 are for $M = 0.964$ and $M = 1.03$. However, the angle at which the interleaved converters have minimum ripple current depends on the shape of the waveform. All ripple currents for $M > 1$ and $M < 1$ have same shape respectively. Therefore, the angle at which the converters have minimum ripple current when interleaved for $M > 1$ and $M < 1$ are same for a given number of converters interleaved.

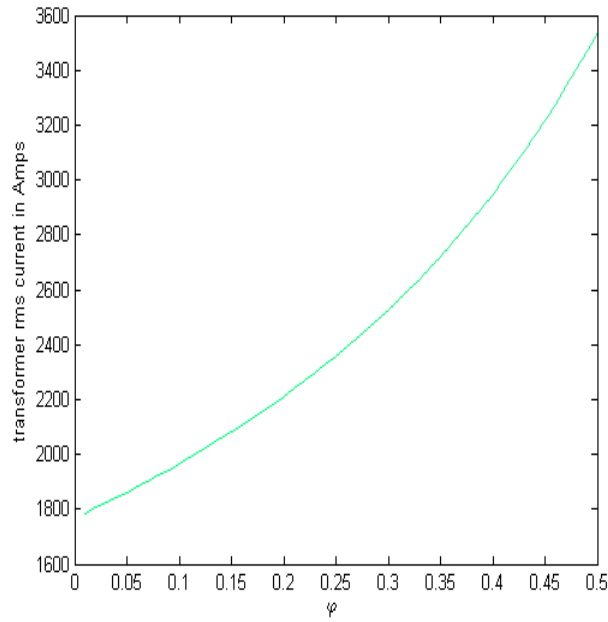


Figure 3.10: RMS transformer current for different values of phase shift of one DAB topology at peak power

3.5.2 Determining Peak Power Transferring Angle

The angle for the peak power transfer is 90° . Figure 3.10 shows the peak current, calculated using equation 3.5, assuming the peak power is delivered to the output by varying the phase shift between 0 and $\frac{\pi}{2}$. For one DAB, for the given specification, the primary peak current becomes 3538 Amps for the 23KW(peak power) at 90° . If 45° is taken for the peak power transfer, the primary current becomes 2358 Amps which decreases the ratings and number of switches and rating of transformer substantially. The mere disadvantage of lowering the peak power transfer angle is that it lowers the angle for transferring rated power at rated voltages from 5.2° to 3.78° calculated using 3.5 with nominal power and nominal voltages. This would cause a significant problem in controlling if the load were variable but the load is constant at rated specifications. Moreover, as can be seen in equation 3.4, the decrease of phase shift decreases the required leakage inductance.

3.5.3 Determining the turns ratio of the transformer

The voltage ratio, $M = \frac{V_i}{\frac{V_o}{n}}$, is not only dependent on the voltage values of the input and output but also dependent on turns ratio of the transformer. Moreover, during motoring the voltage at the primary terminals of the DC/DC converter goes down to 13 Volts due to the loss at series resistance of the battery and during generating the voltage at the primary terminal of the DC/DC converter is at least the battery terminal. Therefore, the selection of a turns ratio should consider both generating and motoring.

During motoring, since the output is a load, not an independent source, the output voltage can be dictated by the duty ratio for a given battery voltage and leakage inductance using equation 3.4. Therefore, for any battery voltage, it is possible to have a voltage ratio of one for any value of turns ratio. However during generating, the battery and the inverter are two independent voltage sources. Therefore, it is impossible to control the two voltage by duty ratio. However, the output of the inverter can be controlled in such a way that when transferred to primary to be equal to the battery side primary full bridge terminal voltage. This makes the voltage ratio equal to one which have greater advantage in terms of having low peak current, low rms currents and small VA rating for a required real power transfer as discussed in previous sections.

Therefore if a voltage ratio, M , can be made to be one during generating, it can be easily made one during motoring. During generating the battery voltage is 28 V and the inverter output is assumed to be the maximum, 270 volts. Therefore,

$$n = \frac{270}{28} \approx 9 \quad (3.13)$$

So, the turns ratio is set to be 1:9, the ratio of primary to secondary voltage.

3.6 Dual Active Bridge Design

This chapter discusses the selection of devices based on the requirements of the current level and voltage. First, switches for the low voltage and high voltage side will be selected and their loss for single DAB, Two interleaved DABs and Three interleaved DABs will be discussed. Secondly, capacitors for each type of topology will be selected and their volume, mass and loss will be calculated and compared. After that, different heat-sink arrangements for cooling the switches will be compared in terms of mass and volume.

3.6.1 Switches Selection Considerations

The rms and average currents of each active device in the primary and secondary switches are calculated using the formula derived in chapter 3. The estimated current values for each topology are listed in appendix in Table A.1, Table A.2 and Table A.3 for one, two and three DABs respectively in generating and motoring modes. Due to the requirements of high current capability of each switch and requirements of limited number of semiconductor devices in parallel for decreasing parameter mismatch, gate circuit drive mismatch or power circuit mismatch [[32], [33]], which may lead to thermal breakdown, MOSFETs and IGBTs with high current capability are chosen. The primary sides switches are chosen to be MOSFETs due to the need of high conduction current and low switching losses. In the secondary side IGBTs are chosen due to the high voltage range of the output side for all topologies. An automotive grade, with small footprint, low on-resistance, high current and double sided cooling directFet power MOSFET, AU1RF7739L2TR, is selected for the primary side and an automotive grade, low $V_{CE(ON)}$, Positive $V_{CE(ON)}$ Temperature Coefficient and low switching loss IGBT, AU1RGP4066D1-E is selected. Their data sheets are in appendix A.6.

The number of switches in each DAB topology are listed in Table 3.4. The number of switches are selected based of the current ratings of each switch and the peak current for peak power at voltage ratio equals to 1.

Table 3.4: Number of switches in each topology

	Number of Mosfets	Number of IGBTs
One DAB Topology	$1 \times 4 \times 10$	$1 \times 4 \times 3$
Two DAB Topology	$2 \times 4 \times 5$	$2 \times 4 \times 2$
Three DAB Topology	$3 \times 4 \times 3$	$3 \times 4 \times 1$

The losses of each topology are calculated based on the parameters of the selected switches. The conduction and switching loss for each DAB topology is calculated for MOSFETs and IGBTs using [50] and [51] respectively. The calculation of the losses, which is mainly dependent on the on-resistance of the Mosfets, IGBTs and diodes and thresh-hold voltage of the diodes and IGBTs, are explained in detail in 3.6.3 in relation to the optimization of the heatsink thermal resistance. The losses for each device in one DAB are shown in figure 3.11 for steady state and transient power transfers. The generating mode is steady state and the motoring mode is transient. The power loss during motoring is higher than during the generating due to the high power transfer at motoring. Figures 3.12 and 3.13 show the losses for two and three interleaved DABs respectively. Comparing all the three DAB topology in losses, the difference in the total losses is due to the number of MOSFETs and IGBTs used in each topology.

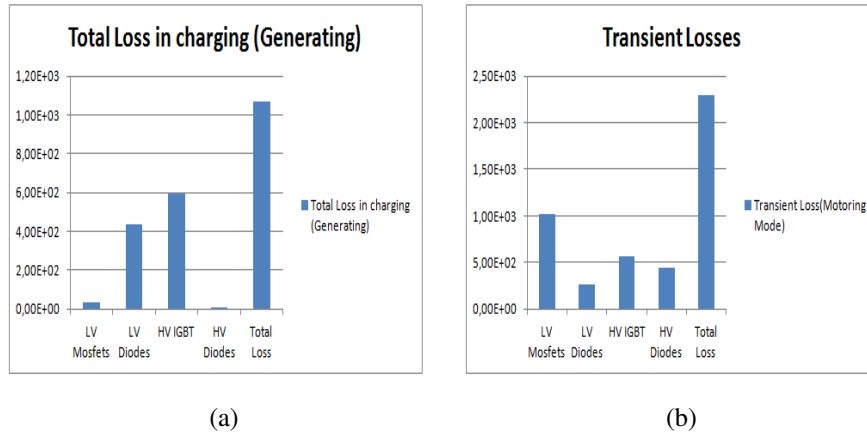


Figure 3.11: Power Losses for one DAB a) Loss at nominal power b) loss at transient

3.6.2 Capacitor Value Determination and Selection

In high current power supply application, either for systems which are sensitive to voltage change or systems sensitive to current, like battery with series resistance, input and output filtering is inevitable. In the system specified, due the high current application, the battery ripple current should

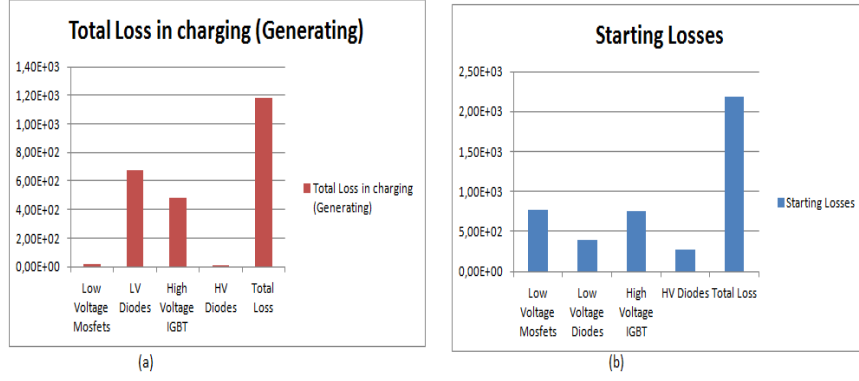


Figure 3.12: Power Losses for two interleaved DABs: a) Loss at nominal power b) loss at transient

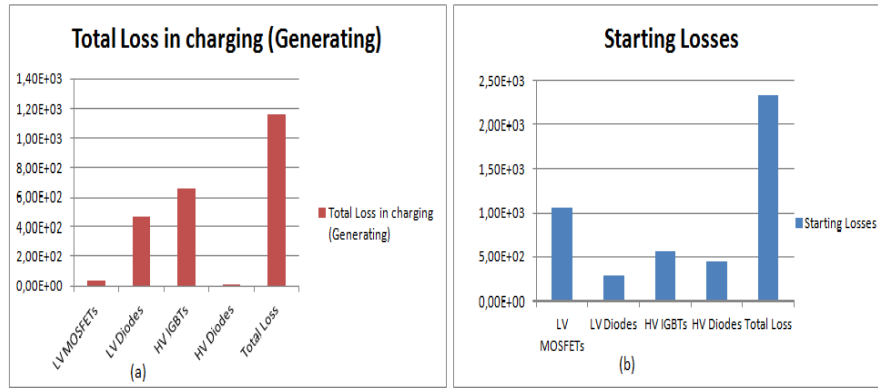


Figure 3.13: Power Losses for three interleaved DABs: a) Loss at nominal power b) loss at transient

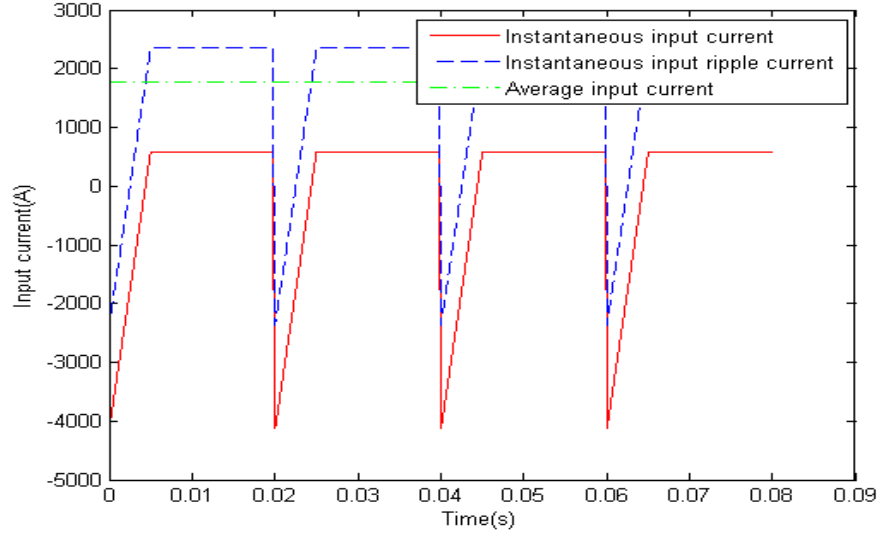
be small to minimize the voltage drop in the series resistance of the battery. A capacitor which satisfies the required ripple current and ripple voltage change has to be calculated and selected. In this section, the capacitance value for each converter and mass and volume of different kinds of capacitors or combination of capacitors will be calculated and compared. More over, different capacitor configurations will be compared for each DAB scenario in terms of mass, volume and loss.

The capacitance of each scenario with one, two and three DAB, is calculated from the waveforms of each topology assuming the voltage ripple to be 0.3%,:

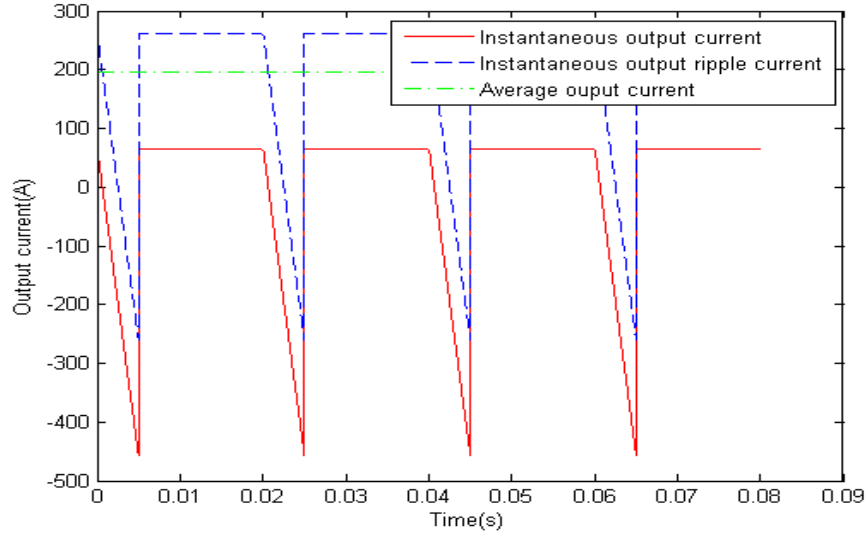
$$C = \frac{\Delta Q}{\Delta V} \quad (3.14)$$

Each topology waveform is drawn using matlab as shown in figures 3.14 and 3.15. In figure refCurrentWaveForm, the two interleaved DABs doubles the input and output filter capacitor current frequency. Moreover, the peak to peak currents is halve of the one DAB. In figure 3.15, the three interleaved DABs triples the input and output capacitors ripple current and decreases by one-third of the peak to peak current of single DAB. The increase in frequency decreases the required capacitance value which decreases the mass and volume. The decrease in ripple current and increasing of the frequency of the ripple current also decrease the number of capacitors to parallel for sake of current handling. As the the number of interleaved DABs increases, the frequency of the input and

output voltages increases. This helps in decreasing the value of the capacitance and also the size of the capacitors. The peak ripple currents also decrease which makes rating of peak capacitors currents less. Figures 3.14 and 3.15 are for 23kW at 45° phase shift at voltage ratio equal to the transformer ratio.



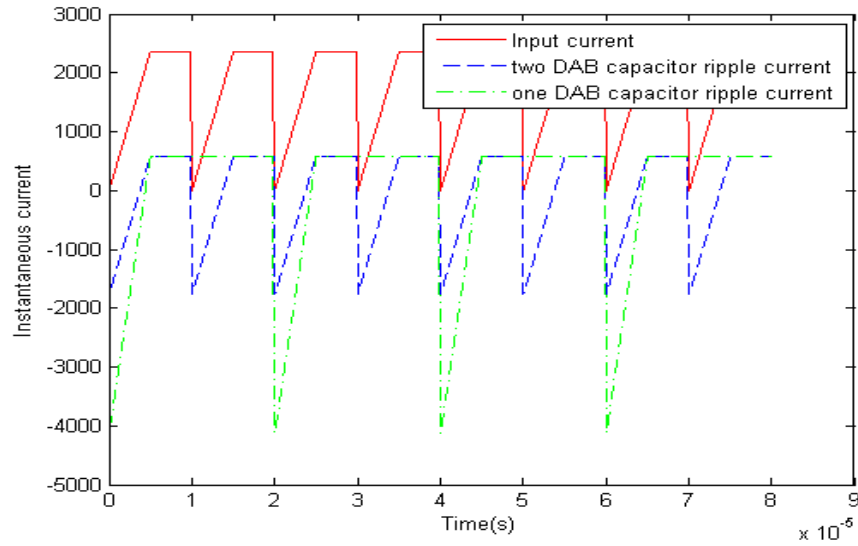
(a)



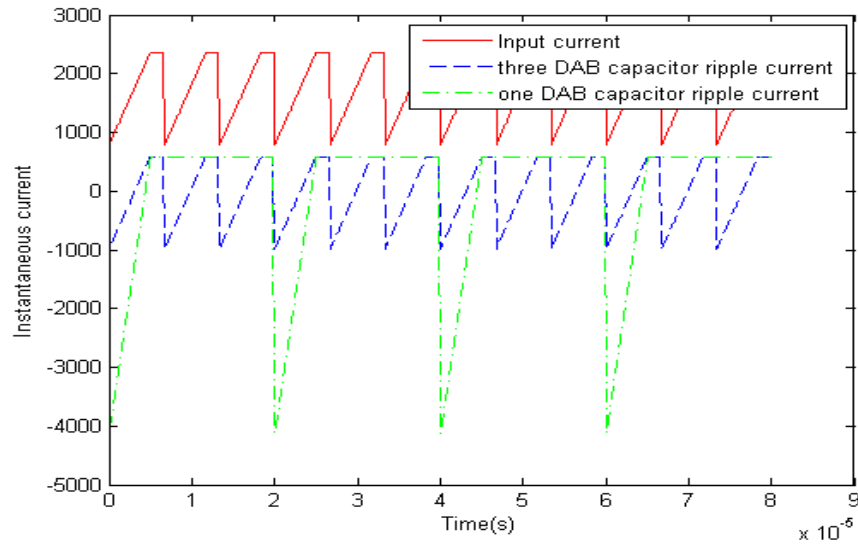
(b)

Figure 3.14: Input and output currents waveforms of one DAB decomposed in average and ripple current a) input current waveform of one DAB b) Output currents waveform of one DAB

The calculated capacitance values for each DAB at rated voltage and power and the ripple rms currents of each DAB topology at peak power is listed in table 3.5.



(a)



(b)

Figure 3.15: Input currents waveforms of interleaved two and three DABs decomposed into average and ripple current at $V_i = 13\text{V}$ and $V_0 = 117$ and 54 and 82 nH leakage inductance transferred to primary a) Two DAB b) Three DAB

In high ripple rms current DC link application, the rms current determines the number of capacitors to be in parallel due to the series resistance of capacitors. Since the rms ripple current is high, capacitors with high ripple rms capability and low ESR are considered. This section selects different types of capacitors and compares them in terms of mass, volume and efficiency.

Table 3.5: Capacitance value and rms ripple currents of input and output capacitors for three different topologies

	one DAB	Two DAB	Three DAB
Input Capacitance(mF)	5.2	2.61	1.74
Output Capacitance(μF)	64.44	33	21.48
Input Ripple RMS current(A)	1230	762.6	520.9
Output Ripple RMS current(A)	136.6	84.7	57.88

Electrolytic Capacitors : Electrolytic capacitors have high range of capacitance and good energy density [34]. However they have low ripple current capability. Currently available electrolytic capacitors with ripple current capability as big as 10 to 20 amps are either in high capacitance range of tens of mF or low capacitance and high voltage ranges (greater than 400 V). Utilizing electrolytic capacitors with 1 to 2 A RMS ripple current capability makes the number of capacitors large which makes the system bulky and the connection between capacitors leads to high inductance, even though they have low loss due a large quantity in parallel and are therefore not considered here. A 20 mF electrolytic capacitor, 101C203U063AF2B, is selected for comparison and the number, volume, mass and loss of these capacitors needed for one DAB are listed in table 3.6.

Polypropylene Capacitors High capacitance polypropylene film capacitors (10 to 100 μF) are becoming an ideal replacements for electrolytic banks with the requirements of high ripple currents. They have low ESR and as much as 10 times ripple current capability of electrolytic and higher voltage ratings. They are also available in low voltage , low capacitance, high ripple current capability and low ESR. However due to their low energy density compared to electrolytic capacitors, they are used in combination with electrolytic capacitors. A polypropylene, UNL4W30K-F, is selected for comparison. Even though only 44 of such capacitors are need in the one DAB input to fulfill the current requirements, it has to be tripled in order for the capacitance to be met which makes capacitor bank bulky and heavy as seen in table 3.6.

Electrolytic and Polypropylene Combination Use electrolytic for the capacitance and the polypropylene for the ripple current optimizes the volume, mass and loss compared to independently using each type of capacitor. The combination of a polypropylene, 935C1W30K-F and an electrolytic capacitor, 381LX1222MO63H012 makes a huge decrease in volume, mass and loss. In table 3.6, the difference can be seen. The number of polypropylene capacitors are determined to fulfill the rms ripple current and the electrolytic for the capacitance value.

Figure 3.6 shows the results of the selected capacitors' number, volume, mass and loss. Each type is listed in detail for the input and output capacitor in Appendix A.2 in tables A.4, A.5 and A.6.

Table 3.6: Capacitance value and ripple rms currents of input and output capacitors for Electrolytic-101C203U063AF2B, and, polypropylene UNL4W30K-F, and combination - 935C1W30K-F and an electrolytic capacitor, 381LX1222MO63H012

	Number	volume(cm^3)	mass (Kg)	Loss (W)
Electrolytic	49	6694	11,27	428
Polypropylene	181	9346.7	11.584	73
Combination	2El + 92Poly	3096.2	2.982	122

The above volumes do not consider space between connections or gaps due the cylindrical nature of the the capacitors, it only represents the raw added volume of each capacitor. Electrolytic has double the volume of the combination and almost three times the mass of the combination. Polypropylene has low loss but has very huge volume. The combination has moderate loss and low volume but higher loss than the polypropylene. The combination is chosen for the design of the capacitor used for comparison of one, two and three DAB converters as outlined below.

Table 3.7 or figure 3.16 compares the total volume, mass and loss of input and output capacitors of each configuration for the peak power assuming that the capacitors have a volume packing factor of 0.6 [35]. Assumed all rms ripple currents flow through the capacitors and used their ESR to determine the losses.

Table 3.7: Volume, Mass and Loss of input and output capacitors for the three topologies: One DAB, Two DAB, and Three DAB : $El = Electrolytic$, $PP = Polypropylene$

	one DAB	Two DAB	Three DAB
Volume(cm^3)	5160.325	3378,645	2246.09
Mass (Kg)	2.982	1.958	1.299
Loss(W)	122	72	50.2
Number of Capacitors	2El + 92PP	2El + 60PP	1El + 40 PP

Table 3.7 shows that increasing the number of phase shifted DABs (at least to three) decreases the mass, volume and loss.

Due to the large number of capacitors in the input, putting them in one PCB would make the volume and surface area of the capacitors very large. Putting them in stacked layers as shown in figure 3.17 would decrease volume. Moreover, the use of cooling sytems, like fan, makes this layering favorable to cool the capacitors.

3.6.3 Heatsink Design

This section deals with the optimized design of heasink based on the work found in [36] with the inclusion of some changes on the design procedure. First, an optimized point between the losses

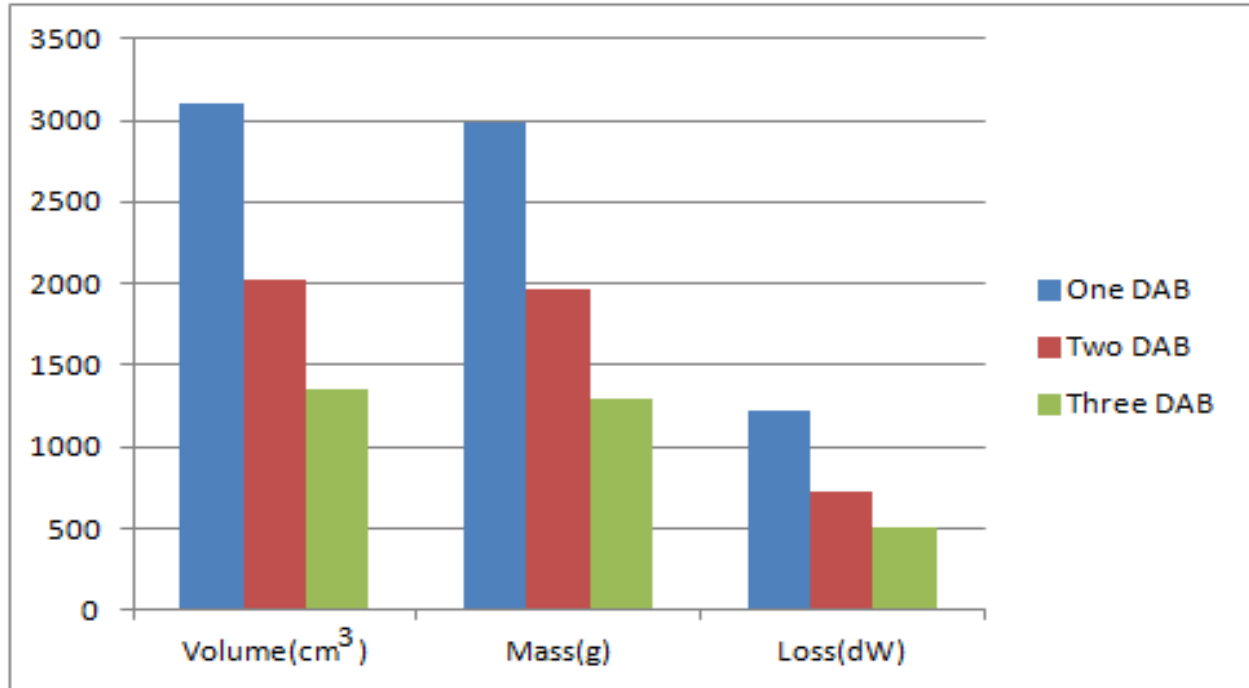


Figure 3.16: Comparison of 1, 2 and 3 DAB in volume, mass and loss for the capacitors

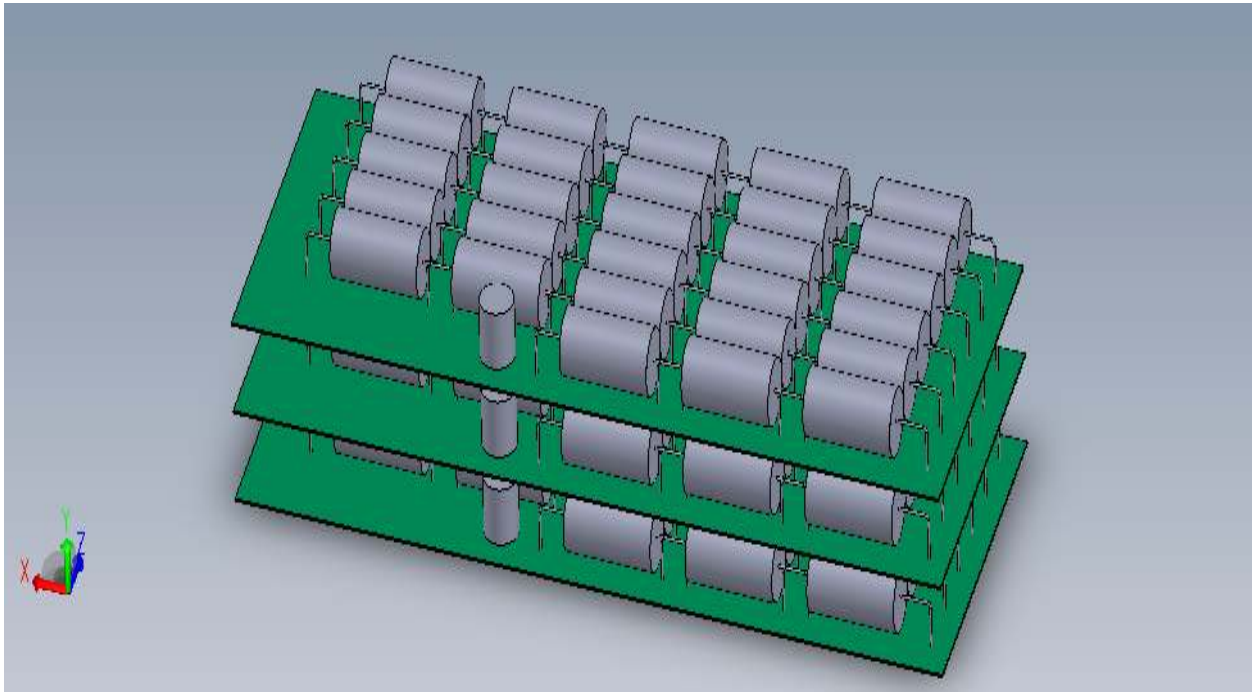


Figure 3.17: Stacked layer of capacitors for one DAB(The gap between the layers is not to scale)

of the active devices selected and thermal resistance of the heatsink will be selected. The junction temperature determines the on-resistance and threshold voltage of the active devices used and has direct influence on losses. Secondly, a mechanical design of the heatsink will be presented.

A small increase in junction temperature changes the on-resistance and threshold voltage of the selected active devices which leads to large loss due the high rms and average currents required. Hence, the on-resistance and threshold voltages are expressed in terms of junction temperature which has large effect on both parameters and can also be read from their data sheets. The conduction and switching losses of the selected MOSFET and its anti-parallel diode are calculated using 3.15 to 3.18

$$P_{CMosfet} = R_{OnMosfet}(T_j) I_{Mosfetrms}^2 \quad (3.15)$$

$$P_{SMOSFET} = E_{OffM} f \quad (3.16)$$

$$P_{Cdiode} = R_{DnDiode}(T_j) I_{Dioderms}^2 + U_{DiodeOn}(T_j) I_{average} \quad (3.17)$$

$$P_{LossMosfet} = P_{CMosfet} + P_{SIGBT} + P_{Cdiode} \quad (3.18)$$

where $P_{CMosfet}$ is the MOSFET conduction loss, $R_{OnMosfet}(T_j)$ is on-resistance of the MOSFET dependent on junction temperature, T_j , $I_{Mosfetrms}$ is rms current of the MOSFET, $P_{SMOSFET}$ is MOSFET switching loss, E_{OffM} is MOSFET switching-off energy, f is switching frequency, P_{Cdiode} is anti-parallel diode conduction loss, $R_{DnDiode}(T_j)$ is diode on-resistance which is dependent on junction temperature, $I_{Dioderms}$ is diode rms current, $U_{DiodeOn}(T_j)$ is diode threshold voltage, $I_{average}$ is diode average current, and $P_{LossMosfet}$ is the switch loss.

The MOSFET's on-resistance dependency on junction temperature is extracted from the datasheet and approximated to second order polynomial. The on-resistance and threshold voltage of the anti-parallel diode are linearly dependent on the junction temperature. They are extrapolated from their respective datasheets and are shown in 3.19. The switching-off loss of the MOSFET is very small compared to the on resistance and here is assumed constant in order to simplify the calculations.

$$R_{OnMosfet}(T_j) = (7.56 \times 10^{-6} T_j^2 + 0.00203 T_j + 0.642) \times 10^{-3} \quad (3.19)$$

$$R_{DnDiode}(T_j) = 5.24 \times 10^{-6} T_j + 0.0027 \quad (3.20)$$

$$U_{DiodeOn}(T_j) = -0.0018 T_j + 0.6023 \quad (3.21)$$

The conduction and switching loss of IGBT and its anti-parallel diode are estimated using equation 3.22.

$$P_{CIGBT} = R_{OnIGBT}(T_j) I_{IGBTrms}^2 + U_{IGBTOn}(T_j) I_{IGBTAverage} \quad (3.22)$$

$$P_{SIGBT} = E_{OffIGBT} f \quad (3.23)$$

$$P_{CdiodeIGBT} = R_{DnDiode}(T_j) I_{Dioderms}^2 + U_{DiodeOn}(T_j) I_{Diodeaverage} \quad (3.24)$$

$$P_{LossIGBT} = P_{CIGBT} + P_{SIGBT} \quad (3.25)$$

The on-resistance and thresh-hold voltage of IGBT and its anti-parallel diode are extracted and extrapolated in Matlab and are shown in 3.26. More ever , since the switching-off loss of IGBTs is high, the switching-off energy is made to be linearly dependent on junction temperature [47].

$$R_{OnIBGt}(T_j) = 1.476 \times 10^{-5} T_j + 0.0055 \quad (3.26)$$

$$R_{DnDiode}(T_j) = 1.49 \times 10^{-5} T_j + 0.0054 \quad (3.27)$$

$$U_{IGBTOn}(T_j) = -0.0012 T_j + 0.7012 \quad (3.28)$$

$$U_{DiodeOn}(T_j) = -0.002 T_j + 0.6642 \quad (3.29)$$

$$E_{OffIGBT}(T_j) = 4.3 \times 10^{-6} T_j + 0.0021 \quad (3.30)$$

where $R_{OnIGBT}(T_j)$ is IGBT on-resistance, $R_{DnDiode}(T_j)$ is Diode on-resistance, $U_{IGBTOn}(T_j)$ is IGBT thresh-hold voltage, $U_{DiodeOn}(T_j)$ is Diode thresh-hold voltage $E_{OffIGBT}(T_j)$ is IGBT switching-off energy.

For a given rms and average current and junction temperature, the power losses of MOSFETs, IGBTs and diodes can be calculated. The optimization of junction temperature and heatsink design for one DAB topology will be described here and for two DAB and three DAB topologies, only their result will be presented. For each topology, three different arrangements of heatsink are analyzed: one heatsink for one switch, one heatsink for two switches and one heatsink for four switches.

Thermal Resistance Optimization by Junction Temperature Figure 3.18 shows the equivalent thermal network of n parallel MOSFETs with thermal interface material and heatsink. The thermal interface material, Blue Ice, with thermal resistance of $3.7 \frac{W}{K}$ [38] and thickness of $50 \mu m$ is used as an interface between the MOSFET and heatsink. It is assumed that only one side of the DirectFET package is used for cooling even though it is also possible to use both sides. The anti-parallel diode of the MOSFET is internally built in and is, therefore, not shown in the network. Thermal network of the selected IGBT is also shown in figure 3.19 with an external anti-parallel diode. The ambient temperature is set to $45^\circ C$.

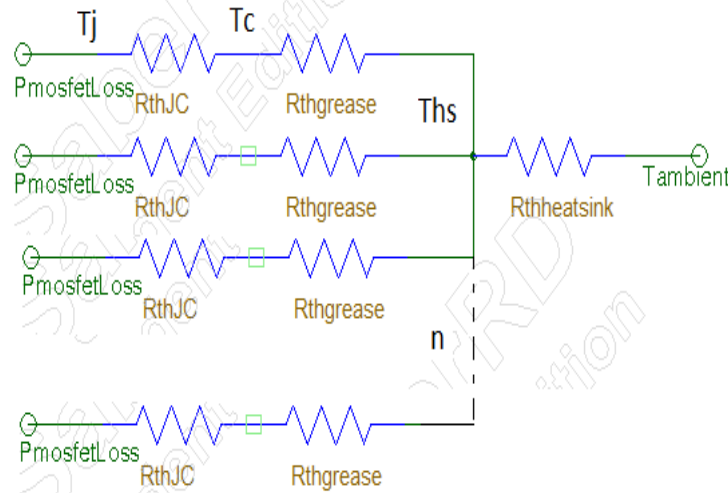


Figure 3.18: Thermal Network of n Paralleled selected Mosfets

The maximum allowable thermal resistance of the heatsink for MOSFET and IGBTs are derived from their respective thermal networks and given by equations (3.31) and (3.32) respectively. With constant rms and average currents, power loss of a MOSFET and its anti-parallel diode can be calculated by varying the junction temperature within the ranges specified in its data sheet using 3.15. If the rate of increase of the junction temperature is greater than the rate of increase of the loss due to the increase in junction temperature in (3.31), the maximum allowable heatsink thermal resistance increases. However, if the rate of increase of loss is greater than the rate of increase of the junction temperature, the allowable maximum thermal resistance decreases. This means

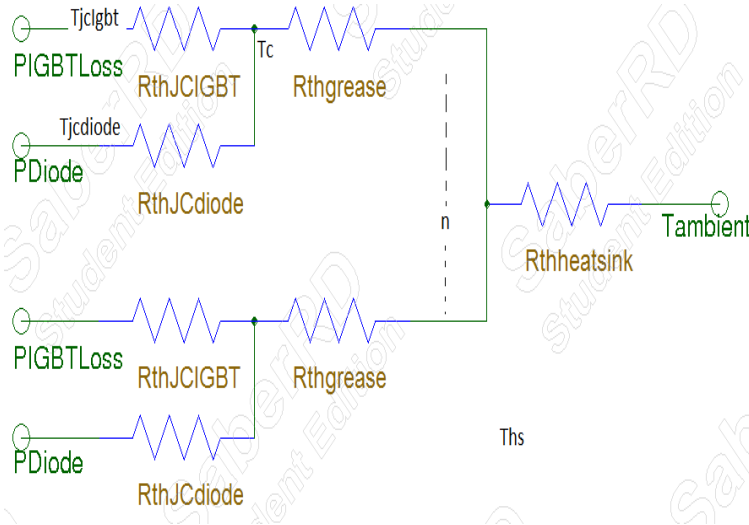


Figure 3.19: Thermal Network of n paralleled selected IGBTs: $R_{thgrease}$ is taken from the IGBT's datasheet

the effect increasing junction temperature to increase the required maximum allowable external heatsink thermal resistance is compensated by the increase on conduction losses [36]. The analysis for MOSFET's heatsink thermal resistance will be presented here for three different heatsink arrangements: one heatsink for one switch, one heatsink for two switches and one heatsink for four switches. A switch can have a number of transistors in parallel. In one DAB topology, one switch in the primary contains 10 MOSFETs. Only the result for the MOSFET thermal network will be presented here since the same approach is used for the IGBT network except that the case temperature is used as the IGBT and its anti-parallel diode are independent and same junction temperature cannot be assumed.

$$R_{thheatsink} = \frac{T_j - T_{ambient}}{P_{LossMosfet}} - \left(\frac{R_{jc} + R_{grease}}{n} \right) \quad (3.31)$$

$$R_{thIBGTheatsink} = \frac{T_c - (P_{IGBTLoss} + P_{Diode})R_{grease} - T_{ambient}}{(P_{IGBTLoss} + P_{Diode})n} \quad (3.32)$$

where $R_{thheatsink}$ is the thermal resistance of the heatsink

T_j the junction temperature

$T_{ambient}$ is the ambient Temperature which is considered $45^\circ C$ in all calculations

R_{jc} is the junction to case thermal resistance of the MOSFET

R_{grease} is the case to heatsink thermal resistance

n is the total number of MOSFETs in parallel

$P_{lossMosfet}$ is individual MOSFET loss

$R_{thIBGTheatsink}$ is the thermal resistance of the IGBT heatsink

T_c is the case temperature

$P_{IGBTLoss}$ is IGBT loss and

P_{Diode} is diode loss.

By varying the junction temperature, the maximum allowable external heatsink thermal resistance and power loss are calculated for the MOSFETs. Figures 3.20, 3.21 and 3.22 show the variation of thermal resistance, loss and efficiency of MOSFET and IGBT¹ with respect to the junction temperature and case temperature respectively. As can be seen from figure 3.20a, for a constant rms and average currents at peak power, the increase in junction temperature increases the thermal resistance of heatsink and allowable loss at the same time. This shows an inverse relationship between the size of heatsink and junction temperature. However, efficiency has to be compromised as shown in figure 3.20. Therefore, an optimized point between junction temperature, power loss and allowable thermal resistance has to be chosen.

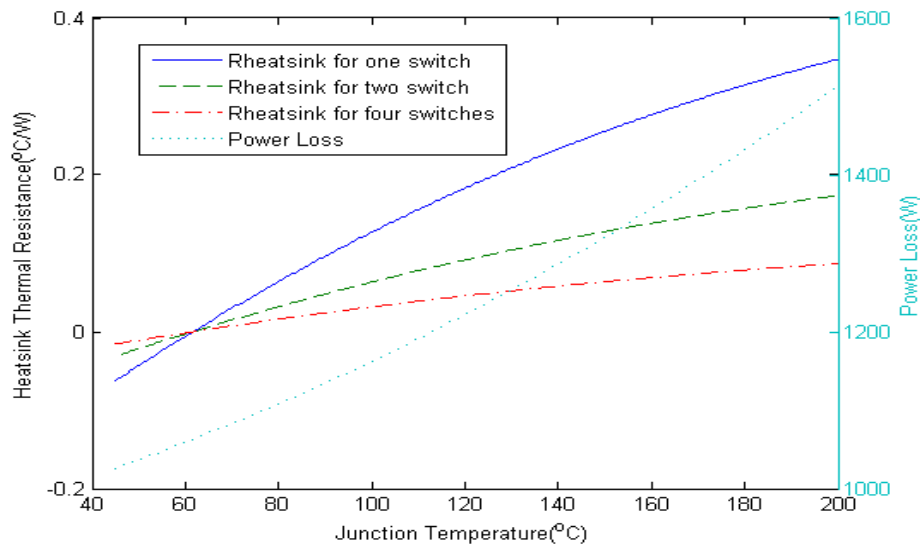
In figure 3.20, the maximum theoretically allowable junction temperature of the selected MOSFETs is set to 200 °C. As the estimated maximum allowable thermal resistance monotonically increases till 200 °C in the figure, this shows that there is no any point in the graph where the rate of increase in junction temperature is less the rate of increase in conduction loss. This means choosing a higher junction temperature would have an advantage in the size of the heatsink even though there is a higher loss.

Figure 3.20a shows that the minimum possible junction temperature is 61.5 °C at a zero maximum allowable heatsink thermal resistance and at the maximum possible efficiency of .956 for all arrangements. However, this leads to an infinite heatsink size which is obviously not feasible. For junction temperature values less than 61.5 °C, a negative thermal resistance is required which is practically impossible. The increase in junction temperature increases the maximum allowable thermal resistance of the heatsink needed but at the same time leads to a decrease in efficiency as shown in figure 3.21. For the MOSFET, at 150A, the case temperature can not be greater than 125 °C (from datasheet), which leads to a theoretically maximum allowable heatsink and junction temperature of 121 °C and 141 °C respectively. Reading these points from figure 3.20a give a maximum heatsink thermal resistance of $0.2358 \frac{^{\circ}\text{C}}{\text{W}}$ for one heatsink per switch, $0.1179 \frac{^{\circ}\text{C}}{\text{W}}$ and $0.05895 \frac{^{\circ}\text{C}}{\text{W}}$ for one heatsink to two switches and one heatsink to four switches respectively. The efficiency goes down to 0.9469. However, practically speaking, the heatsink size has decreased to a very small size compared to the efficiency decrease from the ideally possible point.

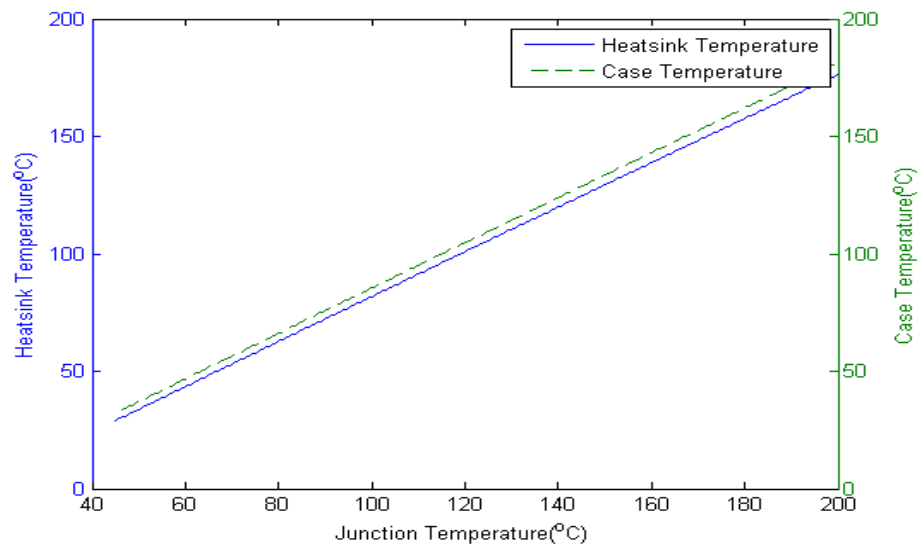
Figure 3.20b shows the case and heatsink temperature as function of junction temperature. Due to the low values of the heatsink thermal resistance required, the case and heatsink temperatures vary by not greater than 5 °C. This shows that how small the maximum allowable thermal resistance of the heatsink to be used for cooling the selected switches.

Figure 3.22a shows the junction temperature of IGBT and diodes as a function of case temperature. For case temperature less than 64 °C, the maximum allowable thermal resistance is negative which shows that it is practically impossible to have a case temperature less than that value because it leads to a requirement of negative maximum allowable thermal resistance. Increasing case temperature above 64 °C increases the maximum allowable thermal resistance. The increase in maximum allowable temperature decrease the mass and volume of the cooling system. However, as can be seen from figure 3.22b, the increase in case temperature to increase the maximum allowable thermal resistance comes with the increase in loss due to the increase in on-resistance of the

¹Efficiency is calculated considering only the loss of MOSFETs for sake of comparison- other losses are not included



(a)



(b)

Figure 3.20: Effect of Junction Temperature on the heatsink thermal resistance, and on power loss loss for the selected MOSFET a)Variation of thermal resistance and power loss as a function of junction temperature for the three heatsink arrangements(one, two and fours switches in one heatsink) b) Case and Heat sink Temperature as a function of junction temperature

IGBTs and their anti-parallel diodes.

For IGBT, at 80A, the maximum allowable case temperature is 112.5 °C (from the datasheet) which limits the heatsink and junction temperature to 110 °C and 126.8 °C respectively. The IGBT efficiency is not as significantly affected by the increase in junction temperature as is the case for the MOSFETs due the dominant effect of the IGBT's negative temperature coefficient.

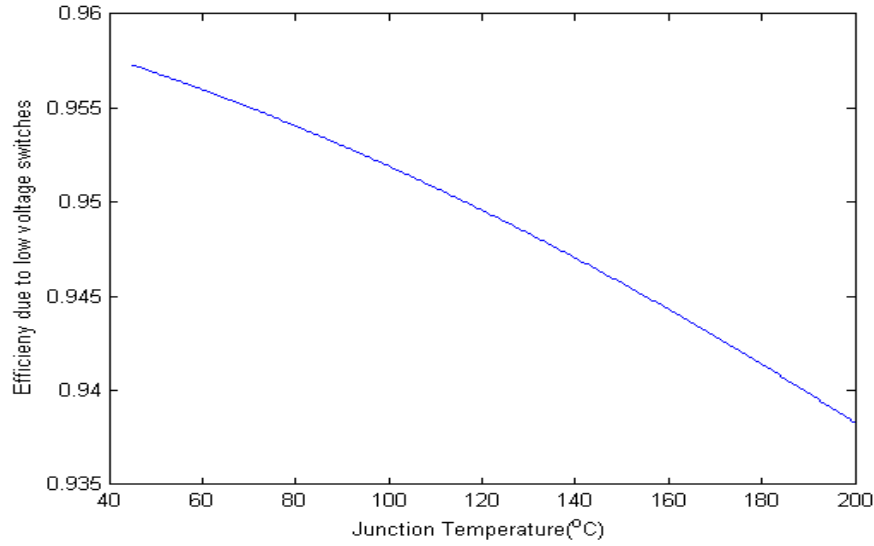


Figure 3.21: Efficiency MOSFETs ignoring losses of other components

The two semiconductors are optimized to find a high thermal resistance (low heatsink volume and mass) at different heatsink temperature. The use of one heatsink for both the MOSFETs and IGBTs may, therefore, make the system unoptimized. If one heatsink is used for both semiconductors, the maximum heatsink temperature is determined by the IGBT which is 110°C . This leads to a reduced junction temperature for the MOSFETs with the effect of decreasing the thermal resistance of the heatsink. However, the efficiency increases.

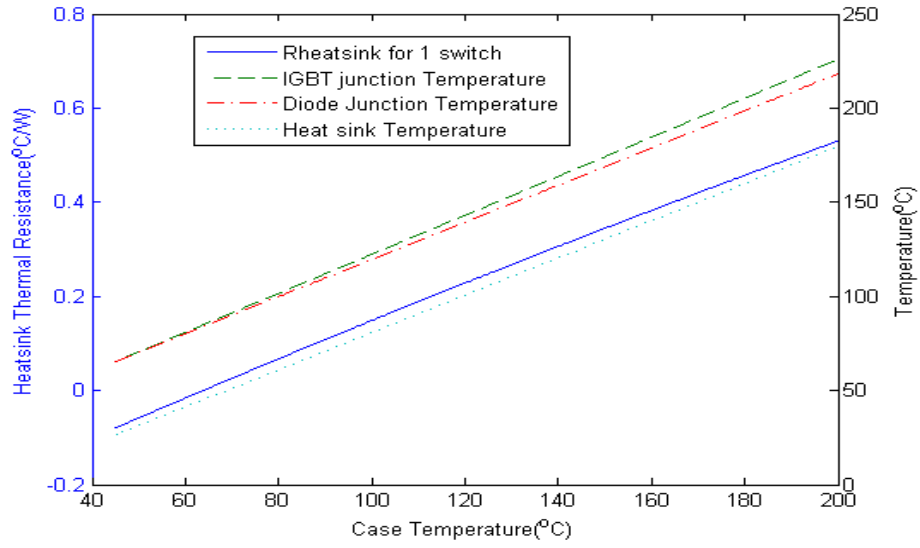
Similarly, the thermal resistance for two DAB and three DAB configurations are calculated and are listed in table 3.6.3.

Table 3.8: Calculated Thermal Resistances of each topology at junction temperature of 121°C and 112.5°C

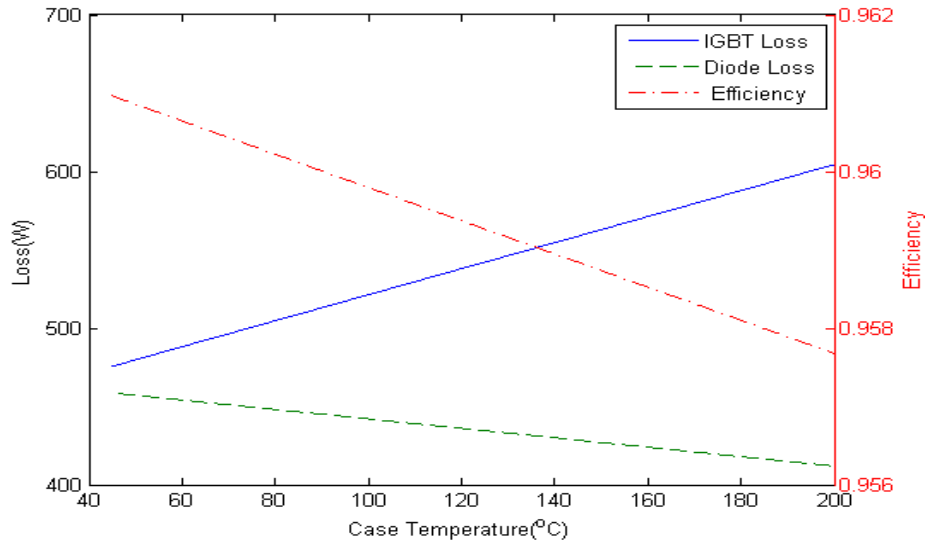
for the MOSFETS and IGBTs respectively

	one DAB		Two DAB		Three DAB	
Heatsink thermal Resistance for one switch($^{\circ}\text{C}/\text{W}$)	MOSFET	IGBT	MOSFET	IGBT	MOSFET	IGBT
	0.235	0.236	0.470	0.3652	0.6081	0.7

Heatsink Design Optimization This section deals with the physical design of the heatsink based on the optimized thermal resistance obtained in the previous section. The heatsink is designed using an optimization method developed in [36]. Heatsinks are compared by their Cooling System Performance Index (CSPI) which is defined as the ratio of power of the converter to the volume of the cooling system. A higher CSPI is therefore preferred. Compared to the commercially available heatsinks which have CSPI in the range of 2 to 4 W/Liters , heatsinks designed based on the method given in [36] have significantly higher power density [36], 15 to 30 W/Liters . The developed method's thermal network is show in figure 3.23. The front geometry is determined by



(a)



(b)

Figure 3.22: Effect of case temperature on the maximum allowable heatsink thermal resistance and efficiency for the selected IGBT for a constant rms and average currents a) Variation of maximum allowable heatsink thermal resistance as a function of case temperature b) Loss of IGBT and anti-parallel diode and efficiency ignoring losses of other components as a function of case temperature

the choice of a fan. The height and the width are equal to the diameter of the fan, $c = b = \text{diameter of the fan}$. S is the fin spacing, t is the fin thickness and n is the number of fins. Since the width is fixed by the choice of the fan, the length of the heatsink is dependent on the switch area required. Therefore, the length is equal to :

$$L = \frac{\text{switch area}}{b} \quad (3.1)$$

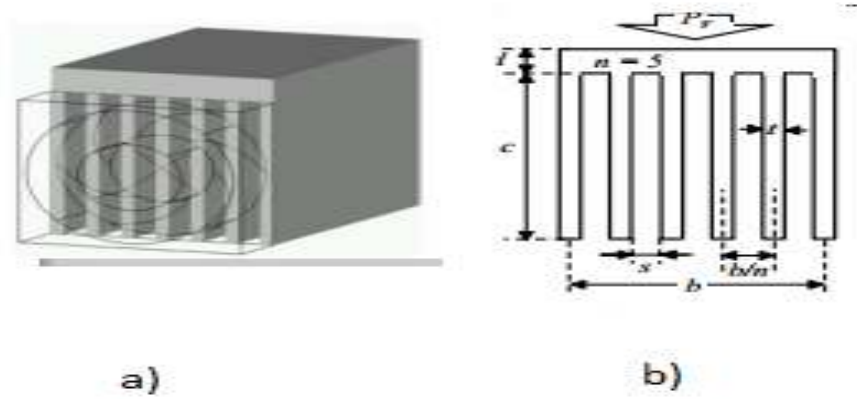


Figure 3.23: a) Geometry of the heatsink designed b) Front geometry of the heatsink with its labels [36].

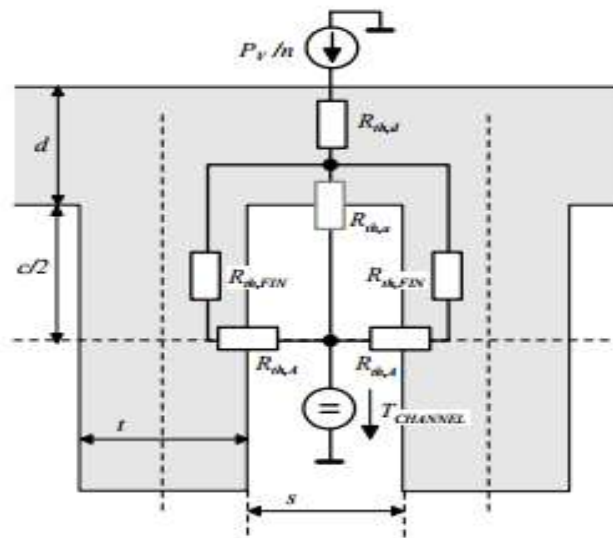


Figure 3.24: Thermal network that shows the heat transfer from heatsink base plate into air for one channel[36]. Each label is defined in the following derivation of the equivalent thermal resistance of the the whole heatsink

where *switcharea* is the total surface area of transistors available for cooling in a switch or switches to be placed on the heatsink.

The fin spacing ratio which determines the heatsink cross-section area available for air flow is defined as

$$k = \frac{S}{\frac{b}{n}} \quad (3.2)$$

The equations which are developed in [36] for designing the heatsink are explained below with their brief description. The design of the heatsink depends on the characteristics fan and heatsink geometry. The mathematical models of the fan and heatsink geometry is described below. However, for more explanation reader can refer the paper work [36].

The fan characteristics, which shows the relationship between the pressure and air flow, is approximated by a 5th order approximation as follows [36]

$$\Delta P_{fan}(V) = A + B \times V + C \times V^2 + D \times V^3 + E \times V^4 + F \times V^5 \quad (3.3)$$

$\Delta P_{fan}(V)$ is the pressure of the fan as a function of air flow volume, V is volume flow in $\frac{m^3}{s}$ and A, B, C, D, E and F constants derived from each fan's datasheet.

The hydraulic diameter of one channel determines the pressure loss and the type of flow in ducts whether it is laminar or turbulent. Laminar flow, sometimes known as streamline flow, occurs when fluid flows in parallel layers, with no disruption between the layers. Where as the opposite is called turbulent flow. It is given by the following formula for the channel in figure 3.23c,

$$d_h = \frac{2Sc}{S + c} \quad (3.4)$$

The pressure drop of the total air flow through a given channel of length, L , for a laminar flow is given by Cooling

$$\Delta P_{lam}(V) = 1.5 \frac{32\rho_{AIR}v_{AIR}L}{n(S.c)d_h^2} \quad (3.5)$$

where $\Delta P_{lam}(V)$ is the pressure drop, $\rho_{AIR} = 0.99 \frac{kg}{m^3}$ is air density ($80^\circ C$), and $v_{AIR} = 2.1 \times 10^{-5} \frac{m^3}{s}$ is cinematic viscosity of the air($80^\circ C$).

If the flow is turbulent, the pressure drop is calculated as follows

$$\Delta P_{turb}(V) = \frac{L(\frac{S+c}{2S.c})\rho_{AIR}\frac{1}{2}(\frac{V}{n.S.c})^2}{(0.79 \times \ln(\frac{2V}{n(S+c)v_{AIR}} - 1.64))^2} \quad (3.6)$$

The average Reynolds number Re_m , a dimensionless number which gives the ratio of inertial forces (which characterize how much a particular fluid resists any change in motion) to viscous forces, is given by

$$Re_m = \frac{2V}{n(S + c)v_{AIR}} \quad (3.7)$$

If the Re_m is greater than 2300, the flow is turbulent, otherwise laminar.

The air flow volume is calculated by using the following formula for a laminar case

$$k\Delta P_{fan}(V) = \Delta P_{lam}(V) \quad (3.8)$$

and if Re_m is greater than 2300, the air flow volume should be calculated for the turbulent case by the following equation

$$k\Delta P_{fan}(V) = \Delta P_{turb}(V) \quad (3.9)$$

The average Nusselt number, Nu_m , a dimensionless number which determines the ratio of convective to conductive heat transfer across a boundary, for a laminar flow is

$$Nu_{m,lam} = \frac{3.657(\tanh(2.264X^{\frac{1}{3}} + 1.7X^{\frac{2}{3}}))^{-1} + \frac{0.0499}{X}\tanh(X)}{\tanh(2.432 \times 0.71^{\frac{1}{6}}X^{\frac{1}{6}})} \quad (3.10)$$

where $X = \frac{L}{0.71d_h Re_m}$ and for a turbulent flow

$$Nu_{m,turb} = \frac{(8(0.79 \ln(Re_m) - 1.64)^2)^{-1}(Re_m - 1000) \times 0.71}{1 + 12.7\sqrt{((8(0.79 \ln(Re_m) - 1.64)^2)^{-1}) \times (0.71^{\frac{2}{3}} - 1)}}(1 + (\frac{d_h}{L})^{\frac{2}{3}}) \quad (3.11)$$

With the calculated Nu_m number, the heat transfer coefficient of the system, h , is calculated as follows

$$h = \frac{Nu_m \lambda_{AIR}}{d_h} \quad (3.12)$$

where $\lambda_{AIR} = 0.03 \frac{W}{mK}$ is thermal conductivity of air.

The thermal resistances in figure 3.23c of the channel model are calculated as follows. The convective thermal resistances of each channel are calculated by

$$R_{th,A} = \frac{1}{hL_c} \quad (3.13)$$

$$R_{th,a} = \frac{1}{hL_s} \quad (3.14)$$

where $R_{th,A} \ll R_{th,a}$ and is neglected in the practical calculations

The fin conductive thermal resistance is calculated as

$$R_{th,FIN} = \frac{\frac{1}{2}}{0.5tL\lambda_{HS}} \quad (3.15)$$

where λ_{HS} the thermal conductivity of heatsink material, which is aluminum in all the calculations below. The conductive thermal resistance of each channel of the heatsink base plate is

$$R_{th,d} = \frac{d}{\frac{1}{n}A_{HS}\lambda_{HS}} \quad (3.16)$$

where A_{HS} is size of the heatsink base plate

The equivalent thermal resistance of the conductive and convective thermal resistance of each channel is

$$R_{th}^n = R_{th,d} + 0.5(R_{th,Fin} + R_{th,A}) \quad (3.17)$$

For n channels, the equivalent thermal resistance of the heatsink is given by

$$R_{th}^{HS} = \frac{1}{n} R_{th}^n + \frac{0.5}{\rho_{AIR} C_{P,AIR} V} \quad (3.18)$$

where $C_{P,AIR} = 1010 \frac{J}{KgK}$ is specific thermal capacitance of air and the second term represents the average temperature rise of the air in each channel due to the heat transported away via convection.

The design procedure is as follows

1. Selecting a fan, which has high volume flow and commercially available. Their fan characteristics, change in pressure as a function flow rate, are approximated in 5th order approximation.
2. For a selected fan, three arrangements of switch area are used: One switch, two switches or four switches as switch area which basically varies the length since the width and height are already fixed by the fan selection.
3. For a selected fan and switch area, an allowable maximum thermal resistance is searched by varying the fin spacing ratio, k and the number of fins, n , simultaneously which basically means varying fin spacing and fin thickness.
4. After the minimum thermal resistance is found, the number of heatsinks is calculated by comparing the calculated thermal resistance to the required thermal resistance.

The switch area for MOSFETs in one switch is calculated by assuming a gap between the MOSFETs given as in the tape reel dimension in their datasheet. Similar assumption is made for the IGBTs. A matlab code is developed to calculate the thermal resistance and volume and mass of heatsink required. The analysis will be presented in here.

The heatsink optimization mechanism depend on the choice of fan and the chip area needed. The optimization is done by varying the fin spacing ratio and fin number simultaneously and from that a local optimum is taken. If a smaller fan is used for a big chip area, the length of the heatsink becomes too big. which has the effect of decreasing the thermal resistance due the temperature gradient decrease even though it increases the fin area. Moreover, the volume and mass becomes large. For that reason three types of fans are used in here for comparison. Fan A is for a fan with diameter of 0.04 meters [36], Fan B diameter of 0.06m and Fan C is diameter of 0.092 meters [39]. The results for one DAB configuration will be discussed here and for the two and three DAB configurations only their result will be presented.

The fin thickness is one of the parameters which determines the mass of heatsink. The mass of heatsink is same for a given fin spacing ratio with different fin numbers as shown in 3.25b.

The change in mass is very insignificant around the local optimum found with the change in fin spacing ratio. Figure 3.25 shows the thermal resistance and mass variation with fin spacing ratio and number of fins for 10 MOSFETs in parallel in one switch in one DAB using fan A. For a fixed fin spacing ratio, 0.5, up to the number of fins is around 20, the thermal resistance decrease since the total surface area increases. However as the number of fins increase above 20, even though the fin surface area increases, the space between fins for air flow decreases. This makes the air flow limited and the convective heat transfer very low.

For a fixed number of fins, decreasing the fin spacing ratio means decreasing the gap between fins. This decrease in spacing leads to less air movement which also limits the convective heat transfer. The minimum thermal resistance is 0.58°C/W at mass of 0.06Kg. To fulfill the needed thermal resistance for one switch in one DAB, 0.235°C/W , two such heatsinks are needed.

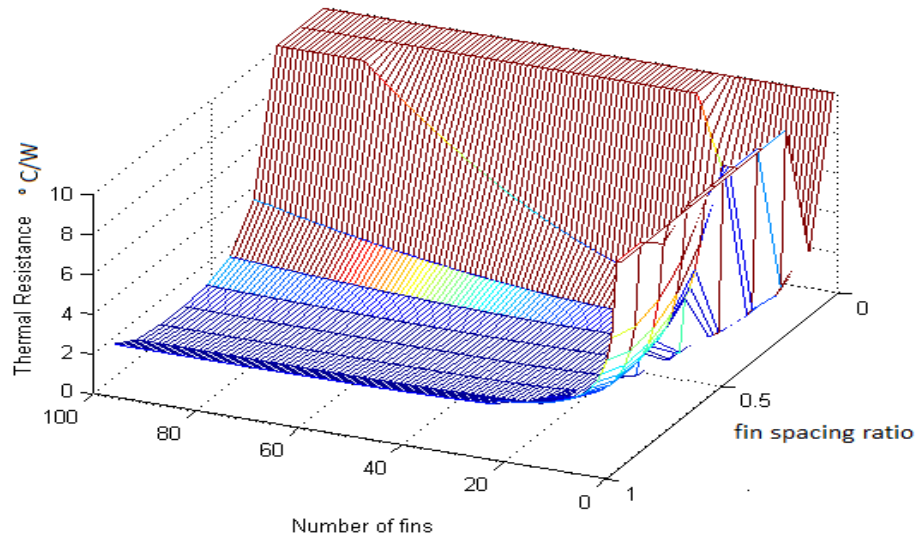
By doubling the Length of heatsink and using one fan A, same chip area as of using two Fan A can be found and the volume less by the volume of the fan. However, the thermal resistance only decreases from 0.58°C/W to 0.409°C/W which needs still another additional heatsink. Doubling the length of heatsink does not change the thermal resistance as needed as using two fans A.

Rather than using two fans of type A, one fan of type B is also used to calculate thermal resistance. The thermal resistance is found to be as low as 0.305°C/W but still needs an additional heatsink to fulfill the requirement which increases the volume and mass. Table 3.9 shows the calculated values of minimum thermal resistance for the three fans with three different switch areas.

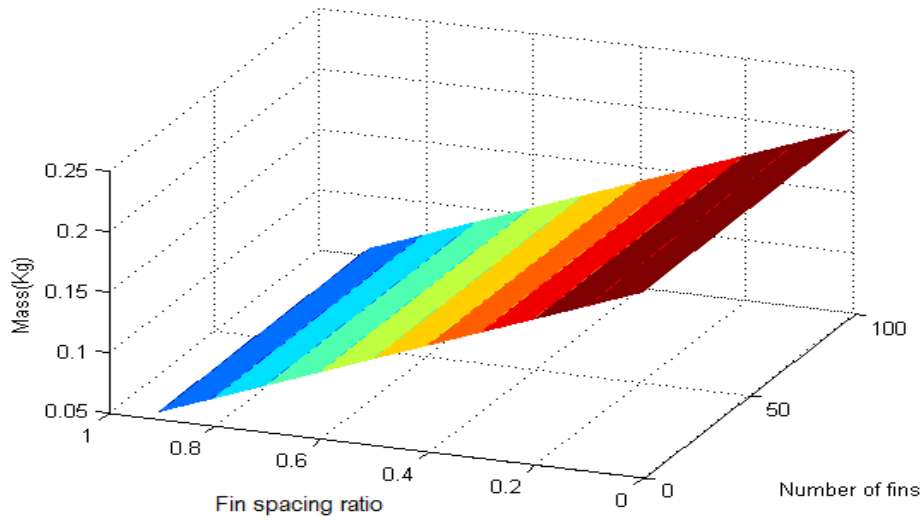
Table 3.9: Calculated values of heatsink numbers, volume and weight for one DAB topology for three different chip areas

Chip Area	Required heatsink thermal resistance ($^{\circ}\text{C/W}$)	Fan Type	Length (mm)	Minimum Calculated Heat sink Thermal resistance ($^{\circ}\text{C/W}$)	Required Number of heatsinks	Volume (Liters)	Weight (Kg)
One Switch	0.235	A	18.8	0.582	4×2	0.7232	1.04
		B	12.55	0.729	4×3	1.9271	2.786
		C	8.1	0.623	4×3	4.678	3.23
Two Switches	0.1175	A	37.6	0.409	2×4	1.024	1.392
		B	25.1	0.555	2×5	2.132	2.99
		C	16.2	0.385	2×3	3.994	2.51
Four Switches	0.05875	A	75.2	0.308	1×5	1.016	1.228
		B	50.1	0.45	1×8	2.54	3.6799
		C	32.4	0.261	1×4	2.471	2.54

For the calculated thermal resistance, the use of Fan B is found to be uninteresting in terms of mass and volume compared to Fan A and Fan C. When the switch area is four switches, Fan C is found better than Fan B in volume in Table 3.10. Moreover, the use of fans less in diameter than Fan A would be expected to be beneficial if they have similar characteristics as Fan A. For a better optimized size, different sizes of fans should be compared. For all the three DABs, the heatsink are optimized by using the three fans selected and their optimized results are shown in Table 3.10.



(a)



(b)

Figure 3.25: Dependence of thermal resistance and mass on fin spacing and fin number for Fan A with chip area of one switch a) Calculated thermal resistance using fan A for one switch of the selected MOSFETs in one DAB topology. b) Calculated Mass of the heatsink with variation in fin spacing ratio. High values thermal resistance are clipped to 10 for visualization purpose

The optimization is done by calculating the minimum thermal resistance of Fan A, Fan B and Fan C for one, two and four switches as switch area in all the three DABs and the best values are taken.

For the MOSFETs, the values for one DAB and two DAB configurations are same since the

Table 3.10: Minimum values of volume and mass of heatsink calculated for each circuit configuration

	one DAB		Two DAB		Three DAB	
	MOSFET	IGBT	MOSFET	IGBT	MOSFET	IGBT
Volume(L)	0.7232	0.88	0.7232	1	1.174	1.06
Mass(Kg)	1.04	1.192	1.04	1.359	1.705	1.542
Chip area	one Switch	one switch	Two Switches	Two Switches	Four Switches	Four Switches

switch area for one switch in one DAB configuration is same as the switch area for two switches in two DAB configuration. However in IGBT, one DAB topology is better. All in all, one DAB topology is better in volume and mass than two DAB and three DAB topologies.

The use of heatsink with fan has one restriction that each fan has to face the open air. The use of many heatsinks with fan makes the use of common switch and heatsink placement on the boards difficult. A heatsink with out fan can be put at the middle of a board. However, putting a heatsink at the middle of a board may not be effective means of cooling. The use of layered heatsink as shown in figure 3.26 can be used where the first two switches and the second two switches are in the upper and lower PCB.

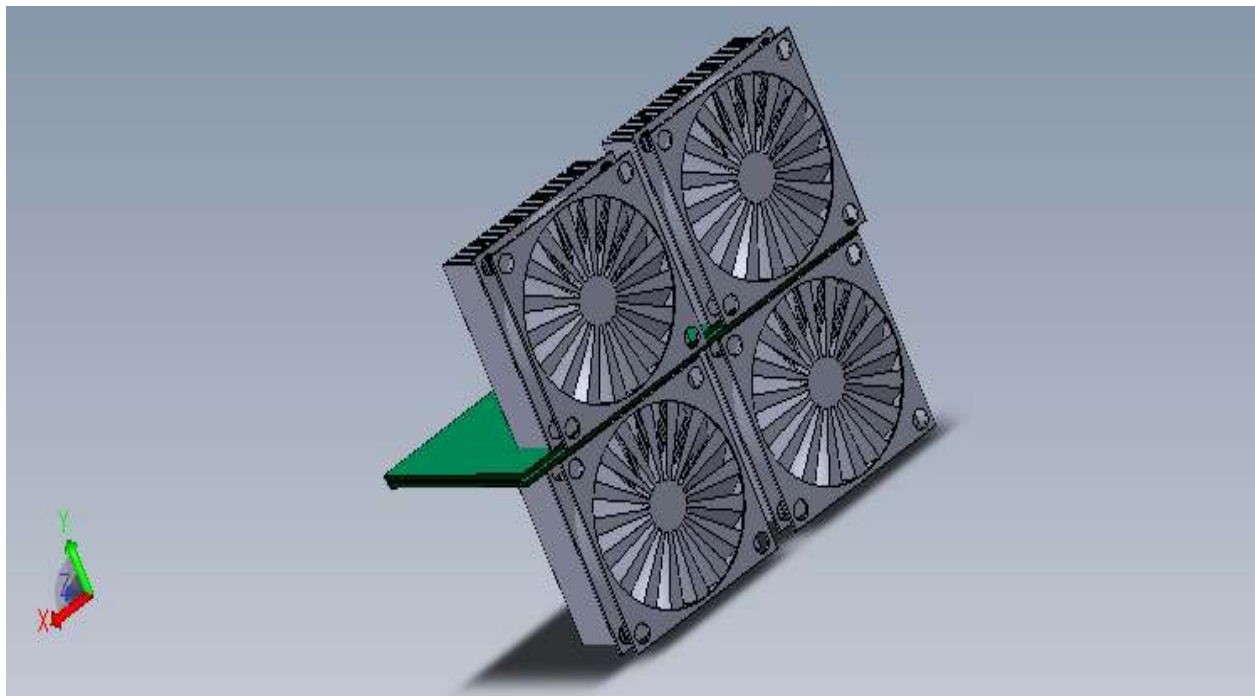


Figure 3.26: Use of layered heatsink for the four switches in one DAB(The gap between the layers is not to scale)

Chapter 4

Transformer Design

This chapter discusses the optimization of the transformer that couples the two full bridges in the primary and secondary of the Dual active bridge DC/DC converter. The general transformer design equations will be first discussed and will be followed by an evolutionary algorithm called particle swarm optimization(PSO) which will be used for the optimization of the transformer dimensions in terms of volume and transformer efficiency. This optimization mechanism will give us the Pareto front of the core dimensions for a given specification. For Pareto front obtained from the optimization method, thermal analysis will be performed to obtain the required thermal resistance of the cooling system. After that, a dimension with the best compromise of loss, volume and thermal resistance will be selected for the transformer designed.

Each topology's transformer, one, two interleaved and three interleaved DABs, will be optimized. For each topology's transformer, an optimized set of dimension which have the best trade-off between loss and volume will be selected and compared with the other topologies' transformer. For the optimized Pareto front of each topology's transformer, comparisons will be done.

The four most important design issues in a high-current, low-voltage DAB transformer are:

1. Core type selection
2. Leakage inductance
3. Winding loss
4. Thermal management

4.1 Core Type Selection

Proper core material selection for a given application is important in transformer design. In most applications, core loss and saturation flux density are the main selection criteria for given frequency. However, for high power, high frequency application, thermal conductivity and operating temperature are also main selection criteria[19]. For high frequency applications, soft magnetic

materials are predominantly used since they have very low core loss which, however, come at the expense of very low saturation flux density [22]. Nanocrystalline and ferrites materials exhibit the above mentioned characteristics. However, the possibility of freely choosing dimensions, as opposed to ferrites whose dimensions are standardized, makes nano-crystalline materials more attractive in high-power transformer optimization[19]. It enables optimizing transformer geometry for low loss, low mass and volume very easy[19]. The freedom of choosing dimensions of nano-crystalline cores is used here to optimize the loss and volume of the required transformer.

Loss densities of the nanocrystalline material FT-3M is given in [23] which is selected as specific core type to be used in this design.

4.1.1 Core Loss

The very common empirical formula for core loss calculation for sinusoidal flux density in mW/cm^3 is given by the following equation [24].

$$P_{CoreLoss} = C_m f^\alpha \hat{B}^\beta \quad (4.1)$$

where f is the frequency, \hat{B} is the peak flux density and C_m , α and β are material properties of the core type which can be found in the respective data sheet. In [25], the empirical formula is modified for non-sinusoidal flux density as follows,

$$P_{CoreLoss} = C_m f_{eq}^{\alpha-1} \hat{B}^\beta f_r \quad (4.2)$$

where f_r is the fundamental frequency and f_{eq} is given by (4.3)

$$f_{eq} = \frac{2}{\Delta B^2 \pi^2} \int_0^T \left(\frac{dB}{dt} \right)^2 dt \quad (4.3)$$

$\Delta B = 2\hat{B}$ and T is the period and the respective flux density. For a flux density with triangular shape of frequency, f_r , f_{eq} is

$$f_{eq} = \frac{8f_r}{\pi^2} \quad (4.4)$$

For FT-3M cut -core , the values of $C_m = 0.4$, $\alpha = 1.621$ and $\beta = 1.982$ [23].

4.2 Leakage Inductance

This sections discusses different methods to achieve the required series inductance with the transformer as shown in figure 3.1 and selects one of the methods to incorporate it in the optimization method as a constraint. Energy transfer of the DAB is done by the series inductance of the transformer. It is the key element in designing DAB. The inductance value should allow the maximum power transfer for a given frequency and input and output voltage ranges.

Different authors has proposed different methods to achieve the required leakage inductance which are briefly described below.

4.2.1 Adding External Inductor

In [26] an external inductor is added to the DAB. This increases the volume and mass of the DAB and also decreases the efficiency of the system.

4.2.2 Introducing Leakage Layers And Interleaving

In [27] leakage layers are introduced to increase the energy storage. This method increases loss. However, the layer material should be protected from saturation at peak flux density. Moreover, special measures should be taken from possible thermal breakdown of the introduced material. Due to the expected limited number of turns in the DAB (one turn for the primary since the current will be in the range of thousands of ampere), interleaving is not expected to have a significant effect.

4.2.3 Shaping Exposed Windings

In [19] the planar transformer is optimized for power loss with leakage inductance tuned by changing the length of the exposed windings which are out of the core. This method has the advantage of improved cooling of the windings but the leakage inductance has a limited range of tuning and external inductor could be introduced. This method also leads to increased winding losses.

4.2.4 Leakage Energy Storage Within Cores

This leakage inductances arise from the magnetic flux that does not completely link the primary and secondary windings. The leakage inductance can be tuned by the dimensions of the transformer. Dowel [28] gives the leakage inductance of a transformer where the window area is full of windings with no gap as follows:

$$Leakage = \frac{\mu_0 N^2 L_m w}{3h} \quad (4.5)$$

where $\mu_o = 4\pi 10^{-7}$ is the permeability of free space, N is the number of turns, L_m is the mean length of the turns, w is the width of the window area and h is the height of the window area.

The difficulty of this method is that there are four variables that can change the leakage inductance. Those are the mean length of the windings, the number of turns, width and height of transformer. Equation 4.5 is used as a constraints in the optimization of section 4.5.

4.3 Winding Losses

Copper loss in the primary and secondary windings are given by,

$$P_{CuLoss} = F_{acPr} R_{dcPri} I_{rmsPr}^2 + F_{acSec} R_{dcSec} I_{rmsSec}^2 \quad (4.6)$$

where F_{acPr} is primary ac-resistance coefficient and F_{acSec} is the secondary ac-resistance coefficient modeled to include effects of proximity. The skin effect is very small compared to the proximity effect in stranded wire where the diameter of each stranded wire are made less than the skin depth at a most important frequency as discussed below[29].

$$F_{ac} = 1 + (F_{\omega_1} - 1) \frac{\omega_{eff}^2}{\omega_1^2} \quad (4.7a)$$

$$F_{\omega_1} = 1 + \frac{\pi^2 \omega_1^2 \mu_0^2 N^2 n^2 d_c^6 k}{768 \rho_c^2 b_c^2} \quad (4.7b)$$

$$\omega_{eff} = \frac{rms\{\frac{di(t)}{dt}\}}{I_{TotalRMS}} \quad (4.7c)$$

where ω_1 is the fundamental frequency of the current waveform expressed in radian, ω_{eff} is the equivalent frequency of a non-sinusoidal waveform, n is the number of strands in a bundle, N is the number of turns, d_c is the diameter of the copper in each strand, ρ_c is the resistivity of the copper conductor, b_c is the breadth of the window area of the core, and k is a factor accounting for the field distribution in multiwinding transformers, normally equal to one.

The rule of thumb for the important highest harmonics number of importance in the DAB, N_{harm} , is given by 4.8 [29],

$$N_{harm} = \frac{0.7}{d} \quad (4.8)$$

where d is the duty ratio of the DAB. The diameter of the strands, d_c is assumed to be equal to skin depth of the highest harmonic frequency.

$$d_c = \frac{1}{\sqrt{\pi f_1 N_{harm} \mu_0 \sigma}} \quad (4.9)$$

where f_1 is the fundamental frequency, μ_0 is permeability of free space and σ is electrical conductivity of copper.

The diameter of a strand with insulation is given by the following empirical formula [29],

$$d_{strand} = d_r \alpha \left(\frac{d_c}{d_r} \right)^\beta \quad (4.10)$$

where d_{strand} is overall diameter, d_c is the diameter of the copper only and d_r is an arbitrarily defined reference diameter used to make the constants α and β unitless. The parameters found for single-build insulation are $\beta = 0.97$ and $\alpha = 1.22$ for d_r chosen to be the diameter of AWG 40 wire (0.079 mm) [29].

The number of strands, n , in a bundle is given by

$$n = \frac{EffectiveCoreWindowArea}{d_{strand}^2 N} \quad (4.11)$$

where $EffectiveWindowArea$ is the core window area times the fill factor and the fill factor is normally between 0.2 to 0.3 for litz wire, with 0.2 is taken here. The shape of the transformer

current for phase shift modulation, when the input and output voltage ratio is equal to the turns ratio, is trapezoidal. For a duty ratio d and Peak Current, I_{peak} , the rms of the current waveform, $I_{TotalRMS}$ and the rms of derivative of current, $I_{DeriRMS}$, are given by:

$$I_{TotalRMS} = I_{peak} \sqrt{1 - \frac{2d}{3}} \quad (4.12a)$$

$$I_{DeriRMS} = rms\left\{\frac{di(t)}{dt}\right\} = \frac{4I_{peak}}{T_s \sqrt{d}} \quad (4.12b)$$

From (4.7c) and (4.12), ω_{eff} is

$$\omega_{eff} = \frac{4}{T_s \sqrt{d} \sqrt{1 - \frac{2d}{3}}} \quad (4.13)$$

where ω_{eff} is the equivalent frequency of a non-sinusoidal waveform and T_s is the period of the fundamental frequency.

4.4 Thermal Management

In high-power, high-frequency magnetic-core applications where the ratio of surface area to volume of the magnetic components is very low and core losses are high, the transferring of heat from the core or winding hot spot to the surface and from surface to the heat exchange point is difficult to realize and advanced thermal management must be implemented [40]. There are different thermal management methods which can be used for cooling high frequency transformers, with forced air cooling being one of the main cooling mechanisms.

Several methods for the transfer of heat from hot spot to surface have been proposed by a number of different authors [[40],[41],[42]]. Petrov's [41] model is used here to analyze the transport of heat from the transformer's core to its surface, as shown in figure 4.1. where the minimum heatsink thermal resistance required for a change of 60 °C at the transformer hot spot is calculated assuming the ambient temperature is 45 °C. The hot spot is taken to be in center core of the volume and all the winding losses are considered to be concentrated at the hot spot. This assumption makes it worst case scenario. The heatsink base area is taken to be either the core's upper and lower surfaces or the exposed winding area. For each surface area, the required heatsink thermal resistances are estimated and the one with the highest value is selected from both.

When the heatsink is assumed to be on the core's lower and upper surface, exposed winding is considered to transfer heat to its surface by conduction and from the surface to air by natural convection. The value of the maximum allowable heatsink thermal resistance required on the core, equation (4.14), is derived from figure 4.1

$$R_{ca} = \frac{\frac{\Delta T}{(P_w + P_c)(R_w + R_{wa})}}{(R_w + R_{wa}) - \frac{\Delta T}{(P_w + P_c)}} \quad (4.14)$$

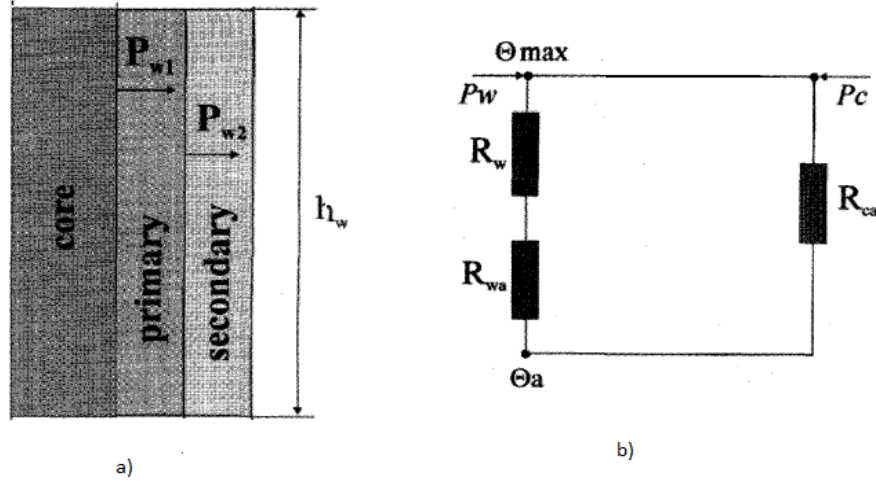


Figure 4.1: Thermal modelling of transformer [41]: a) Half of central section of the transformer: b) transformer thermal circuit when the hot spot is between the inner winding and the core: Θ_{max} is temperature at hot spot, Θ_a is core temperature at the surface

where R_{ca} is maximum allowable heatsink required, ΔT is change in temperature of the hot spot, P_w is the total winding loss, P_c is the core loss, R_w is the conduction thermal resistance of the exposed winding, and R_{wa} is convective thermal resistance of the winding in still air[?].

When heatsink is assumed to be attached to the exposed winding, heat from the core is transferred by convection. The conduction thermal resistance of the core is very small compared to the convective thermal resistance of the core and is short circuited [41]. Equation (4.15) is used to calculate the thermal resistance of external heatsink derived from figure 4.1.

$$R_{wa} = \frac{\left(\frac{\Delta T (R_w + R_{ca})}{(P_w + P_c)(R_{ca})} - R_w \right)}{1 - \frac{\Delta T}{(P_w + P_c)(R_{ca})}} \quad (4.15)$$

4.5 Transformer Dimensions Optimization

An evolutionary algorithm called Particle Swarm Optimization (PSO) initially introduced in [30] is used to optimize the dimensions of the transformer with regard to its volume and loss. It is a population based stochastic optimization inspired by social behavior of bird flocking or fish schooling. PSO is currently being used in wide variety of optimization techniques and is suitable for multiobjective optimization, for it has high convergence [31].

PSO is initialized by random solutions which are called particle swarm. Using some formulas explained in subsection 4.5.1, the particles are updated for a search of best solution. The update of each particle is governed by two rules. The rules are updating each particle by the best solution

each particle has so far achieved (local best) and by the best solution found so far by any particle in the whole population(global best). This process continues until the best solution or solutions is/are found measured by a fitness function.

This section deals with the explanation of the PSO and Multi-Objective Particle Swarm Optimization(MOPSO).

4.5.1 Basic Particle Swarm Optimization Algorithm

In the basic particle swarm optimization algorithm, particle swarm consists of n particles, and the position of each particle stands for the potential solution in D -dimensional space. The particles change their positions according to the following three principles:

1. Keeping their inertias
2. change position each particle's best position
3. the swarm's best position

During each iteration, the position of each particle is updated by the velocity of each particle. Each particle's velocity is influenced by its best position, the swarm's best position, inertia constant and some random numbers. After finding the two best solutions in each iteration(local and global best), the velocity and position of each particle change according to the following equations:

$$V[i + 1] = W \times V[i] + c_1 R_1 \times (PBest[i] - Pop[i]) + c_2 R_2 \times (Gbest[i] - Pop[i]) \quad (4.16a)$$

$$Pop[i + 1] = Pop[i] + V[i + 1] \quad (4.16b)$$

where $V[i + 1]$ is the current particle velocity, $V[i]$ is the previous particle velocity, W is the inertia. R_1 and R_2 are uniformly distributed random numbers between zero and one. c_1 and c_2 are learning rates for individual ability (cognitive) and social influence (group) respectively. $Pop[i + 1]$ is the current population of particles and $Pop[i]$ is the previous population of particles. $PBest[i] - Pop[i]$ is the distance between the particle's best previous position, and its current position. Finally the third term, $Gbest[i] - Pop[i]$, is the distance between the swarm's best experience, and the particle's current position.

In 4.16a, W is crucial for convergence behaviour. It adds the influence of previous velocity on the the current velocity. Depending on the value of W , it regulates the trade-off between global exploration and local exploitation. If the value of W is large, it facilitates global exploration, while a smaller value facilitates fine tuning in the current search area. A value that provides global and local exploration ability should be used.

4.5.2 Multi-objective optimization with PSO

This section defines basic concepts and terminologies necessary for the Multi-objective particle swarm optimization description(MPSO). The definitions are taken from the paper [31].

Definition 1: Global minimum Given a function $f: \Omega \subseteq \mathbb{R}^n \rightarrow \mathbb{R}$, $\Omega \neq \emptyset$, for $\vec{x} \in \Omega$, the value $f^* \triangleq f(\vec{x}^*) \geq -\infty$ is called a global minimum if and only if

$$\forall \vec{x} \in \Omega : f(\vec{x}^*) \leq f(\vec{x})$$

Then, \vec{x}^* is a global minimum solution, f is the objective function, \vec{x} is the feasible decision variable vector and the Ω is the feasible region.

Definition 2: Multi-objective Optimization Many application of PSO are multi-objective optimization as defined below:

$$\begin{aligned} &\text{Minimize } f_i(\vec{x}), \mathbf{x} = (x_1, x_2, \dots, x_n), i = 1, 2 \dots M \\ &\text{subject to } g_k(\vec{x}) \leq 0, k = 1, 2, \dots K \\ &\quad h_p(\vec{x}) = 0, p = 1, 2, \dots P \end{aligned} \tag{4.17}$$

where $f_i()$ are functions to be optimized, and $g_k()$ and $h_p()$ are inequality and equality constraints respectively. The main objective of multi-objective optimization(MOO) algorithms is to find a set of solutions which optimally balance the trade-offs among the objective functions. It differs from the basic PSO in that it returns more than one solution as opposed to the basic PSO's single solution.

Definition 3 : Pareto Optimality A point $\vec{x}^* \in \Omega$ is Pareto optimal if for every $\vec{x} \in \Omega$ and $i = \{1, 2, 3, \dots M\}$ either

$$\forall k \in i (f(\vec{x}) = f(\vec{x}^*))$$

or, there is at least one $k \in i$ such that

$$f(\vec{x}) > f(\vec{x}^*)$$

Definition 4: Pareto Dominance A vector $\mathbf{u} = (u_1, u_2, \dots, u_k)$ is said to dominate vector $\mathbf{v} = (v_1, v_2, \dots, v_k)$ if and only if \mathbf{v} is partially less than \mathbf{u} , i.e, $\forall i \in \{1, 2, \dots, k\}, u_i \leq v_i \wedge \exists i \in \{1, 2, \dots, k\} : u_i < v_i$

Definition 5 : Pareto Optimal Set For a given multi-objective optimization problem (MOP) $f(x)$, the Pareto optimal set (\mathcal{P}^*) is defined as

$$\mathcal{P}^* = \{x \in \Omega \mid \neg \exists x' \in \Omega, f(x') \preceq f(x)\}$$

Definition 6: Pareto front For a given MOO (\mathbf{x}) and the Pareto optimal set (\mathcal{P}^*), the Pareto front (\mathcal{PF}^*) is defined as

$$(\mathcal{PF}^*) := \vec{u} = \vec{f} = (f_1(x), \dots, f_k(x)) \mid x \in \mathcal{P}^*$$

A MPSO algorithm developed by [31] is selected for optimizing the transformer dimensions. The main algorithm is listed below:

1. Initialize the population : For n number of particles, the population, $POP[i]$, is initialized, where $i = 1, 2, ..n$
2. Initialize the speed of each particle: For n number of particles, the speed, $VEL[i]$, is initialized, where $i = 1, 2, ..n$
3. Evaluate each of the particles in POP
4. Store the positions of the non-dominated vectors in the Repository(REP)
5. Generate hypercubes of the search space explored so far. Hypercubes of a search space is grouping of the so far found non-dominated solution into different groups with respect the objective function values. This grouping is used as co-ordinate system for locating the particle's.
6. Initialize the memory of each particles best position so far found: For n number of particles, the best position, $PBEST[i]$, is initialized, where $i = 1, 2, ..n$
7. while maximum numbe of cyles has not been reached
DO

- (a) compute the speed of each part :

$VEL[i+1] = W \times VEL[i] + R_1 \times (PBEST[i] - POP[i]) + R_2 \times (REP[h] - POP[i])$
 where W is the inertia weight which takes a value of 0.4[31]; R_1 and R_2 are random numbers in the range [0....1]. $PBEST[i]$ is the best position a particle has so far; $REP[h]$ is a value that is taken from the repository; the index h is selected in the following way: those hypercubes containing more than one particles are assigned a fitness equal to the result of dividing any number $X > 1$ (10 is used) by the number of particles that they contain. This decreases the fitness of those hypercubes that contain more particles and it can be seen as a form of fitness sharing. Then roulette-wheel selection is applied to these fitness values to select the hypercube from which a corresponding particle will be taken. After a hypercube is selected, particles are randomly selected. $POP[i]$ is the current value of the particle i .

- (b) Calculate the new positions of each particle from the speed and current particles' position: $POP[i + 1] = POP[i] + VEL[i + 1]$
- (c) Maintain the particle with in the search space. Each decision variable takes the value of the corresponding boundary values and their velocities are multiplied by minus one.
- (d) Evaluate each of the particles in $POP[i + 1]$
- (e) Update the contents of REP together with the geographical representation of the particles with in the hypercubes. Any dominated position are eliminated and non-dominated new elements are added to the repository. If the REP is flil, particles from the most populated hyperspace are eliminated.
- (f) The best position of a particle is updated if the current position is better.
 $PBEST[i] = POP[i + 1]$.
 If neither of them dominated, take randomly one of them.

(g) Increment the loop counter

8. END

The above algorithm can be shown in flowchart as follows

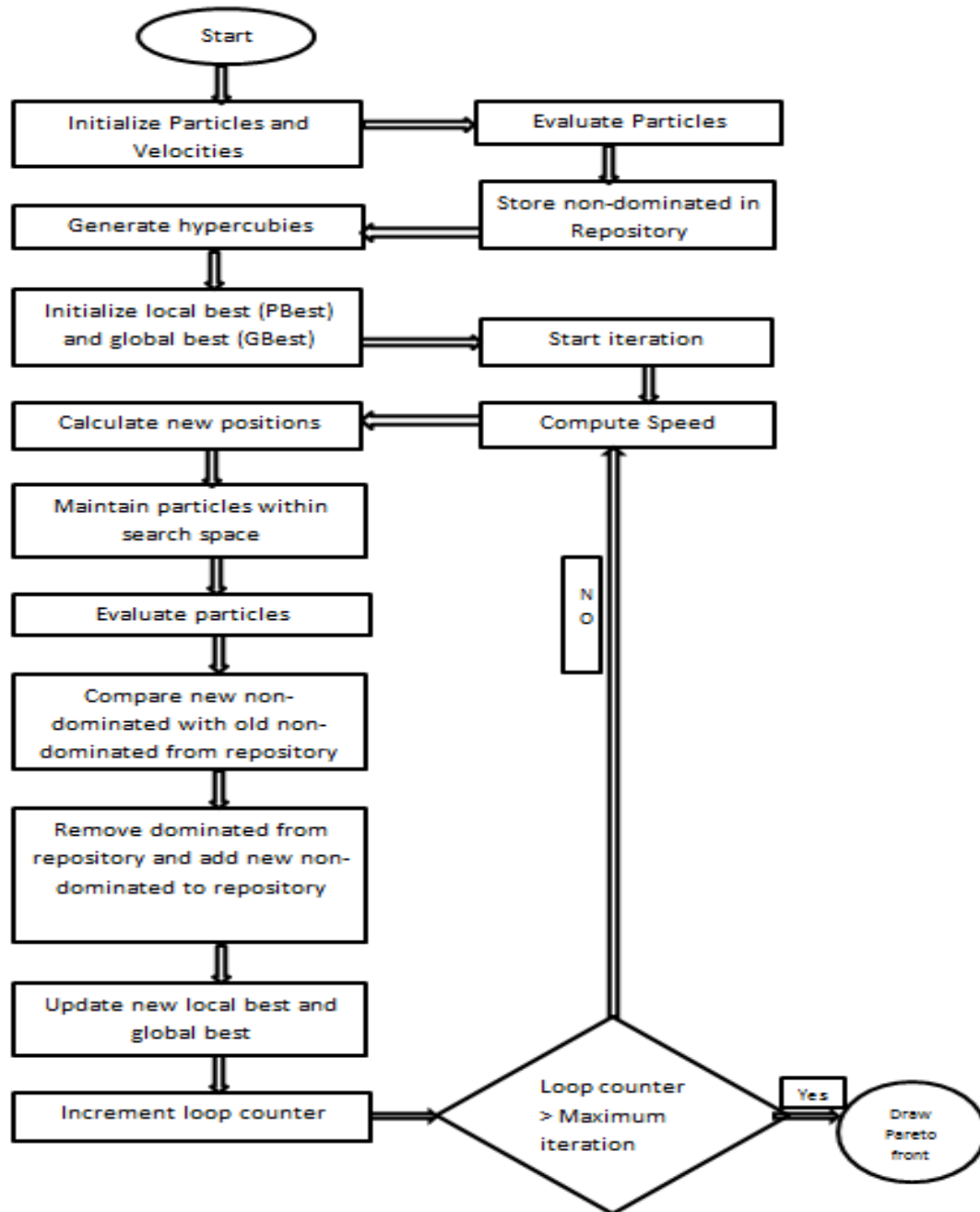


Figure 4.2: Flow chart of the multiobjective particle swarm optimization

4.5.3 Formulating Transformer equations into a multi-objective (MO) function

Two C-cored FT-3M type are assumed to be used for the construction of E core shown in figure 4.3. Four variables are used to describe the dimension of the core: a is the thickness of the outer legs, which is half of the thickness of the center leg, b is the width of window area, h is half of the height of the window core and d is the depth of the core.

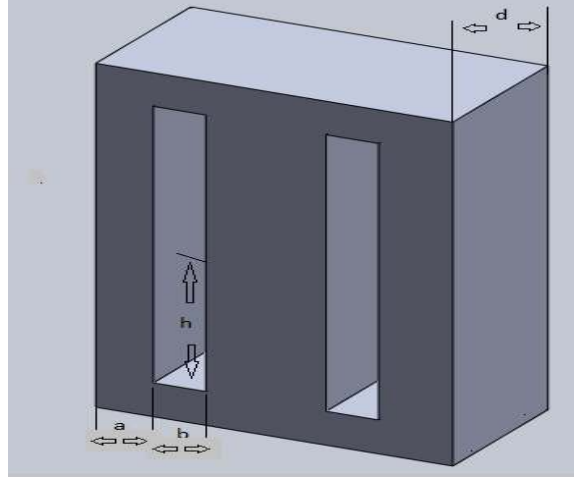


Figure 4.3: Transformer Dimensions

4.5.3.1 Objective functions

The objective functions in the transform design are the volume and loss of the transformer.

1. **Volume of Transformer** In two sides of the transformer, the windings are bulged out. The volume of the transformer includes those humps too. The volume is calculated as follows

$$Volume = Length \times Height \times Width \quad (4.18)$$

where $Length = (4a + 2b)$, $Height = (2a + 2h)$ and $Width = (d + 2b)$.

2. **Loss of the Transformer** The loss of the transformer is the sum of core and winding losses.

$$P_{Loss} = P_{CuLoss} + P_{CoreLoss} \quad (4.19)$$

4.5.3.2 Constraints

The transformer has the following constraints

1. **Dimensions:** All the dimensions, a , b , h and d have to be positive and also be greater than 0.5 mm, as it is the minimum thickness for the core type selected [19].

2. **Area Product of Transformer** The volt-ampere rating, S , of a transformer is defined as $S = V_{Pri}I_{Pri}$, where V_{Pri} and I_{Pri} are the rate of rms values of voltage and current respectively. The power capability of the transformer can be estimated from the area product in (4.20). The area product of the core should be greater than or equal to S [49].

$$A_P = A_C A_W = \frac{V_{Pri} I_{Pri} 10^4}{\hat{B} f J_{rms} K_f K_u} \quad (4.20)$$

$$A_C = 2ad \quad (4.21)$$

$$A_W = 2bh \quad (4.22)$$

$$\hat{B} = \frac{V_{Pri}}{4N_1 A_C f} \quad (4.23)$$

$$J_{rms} = \frac{I_{Pri}}{A_{Cu}} \quad (4.24)$$

where A_C is area of the core, A_W is area of the window, \hat{B} is the peak flux density, J_{rms} is rms current density, K_f is shape coefficient of the primary voltage which is 4 for triangular, K_u is fill factor which 0.2, N_1 is the number of primary turns, A_{Cu} is the copper are of the winding.

3. **Maximum Magnetic Flux:** Every core material has maximum saturation flux density. The maximum possible magnetic flux density, B_{Max} , of the core material should be greater than calculated used in the above
4. **Leakage inductance:** The leakage inductance expressed in equation (4.5), is the fourth constraint. For the power transfer is accomplished by the leakage inductance, the inductance should be capable of transferring the peak power. The leakage inductance calculated are 27.55nH, 55.1nH and 82.65nH transferred to the primary for one, two and three DAB topologies respectively.
5. **Number of turns** Due to the high current in the LV and HV side, the number of turns is set to 1 in the primary and 9 in the secondary.

4.6 Procedure of the Optimization

Objective function and constraints are formulated in the above sections. Those mathematical functions are used in the developed MPSO implementation in Matlab for calculating the Pareto front of the dimensions. The following steps summarize the optimization procedure

1. The inputs to the Matlab code are
 - (a) Frequency
 - (b) RMS current and voltage

- (c) Maximum leakage inductance
 - (d) Phase shift
 - (e) Power
 - (f) Maximum magnetic flux density
2. After the Pareto front is obtained for each topology and each mode of operation (Motor and Generator), thermal analysis as given in section 4.4 is applied to each point in the Pareto front. For each point, an external required thermal resistance is calculated either of the core surface area or exposed surface area.
 3. From the objective function output values and estimated thermal resistance of the Pareto front, comparisons are done and best values are taken, as will be described in the next section.

4.7 MPSO Result

An MPSO algorithm is implemented in Matlab to the core dimension optimization. It is implemented for the motor and generator modes for each circuit configuration (one, two, and three DAB). The shape of the transformer windings are taken as rectangular wires with a number of strand in each wire. The number of strands is calculated in the optimization.

Since the result of the MPSO generally depends on the number of iterations and number of particles selected, the number of iterations has been varied from 2000 to 15000 and the number of particles from 10 to 40 to see what effect this will have on the solution. These ranges of numbers are actually random choices as recommended by the authors of the algorithm[31]. Starting 4000 number of iterations, the output of the MPSO for a given transformer specification does not vary. Five thousand(5000) of iterations is taken for all the transformer dimension optimization simulations as the increase in it only increases the simulation time. More ever, changing the number of particles from 10 to 40 does not show any significant change on the results of the MPSO and 20 is taken in order to reduce required memory size and simulation time.

The simulations are done for both the motoring and generating modes. However, since the motoring mode has basically high current and high conduction losses compared to the generating mode, the design is dominated by the motoring mode requirements. In the motoring mode, there is peak power and average power. The peak power is for a very short period of time compared to the nominal power and is very high. Designing the transformer, assuming the peak power as steady state, would make the transformer unnecessarily big [19]. Rather than designing the transformer for the peak power, it would be beneficial if it is designed for the nominal power and transient thermal analysis for the peak power is implemented by slightly increasing the external heatsink using the thermal network as described in the [19]. This method would decrease the transformer volume and mass and the heatsink size significantly. However, transient thermal analysis is not implemented here, as it does not form part of the scope of this thesis, and as such the transformer design is based on the nominal power.

For the comparison reason, transformer design on the average power in motoring mode is analyzed here. For the average power optimized Pareto fronts obtained, the losses that are generated at

the peak power are also calculated. Moreover, Pareto fronts, taking the peak power as steady state, are in appendix A.4 since they do not form part of this comparison. The results and comparison of all the three DABs will be discussed for the average power. Firstly each topology's transformer optimization output will be discussed. After that a comparison among all the three topologies' output will be discussed.

The selection of a dimension from the Pareto front for each topology basically depends on the compromise among loss, volume and thermal resistance needed and are manually selected as the best compromise in each topology. Each point has been checked for the constraints after the simulation and is found to be within the constraints.

The initial values for the core depth and thickness are set to 0.5 cm as less than that is practically impossible due to the brittle nature of the core type [19] and the window width and height are set to 0.1 cm.

4.7.1 One DAB Optimization Result

Figure 4.4a shows the optimized Pareto front between power loss and volume and 4.4b shows the external thermal resistance calculated for the optimized Pareto fronts. Each point in the Pareto front corresponds to a set of transformer dimension. At lower volume, the high current density resulting from the small window area leads to very high losses. At higher volume, the current density decreases and the loss decreases. However, the decrease in power loss does not go beyond 320W due to the following two reasons.

1. The increase in window area increases the number of strands which increase the AC-resistance coefficient of the proximity effect
2. The increase in volume increases the core loss

The Pareto front graph is clipped to a maximum loss of 3000W and volume of 800 cm^3 , since values greater than those are impractical and similar clipping is done for the other topologies depending on the power rating. For each dimension, a thermal resistance needed for a 60°C temperature change on the hot spot are calculated and shown in plot 4.4b. As can be seen from figure 4.4b, the use of external heatsink on the core is better than the exposed windings for all points in the Pareto front. The series combination of conduction and convection resistance of the windings and the very small conduction resistance makes the use of external heatsink on the core better. Moreover, the optimized cores have big surface area than the exposed windings surface area since most of the windings are inside the core. So it makes the core physically preferable for cooling than the exposed windings.

Table 4.1 shows some the optimized set of dimensions with the total volume and total loss for one DAB. The window width(b) is small and the window height(h) is big for each optimized set of dimensions. This makes the primary and secondary winding to have a thin bus structure. This decreases the proximity effect on the number of strands that could be produced if the window width is big compared to the height. As can be seen from the table, the core thickness(a) is small

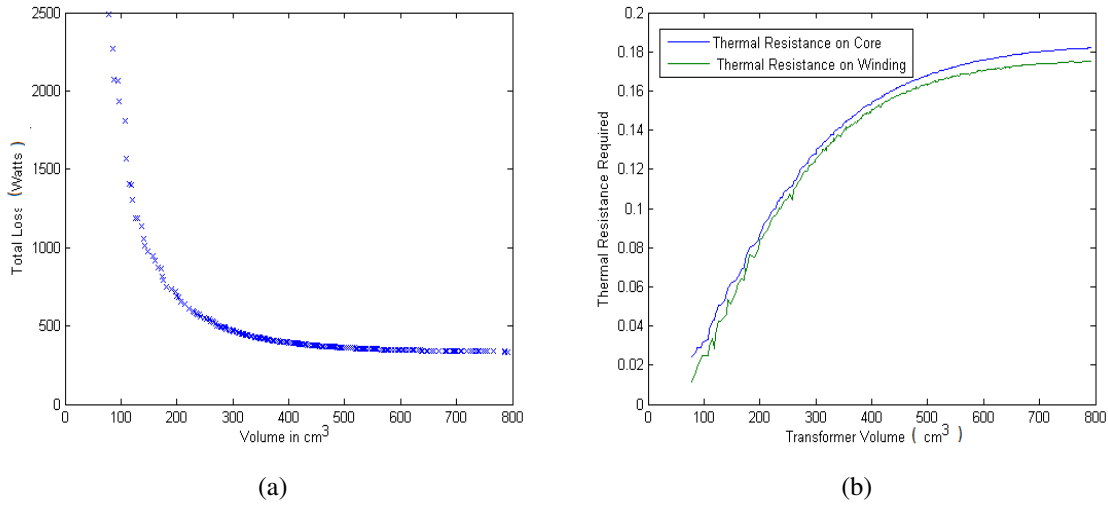


Figure 4.4: One DAB MPSO output at nominal power a)Optimized Pareto front of one DAB topology. Total loss as a function of total volume b)Estimated external thermal resistance: it is calculated for the core surface area and exposed winding

compared to the core depth (d). If the core thickness is big, the volume increases by four fold (two outer cores and the center core). And at the same time, the product of the core thickness and the core depth should have a minimum value in order for magnetic flux density not to go greater than the maximum value set, in this case 0.4T. This will be discussed in detail in the next paragraphs.

Table 4.1: Volume, loss and set of dimensions for some points from the Pareto front in figure 4.4a

total Volume(cm^3)	Loss(W)	a(cm)	b(cm)	h(cm)	d(cm)
391,3930721	396,7900847	1,064770416	1,218957831	4,028722824	3,299116427
395,0054488	396,4206048	1,032547232	1,29962516	3,840221799	3,423826295
397,0945361	396,2995792	1,128111251	1,191201102	4,094082874	3,131845327
397,5543716	395,6353872	0,999940993	1,263982713	4,027127109	3,529481621
398,2083932	395,4053604	1,081687414	1,272068648	3,89679143	3,276505458
399,1987998	393,382305	1,058224999	1,164179778	4,331479711	3,315900836
400,7263062	392,3521113	1,051746363	1,222323407	4,154034981	3,341689921
404,5652521	391,6902476	1,038773515	1,277682644	4,02929309	3,392539661
406,963955	389,8319852	1,071732201	1,243435116	4,141105235	3,275742842
408,5913209	388,530274	1,098651548	1,298539702	3,952723681	3,187444512
411,7475772	388,467118	1,093821559	1,273890498	4,056661937	3,225922906
411,8179964	388,4543282	1,091028928	1,186915028	4,37100082	3,221088298
412,2011529	388,3356208	1,067012085	1,146810473	4,56381864	3,28455742

Table 4.2 shows the bundle diameter, the strand diameter and strand number in the primary and secondary windings. As the strand diameter assumed to be equal to the skin depth of the most important harmonic in the current waveform in the transformer windings, the strand diameter in the primary and secondary are same. However, the number of strands differ as the current in the primary is higher than the current in the secondary. The primary current density for the first set of dimension in table 4.2 is $9.4 \frac{A}{mm^2}$. However, for the last set of dimension, it is $8.85 \frac{A}{mm^2}$. This shows that the current density is not infeasible, of course for high current application, such current densities are recommended [13].

Table 4.2: Bundle diameter, strand diameter and number of strands for the primary and secondary windings designed for each set of dimension in table 4.1

Primary winding			Secondary winding		
bundle diameter (Meters)	strand diameter (Meter)	No. of strands	bundle diameter (Meter)	strand diameter (Meter)	No. of strands
0,018003212	0,000280197	1238	0,006001071	0,000280197	161
0,018149271	0,000280197	1259	0,006049757	0,000280197	163
0,017940842	0,000280197	1230	0,005980281	0,000280197	160
0,01832906	0,000280197	1284	0,006109687	0,000280197	167
0,018087595	0,000280197	1250	0,006029198	0,000280197	162
0,018243163	0,000280197	1272	0,006081054	0,000280197	165
0,01830628	0,000280197	1281	0,006102093	0,000280197	166
0,018433079	0,000280197	1298	0,00614436	0,000280197	169
0,018434937	0,000280197	1299	0,006144979	0,000280197	169
0,018405508	0,000280197	1294	0,006135169	0,000280197	168
0,018468109	0,000280197	1303	0,006156036	0,000280197	169
0,018504281	0,000280197	1308	0,006168094	0,000280197	170
0,018585831	0,000280197	1320	0,006195277	0,000280197	171

Table 4.3 shows the core and copper losses, magnetic flux density, core and winding thermal resistance required for cooling the transformers, and leakage inductance of the cores.

The copper is the major loss contributor than the core. For each optimized core, the magnetic flux approaches to $0.4T$. The core thickness and core depth decreases to attain a small transformer volume. However, their product can not be less than a minimum value that makes the magnetic flux density in the core greater than $0.4T$ as the core saturates. This means their product should be increased to decrease the magnetic flux density which in turn decreases the core loss. However, the product can not increase indefinitely as the volume increases. The optimal point is that having their product as small as possible but the core saturation magnetic flux density is not violated. That is why all the optimized cores have a magnetic flux density near to $0.4T$.

The leakage inductance for one DAB is estimated to be $27.55nH$. Each core has a value less than the estimated value as can be seen from table 4.3 column six.

Table 4.3: Losses, magnetic flux density, core and winding thermals and Leakage inductance for the dimensions in table 4.1

Copper Loss (W)	Core Loss (W)	Magnetic Flux density(T)	Core thermal resistance($\frac{^{\circ}C}{W}$)	Winding thermal resistance($\frac{^{\circ}C}{W}$)	Leakage Inductance H
363,2553687	33,534716	0,398542295	0,152584225	0,148820087	9,97001E-09
364,1492412	32,27136364	0,396010212	0,152736721	0,148502321	1,14657E-08
362,2824133	34,01716596	0,396255953	0,152807721	0,149237284	9,47031E-09
362,511406	33,12398121	0,396682223	0,153024794	0,149075729	1,05932E-08
362,6776296	32,72773089	0,395016615	0,153154084	0,149117652	1,09173E-08
358,2291931	35,15311194	0,398977573	0,15392271	0,150595696	8,73723E-09
358,164507	34,18760425	0,398337202	0,154342216	0,150680913	9,72461E-09
358,2378597	33,45238785	0,397266765	0,154619393	0,150660697	1,06599E-08
355,5035489	34,32843633	0,398778702	0,155379058	0,151651661	9,9439E-09
354,9066841	33,62358986	0,39978402	0,155935114	0,151869476	1,09837E-08
354,5852585	33,88185948	0,396759718	0,155956188	0,152076322	1,04722E-08
352,861661	35,5926672	0,398372306	0,155944172	0,152596452	8,84582E-09
351,7701663	36,56545452	0,399467856	0,155975145	0,152887552	8,11765E-09

In figure 4.4, the decrease in the power loss and the increase in thermal resistance after 400 cm^3 is very small. That point is taken as the best choice and the corresponding dimensions are $a=1.051 \text{ cm}$, $b=1.222 \text{ cm}$, $h=4.154 \text{ cm}$ and $d=3.34 \text{ cm}$. The strand diameter, the number of strands in the primary and secondary are 0.2802 mm and 1076 and 0.2802 mm and 140 respectively. For each point in the Pareto front, all other parameters are listed in appendix A.5 table A.7.

The power loss at peak power (23 kW) for each point in the Pareto front is shown in figure 4.5. The peak power loss for the selected dimension is 1680 W .

An external heatsink with a thermal resistance of $0.154 \text{ }^{\circ}\text{C}/\text{W}$ on the core or $0.1543 \text{ }^{\circ}\text{C}/\text{W}$ on the winding is needed to cool the transformer to $105 \text{ }^{\circ}\text{C}$. This is very difficult to attain by external heatsink as most thermal interface materials have too low thermal conductivity which leads to high thermal resistance. The value of external heatsink thermal resistance will be very low which leads to a bigger volume and mass. Therefore, the use of another cooling methodology like heat pipes or liquid cooling is recommended [40]. This leads to an increase in price and complexity.

4.7.2 Two DAB Optimization Result

Similarly the output of the MPSO for two DAB topology are shown in figure 4.6.

The selection of the dimension is based on the same principle described in one DAB topology. The value of the dimension selected are $a=0.811 \text{ cm}$, $b=0.901 \text{ cm}$, $h=2.44 \text{ cm}$, $d=4.312 \text{ cm}$. The loss is 182.9 W at a transformer volume of 201 cm^3 for each DAB..

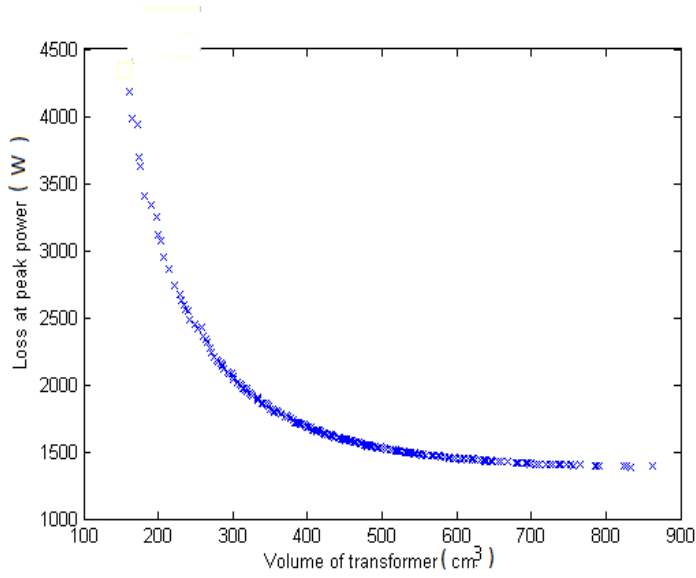
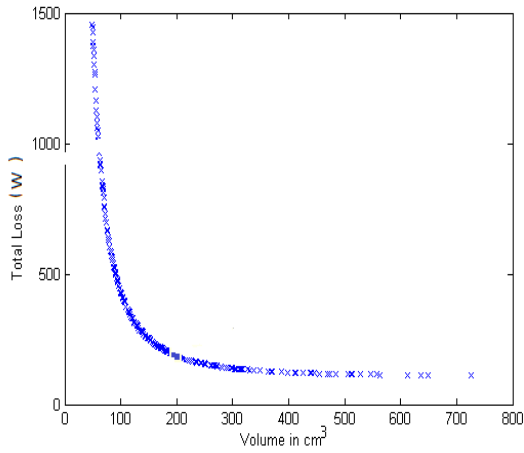
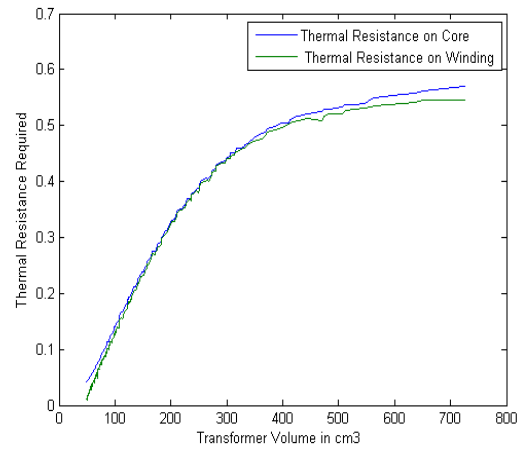


Figure 4.5: The power loss at peak power for Pareto front obtained at nominal power



(a)



(b)

Figure 4.6: Two DAB MPSO output at nominal power a)Pareto front for two DAB topology per DAB b)Required external thermal resistance: it is calculated for the core surface area and exposed winding

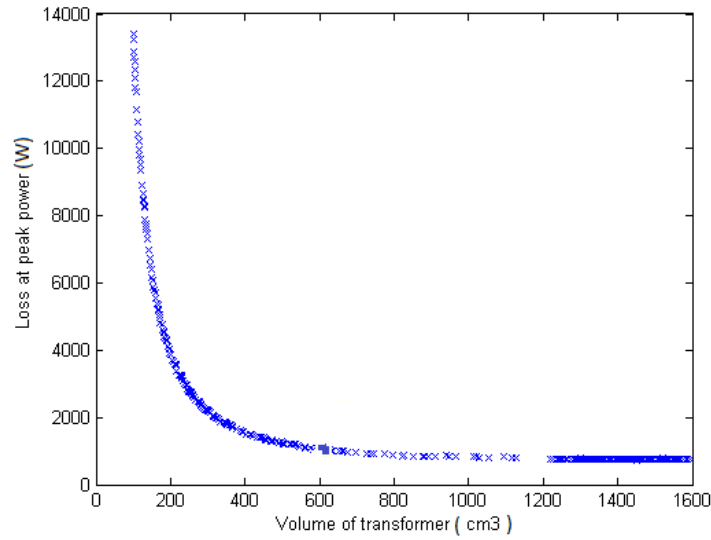


Figure 4.7: The power loss at peak power for Pareto front obtained at nominal power for two DAB topology

The power loss at peak power(23kW) for each point in the Pareto front is shown in figure 4.7. The peak power loss for the selected dimension is 1511 W.

4.7.3 Three DAB Optimization Result

Figure 4.8 shows the MPSO output for the three DAB transformer. The selection of the dimension is based on the same principle described in one DAB topology. The loss for each topology is 84.85W at a volume of 197.4 cm^3 . The value of the dimension selected are $a = 0.81 \text{ cm}$, $b = 1.179 \text{ cm}$, $h = 1.826 \text{ cm}$, $d = 4.324 \text{ cm}$.

The peak power loss (23kw) for each point in the Pareto front is shown in figure 4.9. The peak power loss for the selected dimension is 1017W.

4.7.4 Comparison of the topologies

For a given transformer volume, in the low volume and high loss region of the Pareto front, one DAB topology is found to be better because the transformers initial sizes are same for all of them. However, in low loss and high volume region, the two DAB and three DAB topology are better due to the number of strands increase has large effect in the conduction loss for the one DAB transformer as seen in Table 4.4. More ever, the use of two or three DABs have significant advantage in terms of cooling due to large surface area compared to the single DAB in the high volume and low loss region of the curve and have low loss at peak power.

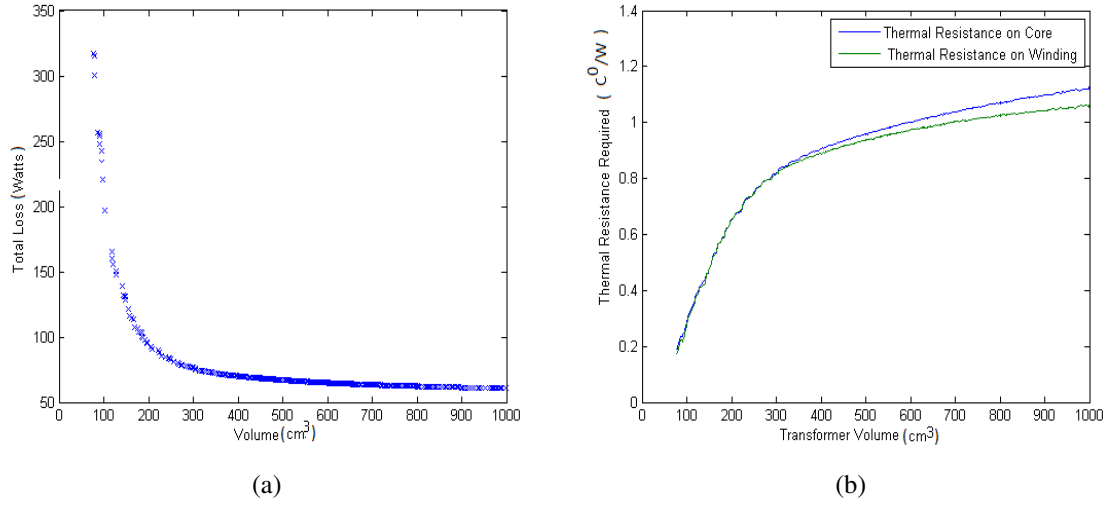


Figure 4.8: Three DAB MPSO output at nominal power a)Pareto front for three DAB topology: The values shown are per DAB b) required external thermal resistance. It is calculated for the core surface area and exposed winding area

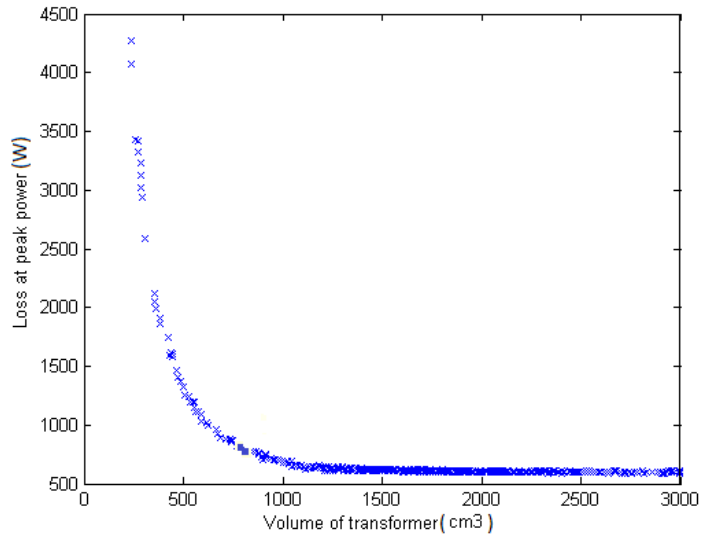


Figure 4.9: The power loss at peak power for Pareto front obtained at nominal power for three DAB Topology

Table 4.4: Comparison of the three transformer topologies optimized outputs

total Volume(cm ³)	Loss at nominal power(Watts)		
	One DAB	Two DAB	Three DAB
230	585	710	951
300	472	508	594
400	392	366	444
500	361	310	339
600	346	278	279
750	337	250	246
900	334	240	230

The transformers designed with one turn primary and nine turns of secondary has the structure as shown in figure 4.10. The primary turn is a bus of the litz wire.

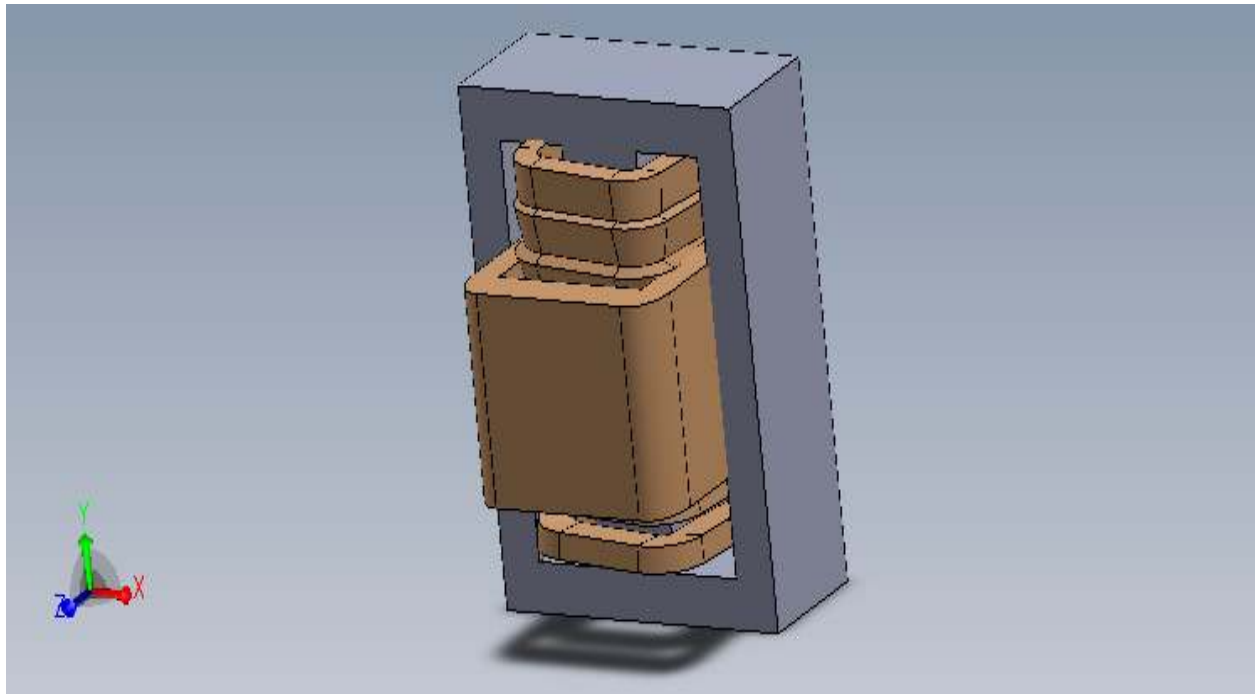


Figure 4.10: Transformer model designed using the optimization method(The transformer not to scale)

Chapter 5

Conclusion

A literature review of different circuit configurations has been studied briefly. The single Dual Active Bridge is found to be suitable to the specifications required in terms of switch count, inherent soft-switching, weight, volume and efficiency. The selection of the switching mechanism and its steady state analysis is described to determine the rating of the active and passive components. The estimated high current at the LV and HV sides induce the use of interleaved DABs. The interleaved three DABs is obtained to have a significantly less capacitor number requirement. It has substantially less capacitor volume and mass compared to the one and interleaved two DABs.

After selecting the active devices which meet the current and voltage requirements estimated, MOSFETs in the primary and IGBTs in the secondary, the required external thermal resistance of the heatsink for the switches is optimized by varying the junction temperature. The selection of the junction temperature has a large effect on the volume of the cooling system and efficiency of the DC/DC converter. The increase in junction temperature of the MOSFETs and IGBTs increases the maximum allowable thermal resistance. This increase of thermal resistance decreases the volume and mass of the cooling system implemented. However, it increases the conduction losses of the transistors. A compromise between the efficiency and maximum allowable external thermal resistance is made.

Afterwards, heatsinks with fan are designed for every maximum allowable external thermal resistance estimated. The heatsinks are optimized for volume and mass with respect the number of switches placed on them. It is found that in the one DAB configuration, one heatsink for each switch is better. However, the use of two switches and four switches per heatsink are found to be better in terms of mass and volume for two and three interleaved DABs configuration respectively. Heatsinks designed for one DAB circuit configuration have less volume and mass than for two and three interleaved DABs even though the difference in volume and mass is not as significant as the difference in capacitor volume and mass calculated for the three configurations.

Finally, transformer dimension optimization for each circuit configuration is implemented using an evolutionary algorithm, particle swarm optimization. For each configuration, after the optimization is carried out, a set of dimensions is selected which has good compromise among volume, mass and required thermal resistance for cooling. The requirements of external cooling system for the three interleaved DABs configuration is determined to have been better due the large core surface

area of the three transformers.

For a transformer volume of 400 cm^3 , the efficiency at constant generating power (12KW) are 0.903, 0.8892 and 0.892 for one, two and three interleaved DABs respectively. Since the loss is mainly due to the transistor conduction and switching losses, the effect of transformer loss and capacitor losses at nominal power in the efficiency is very small.

The interleaved three DAB is found to be attractive in terms of capacitor number which leads to a small volume and mass. It is also found to be attractive in terms of thermal management of the transformers designed using the particle swarm optimization. This decreases the volume of cooling systems needed for the transformer. Interleaved three DAB is selected as best in terms of volume, mass and thermal management, even though it has slightly less efficiency due to the less number of MOSFETs used.

5.1 Future Work

1. The number of interleaved DABs investigated is limited to three. However, a large number of interleaved DABs would be expected to decrease the number of capacitors to a very small number. Increasing the number of DABs interleaved decreases the volume and mass of the DC/DC converter considerably as the volume and mass of the three investigated DABs is dictated by the capacitor mass and volume. So further investigation in the increase of interleaved has to be done.
2. The heatsink and transformer optimization is calculated for the peak power. Using these values as maximum starting point, transient thermal analysis for determining the switches' and transformer external thermal resistance could be implemented and a large decrease in the volume and mass of external cooling system could be found. Therefore, modeling of transformers for transient thermal analysis has to be implemented for high-frequency and high-power as the transient thermal analysis for switches is implemented in the paper work by [19].
3. The effect of decreasing the phase shift between the two full bridges in a DAB has been studied. It has an advantage in decreasing the circulating current which decrease the components' rating. However, the decrease has a disadvantage in increasing the important harmonic frequency of the transformer which leads to higher proximity and skin effect losses. Therefore, the compromise between phase shift decrease and an increase in the important harmonic frequency has to be studied thoroughly.
4. Each component has been optimized and the assembly of the whole system is not finished. Systematic integration of the whole components with detail inter-connections would definitely has a significant effect on the total volume. This could also be further investigated.

Appendices

Appendix A

RMS and Average Currents of Devices

A.1 Estimated Current Values and Switch Losses

Device	Power					
	Motoring Mode				Generating Mode	
	12kw		23kw		12kw	
	RMS	Average	RMS	Average	RMS	Average
Transformer Current	9.98e+002	0	2.15e+003	0	4.35e+002	0
LV Switches	6.98e+002	4.76e+002	1.48e+003	9.58e+002	3.07e+002	2.16e+002
LV Diodes	9.92e+001	1.42e+001	3.41e+002	7.37e+001	1.85e+001	1.18e+000
HV Switches	1.10e+001	1.58e+000	3.78e+001	8.19e+00	2.06e+000	1.31e-001
HV Diodes	7.77e+001	5.28e+001	1.65e+002	1.07e+002	3.41e+001	2.39e+001

Table A.1: RMS and average currents of each device in the primary and secondary switches and transformer for a single DAB design during motoring and generating

Device	Power					
	Motoring Mode				Generating Mode	
	12kw		23kw		12kw	
	RMS	Average	RMS	Average	RMS	Average
Transformer Current	4.99e+002	0	1.07e+003	0	2.17e+002	0
LV Switches	3.49e+002	2.38e+002	7.42e+002	4.79e+02	1.54e+002	1.08e+002
LV Diodes	4.96e+001	7.12e+000	1.70e+002	3.69e+001	9.28e+000	5.90e-001
HV Switches	5.51e+000	7.91e-001	1.89e+001	4.09e+000	1.03e+000	6.55e-002
HV Diodes	3.88e+001	2.64e+001	8.25e+001	5.32e+001	1.70e+001	1.19e+001

Table A.2: RMS and average currents of each device in the primary and secondary switches and transformer for two DAB design during motoring and generating

Device	Power					
	Motoring Mode				Generating Mode	
	12kw		23kw		12kw	
	RMS	Average	RMS	Average	RMS	Average
Transformer Current	3.33e+002	0	7.18e+002	0	1.45e+002	0
LV Switches	2.33e+002	1.58e+002	4.95e+002	3.19e+002	1.02e+002	7.18e+001
LV Diodes	3.31e+001	4.75e+000	1.14e+002	2.46e+001	6.19e+000	3.93e-001
HV Switches	3.67e+000	5.27e-001	1.26e+001	2.73e+000	6.87e-001	4.37e-002
HV Diodes	2.58e+001	1.76e+001	5.50e+001	3.55e+001	1.14e+001	7.98e+000

Table A.3: RMS and average currents of each device in the primary and secondary switches and transformer for three DAB design during motoring and generating

A.2 Capacitor Comparison Tables

The tables show the volume, mass and loss for a one DAB topology for an electrolytic, polypropylene and a combination of electrolytic and polypropylene.

	Number	volume(cm^3)	mass (Kg)	Loss (W)
Input Capacitor	46	6284	10.58	361
Output Capacitor	3	410	.69	67.8
Total	49	6694	11.27	428.8

Table A.4: Capacitor Number, volume, mass and loss calculation for 101C203U063AF2B , electrolytic type

	Number	volume(cm^3)	mass (Kg)	Loss (W)
Input Capacitor	176	9088.51	11.264	51
Output Capacitor	5	258	0.32	22.4
Total	181	9346.51	11.584	73.4

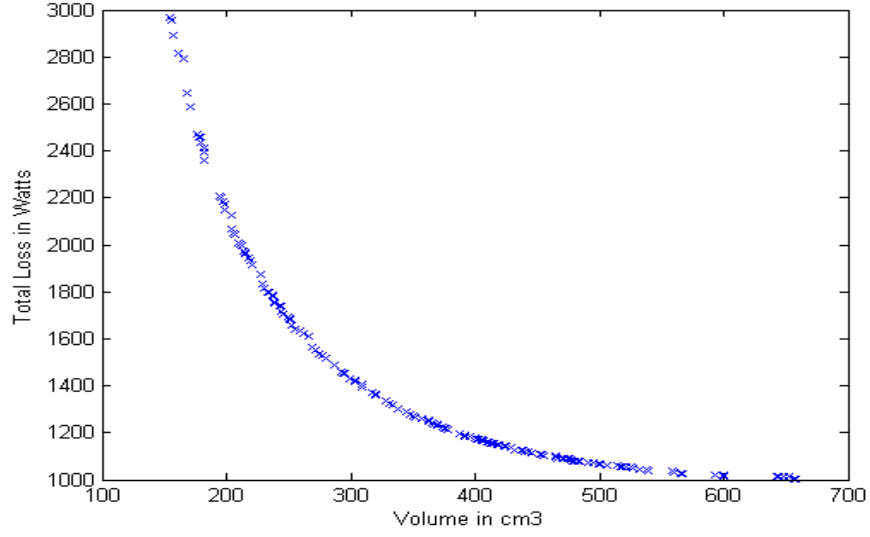
Table A.5: Capacitor Number, volume, mass and loss calculation for UNL4W30K-F. polypropylene

	Number	volume(cm^3)	mass (Kg)	Loss (W)
Input Capacitor	2EL + 82 Poly	2762	2.662	111
Output Capacitor	10 Poly	334	.32	11
Total	2El + 92Poly	3096	2.962	122

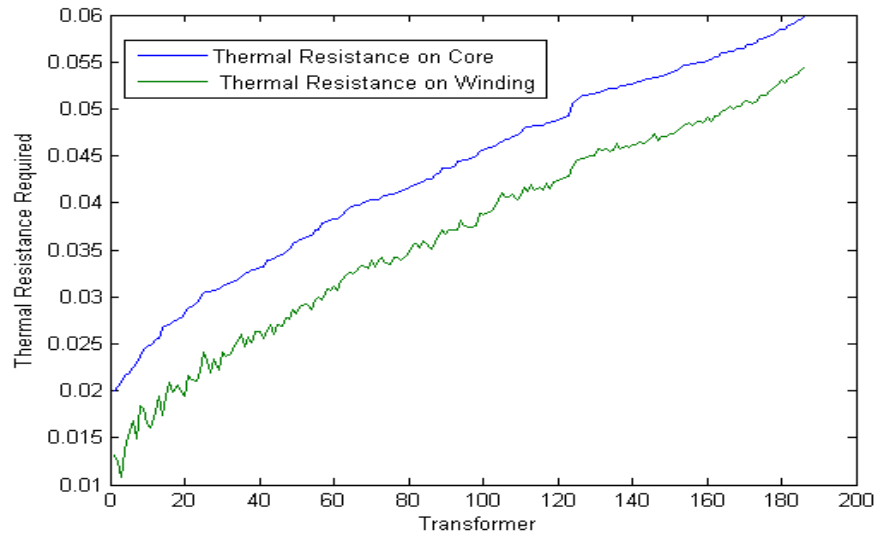
Table A.6: Capacitor Number , volume , mass and loss calculation for polypropylene, 935C1W30K-F and an electrolytic capacitor, 381LX1222MO63H012

A.3 Switches temperature dependent parameter equations and graphs

A.4 MPSO Graphs for 23Kw

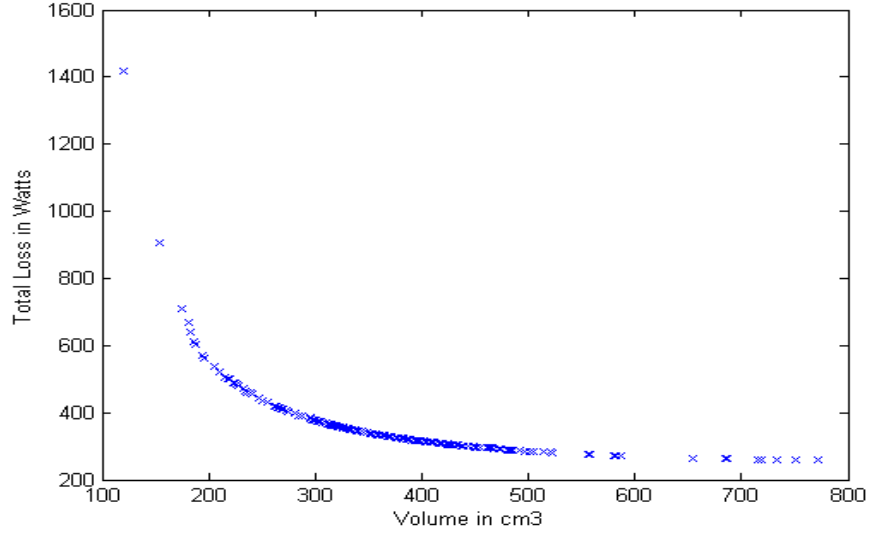


(a) Pareto front for Two DAB topology

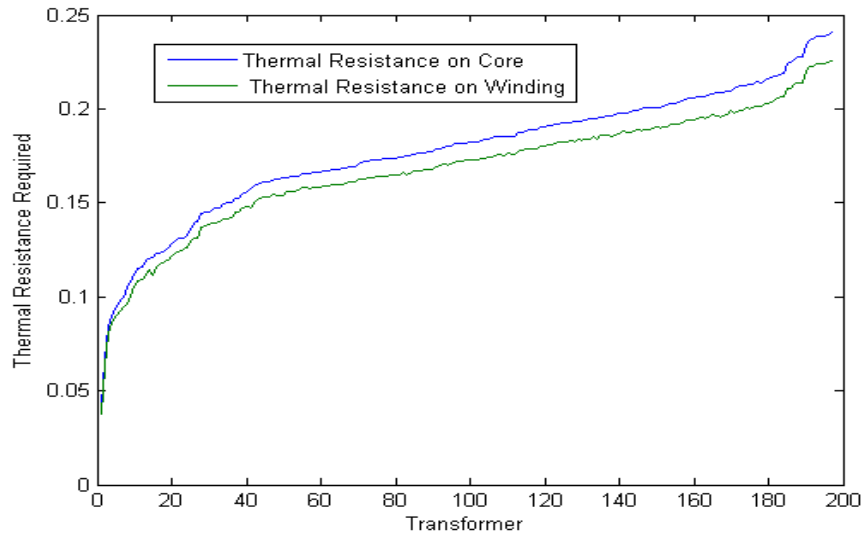


(b) External thermal resistance needed: it is calculated either for the core area or exposed winding area

Figure A.1: One DAB MPSO out put

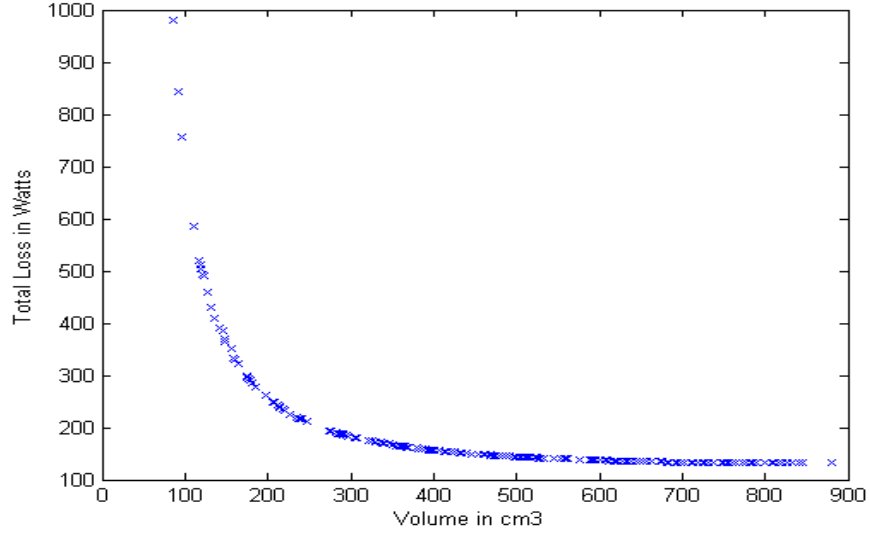


(a) Pareto front for Two DAB topology

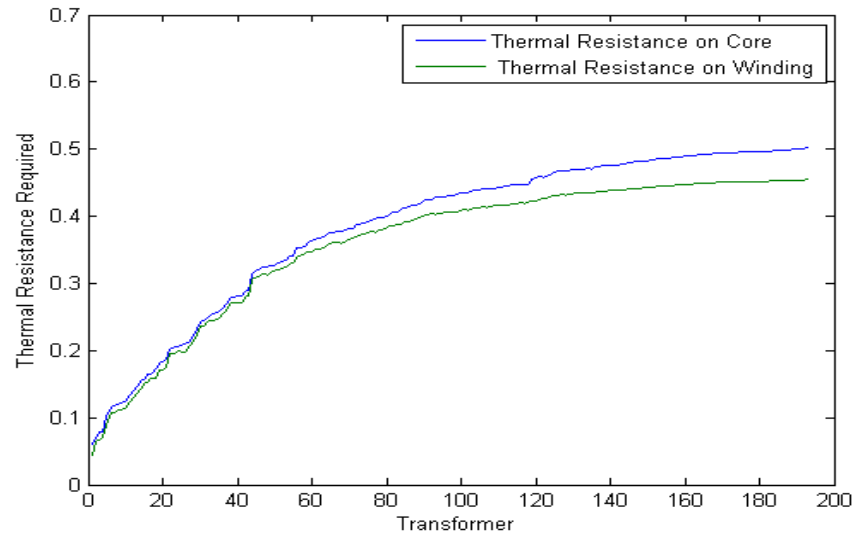


(b) External thermal resistance needed: it is calculated either for the core area or exposed winding area

Figure A.2: Two DAB MPSO out put



(a) Pareto front for three DAB topology



(b) External thermal resistance needed: it is calculated either for the core area or exposed winding area

Figure A.3: Three DAB MPSO out put

A.5 Pareto Front Results

Table A.7: Output of MPSO for one DAB topology for average power inputs

Volume (cm ³)	Loss(W)	a	b	h	d	Primary Winding			Secondary Winding			Copper Loss	core Loss	Magnetic Flux
						bundle Diameter	Wire Di- ameter	number of Strands	bundle Diameter	Strand Diameter	No. Of Strands			
2,81E+01	5,60E+04	5,00E-01	1,00E-01	2,76E-01	8,03E+00	1,35E-03	2,80E-04	7,00E+00	4,50E-04	2,80E-04	1,00E+00	5,60E+04	4,26E+00	3,49E-01
3,11E+01	3,89E+04	5,00E-01	1,00E-01	3,86E-01	7,78E+00	1,60E-03	2,80E-04	1,00E+01	5,32E-04	2,80E-04	1,00E+00	3,89E+04	4,98E+00	3,60E-01
4,47E+01	3,52E+04	6,85E-01	1,00E-01	3,98E-01	6,81E+00	1,62E-03	2,80E-04	1,00E+01	5,40E-04	2,80E-04	1,00E+00	3,52E+04	5,04E+00	3,00E-01
4,57E+01	1,04E+04	5,27E-01	2,36E-01	6,05E-01	7,36E+00	3,07E-03	2,80E-04	3,60E+01	1,02E-03	2,80E-04	5,00E+00	1,04E+04	6,67E+00	3,61E-01
4,61E+01	1,04E+04	5,93E-01	2,03E-01	6,31E-01	6,37E+00	2,91E-03	2,80E-04	3,20E+01	9,70E-04	2,80E-04	4,00E+00	1,04E+04	7,26E+00	3,71E-01
5,65E+01	8,13E+03	5,40E-01	3,41E-01	5,96E-01	8,08E+00	3,66E-03	2,80E-04	5,10E+01	1,22E-03	2,80E-04	7,00E+00	8,13E+03	6,21E+00	3,21E-01
5,95E+01	7,34E+03	6,02E-01	3,83E-01	5,55E-01	7,34E+00	3,75E-03	2,80E-04	5,40E+01	1,25E-03	2,80E-04	7,00E+00	7,34E+03	6,33E+00	3,17E-01
6,11E+01	6,45E+03	6,64E-01	1,73E-01	1,08E+00	5,49E+00	3,51E-03	2,80E-04	4,70E+01	1,17E-03	2,80E-04	6,00E+00	6,44E+03	1,04E+01	3,84E-01
6,90E+01	3,83E+03	5,90E-01	2,97E-01	1,16E+00	6,07E+00	4,78E-03	2,80E-04	8,70E+01	1,59E-03	2,80E-04	1,10E+01	3,82E+03	1,10E+01	3,91E-01
7,46E+01	3,56E+03	8,52E-01	3,95E-01	8,34E-01	4,47E+00	4,67E-03	2,80E-04	8,30E+01	1,56E-03	2,80E-04	1,10E+01	3,55E+03	1,02E+01	3,67E-01
7,75E+01	2,49E+03	6,58E-01	5,45E-01	9,65E-01	5,33E+00	5,89E-03	2,80E-04	1,33E+02	1,96E-03	2,80E-04	1,70E+01	2,48E+03	1,12E+01	4,00E-01
8,64E+01	2,27E+03	5,98E-01	4,92E-01	1,24E+00	5,97E+00	6,35E-03	2,80E-04	1,54E+02	2,12E-03	2,80E-04	2,00E+01	2,26E+03	1,21E+01	3,92E-01
8,71E+01	2,08E+03	7,25E-01	5,59E-01	1,09E+00	4,86E+00	6,34E-03	2,80E-04	1,54E+02	2,11E-03	2,80E-04	2,00E+01	2,06E+03	1,23E+01	3,98E-01
9,55E+01	2,06E+03	1,02E+00	4,10E-01	1,27E+00	3,44E+00	5,86E-03	2,80E-04	1,31E+02	1,95E-03	2,80E-04	1,70E+01	2,05E+03	1,47E+01	3,99E-01
9,70E+01	1,93E+03	7,16E-01	4,37E-01	1,48E+00	5,02E+00	6,55E-03	2,80E-04	1,64E+02	2,18E-03	2,80E-04	2,10E+01	1,92E+03	1,39E+01	3,90E-01
1,07E+02	1,81E+03	9,28E-01	5,80E-01	1,16E+00	4,10E+00	6,66E-03	2,80E-04	1,69E+02	2,22E-03	2,80E-04	2,20E+01	1,80E+03	1,29E+01	3,68E-01
1,09E+02	1,57E+03	9,13E-01	6,07E-01	1,26E+00	3,93E+00	7,10E-03	2,80E-04	1,92E+02	2,37E-03	2,80E-04	2,50E+01	1,56E+03	1,42E+01	3,89E-01
1,14E+02	1,41E+03	6,32E-01	6,37E-01	1,57E+00	5,55E+00	8,12E-03	2,80E-04	2,52E+02	2,71E-03	2,80E-04	3,30E+01	1,39E+03	1,48E+01	4,00E-01
1,19E+02	1,40E+03	6,00E-01	8,78E-01	1,25E+00	5,96E+00	8,52E-03	2,80E-04	2,77E+02	2,84E-03	2,80E-04	3,60E+01	1,39E+03	1,32E+01	3,92E-01
1,20E+02	1,30E+03	7,07E-01	7,35E-01	1,44E+00	5,03E+00	8,34E-03	2,80E-04	2,66E+02	2,78E-03	2,80E-04	3,50E+01	1,29E+03	1,46E+01	3,94E-01
1,26E+02	1,19E+03	8,52E-01	7,30E-01	1,46E+00	4,13E+00	8,40E-03	2,80E-04	2,70E+02	2,80E-03	2,80E-04	3,50E+01	1,17E+03	1,58E+01	3,98E-01
1,29E+02	1,19E+03	8,47E-01	7,44E-01	1,46E+00	4,23E+00	8,48E-03	2,80E-04	2,75E+02	2,83E-03	2,80E-04	3,60E+01	1,17E+03	1,55E+01	3,91E-01
1,37E+02	1,13E+03	1,01E+00	8,00E-01	1,37E+00	3,49E+00	8,49E-03	2,80E-04	2,76E+02	2,83E-03	2,80E-04	3,60E+01	1,12E+03	1,63E+01	3,97E-01
1,41E+02	1,05E+03	6,91E-01	9,25E-01	1,51E+00	5,11E+00	9,59E-03	2,80E-04	3,51E+02	3,20E-03	2,80E-04	4,60E+01	1,04E+03	1,56E+01	3,97E-01
1,43E+02	1,01E+03	7,39E-01	6,53E-01	2,04E+00	4,73E+00	9,37E-03	2,80E-04	3,36E+02	3,12E-03	2,80E-04	4,40E+01	9,91E+02	1,83E+01	4,00E-01
1,49E+02	9,75E+02	7,87E-01	9,51E-01	1,52E+00	4,49E+00	9,76E-03	2,80E-04	3,64E+02	3,25E-03	2,80E-04	4,70E+01	9,59E+02	1,63E+01	3,96E-01
1,57E+02	9,48E+02	7,82E-01	6,65E-01	2,16E+00	4,65E+00	9,73E-03	2,80E-04	3,61E+02	3,24E-03	2,80E-04	4,70E+01	9,29E+02	1,86E+01	3,85E-01
1,61E+02	9,18E+02	1,11E+00	5,81E-01	2,21E+00	3,18E+00	9,21E-03	2,80E-04	3,24E+02	3,07E-03	2,80E-04	4,20E+01	8,97E+02	2,12E+01	3,98E-01
1,66E+02	8,73E+02	8,95E-01	6,46E-01	2,29E+00	4,04E+00	9,89E-03	2,80E-04	3,73E+02	3,30E-03	2,80E-04	4,80E+01	8,53E+02	2,01E+01	3,87E-01
1,72E+02	8,63E+02	1,06E+00	8,20E-01	1,82E+00	3,42E+00	9,93E-03	2,80E-04	3,76E+02	3,31E-03	2,80E-04	4,90E+01	8,44E+02	1,87E+01	3,86E-01
1,73E+02	8,14E+02	9,87E-01	6,88E-01	2,27E+00	3,62E+00	1,02E-02	2,80E-04	3,94E+02	3,39E-03	2,80E-04	5,10E+01	7,93E+02	2,09E+01	3,92E-01
1,76E+02	7,97E+02	8,17E-01	9,12E-01	1,97E+00	4,39E+00	1,09E-02	2,80E-04	4,53E+02	3,63E-03	2,80E-04	5,90E+01	7,78E+02	1,87E+01	3,90E-01
1,82E+02	7,51E+02	9,34E-01	6,51E-01	2,64E+00	3,75E+00	1,06E-02	2,80E-04	4,33E+02	3,55E-03	2,80E-04	5,60E+01	7,28E+02	2,30E+01	3,99E-01
1,91E+02	7,35E+02	1,02E+00	9,61E-01	1,93E+00	3,47E+00	1,11E-02	2,80E-04	4,67E+02	3,69E-03	2,80E-04	6,10E+01	7,15E+02	2,00E+01	3,94E-01
1,99E+02	7,18E+02	1,04E+00	7,86E-01	2,36E+00	3,50E+00	1,11E-02	2,80E-04	4,68E+02	3,69E-03	2,80E-04	6,10E+01	6,96E+02	2,15E+01	3,83E-01
1,99E+02	6,93E+02	9,60E-01	6,25E-01	3,02E+00	3,66E+00	1,12E-02	2,80E-04	4,76E+02	3,72E-03	2,80E-04	6,20E+01	6,67E+02	2,52E+01	3,98E-01
2,04E+02	6,81E+02	1,03E+00	7,11E-01	2,72E+00	3,47E+00	1,13E-02	2,80E-04	4,88E+02	3,77E-03	2,80E-04	6,30E+01	6,58E+02	2,37E+01	3,91E-01
2,07E+02	6,53E+02	9,94E-01	9,17E-01	2,32E+00	3,55E+00	1,19E-02	2,80E-04	5,37E+02	3,95E-03	2,80E-04	7,00E+01	6,31E+02	2,21E+01	3,97E-01
2,14E+02	6,36E+02	8,41E-01	8,99E-01	2,59E+00	4,24E+00	1,24E-02	2,80E-04	5,88E+02	4,13E-03	2,80E-04	7,60E+01	6,14E+02	2,25E+01	3,92E-01
2,22E+02	6,13E+02	1,05E+00	7,33E-01	3,02E+00	3,38E+00	1,21E-02	2,80E-04	5,58E+02	4,03E-03	2,80E-04	7,20E+01	5,87E+02	2,59E+01	3,97E-01
2,28E+02	5,99E+02	9,78E-01	7,60E-01	3,09E+00	3,65E+00	1,24E-02	2,80E-04	5,92E+02	4,15E-03	2,80E-04	7,70E+01	5,73E+02	2,58E+01	3,93E-01
2,32E+02	5,85E+02	9,68E-01	9,49E-01	2,64E+00	3,67E+00	1,28E-02	2,80E-04	6,31E+02	4,28E-03	2,80E-04	8,20E+01	5,61E+02	2,37E+01	3,94E-01
2,35E+02	5,81E+02	1,02E+00	7,92E-01	3,07E+00	3,49E+00	1,27E-02	2,80E-04	6,13E+02	4,22E-03	2,80E-04	8,00E+01	5,55E+02	2,61E+01	3,94E-01
2,36E+02	5,71E+02	9,51E-01	1,03E+00	2,56E+00	3,71E+00	1,32E-02	2,80E-04	6,61E+02	4,38E-03	2,80E-04	8,60E+01	5,48E+02	2,36E+01	3,97E-01
2,40E+02	5,71E+02	1,06E+00	8,84E-01	2,83E+00	3,36E+00	1,29E-02	2,80E-04	6,31E+02	4,28E-03	2,80E-04	8,20E+01	5,46E+02	2,51E+01	3,93E-01
2,42E+02	5,57E+02	9,37E-01	9,89E-01	2,75E+00	3,77E+00	1,34E-02	2,80E-04	6,85E+02	4,46E-03	2,80E-04	8,90E+01	5,33E+02	2,44E+01	3,96E-01
2,49E+02	5,48E+02	8,21E-01	9,98E-01	2,93E+00	4,30E+00	1,39E-02	2,80E-04	7,38E+02	4,63E-03	2,80E-04	9,60E+01	5,24E+02	2,49E+01	3,97E-01
2,52E+02	5,45E+02	1,03E+00	7,71E-01	3,44E+00	3,43E+00	1,32E-02	2,80E-04	6,69E+02	4,41E-03	2,80E-04	8,70E+01	5,17E+02	2,83E+01	3,95E-01
2,58E+02	5,42E+02	9,64E-01	1,25E+00	2,34E+00	3,65E+00	1,39E-02	2,80E-04	7,37E+02	4,63E-03	2,80E-04	9,60E+01	5,19E+02	2,31E+01	3,98E-01
2,60E+02	5,30E+02	9,74E-01	9,44E-01	3,06E+00	3,68E+00	1,38E-02	2,80E-04	7,28E+02	4,60E-03	2,80E-04	9,40E+01	5,04E+02	2,60E+01	3,91E-01
2,63E+02	5,27E+02	1,07E+00	9,03E-01	3,13E+00	3,36E+00	1,37E-02	2,80E-04	7,12E+02	4,55E-03	2,80E-04	9,20E+01	5,00E+02	2,68E+01	3,91E-01
2,66E+02	5,23E+02	9,39E-01	8,84E-01	3,37E+00	3,83E+00	1,40E-02	2,80E-04	7,51E+02	4,67E-03	2,80E-04	9,80E+01	4,95E+02	2,73E+01	3,90E-01
2,70E+02	5,14E+02	1,17E+00	9,01E-01	3,17E+00	2,99E+00	1,37E-02	2,80E-04	7,21E+02	4,58E-03	2,80E-04	9,40E+01	4,86E+02	2,83E+01	4,00E-01
2,71E+02	5,04E+02	9,49E-01	1,10E+00	2,87E+00	3,69E+00	1,45E-02	2,80E-04	8,00E+02	4,82E-03	2,80E-04	1,04E+02	4,78E+02	2,58E+01	4,00E-01
2,76E+02	5,00E+02	1,05E+00	9,68E-01	3,19E+00	3,38E+00	1,43E-02	2,80E-04	7,79E+02	4,76E-03	2,80E-04	1,01E+02	4,72E+02	2,76E+01	3,96E-01
2,79E+02	4,96E+02	9,86E-01	8,84E-01	3,57E+00	3,60E+00	1,44E-02	2,80E-04	7,95E+02	4,81E-03	2,80E-04	1,03E+02	4,67E+02	2,91E+01	3,95E-01
2,81E+02	4,95E+02	1,05E+00	8,25E-01	3,74E+00	3,38E+00	1,43E-02	2,80E-04	7,79E+02	4,76E-03	2,80E-04	1,01E+02	4,65E+02	3,04E+01	3,96E-01
2,85E+02	4,90E+02	1,08E+00	9,97E-01	3,19E+00	3,27E+00	1,45E-02	2,80E-04	8,02E+02	4,83E-03	2,80E-04	1,04E+02	4,62E+02	2,78E+01	3,95E-01
2,85E+02	4,90E+02	1,07E+00	8,19E-01	3,83E+00	3,30E+00	1,44E-02	2,80E-04	7,90E+02	4,79E-03	2,80E-04	1,03E+02	4,59E+02	3,11E+01	3,97E-01
2,86E+02	4,86E+02	1,06E+00	1,02E+00	3,18E+00										

Table A.7 – continued from previous page

Volume (cm ³)	Loss(W)	a	b	h	d	Primary Winding			Secondary Winding			Copper Loss	core Loss	Magnetic Flux
						bundle Diameter	Wire Di- ameter	number of Strands	bundle Diameter	Strand Diameter	No. Of Strands			
3,16E+02	4,49E+02	1,07E+00	1,05E+00	3,54E+00	3,29E+00	1,57E-02	2,80E-04	9,36E+02	5,22E-03	2,80E-04	1,22E+02	4,19E+02	3,02E+01	3,98E-01
3,19E+02	4,49E+02	1,04E+00	1,21E+00	3,14E+00	3,38E+00	1,58E-02	2,80E-04	9,59E+02	5,28E-03	2,80E-04	1,24E+02	4,21E+02	2,81E+01	3,99E-01
3,19E+02	4,47E+02	1,01E+00	1,08E+00	3,55E+00	3,52E+00	1,59E-02	2,80E-04	9,65E+02	5,30E-03	2,80E-04	1,25E+02	4,18E+02	2,97E+01	3,96E-01
3,23E+02	4,43E+02	1,06E+00	1,12E+00	3,44E+00	3,32E+00	1,59E-02	2,80E-04	9,68E+02	5,31E-03	2,80E-04	1,26E+02	4,14E+02	2,97E+01	3,99E-01
3,25E+02	4,42E+02	1,00E+00	1,13E+00	3,47E+00	3,51E+00	1,61E-02	2,80E-04	9,92E+02	5,37E-03	2,80E-04	1,29E+02	4,13E+02	2,95E+01	3,97E-01
3,27E+02	4,39E+02	1,09E+00	1,06E+00	3,65E+00	3,23E+00	1,59E-02	2,80E-04	9,72E+02	5,32E-03	2,80E-04	1,26E+02	4,08E+02	3,10E+01	3,99E-01
3,33E+02	4,38E+02	9,72E-01	1,09E+00	3,73E+00	3,66E+00	1,64E-02	2,80E-04	1,02E+03	5,45E-03	2,80E-04	1,33E+02	4,08E+02	3,05E+01	3,94E-01
3,33E+02	4,36E+02	1,07E+00	9,29E-01	4,22E+00	3,28E+00	1,61E-02	2,80E-04	9,88E+02	5,36E-03	2,80E-04	1,28E+02	4,02E+02	3,39E+01	4,00E-01
3,33E+02	4,35E+02	1,02E+00	1,14E+00	3,55E+00	3,44E+00	1,63E-02	2,80E-04	1,02E+03	5,44E-03	2,80E-04	1,32E+02	4,05E+02	3,01E+01	3,97E-01
3,33E+02	4,33E+02	1,07E+00	1,12E+00	3,55E+00	3,29E+00	1,62E-02	2,80E-04	1,01E+03	5,41E-03	2,80E-04	1,31E+02	4,03E+02	3,05E+01	3,99E-01
3,39E+02	4,29E+02	1,06E+00	1,05E+00	3,89E+00	3,30E+00	1,64E-02	2,80E-04	1,03E+03	5,46E-03	2,80E-04	1,33E+02	3,97E+02	3,22E+01	3,99E-01
3,40E+02	4,28E+02	1,08E+00	1,15E+00	3,55E+00	3,25E+00	1,64E-02	2,80E-04	1,03E+03	5,48E-03	2,80E-04	1,34E+02	3,97E+02	3,07E+01	4,00E-01
3,44E+02	4,27E+02	9,96E-01	1,25E+00	3,40E+00	3,54E+00	1,68E-02	2,80E-04	1,07E+03	5,58E-03	2,80E-04	1,39E+02	3,98E+02	2,94E+01	3,97E-01
3,47E+02	4,26E+02	9,99E-01	1,11E+00	3,85E+00	3,55E+00	1,68E-02	2,80E-04	1,07E+03	5,59E-03	2,80E-04	1,39E+02	3,94E+02	3,14E+01	3,94E-01
3,48E+02	4,24E+02	1,06E+00	1,11E+00	3,78E+00	3,35E+00	1,66E-02	2,80E-04	1,06E+03	5,55E-03	2,80E-04	1,37E+02	3,93E+02	3,15E+01	3,96E-01
3,49E+02	4,23E+02	1,01E+00	1,13E+00	3,81E+00	3,52E+00	1,68E-02	2,80E-04	1,08E+03	5,61E-03	2,80E-04	1,40E+02	3,92E+02	3,14E+01	3,96E-01
3,50E+02	4,21E+02	1,05E+00	1,07E+00	3,99E+00	3,35E+00	1,68E-02	2,80E-04	1,08E+03	5,59E-03	2,80E-04	1,40E+02	3,88E+02	3,28E+01	3,99E-01
3,53E+02	4,19E+02	1,03E+00	1,20E+00	3,65E+00	3,43E+00	1,70E-02	2,80E-04	1,10E+03	5,65E-03	2,80E-04	1,43E+02	3,88E+02	3,09E+01	3,98E-01
3,55E+02	4,17E+02	1,04E+00	1,17E+00	3,73E+00	3,38E+00	1,70E-02	2,80E-04	1,10E+03	5,67E-03	2,80E-04	1,43E+02	3,86E+02	3,15E+01	3,98E-01
3,58E+02	4,17E+02	1,11E+00	1,14E+00	3,79E+00	3,18E+00	1,69E-02	2,80E-04	1,09E+03	5,62E-03	2,80E-04	1,41E+02	3,85E+02	3,21E+01	3,97E-01
3,61E+02	4,16E+02	1,09E+00	1,16E+00	3,79E+00	3,26E+00	1,70E-02	2,80E-04	1,10E+03	5,66E-03	2,80E-04	1,43E+02	3,84E+02	3,18E+01	3,96E-01
3,61E+02	4,15E+02	9,66E-01	1,11E+00	4,09E+00	3,64E+00	1,73E-02	2,80E-04	1,15E+03	5,78E-03	2,80E-04	1,49E+02	3,82E+02	3,30E+01	3,98E-01
3,64E+02	4,14E+02	1,05E+00	1,06E+00	4,20E+00	3,35E+00	1,71E-02	2,80E-04	1,12E+03	5,71E-03	2,80E-04	1,46E+02	3,80E+02	3,38E+01	3,97E-01
3,65E+02	4,11E+02	9,81E-01	1,27E+00	3,64E+00	3,57E+00	1,75E-02	2,80E-04	1,17E+03	5,82E-03	2,80E-04	1,51E+02	3,80E+02	3,10E+01	3,99E-01
3,71E+02	4,09E+02	1,16E+00	1,13E+00	3,92E+00	3,04E+00	1,71E-02	2,80E-04	1,12E+03	5,71E-03	2,80E-04	1,45E+02	3,76E+02	3,32E+01	3,99E-01
3,73E+02	4,09E+02	9,63E-01	1,30E+00	3,65E+00	3,66E+00	1,77E-02	2,80E-04	1,20E+03	5,90E-03	2,80E-04	1,55E+02	3,78E+02	3,09E+01	3,97E-01
3,74E+02	4,08E+02	1,02E+00	1,15E+00	4,06E+00	3,49E+00	1,76E-02	2,80E-04	1,18E+03	5,85E-03	2,80E-04	1,53E+02	3,75E+02	3,29E+01	3,95E-01
3,74E+02	4,07E+02	1,00E+00	1,31E+00	3,60E+00	3,50E+00	1,77E-02	2,80E-04	1,19E+03	5,88E-03	2,80E-04	1,55E+02	3,76E+02	3,09E+01	3,99E-01
3,77E+02	4,04E+02	9,70E-01	1,29E+00	3,74E+00	3,61E+00	1,79E-02	2,80E-04	1,22E+03	5,95E-03	2,80E-04	1,58E+02	3,73E+02	3,16E+01	4,00E-01
3,81E+02	4,03E+02	1,02E+00	1,27E+00	3,78E+00	3,47E+00	1,78E-02	2,80E-04	1,21E+03	5,94E-03	2,80E-04	1,57E+02	3,71E+02	3,19E+01	3,98E-01
3,83E+02	4,01E+02	1,08E+00	1,18E+00	4,02E+00	3,24E+00	1,77E-02	2,80E-04	1,20E+03	5,91E-03	2,80E-04	1,56E+02	3,67E+02	3,35E+01	3,99E-01
3,84E+02	4,00E+02	1,03E+00	1,24E+00	3,91E+00	3,40E+00	1,79E-02	2,80E-04	1,22E+03	5,97E-03	2,80E-04	1,59E+02	3,67E+02	3,28E+01	3,99E-01
3,85E+02	3,99E+02	1,02E+00	1,26E+00	3,89E+00	3,44E+00	1,80E-02	2,80E-04	1,23E+03	5,99E-03	2,80E-04	1,60E+02	3,67E+02	3,26E+01	4,00E-01
3,86E+02	3,99E+02	1,04E+00	1,21E+00	4,02E+00	3,40E+00	1,79E-02	2,80E-04	1,23E+03	5,98E-03	2,80E-04	1,59E+02	3,66E+02	3,33E+01	3,98E-01
3,88E+02	3,99E+02	1,11E+00	1,21E+00	3,95E+00	3,16E+00	1,78E-02	2,80E-04	1,21E+03	5,92E-03	2,80E-04	1,57E+02	3,66E+02	3,34E+01	3,99E-01
3,90E+02	3,98E+02	1,12E+00	1,22E+00	3,96E+00	3,13E+00	1,78E-02	2,80E-04	1,22E+03	5,94E-03	2,80E-04	1,58E+02	3,64E+02	3,35E+01	3,99E-01
3,91E+02	3,97E+02	1,06E+00	1,22E+00	4,03E+00	3,30E+00	1,80E-02	2,80E-04	1,24E+03	6,00E-03	2,80E-04	1,61E+02	3,63E+02	3,35E+01	3,99E-01
3,95E+02	3,96E+02	1,03E+00	1,30E+00	3,84E+00	3,42E+00	1,81E-02	2,80E-04	1,26E+03	6,05E-03	2,80E-04	1,63E+02	3,64E+02	3,23E+01	3,96E-01
3,97E+02	3,96E+02	1,13E+00	1,19E+00	4,09E+00	3,13E+00	1,79E-02	2,80E-04	1,23E+03	5,98E-03	2,80E-04	1,60E+02	3,62E+02	3,40E+01	3,96E-01
3,98E+02	3,96E+02	1,00E+00	1,26E+00	4,03E+00	3,53E+00	1,83E-02	2,80E-04	1,28E+03	6,11E-03	2,80E-04	1,67E+02	3,63E+02	3,31E+01	3,97E-01
3,98E+02	3,95E+02	1,08E+00	1,27E+00	3,90E+00	3,28E+00	1,81E-02	2,80E-04	1,25E+03	6,03E-03	2,80E-04	1,62E+02	3,63E+02	3,27E+01	3,95E-01
3,99E+02	3,93E+02	1,06E+00	1,16E+00	4,33E+00	3,32E+00	1,82E-02	2,80E-04	1,27E+03	6,08E-03	2,80E-04	1,65E+02	3,58E+02	3,52E+01	3,99E-01
4,01E+02	3,92E+02	1,05E+00	1,22E+00	4,15E+00	3,34E+00	1,83E-02	2,80E-04	1,28E+03	6,10E-03	2,80E-04	1,66E+02	3,58E+02	3,42E+01	3,98E-01
4,05E+02	3,92E+02	1,04E+00	1,28E+00	4,03E+00	3,39E+00	1,84E-02	2,80E-04	1,30E+03	6,14E-03	2,80E-04	1,69E+02	3,58E+02	3,35E+01	3,97E-01
4,07E+02	3,90E+02	1,07E+00	1,24E+00	4,14E+00	3,28E+00	1,84E-02	2,80E-04	1,30E+03	6,14E-03	2,80E-04	1,69E+02	3,56E+02	3,43E+01	3,99E-01
4,09E+02	3,89E+02	1,10E+00	1,30E+00	3,95E+00	3,19E+00	1,84E-02	2,80E-04	1,29E+03	6,14E-03	2,80E-04	1,68E+02	3,55E+02	3,36E+01	4,00E-01
4,12E+02	3,88E+02	1,09E+00	1,27E+00	4,06E+00	3,23E+00	1,85E-02	2,80E-04	1,30E+03	6,16E-03	2,80E-04	1,69E+02	3,55E+02	3,39E+01	3,97E-01
4,12E+02	3,88E+02	1,09E+00	1,19E+00	4,37E+00	3,22E+00	1,85E-02	2,80E-04	1,31E+03	6,17E-03	2,80E-04	1,70E+02	3,53E+02	3,56E+01	3,98E-01
4,12E+02	3,88E+02	1,07E+00	1,15E+00	4,56E+00	3,28E+00	1,86E-02	2,80E-04	1,32E+03	6,20E-03	2,80E-04	1,71E+02	3,52E+02	3,66E+01	3,99E-01
4,14E+02	3,88E+02	9,72E-01	1,34E+00	4,03E+00	3,61E+00	1,89E-02	2,80E-04	1,36E+03	6,30E-03	2,80E-04	1,77E+02	3,54E+02	3,34E+01	3,99E-01
4,17E+02	3,88E+02	1,14E+00	1,41E+00	3,64E+00	3,07E+00	1,84E-02	2,80E-04	1,30E+03	6,14E-03	2,80E-04	1,68E+02	3,55E+02	3,24E+01	4,00E-01
4,18E+02	3,85E+02	1,12E+00	1,29E+00	4,06E+00	3,12E+00	1,86E-02	2,80E-04	1,32E+03	6,19E-03	2,80E-04	1,71E+02	3,51E+02	3,43E+01	3,99E-01
4,21E+02	3,85E+02	1,02E+00	1,27E+00	4,27E+00	3,46E+00	1,90E-02	2,80E-04	1,37E+03	6,32E-03	2,80E-04	1,78E+02	3,50E+02	3,47E+01	3,97E-01
4,22E+02	3,83E+02	1,07E+00	1,29E+00	4,18E+00	3,29E+00	1,89E-02	2,80E-04	1,36E+03	6,30E-03	2,80E-04	1,77E+02	3,48E+02	3,47E+01	3,99E-01
4,23E+02	3,83E+02	1,12E+00	1,25E+00	4,27E+00	3,13E+00	1,88E-02	2,80E-04	1,35E+03	6,26E-03	2,80E-04	1,75E+02	3,47E+02	3,55E+01	4,00E-01
4,28E+02	3,82E+02	1,07E+00	1,34E+00	4,09E+00	3,30E+00	1,90E-02	2,80E-04	1,38E+03	6,33E-03	2,80E-04	1,79E+02	3,48E+02	3,42E+01	3,98E-01
4,30E+02	3,81E+02	1,06E+00	1,33E+00	4,14E+00	3,34E+00	1,91E-02	2,80E-04	1,39E+03	6,36E-03	2,80E-04	1,80E+02	3,47E+02	3,43E+01	3,97E-01
4,32E+02	3,81E+02	1,12E+00	1,30E+00	4,17E+00	3,14E+00	1,89E-02	2,80E-04	1,37E+03	6,32E-03	2,80E-04	1,78E+02	3,46E+02	3,48E+01	3,97E-01
4,33E+02	3,80E+02	1,01E+00	1,34E+00	4,22E+00	3,47E+00	1,93E-02	2,80E-04	1,43E+03	6,44E-03	2,80E-04	1,85E+02	3,45E+02	3,48E+01	3,99E-01
4,34E+02	3,79E+02	1,12E+00	1,31E+00	4,18E+00	3,14E+00	1,91E-02	2,80E-04	1,39E+03	6,35E-03					

Table A.7 – continued from previous page

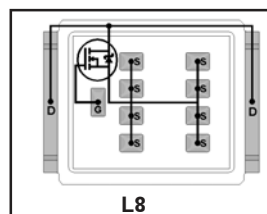
Volume (cm ³)	Loss(W)	a	b	h	d	Primary Winding			Secondary Winding			Copper Loss	core Loss	Magnetic Flux
						bundle Diameter	Wire Di- ameter	number of Strands	bundle Diameter	Strand Diameter	No. Of Strands			
4.79E+02	3.67E+02	1.05E+00	1.41E+00	4.50E+00	3.32E+00	2.04E-02	2.80E-04	1.59E+03	6.81E-03	2.80E-04	2.07E+02	3.30E+02	3.69E+01	4.00E-01
4.79E+02	3.67E+02	1.10E+00	1.48E+00	4.17E+00	3.20E+00	2.02E-02	2.80E-04	1.56E+03	6.73E-03	2.80E-04	2.02E+02	3.31E+02	3.52E+01	3.97E-01
4.79E+02	3.66E+02	1.06E+00	1.54E+00	4.08E+00	3.32E+00	2.03E-02	2.80E-04	1.58E+03	6.78E-03	2.80E-04	2.05E+02	3.32E+02	3.48E+01	3.99E-01
4.79E+02	3.66E+02	1.12E+00	1.53E+00	4.01E+00	3.13E+00	2.01E-02	2.80E-04	1.55E+03	6.71E-03	2.80E-04	2.01E+02	3.31E+02	3.47E+01	3.99E-01
4.80E+02	3.66E+02	1.11E+00	1.40E+00	4.46E+00	3.17E+00	2.03E-02	2.80E-04	1.57E+03	6.76E-03	2.80E-04	2.04E+02	3.29E+02	3.69E+01	3.99E-01
4.82E+02	3.66E+02	1.15E+00	1.45E+00	4.25E+00	3.04E+00	2.02E-02	2.80E-04	1.55E+03	6.72E-03	2.80E-04	2.02E+02	3.30E+02	3.61E+01	4.00E-01
4.83E+02	3.66E+02	1.07E+00	1.58E+00	3.98E+00	3.29E+00	2.04E-02	2.80E-04	1.58E+03	6.78E-03	2.80E-04	2.05E+02	3.31E+02	3.43E+01	3.98E-01
4.86E+02	3.65E+02	1.20E+00	1.44E+00	4.25E+00	2.92E+00	2.01E-02	2.80E-04	1.54E+03	6.70E-03	2.80E-04	2.00E+02	3.29E+02	3.63E+01	3.99E-01
4.86E+02	3.65E+02	1.10E+00	1.49E+00	4.23E+00	3.20E+00	2.04E-02	2.80E-04	1.59E+03	6.80E-03	2.80E-04	2.07E+02	3.29E+02	3.57E+01	3.98E-01
4.90E+02	3.64E+02	1.15E+00	1.44E+00	4.39E+00	3.05E+00	2.04E-02	2.80E-04	1.59E+03	6.80E-03	2.80E-04	2.07E+02	3.27E+02	3.69E+01	3.99E-01
4.92E+02	3.63E+02	1.14E+00	1.49E+00	4.22E+00	3.07E+00	2.04E-02	2.80E-04	1.59E+03	6.80E-03	2.80E-04	2.06E+02	3.27E+02	3.59E+01	3.98E-01
4.93E+02	3.63E+02	1.16E+00	1.50E+00	4.20E+00	3.02E+00	2.04E-02	2.80E-04	1.59E+03	6.80E-03	2.80E-04	2.06E+02	3.27E+02	3.60E+01	4.00E-01
4.95E+02	3.63E+02	1.07E+00	1.51E+00	4.33E+00	3.27E+00	2.08E-02	2.80E-04	1.65E+03	6.92E-03	2.80E-04	2.14E+02	3.26E+02	3.63E+01	4.00E-01
4.99E+02	3.62E+02	1.07E+00	1.56E+00	4.17E+00	3.29E+00	2.07E-02	2.80E-04	1.65E+03	6.92E-03	2.80E-04	2.13E+02	3.27E+02	3.53E+01	3.97E-01
4.99E+02	3.61E+02	1.12E+00	1.57E+00	4.11E+00	3.11E+00	2.06E-02	2.80E-04	1.63E+03	6.87E-03	2.80E-04	2.11E+02	3.26E+02	3.55E+01	4.00E-01
5.04E+02	3.61E+02	1.15E+00	1.59E+00	4.04E+00	3.07E+00	2.06E-02	2.80E-04	1.62E+03	6.86E-03	2.80E-04	2.10E+02	3.26E+02	3.51E+01	3.98E-01
5.06E+02	3.60E+02	1.11E+00	1.55E+00	4.26E+00	3.17E+00	2.08E-02	2.80E-04	1.66E+03	6.95E-03	2.80E-04	2.15E+02	3.24E+02	3.61E+01	3.98E-01
5.11E+02	3.59E+02	1.16E+00	1.52E+00	4.34E+00	3.02E+00	2.08E-02	2.80E-04	1.66E+03	6.94E-03	2.80E-04	2.15E+02	3.22E+02	3.68E+01	3.99E-01
5.14E+02	3.59E+02	1.09E+00	1.54E+00	4.40E+00	3.22E+00	2.11E-02	2.80E-04	1.71E+03	7.05E-03	2.80E-04	2.22E+02	3.22E+02	3.69E+01	3.99E-01
5.15E+02	3.59E+02	1.08E+00	1.64E+00	4.12E+00	3.24E+00	2.11E-02	2.80E-04	1.70E+03	7.03E-03	2.80E-04	2.21E+02	3.23E+02	3.55E+01	4.00E-01
5.18E+02	3.58E+02	1.13E+00	1.61E+00	4.16E+00	3.13E+00	2.10E-02	2.80E-04	1.68E+03	7.00E-03	2.80E-04	2.18E+02	3.23E+02	3.56E+01	3.97E-01
5.19E+02	3.58E+02	1.10E+00	1.51E+00	4.54E+00	3.18E+00	2.13E-02	2.80E-04	1.73E+03	7.09E-03	2.80E-04	2.24E+02	3.20E+02	3.77E+01	3.99E-01
5.19E+02	3.57E+02	1.10E+00	1.57E+00	4.32E+00	3.18E+00	2.12E-02	2.80E-04	1.71E+03	7.06E-03	2.80E-04	2.22E+02	3.21E+02	3.65E+01	3.98E-01
5.20E+02	3.57E+02	1.12E+00	1.56E+00	4.37E+00	3.14E+00	2.12E-02	2.80E-04	1.71E+03	7.06E-03	2.80E-04	2.22E+02	3.21E+02	3.68E+01	3.98E-01
5.22E+02	3.57E+02	1.13E+00	1.57E+00	4.31E+00	3.11E+00	2.11E-02	2.80E-04	1.71E+03	7.04E-03	2.80E-04	2.21E+02	3.21E+02	3.65E+01	3.98E-01
5.22E+02	3.57E+02	1.15E+00	1.56E+00	4.32E+00	3.05E+00	2.11E-02	2.80E-04	1.70E+03	7.04E-03	2.80E-04	2.21E+02	3.20E+02	3.69E+01	3.99E-01
5.23E+02	3.57E+02	1.10E+00	1.55E+00	4.46E+00	3.18E+00	2.13E-02	2.80E-04	1.74E+03	7.11E-03	2.80E-04	2.26E+02	3.20E+02	3.74E+01	4.00E-01
5.29E+02	3.56E+02	1.11E+00	1.66E+00	4.16E+00	3.17E+00	2.13E-02	2.80E-04	1.74E+03	7.11E-03	2.80E-04	2.26E+02	3.20E+02	3.59E+01	3.99E-01
5.31E+02	3.56E+02	1.10E+00	1.64E+00	4.24E+00	3.18E+00	2.14E-02	2.80E-04	1.76E+03	7.14E-03	2.80E-04	2.28E+02	3.19E+02	3.63E+01	4.00E-01
5.33E+02	3.55E+02	1.12E+00	1.62E+00	4.30E+00	3.14E+00	2.14E-02	2.80E-04	1.75E+03	7.14E-03	2.80E-04	2.27E+02	3.19E+02	3.65E+01	3.98E-01
5.34E+02	3.55E+02	1.10E+00	1.54E+00	4.59E+00	3.18E+00	2.16E-02	2.80E-04	1.78E+03	7.20E-03	2.80E-04	2.31E+02	3.17E+02	3.80E+01	3.99E-01
5.37E+02	3.55E+02	1.07E+00	1.65E+00	4.31E+00	3.30E+00	2.16E-02	2.80E-04	1.79E+03	7.22E-03	2.80E-04	2.32E+02	3.19E+02	3.64E+01	3.97E-01
5.39E+02	3.55E+02	1.04E+00	1.68E+00	4.28E+00	3.36E+00	2.18E-02	2.80E-04	1.81E+03	7.26E-03	2.80E-04	2.35E+02	3.18E+02	3.63E+01	4.00E-01
5.43E+02	3.54E+02	1.16E+00	1.53E+00	4.61E+00	3.02E+00	2.16E-02	2.80E-04	1.78E+03	7.20E-03	2.80E-04	2.31E+02	3.16E+02	3.84E+01	3.98E-01
5.44E+02	3.54E+02	1.15E+00	1.67E+00	4.19E+00	3.05E+00	2.15E-02	2.80E-04	1.77E+03	7.17E-03	2.80E-04	2.30E+02	3.18E+02	3.64E+01	3.99E-01
5.44E+02	3.53E+02	1.15E+00	1.65E+00	4.28E+00	3.04E+00	2.16E-02	2.80E-04	1.78E+03	7.18E-03	2.80E-04	2.30E+02	3.17E+02	3.68E+01	3.99E-01
5.49E+02	3.53E+02	1.07E+00	1.65E+00	4.43E+00	3.28E+00	2.20E-02	2.80E-04	1.84E+03	7.32E-03	2.80E-04	2.39E+02	3.16E+02	3.72E+01	3.98E-01
5.50E+02	3.53E+02	1.14E+00	1.66E+00	4.30E+00	3.10E+00	2.17E-02	2.80E-04	1.80E+03	7.23E-03	2.80E-04	2.33E+02	3.17E+02	3.66E+01	3.96E-01
5.51E+02	3.53E+02	1.17E+00	1.65E+00	4.30E+00	3.03E+00	2.16E-02	2.80E-04	1.79E+03	7.22E-03	2.80E-04	2.32E+02	3.16E+02	3.68E+01	3.96E-01
5.52E+02	3.53E+02	1.09E+00	1.66E+00	4.39E+00	3.22E+00	2.19E-02	2.80E-04	1.84E+03	7.31E-03	2.80E-04	2.38E+02	3.16E+02	3.70E+01	3.97E-01
5.53E+02	3.52E+02	1.15E+00	1.60E+00	4.51E+00	3.05E+00	2.18E-02	2.80E-04	1.82E+03	7.28E-03	2.80E-04	2.36E+02	3.14E+02	3.80E+01	3.98E-01
5.54E+02	3.52E+02	1.14E+00	1.66E+00	4.33E+00	3.08E+00	2.18E-02	2.80E-04	1.82E+03	7.27E-03	2.80E-04	2.36E+02	3.15E+02	3.78E+01	3.98E-01
5.55E+02	3.52E+02	1.12E+00	1.72E+00	4.20E+00	3.14E+00	2.18E-02	2.80E-04	1.82E+03	7.28E-03	2.80E-04	2.36E+02	3.16E+02	3.62E+01	3.97E-01
5.56E+02	3.52E+02	1.11E+00	1.76E+00	4.13E+00	3.16E+00	2.19E-02	2.80E-04	1.83E+03	7.29E-03	2.80E-04	2.37E+02	3.16E+02	3.61E+01	4.00E-01
5.58E+02	3.51E+02	1.16E+00	1.66E+00	4.39E+00	3.03E+00	2.19E-02	2.80E-04	1.84E+03	7.30E-03	2.80E-04	2.38E+02	3.14E+02	3.76E+01	4.00E-01
5.65E+02	3.51E+02	1.12E+00	1.73E+00	4.27E+00	3.13E+00	2.21E-02	2.80E-04	1.87E+03	7.37E-03	2.80E-04	2.43E+02	3.14E+02	3.69E+01	4.00E-01
5.69E+02	3.50E+02	1.13E+00	1.74E+00	4.28E+00	3.12E+00	2.21E-02	2.80E-04	1.87E+03	7.38E-03	2.80E-04	2.43E+02	3.13E+02	3.69E+01	3.98E-01
5.69E+02	3.50E+02	1.12E+00	1.69E+00	4.42E+00	3.14E+00	2.22E-02	2.80E-04	1.89E+03	7.41E-03	2.80E-04	2.45E+02	3.13E+02	3.76E+01	3.99E-01
5.70E+02	3.50E+02	1.12E+00	1.76E+00	4.26E+00	3.14E+00	2.22E-02	2.80E-04	1.89E+03	7.40E-03	2.80E-04	2.45E+02	3.13E+02	3.68E+01	3.99E-01
5.75E+02	3.50E+02	1.14E+00	1.82E+00	4.08E+00	3.10E+00	2.21E-02	2.80E-04	1.87E+03	7.37E-03	2.80E-04	2.42E+02	3.14E+02	3.59E+01	3.97E-01
5.76E+02	3.49E+02	1.12E+00	1.81E+00	4.14E+00	3.14E+00	2.22E-02	2.80E-04	1.89E+03	7.42E-03	2.80E-04	2.45E+02	3.13E+02	3.62E+01	3.99E-01
5.78E+02	3.49E+02	1.10E+00	1.75E+00	4.36E+00	3.20E+00	2.25E-02	2.80E-04	1.93E+03	7.49E-03	2.80E-04	2.50E+02	3.12E+02	3.73E+01	3.99E-01
5.85E+02	3.48E+02	1.16E+00	1.82E+00	4.16E+00	3.03E+00	2.23E-02	2.80E-04	1.91E+03	7.44E-03	2.80E-04	2.47E+02	3.11E+02	3.67E+01	4.00E-01
5.90E+02	3.47E+02	1.14E+00	1.85E+00	4.13E+00	3.08E+00	2.25E-02	2.80E-04	1.93E+03	7.49E-03	2.80E-04	2.50E+02	3.11E+02	3.65E+01	4.00E-01
5.90E+02	3.47E+02	1.16E+00	1.74E+00	4.42E+00	3.03E+00	2.26E-02	2.80E-04	1.94E+03	7.52E-03	2.80E-04	2.52E+02	3.09E+02	3.80E+01	4.00E-01
5.95E+02	3.47E+02	1.16E+00	1.78E+00	4.36E+00	3.04E+00	2.26E-02	2.80E-04	1.95E+03	7.54E-03	2.80E-04	2.53E+02	3.09E+02	3.76E+01	3.98E-01
5.98E+02	3.47E+02	1.12E+00	1.89E+00	4.13E+00	3.14E+00	2.27E-02	2.80E-04	1.97E+03	7.56E-03	2.80E-04	2.55E+02	3.10E+02	3.65E+01	4.00E-01
5.99E+02	3.47E+02	1.10E+00	1.83E+00	4.33E+00	3.20E+00	2.29E-02	2.80E-04	2.00E+03	7.62E-03	2.80E-04	2.59E+02	3.09E+02	3.74E+01	3.99E-01
6.04E+02	3.46E+02	1.16E+00	1.85E+00	4.21E+00	3.04E+00	2.27E-02	2.80E-04	1.97E+03	7.56E-03	2.80E-04	2.55E+02	3.09E+02	3.69E+01	3.97E-01
6.06E+02	3.46E+02	1.17E+00	1.75E+00	4.52E+00	2.99E+00	2.29E-02	2.80E-04	2.00E+03	7.62E-03</					

Table A.7 – continued from previous page															
Volume (cm ³)	Loss(W)	a	b	h	d	Primary Winding			Secondary Winding			Copper Loss	core Loss	Magnetic Flux	
						bundle Diameter	Wire Di- ameter	number of Strands	bundle Diameter	Strand Diameter	No. Of Strands				
6,96E+02	3,40E+02	1,16E+00	2,02E+00	4,50E+00	3,01E+00	2,45E-02	2,80E-04	2,30E+03	8,17E-03	2,80E-04	2,98E+02	3,00E+02	3,93E+01	3,99E-01	
6,97E+02	3,40E+02	1,17E+00	1,99E+00	4,61E+00	2,99E+00	2,46E-02	2,80E-04	2,31E+03	8,19E-03	2,80E-04	2,99E+02	3,00E+02	3,98E+01	3,99E-01	
7,00E+02	3,39E+02	1,16E+00	2,08E+00	4,37E+00	3,02E+00	2,45E-02	2,80E-04	2,29E+03	8,16E-03	2,80E-04	2,97E+02	3,01E+02	3,86E+01	3,98E-01	
7,07E+02	3,39E+02	1,20E+00	2,09E+00	4,33E+00	2,91E+00	2,44E-02	2,80E-04	2,28E+03	8,15E-03	2,80E-04	2,96E+02	3,00E+02	3,88E+01	3,99E-01	
7,10E+02	3,39E+02	1,19E+00	2,12E+00	4,28E+00	2,94E+00	2,45E-02	2,80E-04	2,29E+03	8,16E-03	2,80E-04	2,97E+02	3,00E+02	3,85E+01	3,99E-01	
7,19E+02	3,39E+02	1,16E+00	2,15E+00	4,32E+00	3,03E+00	2,48E-02	2,80E-04	2,35E+03	8,26E-03	2,80E-04	3,05E+02	3,00E+02	3,86E+01	3,99E-01	
7,25E+02	3,38E+02	1,18E+00	2,17E+00	4,29E+00	2,96E+00	2,48E-02	2,80E-04	2,35E+03	8,26E-03	2,80E-04	3,05E+02	3,00E+02	3,87E+01	4,00E-01	
7,30E+02	3,38E+02	1,17E+00	2,21E+00	4,24E+00	3,00E+00	2,49E-02	2,80E-04	2,36E+03	8,29E-03	2,80E-04	3,07E+02	3,00E+02	3,84E+01	4,00E-01	
7,35E+02	3,38E+02	1,22E+00	2,20E+00	4,22E+00	2,90E+00	2,47E-02	2,80E-04	2,34E+03	8,25E-03	2,80E-04	3,03E+02	3,00E+02	3,82E+01	3,96E-01	
7,38E+02	3,38E+02	1,14E+00	2,22E+00	4,31E+00	3,07E+00	2,51E-02	2,80E-04	2,41E+03	8,38E-03	2,80E-04	3,13E+02	2,99E+02	3,86E+01	3,99E-01	
7,40E+02	3,38E+02	1,21E+00	2,19E+00	4,32E+00	2,90E+00	2,50E-02	2,80E-04	2,38E+03	8,32E-03	2,80E-04	3,09E+02	2,99E+02	3,90E+01	3,99E-01	
7,48E+02	3,37E+02	1,19E+00	2,23E+00	4,28E+00	2,96E+00	2,51E-02	2,80E-04	2,41E+03	8,36E-03	2,80E-04	3,12E+02	2,99E+02	3,86E+01	3,98E-01	
7,52E+02	3,37E+02	1,14E+00	2,27E+00	4,28E+00	3,07E+00	2,53E-02	2,80E-04	2,45E+03	8,45E-03	2,80E-04	3,18E+02	2,98E+02	3,87E+01	4,00E-01	
7,56E+02	3,37E+02	1,16E+00	2,23E+00	4,40E+00	3,02E+00	2,54E-02	2,80E-04	2,47E+03	8,47E-03	2,80E-04	3,20E+02	2,98E+02	3,93E+01	3,99E-01	
7,65E+02	3,37E+02	1,22E+00	2,27E+00	4,25E+00	2,87E+00	2,52E-02	2,80E-04	2,43E+03	8,41E-03	2,80E-04	3,16E+02	2,98E+02	3,89E+01	3,99E-01	
7,86E+02	3,37E+02	1,21E+00	2,30E+00	4,32E+00	2,91E+00	2,56E-02	2,80E-04	2,51E+03	8,54E-03	2,80E-04	3,26E+02	2,98E+02	3,92E+01	3,97E-01	
7,87E+02	3,36E+02	1,20E+00	2,32E+00	4,31E+00	2,91E+00	2,57E-02	2,80E-04	2,52E+03	8,56E-03	2,80E-04	3,27E+02	2,97E+02	3,93E+01	4,00E-01	
7,92E+02	3,36E+02	1,19E+00	2,41E+00	4,12E+00	2,94E+00	2,56E-02	2,80E-04	2,51E+03	8,54E-03	2,80E-04	3,25E+02	2,97E+02	3,85E+01	4,00E-01	
8,24E+02	3,36E+02	1,21E+00	2,51E+00	4,06E+00	2,92E+00	2,59E-02	2,80E-04	2,57E+03	8,64E-03	2,80E-04	3,33E+02	2,98E+02	3,82E+01	3,97E-01	
8,27E+02	3,36E+02	1,20E+00	2,44E+00	4,29E+00	2,94E+00	2,63E-02	2,80E-04	2,64E+03	8,75E-03	2,80E-04	3,42E+02	2,96E+02	3,94E+01	3,99E-01	
8,34E+02	3,35E+02	1,21E+00	2,43E+00	4,35E+00	2,90E+00	2,64E-02	2,80E-04	2,66E+03	8,80E-03	2,80E-04	3,45E+02	2,95E+02	3,99E+01	4,00E-01	
8,62E+02	3,35E+02	1,22E+00	2,52E+00	4,26E+00	2,87E+00	2,66E-02	2,80E-04	2,71E+03	8,87E-03	2,80E-04	3,51E+02	2,95E+02	3,96E+01	3,99E-01	

A.6 Datatsheet

- Advanced Process Technology
- Optimized for Automotive Motor Drive, DC-DC and other Heavy Load Applications
- Exceptionally Small Footprint and Low Profile
- High Power Density
- Low Parasitic Parameters
- Dual Sided Cooling
- 175°C Operating Temperature
- Repetitive Avalanche Capability for Robustness and Reliability
- Lead free, RoHS Compliant and Halogen free
- Automotive Qualified*

$V_{(BR)DSS}$	40V
$R_{DS(on)}$ typ.	700μΩ
max.	1000μΩ
I_D (Silicon Limited)	270A
Q_g	220nC



Applicable DirectFET® Outline and Substrate Outline ①

SB	SC			M2	M4		L4	L6	L8	
----	----	--	--	----	----	--	----	----	-----------	--

Description

The AUIRF7739L2TR(1) combines the latest Automotive HEXFET® Power MOSFET Silicon technology with the advanced DirectFET® packaging to achieve the lowest on-state resistance in a package that has the footprint of a DPak (TO-252AA) and only 0.7 mm profile. The DirectFET package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infra-red or convection soldering techniques, when application note AN-1035 is followed regarding the manufacturing methods and processes. The DirectFET package allows dual sided cooling to maximize thermal transfer in automotive power systems.

This HEXFET® Power MOSFET is designed for applications where efficiency and power density are essential. The advanced DirectFET® packaging platform coupled with the latest silicon technology allows the AUIRF7739L2TR(1) to offer substantial system level savings and performance improvement specifically in motor drive, high frequency DC-DC and other heavy load applications on ICE, HEV and EV platforms. This MOSFET utilizes the latest processing techniques to achieve low on-resistance and low Q_g per silicon area. Additional features of this MOSFET are 175°C operating junction temperature and high repetitive peak current capability. These features combine to make this MOSFET a highly efficient, robust and reliable device for high current automotive applications.

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (T_A) is 25°C, unless otherwise specified.

	Parameter	Max.	Units
V _{DS}	Drain-to-Source Voltage	40	V
V _{GS}	Gate-to-Source Voltage	± 20	
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V (Silicon Limited)④	270	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V (Silicon Limited)④	190	
I _D @ T _A = 25°C	Continuous Drain Current, V _{GS} @ 10V (Silicon Limited)③	46	
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V (Package Limited)	375	
I _{DM}	Pulsed Drain Current ④	1070	
P _D @T _C = 25°C	Power Dissipation ④	125	W
P _D @T _A = 25°C	Power Dissipation ③	3.8	
E _{AS}	Single Pulse Avalanche Energy (Thermally Limited) ⑥	270	mJ
E _{AS} (tested)	Single Pulse Avalanche Energy Tested Value ⑤	160	
I _{AR}	Avalanche Current ⑤	See Fig.12a, 12b, 15, 16	A
E _{AR}	Repetitive Avalanche Energy ⑤		mJ
T _P	Peak Soldering Temperature	270	°C
T _J	Operating Junction and	-55 to + 175	
T _{STG}	Storage Temperature Range		

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ③	—	40	°C/W
$R_{\theta JA}$	Junction-to-Ambient ⑥	12.5	—	
$R_{\theta JA}$	Junction-to-Ambient ⑥	20	—	
$R_{\theta JCan}$	Junction-to-Can ④⑥	—	1.2	
$R_{\theta J-PCB}$	Junction-to-PCB Mounted	—	0.5	
	Linear Derating Factor ④	0.83		W/°C

HEXFET® is a registered trademark of International Rectifier.

*Qualification standards can be found at <http://www.irf.com/>

Static Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise stated)

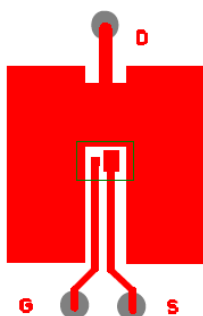
	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.008	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	700	1000	$\mu\Omega$	$V_{GS} = 10V, I_D = 160A$ ⑦
$V_{GS(th)}$	Gate Threshold Voltage	2.0	2.8	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-6.7	—	mV/ $^\circ\text{C}$	
g_{fs}	Forward Transconductance	280	—	—	S	$V_{DS} = 10V, I_D = 160A$
R_G	Gate Resistance	—	1.5	—	Ω	
I_{DSS}	Drain-to-Source Leakage Current	—	—	5.0	μA	$V_{DS} = 40V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 40V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$

Dynamic Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise stated)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge	—	220	330	nC	$V_{DS} = 20V, V_{GS} = 10V$ $I_D = 160A$ See Fig. 11
Q_{gs1}	Pre-Vth Gate-to-Source Charge	—	46	—		
Q_{gs2}	Post-Vth Gate-to-Source Charge	—	19	—		
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	81	—		
Q_{godr}	Gate Charge Overdrive	—	74	—		
Q_{sw}	Switch Charge ($Q_{gs2} + Q_{gd}$)	—	100	—	nC	$V_{DS} = 16V, V_{GS} = 0V$
Q_{oss}	Output Charge	—	83	—	nC	$V_{DD} = 20V, V_{GS} = 10V$ ⑦
$t_{d(on)}$	Turn-On Delay Time	—	21	—	ns	$I_D = 160A$ $R_G = 1.8\Omega$
t_r	Rise Time	—	71	—		
$t_{d(off)}$	Turn-Off Delay Time	—	56	—		
t_f	Fall Time	—	42	—		
C_{iss}	Input Capacitance	—	11880	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	2510	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	1240	—		$f = 1.0MHz$
C_{oss}	Output Capacitance	—	8610	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$
C_{oss}	Output Capacitance	—	2230	—		$V_{GS} = 0V, V_{DS} = 32V, f = 1.0MHz$
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	3040	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 32V$

Diode Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise stated)

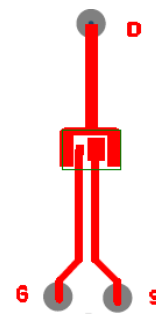
	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	110	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ⑤	—	—	1070		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$I_S = 160A, V_{GS} = 0V$ ⑦
t_{rr}	Reverse Recovery Time	—	87	130	ns	$I_F = 160A, V_{DD} = 20V$
Q_{rr}	Reverse Recovery Charge	—	250	380	nC	$di/dt = 100A/\mu s$ ⑦



③ Surface mounted on 1 in. square Cu (still air).



⑨ Mounted to a PCB with small clip heatsink (still air)



⑨ Mounted on minimum footprint full size board with metalized back and with small clip heatsink (still air)

Notes ① through ⑩ are on page 10

Qualification Information[†]

Qualification Level		Automotive (per AEC-Q101) ^{††}	
		Comments: This part number(s) passed Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		DFET2	MSL1
ESD	Machine Model	Class M4 (800V) AEC-Q101-002	
	Human Body Model	Class H3A (7000V) AEC-Q101-001	
	Charged Device Model	N/A AEC-Q101-005	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com>

†† Exceptions to AEC-Q101 requirements are noted in the qualification report.

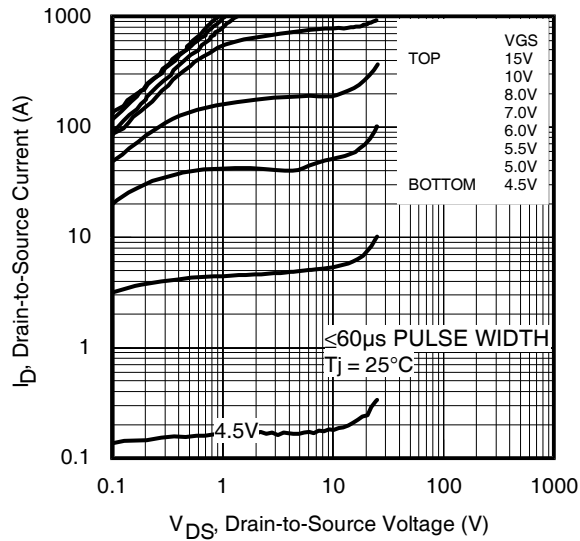


Fig 1. Typical Output Characteristics

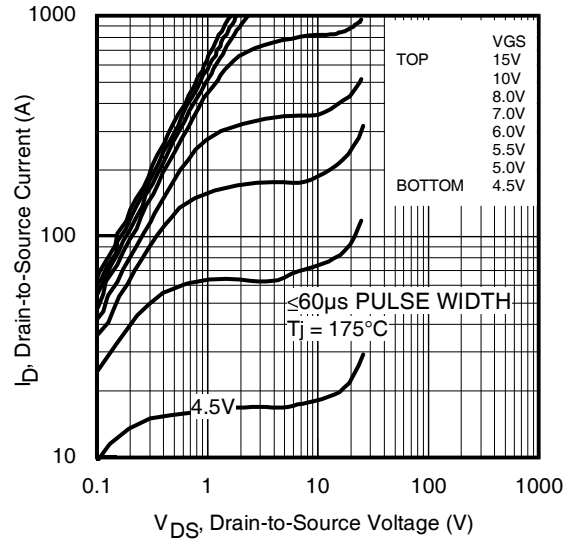


Fig 2. Typical Output Characteristics

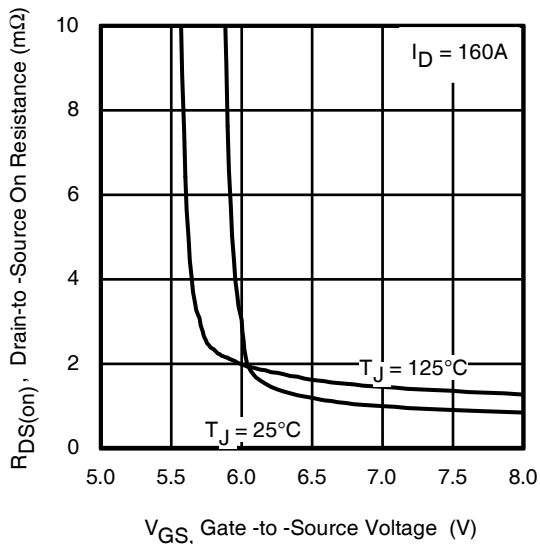


Fig 3. Typical On-Resistance vs. Gate Voltage

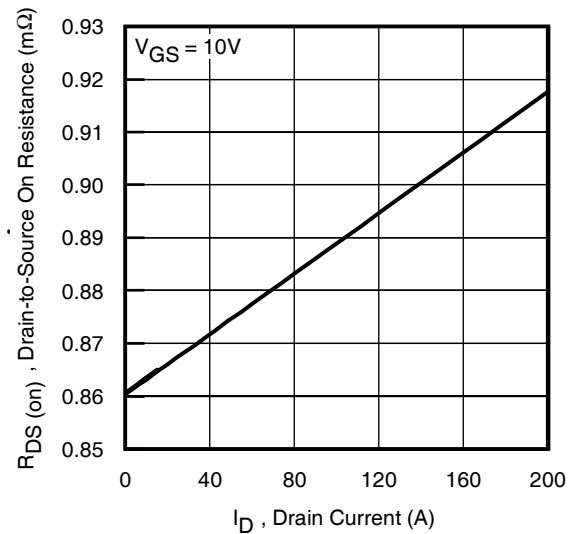


Fig 4. Typical On-Resistance vs. Drain Current

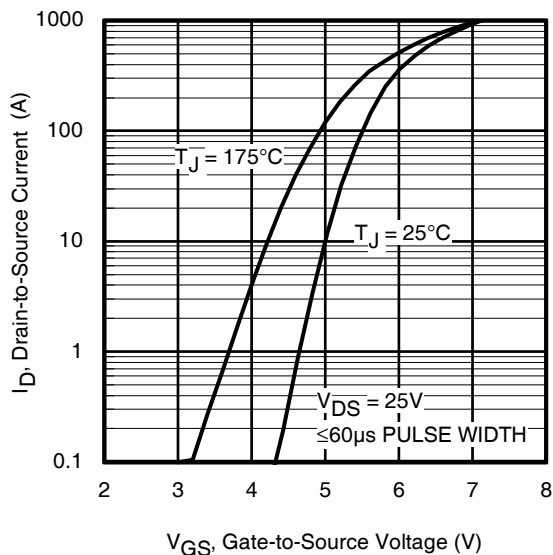


Fig 5. Typical Transfer Characteristics

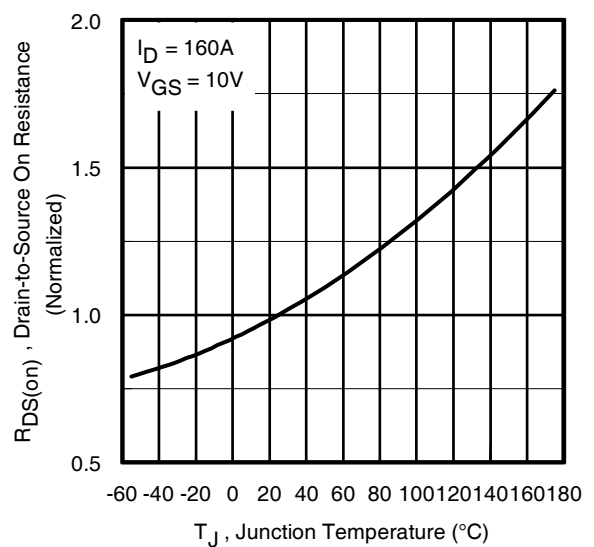


Fig 6. Normalized On-Resistance vs. Temperature

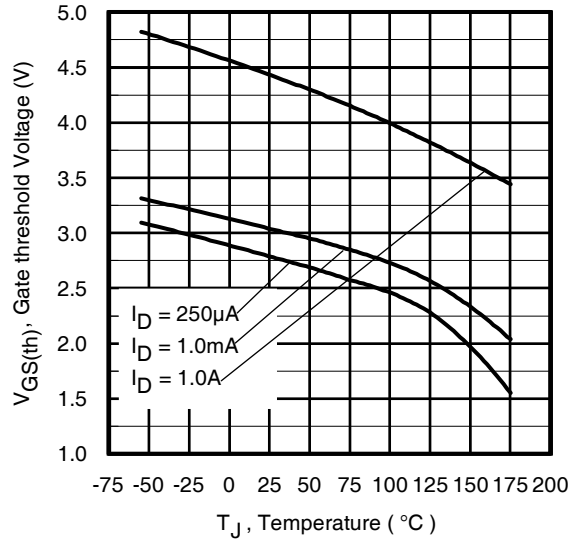


Fig 7. Typical Threshold Voltage vs. Junction Temperature

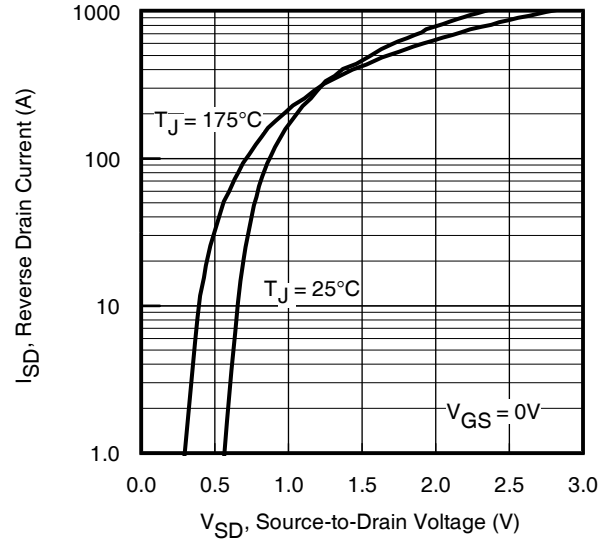


Fig 8. Typical Source-Drain Diode Forward Voltage

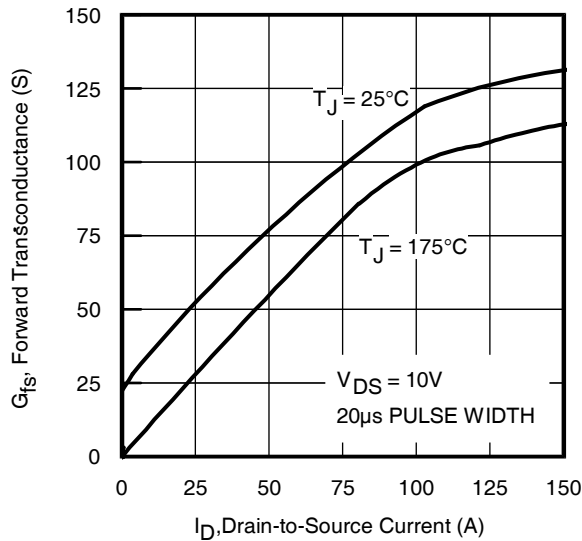


Fig 9. Typical Forward Transconductance vs. Drain Current

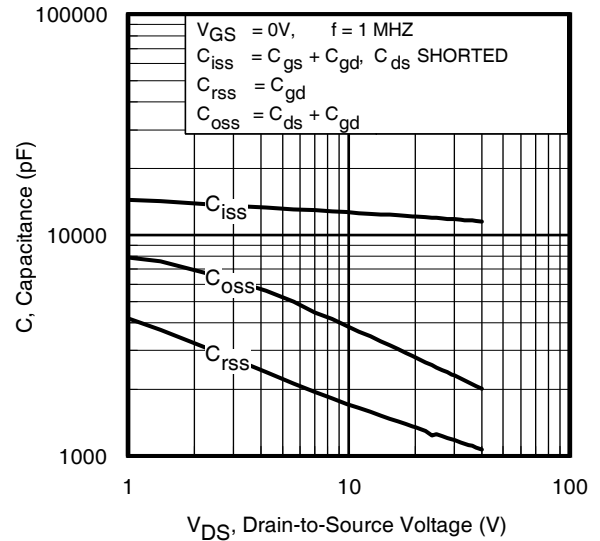


Fig 10. Typical Capacitance vs. Drain-to-Source Voltage

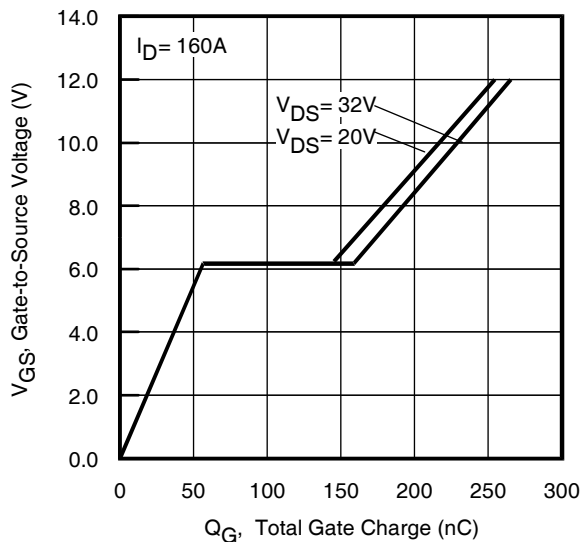


Fig.11 Typical Gate Charge vs. Gate-to-Source Voltage

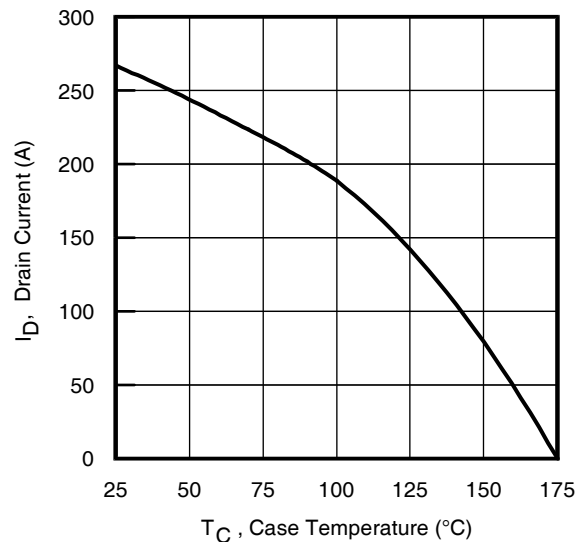


Fig 12. Maximum Drain Current vs. Case Temperature

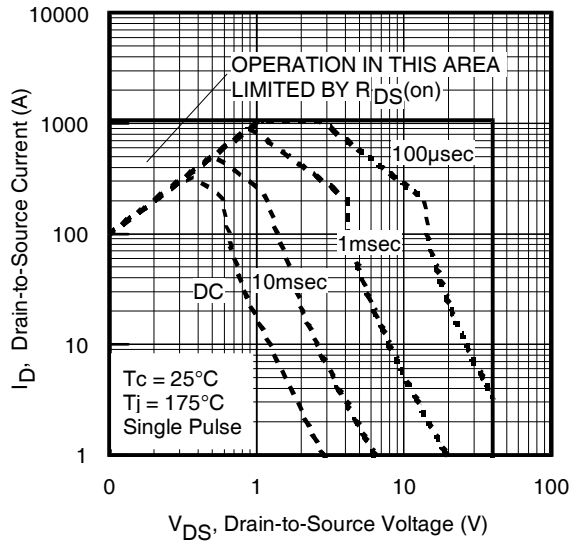


Fig 13. Maximum Safe Operating Area

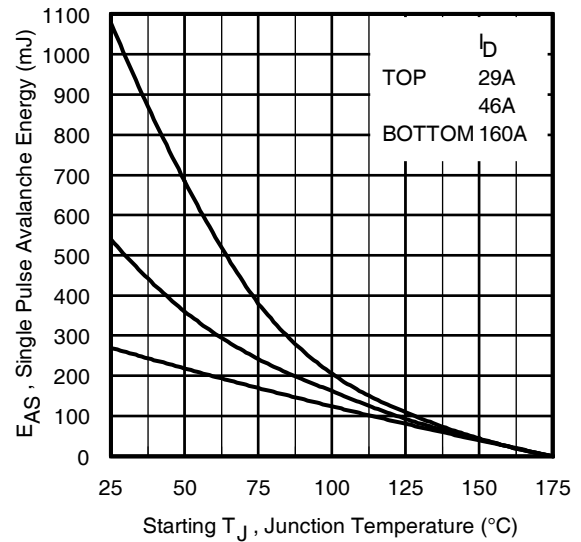


Fig 14. Maximum Avalanche Energy vs. Temperature

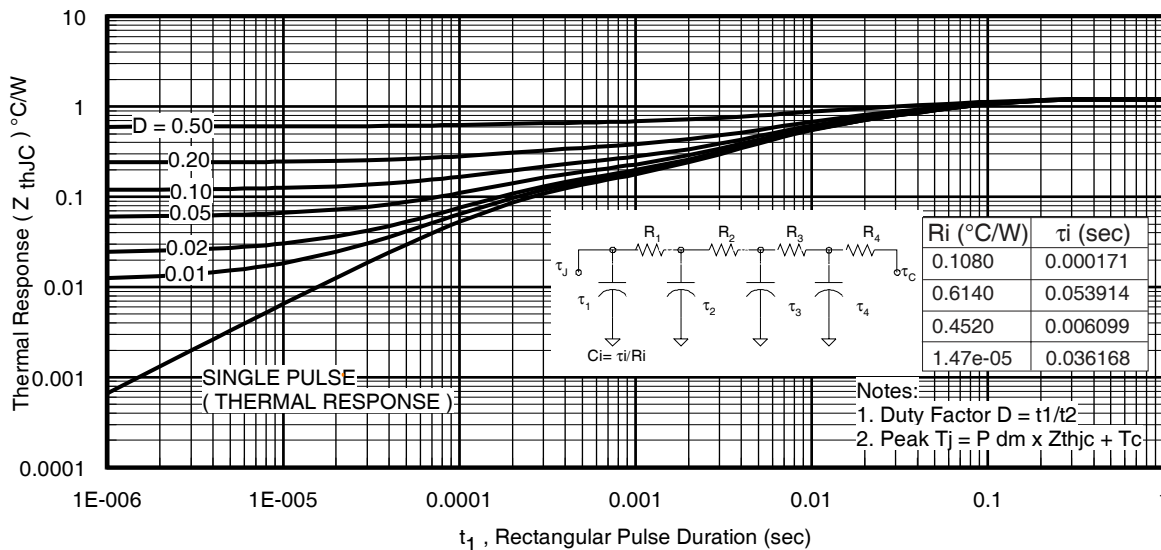


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Case

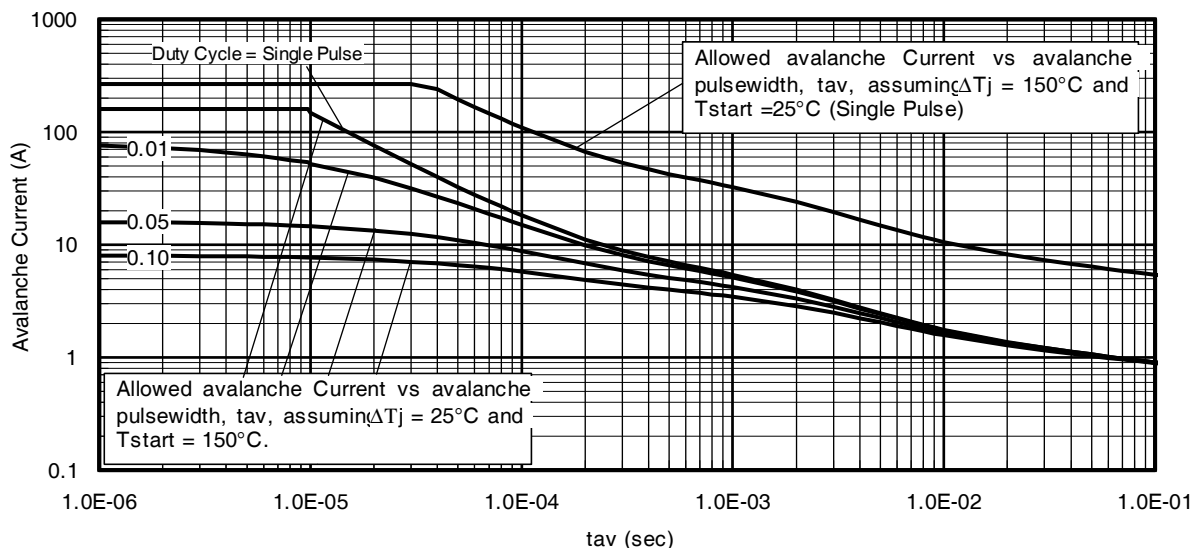


Fig 16. Typical Avalanche Current vs. Pulsewidth

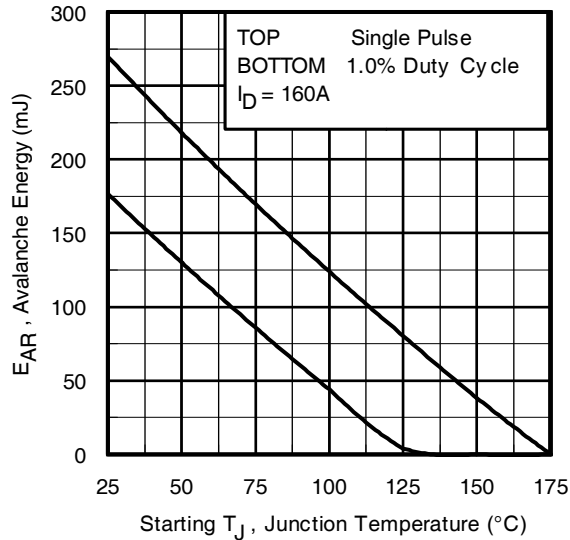


Fig 17. Maximum Avalanche Energy vs. Temperature

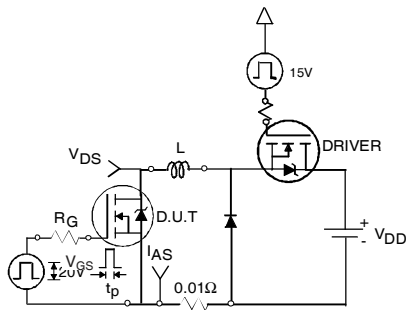


Fig 18a. Unclamped Inductive Test Circuit

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

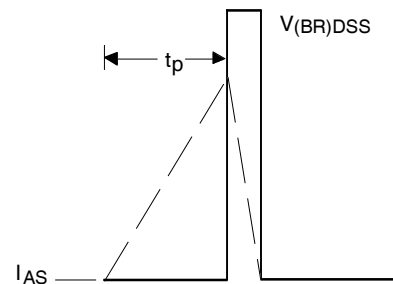


Fig 18b. Unclamped Inductive Waveforms

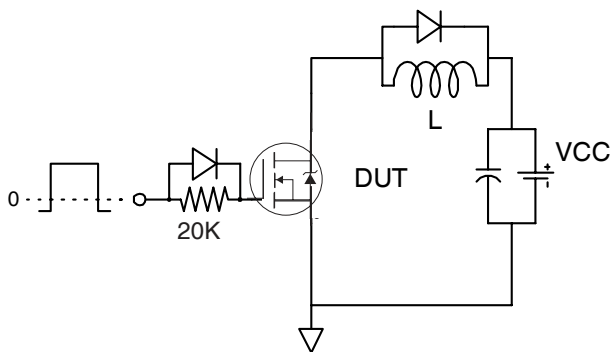


Fig 19a. Gate Charge Test Circuit

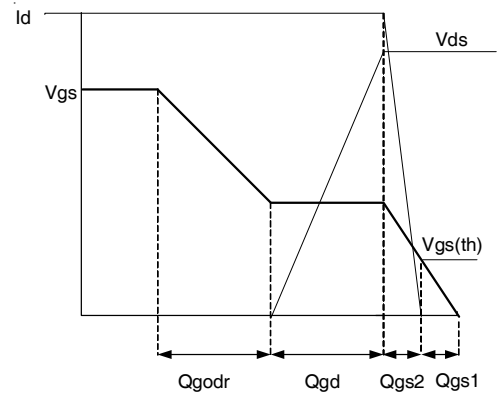


Fig 19b. Gate Charge Waveform

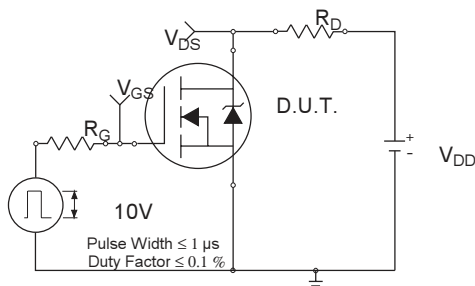


Fig 20a. Switching Time Test Circuit

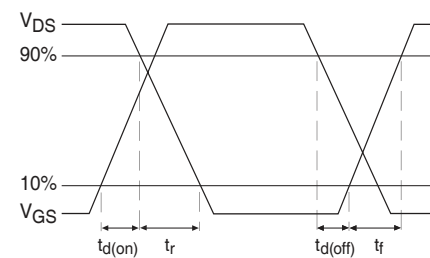


Fig 20b. Switching Time Waveforms

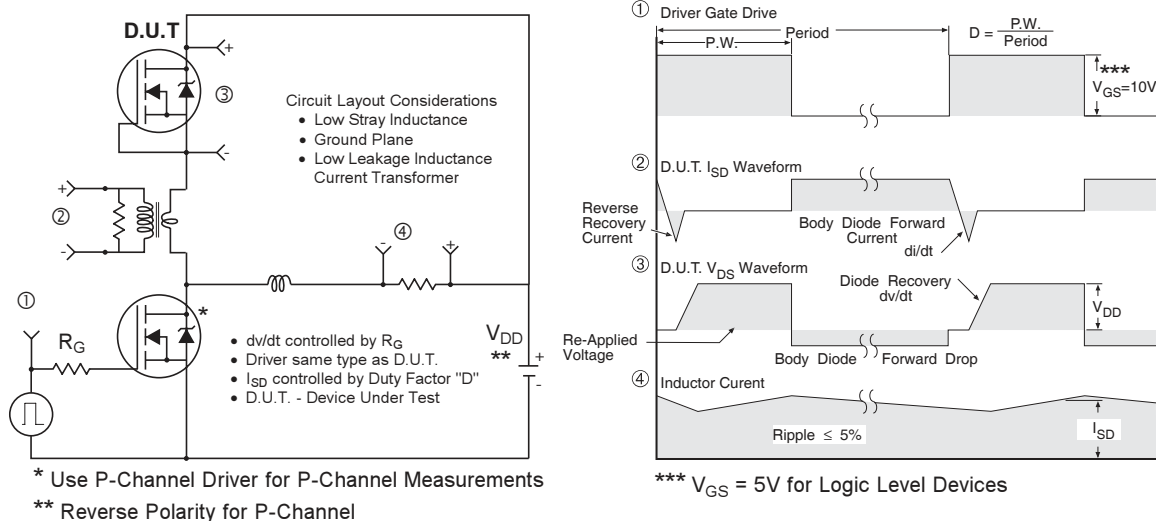
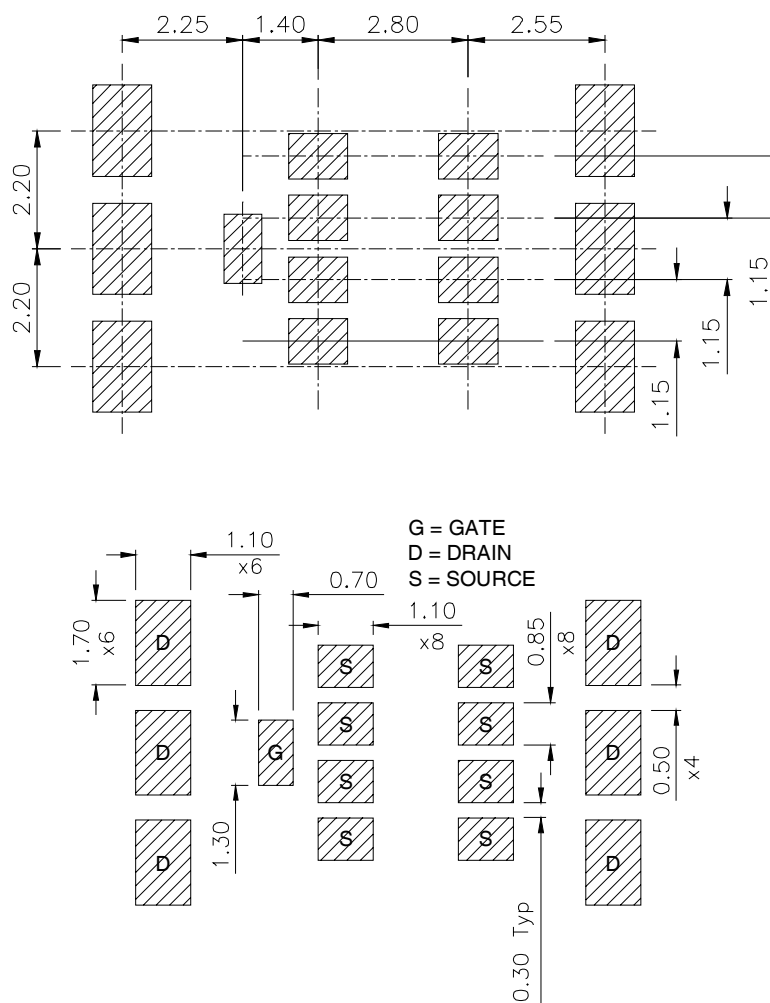


Fig 21. Diode Reverse Recovery Test Circuit for HEXFET® Power MOSFETs

Automotive DirectFET® Board Footprint, L8 (Large Size Can).

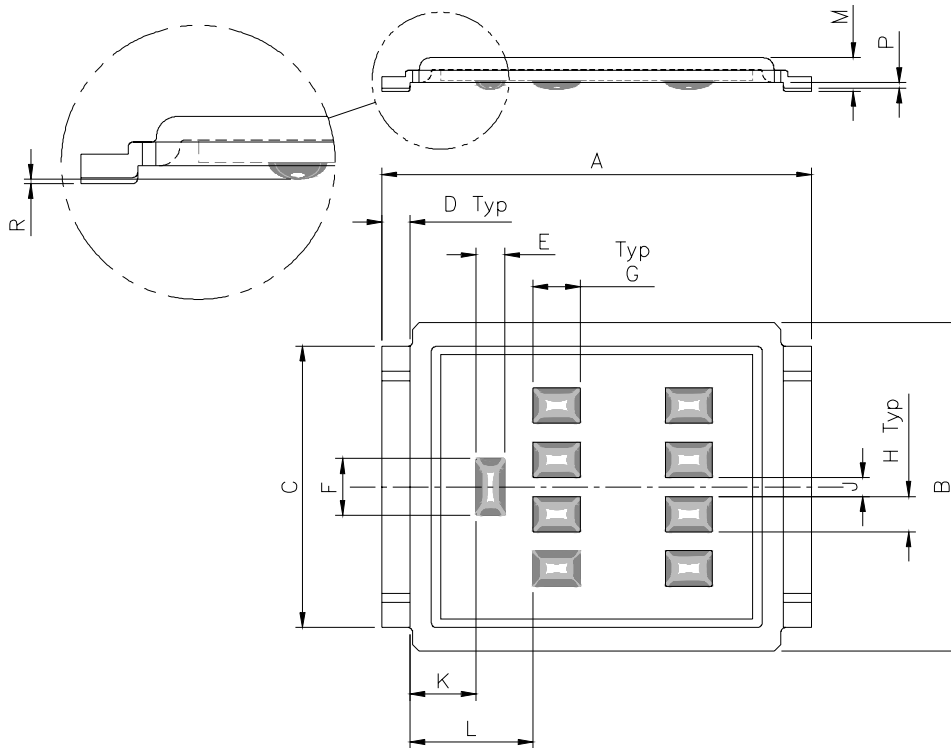
Please see AN-1035 for DirectFET® assembly details and stencil and substrate design recommendations



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package>

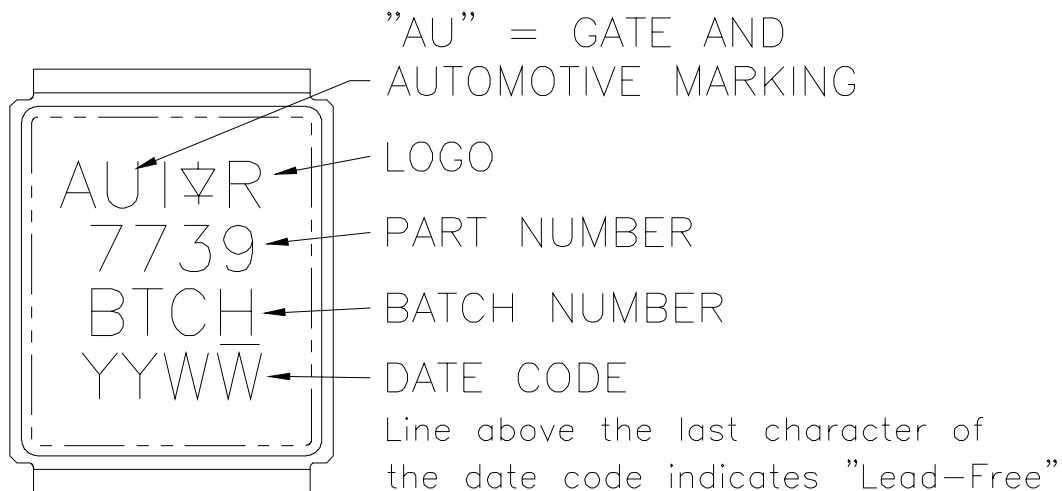
Automotive DirectFET® Outline Dimension, L8 Outline (LargeSize Can).

Please see AN-1035 for DirectFET® assembly details and stencil and substrate design recommendations

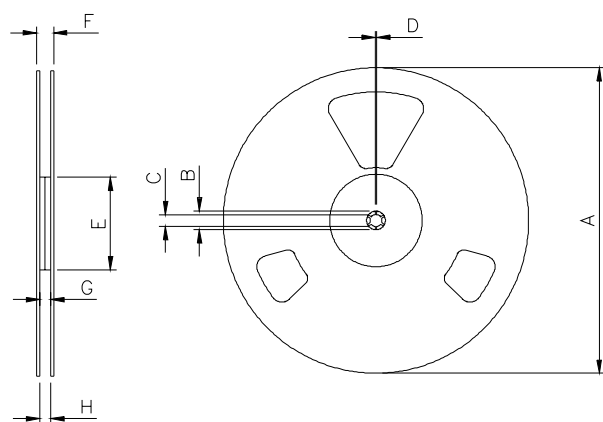


DIMENSIONS				
	METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX
A	9.05	9.15	0.356	0.360
B	6.85	7.10	0.270	0.280
C	5.90	6.00	0.232	0.236
D	0.55	0.65	0.022	0.026
E	0.58	0.62	0.023	0.024
F	1.18	1.22	0.046	0.048
G	0.98	1.02	0.039	0.040
H	0.73	0.77	0.029	0.030
J	0.38	0.42	0.015	0.017
K	1.35	1.45	0.053	0.057
L	2.55	2.65	0.100	0.104
M	0.68	0.74	0.027	0.029
P	0.09	0.17	0.003	0.007
R	0.02	0.08	0.001	0.003

Automotive DirectFET® Part Marking

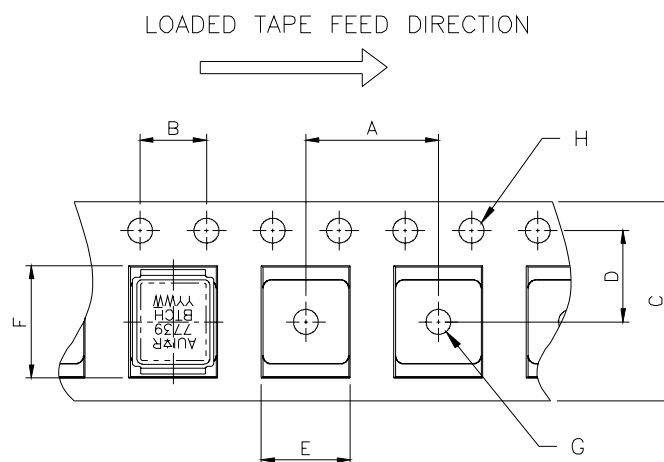


Automotive DirectFET® Tape & Reel Dimension (Showing component orientation).



NOTE: Controlling dimensions in mm
Std reel quantity is 4000 parts. (ordered as AUIRF7739L2TR). For 1000 parts on 7" reel, order AUIRF7739L2TR1

REEL DIMENSIONS								
STANDARD OPTION (QTY 4000)					TR1 OPTION (QTY 1000)			
CODE	METRIC		IMPERIAL		METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	330.00	N.C	12.992	N.C	177.80	N.C	7.000	N.C
B	20.20	N.C	0.795	N.C	20.20	N.C	0.795	N.C
C	12.80	13.20	0.504	0.520	12.98	13.50	0.331	0.50
D	1.50	N.C	0.059	N.C	1.50	2.50	0.059	N.C
E	99.00	100.00	3.900	3.940	62.48	N.C	2.460	N.C
F	N.C	22.40	N.C	0.880	N.C	N.C	N.C	0.53
G	16.40	18.40	0.650	0.720	N.C	N.C	N.C	N.C
H	15.90	19.40	0.630	0.760	16.00	N.C	0.630	N.C



NOTE: CONTROLLING DIMENSIONS IN MM

DIMENSIONS				
CODE	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	11.90	12.10	4.69	0.476
B	3.90	4.10	0.154	0.161
C	15.90	16.30	0.623	0.642
D	7.40	7.60	0.291	0.299
E	7.20	7.40	0.283	0.291
F	9.90	10.10	0.390	0.398
G	1.50	N.C	0.059	N.C
H	1.50	1.60	0.059	0.063

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package>

Notes:

- Click on this section to link to the appropriate technical paper.
- Click on this section to link to the DirectFET® Website.
- Surface mounted on 1 in. square Cu board, steady state.
- T_C measured with thermocouple mounted to top (Drain) of part.
- Repetitive rating; pulse width limited by max. junction temperature.
- Starting $T_J = 25^\circ\text{C}$, $L = 0.021\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 160\text{A}$.
- Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- Used double sided cooling, mounting pad with large heatsink.
- Mounted on minimum footprint full size board with metalized back and with small clip heatsink.
- R_θ is measured at T_J of approximately 90°C .

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For technical support, please contact IR’s Technical Assistance Center

<http://www.irf.com/technical-info/>

WORLD HEADQUARTERS:

233 Kansas St., El Segundo, California 90245
Tel: (310) 252-7105

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

Features

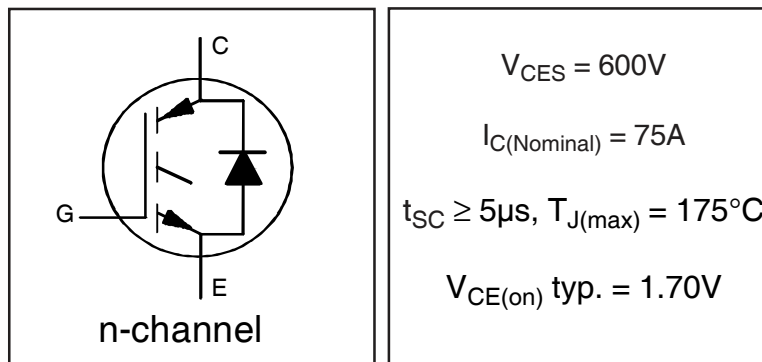
- Low $V_{CE(ON)}$ Trench IGBT Technology
- Low switching losses
- Maximum Junction temperature 175 °C
- 5 μ S short circuit SOA
- Square RBSOA
- 100% of the parts tested for 4X rated current (I_{LM})
- Positive $V_{CE(ON)}$ Temperature Coefficient
- Soft Recovery Co-Pak Diode
- Tight parameter distribution
- Lead-Free, RoHS Compliant
- Automotive Qualified *

Benefits

- High Efficiency in a wide range of applications
- Suitable for a wide range of switching frequencies due to Low $V_{CE(ON)}$ and Low Switching losses
- Rugged transient Performance for increased reliability
- Excellent Current sharing in parallel operation
- Low EMI

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (T_A) is 25°C, unless otherwise specified.

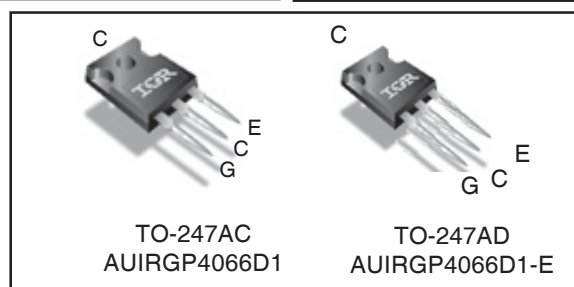


$$V_{CES} = 600V$$

$$I_{C(Nominal)} = 75A$$

$$t_{SC} \geq 5\mu s, T_{J(max)} = 175^{\circ}C$$

$$V_{CE(on)} \text{ typ.} = 1.70V$$



G	C	E
Gate	Collector	Emitter

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
$I_C @ T_C = 25^{\circ}C$	Continuous Collector Current	140	A
$I_C @ T_C = 100^{\circ}C$	Continuous Collector Current	90	
$I_{NOMINAL}$	Nominal Current	75	
I_{CM}	Pulse Collector Current $V_{GE} = 15V$	225	
I_{LM}	Clamped Inductive Load Current $V_{GE} = 20V$ ①	300	
$I_F @ T_C = 25^{\circ}C$	Diode Continuous Forward Current	140	
$I_F @ T_C = 100^{\circ}C$	Diode Continuous Forward Current	90	V
I_{FM}	Diode Maximum Forward Current ②	300	
V_{GE}	Continuous Gate-to-Emitter Voltage	± 20	V
	Transient Gate-to-Emitter Voltage	± 30	
$P_D @ T_C = 25^{\circ}C$	Maximum Power Dissipation	454	W
$P_D @ T_C = 100^{\circ}C$	Maximum Power Dissipation	227	
T_J	Operating Junction and	-55 to +175	$^{\circ}C$
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw	10 lbf-in (1.1 N-m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$ (IGBT)	Thermal Resistance Junction-to-Case-(each IGBT) ④	—	—	0.33	$^{\circ}C/W$
$R_{\theta JC}$ (Diode)	Thermal Resistance Junction-to-Case-(each Diode) ④	—	—	0.53	
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink (flat, greased surface)	—	0.24	—	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (typical socket mount)	—	40	—	

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	$V_{GE} = 0V, I_C = 200\mu A$ ④
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.78	—	V/ $^\circ\text{C}$	$V_{GE} = 0V, I_C = 10mA$ (25 $^\circ\text{C}$ -175 $^\circ\text{C}$)
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	1.70	2.1	V	$I_C = 75A, V_{GE} = 15V, T_J = 25^\circ\text{C}$ ②
		—	2.0	—		$I_C = 75A, V_{GE} = 15V, T_J = 150^\circ\text{C}$ ②
		—	2.1	—		$I_C = 75A, V_{GE} = 15V, T_J = 175^\circ\text{C}$ ②
$V_{GE(th)}$	Gate Threshold Voltage	4.0	—	6.5	V	$V_{CE} = V_{GE}, I_C = 2.1mA$
$\Delta V_{GE(th)}/\Delta T_J$	Threshold Voltage temp. coefficient	—	-21	—	mV/ $^\circ\text{C}$	$V_{CE} = V_{GE}, I_C = 2.1mA$ (25 $^\circ\text{C}$ - 175 $^\circ\text{C}$)
g_{fe}	Forward Transconductance	—	50	—	S	$V_{CE} = 50V, I_C = 75A, PW = 25\mu s$
I_{CES}	Collector-to-Emitter Leakage Current	—	3.0	200	μA	$V_{GE} = 0V, V_{CE} = 600V$
		—	10	—	mA	$V_{GE} = 0V, V_{CE} = 600V, T_J = 175^\circ\text{C}$
V_{FM}	Diode Forward Voltage Drop	—	1.60	1.77	V	$I_F = 75A$
		—	1.54	—		$I_F = 75A, T_J = 175^\circ\text{C}$
I_{GES}	Gate-to-Emitter Leakage Current	—	—	± 100	nA	$V_{GE} = \pm 20V$

Switching Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	150	225	nC	$I_C = 75A$ $V_{GE} = 15V$ $V_{CC} = 400V$
Q_{ge}	Gate-to-Emitter Charge (turn-on)	—	40	60		
Q_{gc}	Gate-to-Collector Charge (turn-on)	—	60	90		
E_{on}	Turn-On Switching Loss	—	4240	5190	μJ	$I_C = 75A, V_{CC} = 400V, V_{GE} = 15V$ $R_G = 10\Omega, L = 100\mu H, T_J = 25^\circ\text{C}$ Energy losses include tail & diode reverse recovery
E_{off}	Turn-Off Switching Loss	—	2170	3060		
E_{total}	Total Switching Loss	—	6410	8250		
$t_{d(on)}$	Turn-On delay time	—	50	70	ns	$I_C = 75A, V_{CC} = 400V, V_{GE} = 15V$ $R_G = 10\Omega, L = 100\mu H$ $T_J = 25^\circ\text{C}$
t_r	Rise time	—	80	100		
$t_{d(off)}$	Turn-Off delay time	—	200	230		
t_f	Fall time	—	60	80		
E_{on}	Turn-On Switching Loss	—	6210	—	μJ	$I_C = 75A, V_{CC} = 400V, V_{GE} = 15V$ $R_G = 10\Omega, L = 100\mu H, T_J = 175^\circ\text{C}$ Energy losses include tail & diode reverse recovery
E_{off}	Turn-Off Switching Loss	—	2815	—		
E_{total}	Total Switching Loss	—	9025	—		
$t_{d(on)}$	Turn-On delay time	—	45	—	ns	$I_C = 75A, V_{CC} = 400V, V_{GE} = 15V$ $R_G = 10\Omega, L = 100\mu H$ $T_J = 175^\circ\text{C}$
t_r	Rise time	—	70	—		
$t_{d(off)}$	Turn-Off delay time	—	240	—		
t_f	Fall time	—	80	—		
C_{ies}	Input Capacitance	—	4470	—	pF	$V_{GE} = 0V$ $V_{CC} = 30V$ $f = 1.0MHz$
C_{oes}	Output Capacitance	—	350	—		
C_{res}	Reverse Transfer Capacitance	—	140	—		
RBSOA	Reverse Bias Safe Operating Area	FULL SQUARE				$T_J = 175^\circ\text{C}, I_C = 300A$ $V_{CC} = 480V, V_p \leq 600V$ $R_g = 10\Omega, V_{GE} = +20V$ to 0V
SCSOA	Short Circuit Safe Operating Area	5	—	—	μs	$V_{CC} = 400V, V_p \leq 600V$ $R_g = 10\Omega, V_{GE} = +15V$ to 0V
E_{rec}	Reverse Recovery Energy of the Diode	—	680	—	μJ	$T_J = 175^\circ\text{C}$
t_{rr}	Diode Reverse Recovery Time	—	240	—	ns	$V_{CC} = 400V, I_F = 75A$
I_{rr}	Peak Reverse Recovery Current	—	50	—	A	$V_{GE} = 15V, R_g = 10\Omega, L = 100\mu H$

Notes:

- ① $V_{CC} = 80\% (V_{CES}), V_{GE} = 20V, L = 100\mu H, R_G = 10\Omega$.
- ② Pulse width limited by max. junction temperature.
- ③ Refer to AN-1086 for guidelines for measuring $V_{(BR)CES}$ safely.
- ④ R_θ is measured at T_J of approximately 90 $^\circ\text{C}$.

Qualification Information[†]

Qualification Level		Automotive (per AEC-Q101) ^{††}	
		Comments: This part number(s) passed Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		TO-247AC	N/A
		TO-247AD	
ESD	Machine Model	Class M4 (+/-425V) ^{†††} AEC-Q101-002	
	Human Body Model	Class H2 (+/-4000V) ^{†††} AEC-Q101-001	
	Charged Device Model	Class C5 (+/-1125V) ^{†††} AEC-Q101-005	
RoHS Compliant		Yes	

[†] Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/>

^{††} Exceptions (if any) to AEC-Q101 requirements are noted in the qualification report.

^{†††} Highest passing voltage

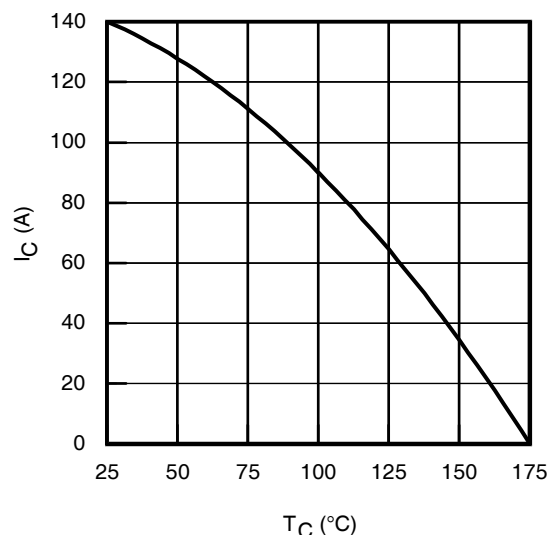


Fig. 1 - Maximum DC Collector Current vs. Case Temperature

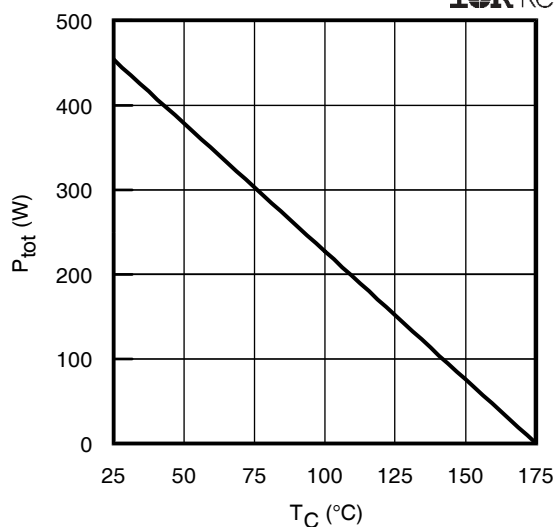


Fig. 2 - Power Dissipation vs. Case Temperature

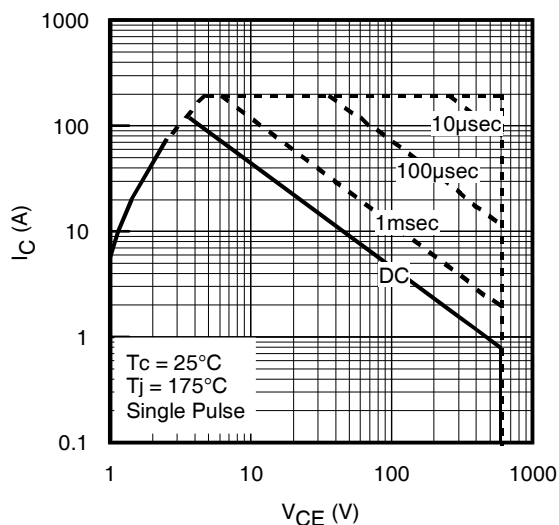


Fig. 3 - Forward SOA
 $T_C = 25^\circ\text{C}$, $T_J \leq 175^\circ\text{C}$; $V_{GE} = 15\text{V}$

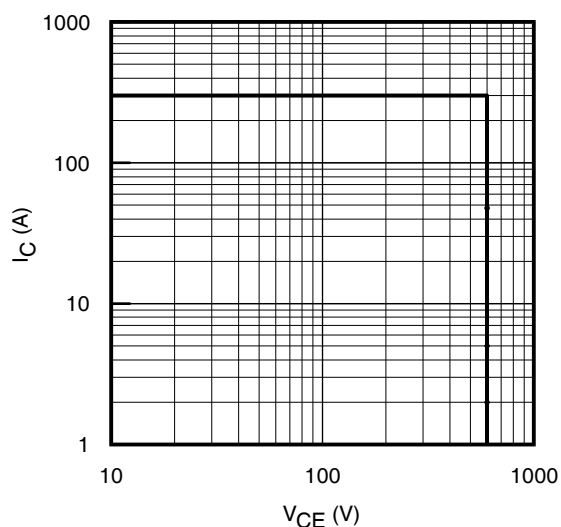


Fig. 4 - Reverse Bias SOA
 $T_J = 175^\circ\text{C}$; $V_{GE} = 20\text{V}$

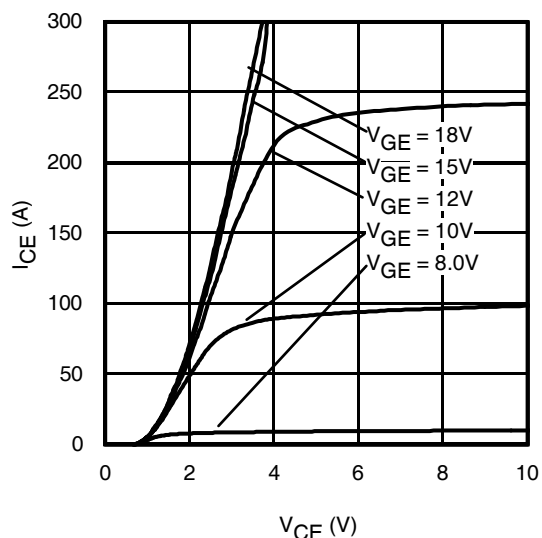


Fig. 5 - Typ. IGBT Output Characteristics
 $T_J = -40^\circ\text{C}$; $t_p \leq 60\mu\text{s}$

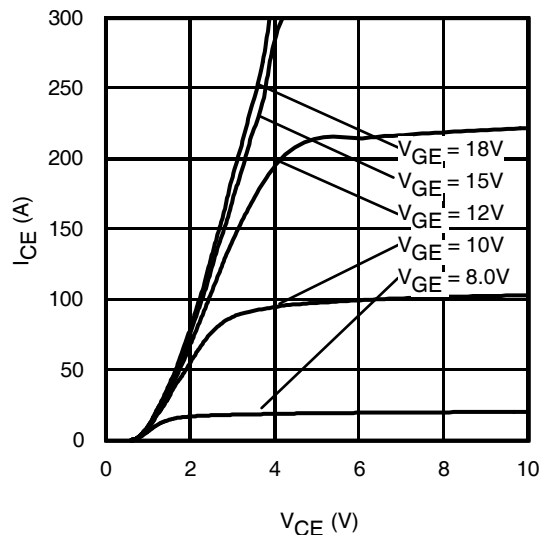


Fig. 6 - Typ. IGBT Output Characteristics
 $T_J = 25^\circ\text{C}$; $t_p \leq 60\mu\text{s}$

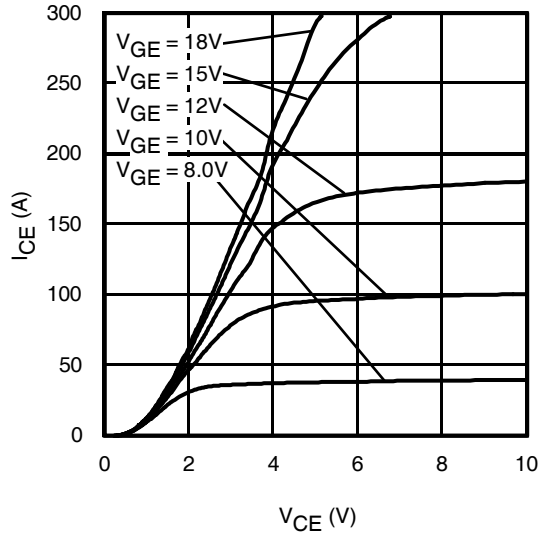


Fig. 7 - Typ. IGBT Output Characteristics
 $T_J = 175^\circ\text{C}$; $t_p \leq 60\mu\text{s}$

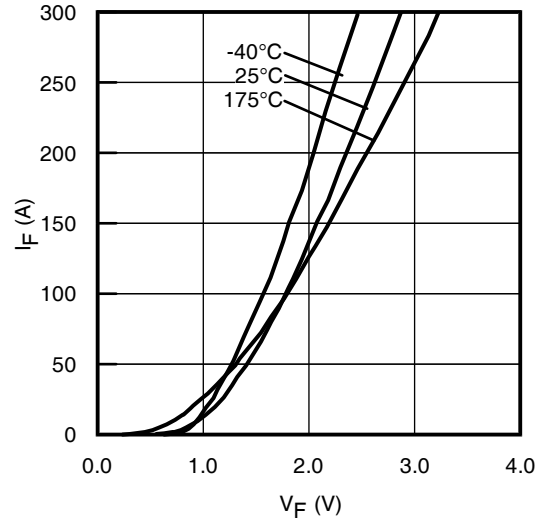


Fig. 8 - Typ. Diode Forward Characteristics
 $t_p \leq 60\mu\text{s}$

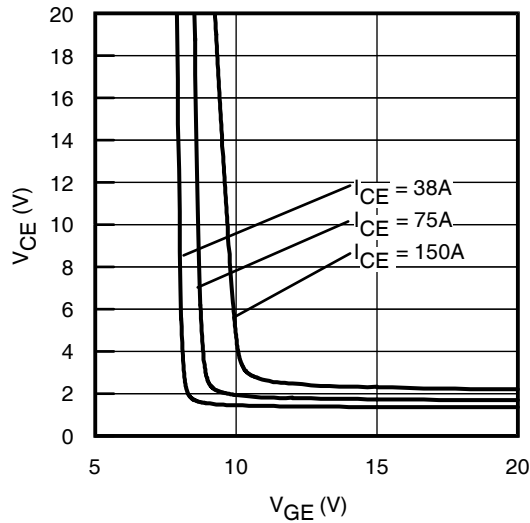


Fig. 9 - Typical V_{CE} vs. V_{GE}
 $T_J = -40^\circ\text{C}$

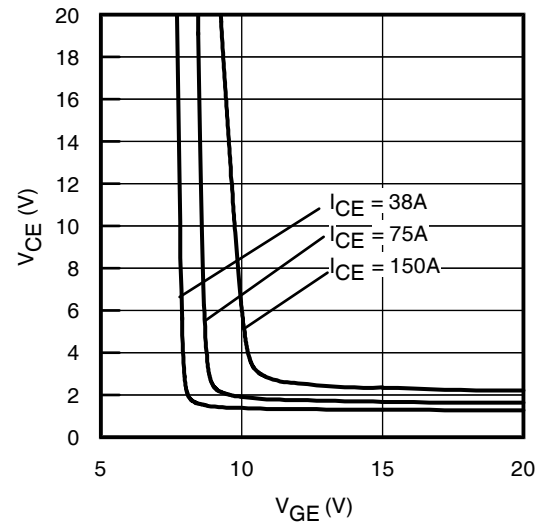


Fig. 10 - Typical V_{CE} vs. V_{GE}
 $T_J = 25^\circ\text{C}$

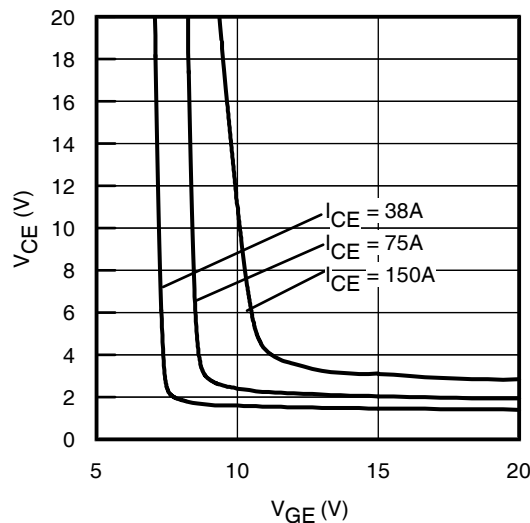


Fig. 11 - Typical V_{CE} vs. V_{GE}
 $T_J = 175^\circ\text{C}$

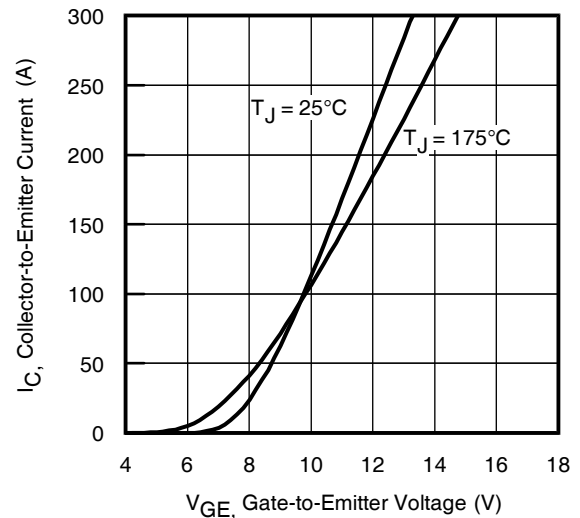


Fig. 12 - Typ. Transfer Characteristics
 $V_{CE} = 50\text{V}$; $t_p \leq 60\mu\text{s}$

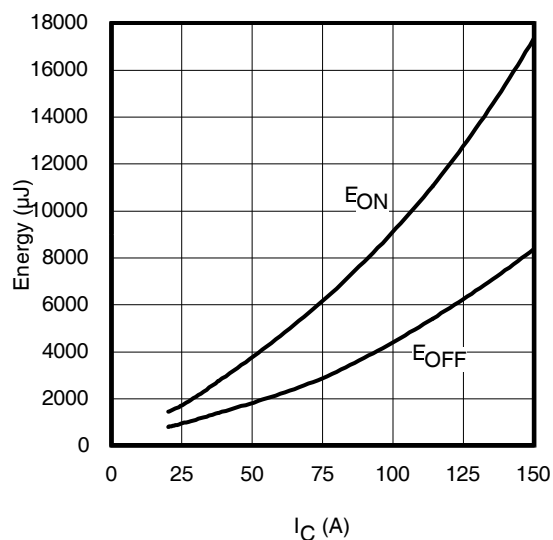


Fig. 13 - Typ. Energy Loss vs. I_C
 $T_J = 175^\circ\text{C}$; $L = 100\mu\text{H}$; $V_{CE} = 400\text{V}$; $R_G = 10\Omega$; $V_{GE} = 15\text{V}$

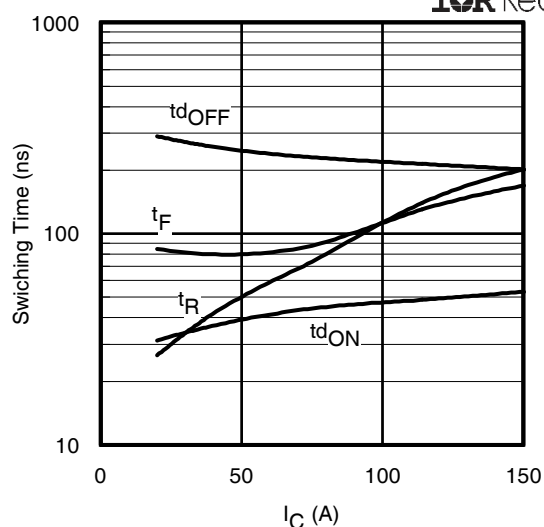


Fig. 14 - Typ. Switching Time vs. I_C
 $T_J = 175^\circ\text{C}$; $L = 100\mu\text{H}$; $V_{CE} = 400\text{V}$; $R_G = 10\Omega$; $V_{GE} = 15\text{V}$

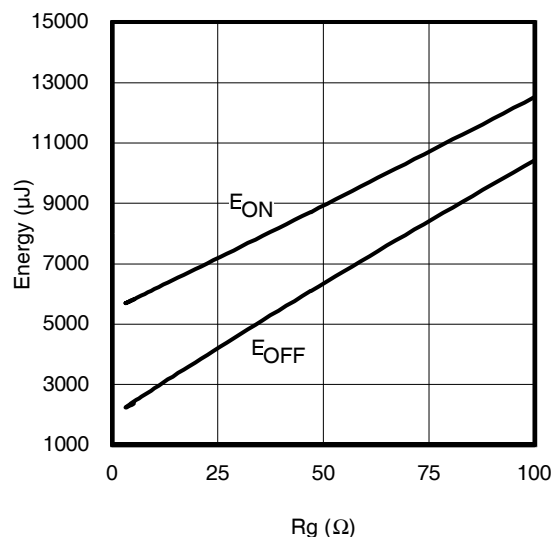


Fig. 15 - Typ. Energy Loss vs. R_G
 $T_J = 175^\circ\text{C}$; $L = 100\mu\text{H}$; $V_{CE} = 400\text{V}$; $I_{CE} = 75\text{A}$; $V_{GE} = 15\text{V}$

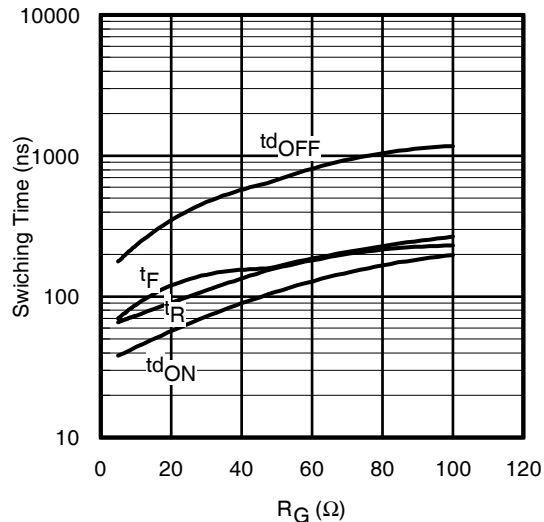


Fig. 16 - Typ. Switching Time vs. R_G
 $T_J = 175^\circ\text{C}$; $L = 100\mu\text{H}$; $V_{CE} = 400\text{V}$; $I_{CE} = 75\text{A}$; $V_{GE} = 15\text{V}$

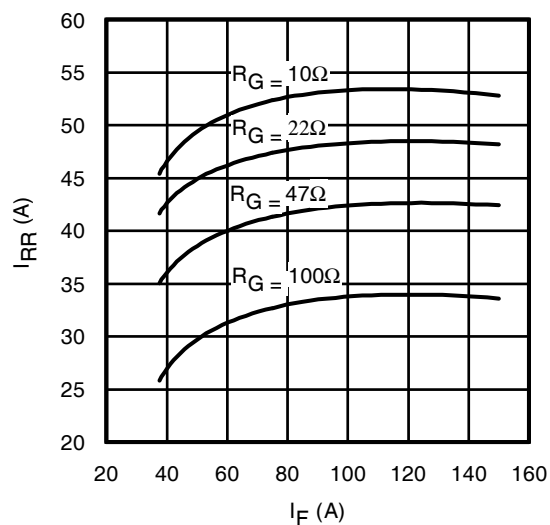


Fig. 17 - Typ. Diode I_{RR} vs. I_F
 $T_J = 175^\circ\text{C}$

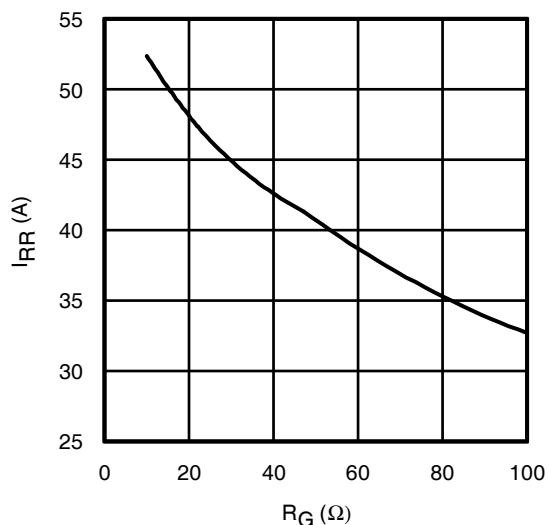


Fig. 18 - Typ. Diode I_{RR} vs. R_G
 $T_J = 175^\circ\text{C}$

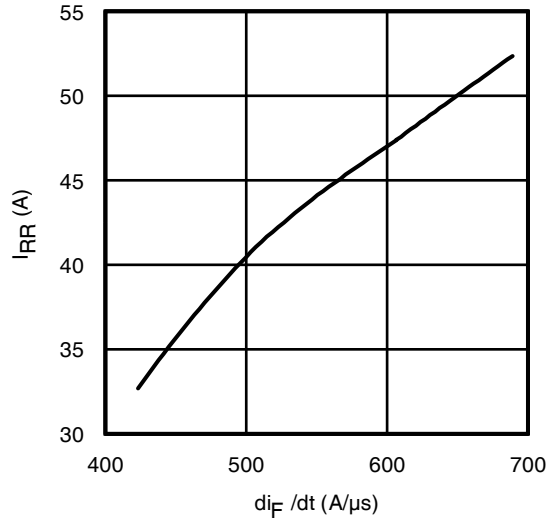


Fig. 19 - Typ. Diode I_{RR} vs. di_F/dt
 $V_{CC} = 400V$; $V_{GE} = 15V$; $I_F = 75A$; $T_J = 175^\circ C$

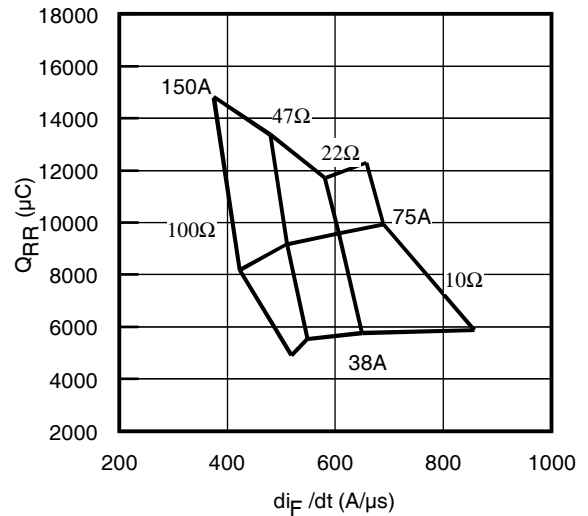


Fig. 20 - Typ. Diode Q_{RR} vs. di_F/dt
 $V_{CC} = 400V$; $V_{GE} = 15V$; $T_J = 175^\circ C$

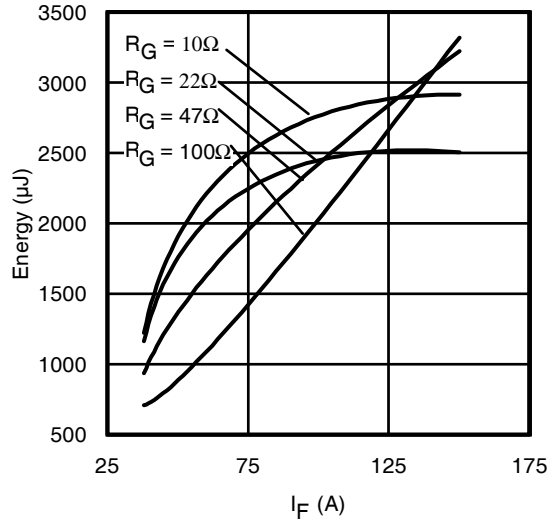


Fig. 21 - Typ. Diode E_{RR} vs. I_F
 $T_J = 175^\circ C$

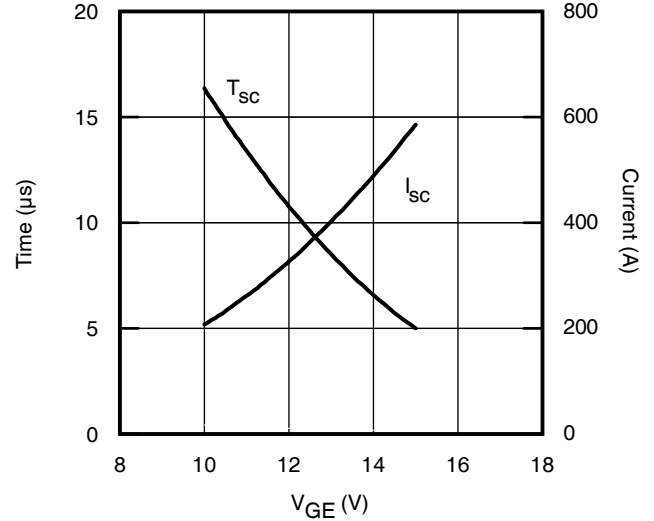


Fig. 22 - V_{GE} vs. Short Circuit Time
 $V_{CC} = 400V$; $T_C = 25^\circ C$

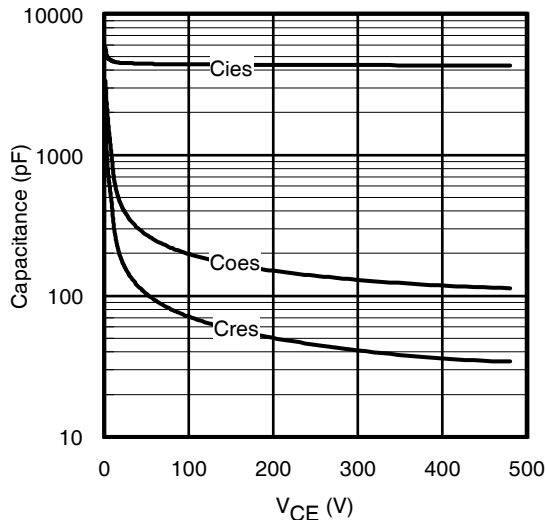


Fig. 23 - Typ. Capacitance vs. V_{CE}
 $V_{GE} = 0V$; $f = 1MHz$

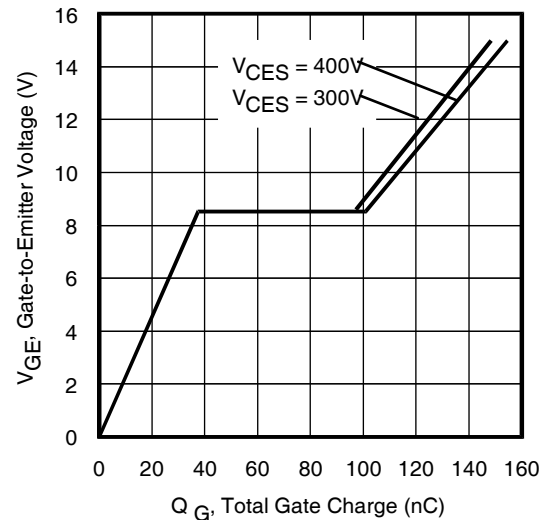


Fig. 24 - Typical Gate Charge vs. V_{GE}
 $I_{CE} = 75A$; $L = 485\mu H$

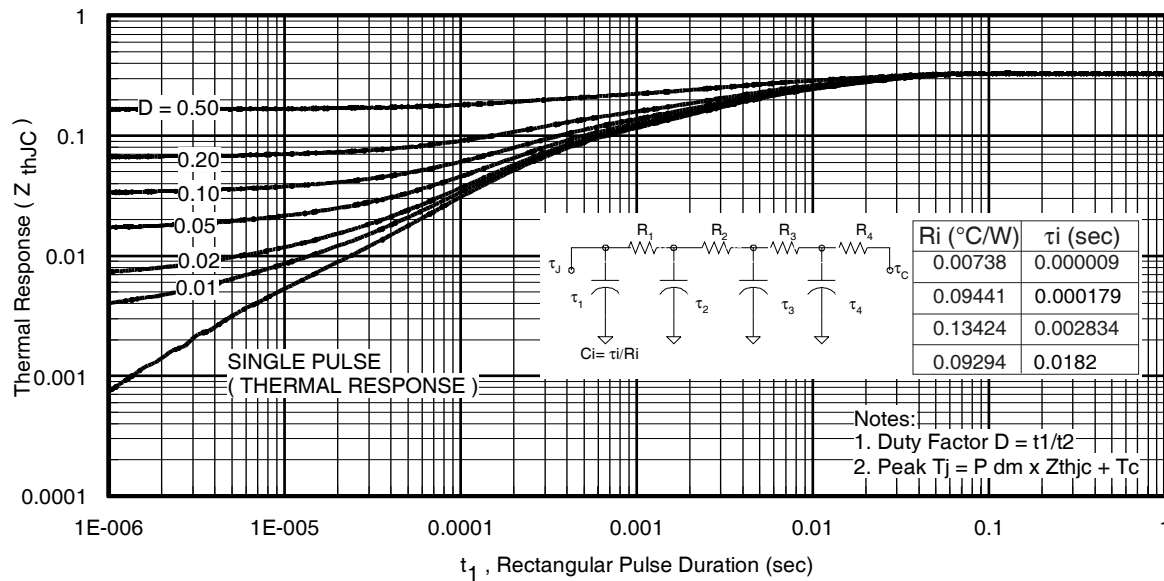


Fig 25. Maximum Transient Thermal Impedance, Junction-to-Case (IGBT)

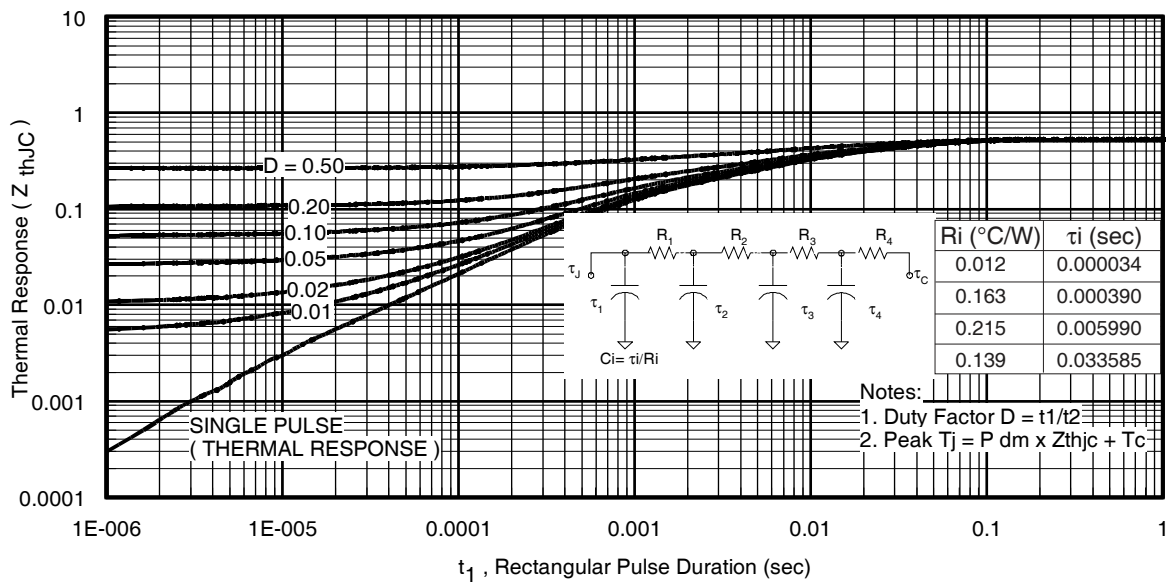


Fig. 26. Maximum Transient Thermal Impedance, Junction-to-Case (DIODE)

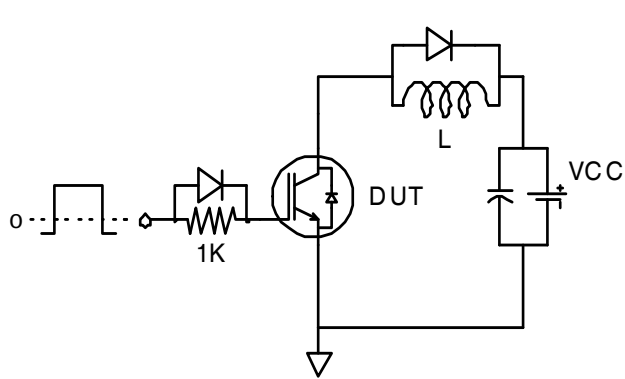


Fig.C.T.1 - Gate Charge Circuit (turn-off)

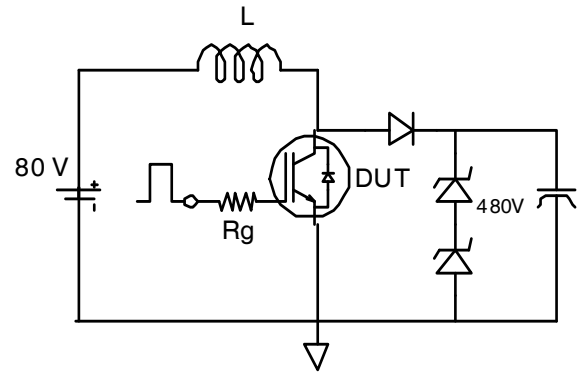


Fig.C.T.2 - RBSOA Circuit

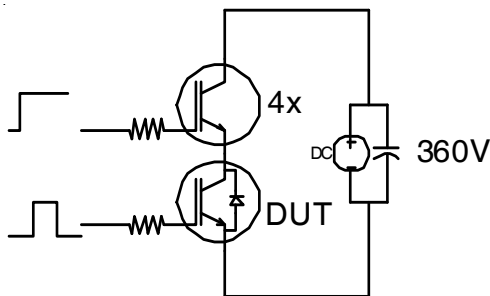


Fig.C.T.3 - S.C. SOA Circuit

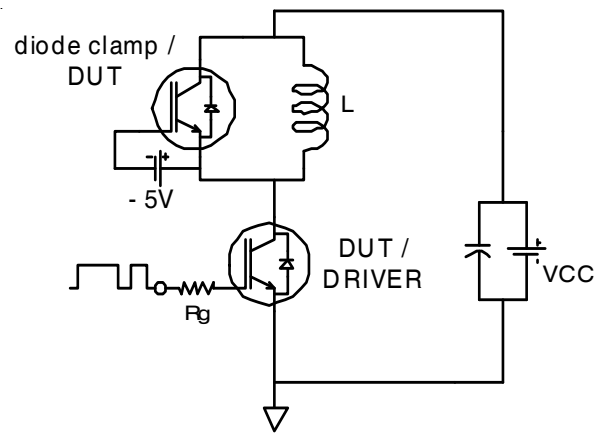


Fig.C.T.4 - Switching Loss Circuit

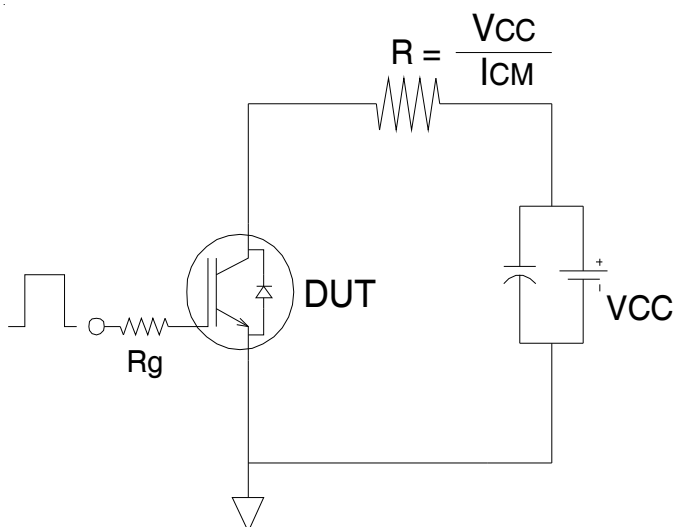


Fig.C.T.5 - Resistive Load Circuit

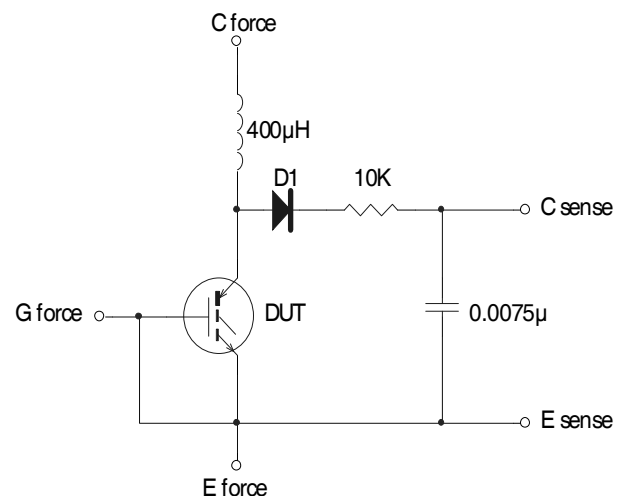


Fig.C.T.6 - BV CES Filter Circuit

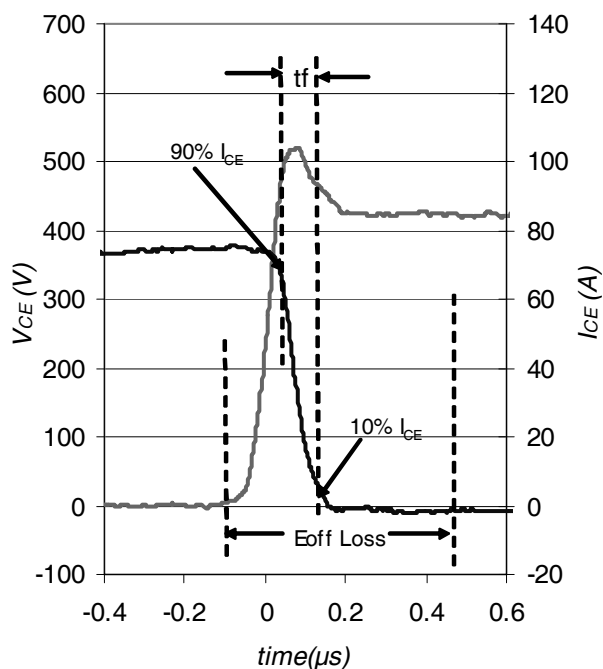


Fig. WF1 - Typ. Turn-off Loss Waveform
@ $T_J = 175^\circ\text{C}$ using Fig. CT.4

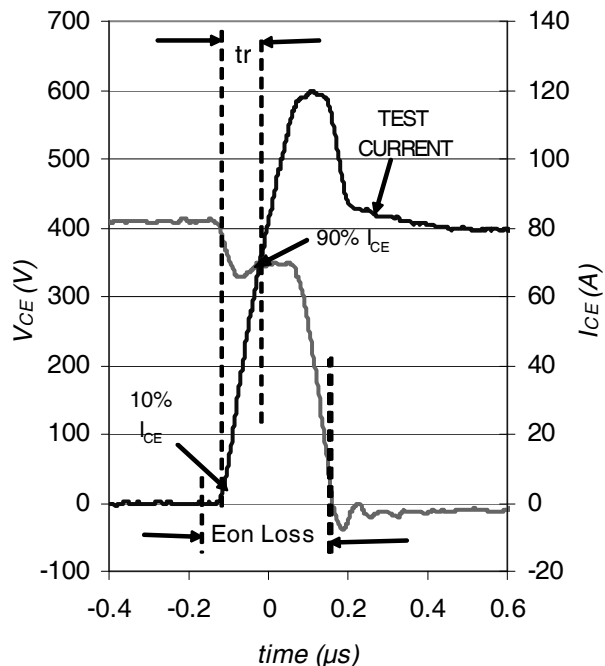


Fig. WF2 - Typ. Turn-on Loss Waveform
@ $T_J = 175^\circ\text{C}$ using Fig. CT.4

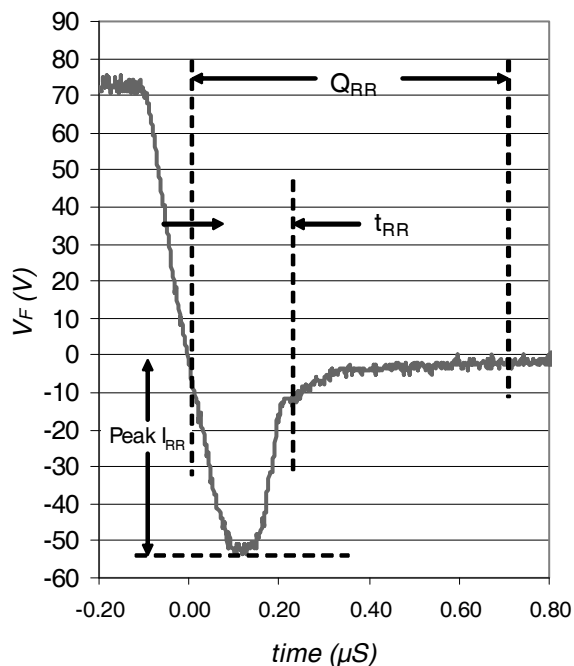


Fig. WF3 - Typ. Diode Recovery Waveform
@ $T_J = 175^\circ\text{C}$ using Fig. CT.4

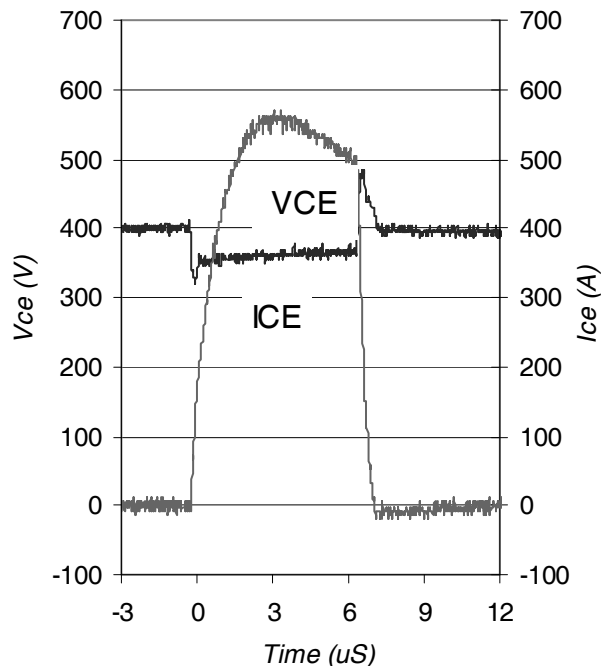
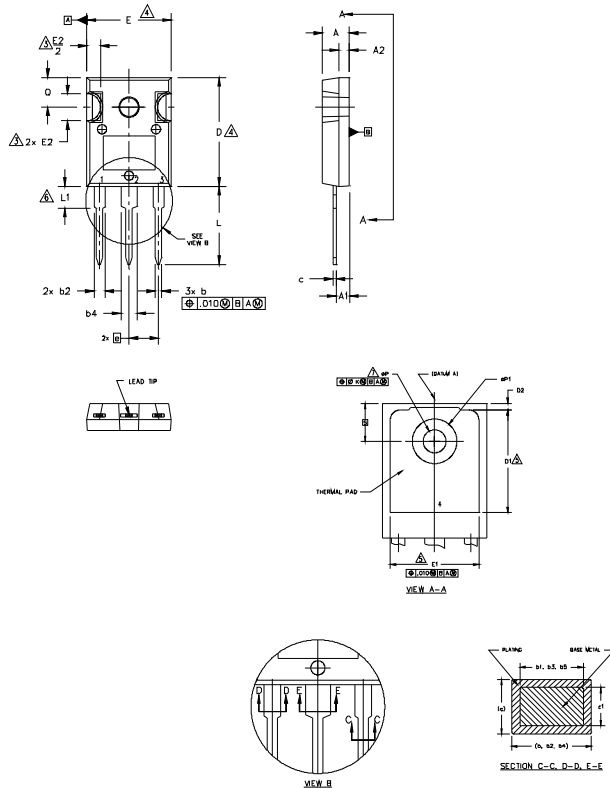


Fig. WF4 - Typ. S.C. Waveform
@ $T_J = 25^\circ\text{C}$ using Fig. CT.3

TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. ØP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC .

SYMBOL	DIMENSIONS				NOTE
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	—	13.08	—	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	—	13.46	—	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
Øk	.010		0.25		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
ØP	.140	.144	3.56	3.66	
ØP1	—	.291	—	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

- 1.— GATE
- 2.— DRAIN
- 3.— SOURCE
- 4.— DRAIN

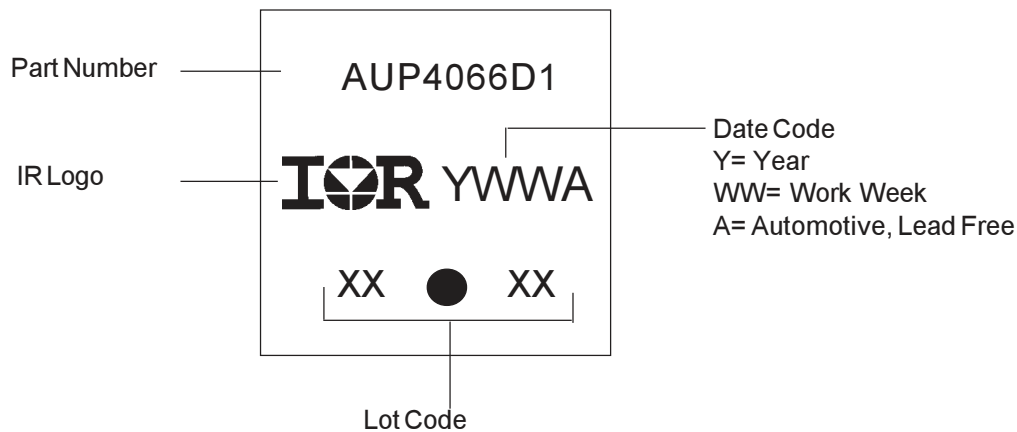
IGBTs, CoPACK

- 1.— GATE
- 2.— COLLECTOR
- 3.— EMITTER
- 4.— COLLECTOR

DIODES

- 1.— ANODE/OPEN
- 2.— CATHODE
- 3.— ANODE

TO-247AC Part Marking Information

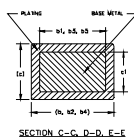
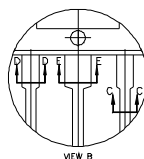
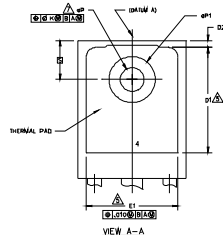
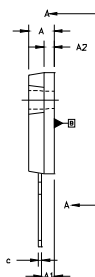
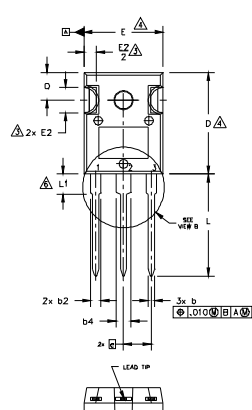


TO-247AC package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

TO-247AD Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. ϕP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AD.

SYMBOL	DIMENSIONS				NOTE
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	4
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	4
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	4
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	
D1	.515	—	13.08	—	5
D2	.020	.053	0.51	1.36	4
E	.602	.625	15.29	15.87	
E1	.530	—	13.46	—	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		4
ek	.010		0.25		
L	.780	.827	19.57	21.00	4
L1	.146	.169	3.71	4.29	
L2	.140	.144	3.56	3.66	
ep1	—	.291	—	7.39	
O	.209	.224	5.31	5.69	4
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

1. - GATE
2. - DRAIN
3. - SOURCE
4. - DRAIN

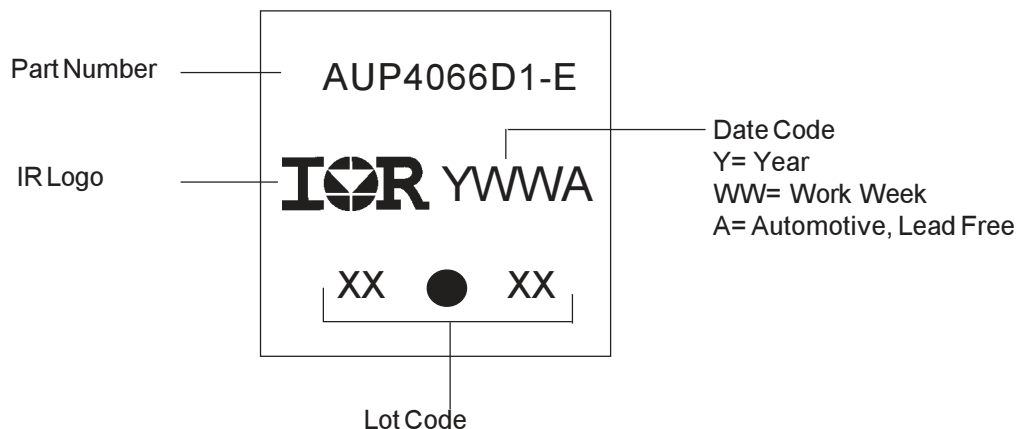
IGBTs, CoPACK

1. - GATE
2. - COLLECTOR
3. - EMITTER
4. - COLLECTOR

DIODES

1. - ANODE/OPEN
2. - CATHODE
3. - ANODE

TO-247AD Part Marking Information



TO-247AD package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Ordering Information

Base part number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIRGP4066D1	TO-247AC	Tube	25	AUIRGP4066D1
AUIRGP4066D1-E	TO-247AD	Tube	25	AUIRGP4066D1-E

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Tel: (310) 252-7105

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