

# DC Impedance-Model-Based Resonance Analysis of a VSC-HVDC System

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**Abstract**—Resonances can have negative impact on a Voltage Source Converter-High Voltage DC (VSC-HVDC) system. This paper develops dc impedance models for the rectifier and inverter stations for a VSC-HVDC system when they are viewed from a dc terminal. The impedance models take converter controllers into account. The derived impedance models are validated by comparing frequency responses of the analytical model and the impedance measured at the dc terminal from a detailed VSC-HVDC model simulated in a real-time digital simulator. Resonances are examined in frequency domain (e.g., Bode plots and Nyquist plots) using the derived analytical impedance models. The analysis is verified by time-domain simulations. Real-time digital simulation in RT-Lab demonstrates that the dc capacitor has a significant impact on resonances while power transfer level has an insignificant impact on resonances.

**Index Terms**—Admittance, impedance, resonance, VSC-HVDC.

## I. INTRODUCTION

**R**esonances in line commutating converter (LCC)-HVDC systems have been studied in [1]–[3] in the previous decades. VSC-HVDC is becoming a preferred transmission solution to integrate renewable energy sources, especially offshore wind farms [4]–[8]. Since a VSC-HVDC system is a hybrid system which consists of ac and dc parts, the harmonic resonances can impact both sides but may have different characteristics. Normally, high frequency harmonic resonances exist on both ac and dc sides, which are generated by the high frequency switching IGBTs and can be eliminated by filters. However, there are some low frequency resonances due to the interactions between an ac grid and a grid-connected converter [9]–[13] or the interactions between a dc grid and a dc/ac converters, e.g., in an electric propulsion system [14].

The harmonic resonances in VSC interfaced ac grids have been examined in [9]–[13]. In addition, subsynchronous resonances due to the interaction of a VSC and a series compensated ac network are examined in [15], [16]. Most recently, the authors have published a paper [17] with a comprehensive examination of both the ac systems (the rectifier side and the inverter side) of a VSC-HVDC system. Impedance models for the two ac systems were derived and used for resonance analysis. However, a comprehensive dc impedance based analysis on the dc system while taking both rectifier and inverter stations into account has not been seen in the literature. This paper will address this topic.

The VSC-HVDC system can be implemented in various different converter topologies. Among those topologies, two-level converters, three-level converters and modular multilevel converters (MMC) are three topologies with most interest. At the ac side of the VSC-HVDC system, the most significant harmonics would be around the switching frequency (1.6 kHz) for two-level converters. For three-level converters, the harmonic frequency will be double of the switching frequency. The current waveforms have significant improvement for MMC topology, and the most significant harmonic is always higher than two-level and three-level converters, and would depend on the number of converter modules in each leg.

In our study of ac-side resonance analysis [17], the resonance frequencies discovered are at a low frequency range far away from the switching frequencies, such as below 200 Hz. This implies that the topology has limited impacts on ac-side resonances.

The dc-impedance modeling depends on the topology of the dc-side. Topology variation will make a difference. For a three-level converter topology, the dc side is similar to that of two-level converters. However, the neutral point voltage clamp structure brings additional unique inherent voltage variations compared to two-level converters. The neutral point voltage varies at three times of the fundamental frequency [18]. This harmonic frequency is in a close range of the resonance frequencies discovered in this project. Therefore, consideration of the neutral point voltage harmonic should be considered when studying three-level converter based HVDC.

Instead of using a single or two capacitors, the MMC topology consists of a large number of submodules and each module has a capacitor. The equivalent dc capacitor is now a series connection of various capacitors [19], [20]. Furthermore, the series number is not a constant and depends on the switching state of each submodule. That characteristic would impose high frequency voltage oscillations on dc side and requires additional investigation. **In dynamic analysis, an equivalent dc capacitor can be used to simulate the series of submodule capacitors [20]. The dc-capacitor dynamics are modified with additional oscillating terms.**

This paper will focus on the two-level converter topology which has a single capacitor on the dc side. **The results from this paper are valid for MMC-HVDC if the dc-bus voltage ripples are insignificant. If the ripples are significant, then additional investigation is required to re-derive the dc-bus dynamics and include the dynamics into the dc-impedance model.**

In order to understand resonances in electrical systems, impedance or admittance model based analysis, a feasible

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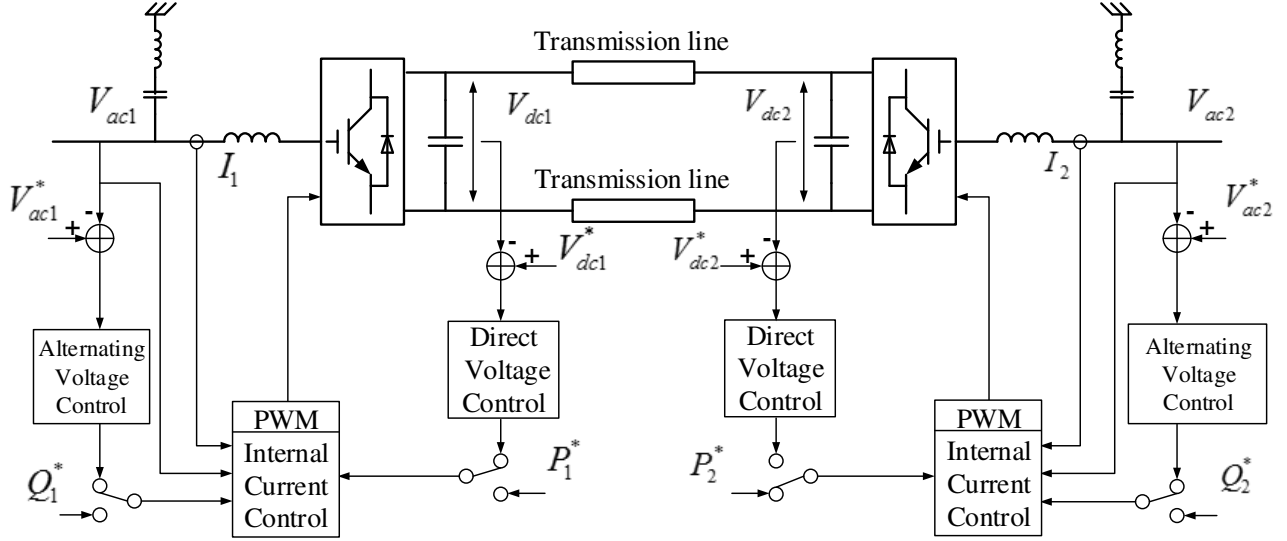


Fig. 1. A two-terminal VSC-HVDC system.

tool as indicated in [21], will be adopted. The impedance or admittance models of ac grid interfaced inverters are developed in [11]–[13]. The authors developed impedance models for both rectifier and inverter stations for a VSC-HVDC system in [17]. In addition, impacts of a feed-forward filter, power level and ac line length on resonances are analyzed and validated via time-domain simulations.

The above mentioned models are from the ac side's point of view. Therefore, the analysis only examines resonance issues in the ac systems. The factors affecting ac side resonances such as control loops, feed-forward filter and power transfer level may have different impact on dc systems. To be able to examine resonances in the dc systems, dc impedance models will be developed in this paper.

DC impedance modeling for converters focuses on single converter and machine drive applications in the literature [14], [22], [23]. In addition, few papers have presented dc impedance models with the effect of converter controls included. For example, Sudhoff *et al* in [14] derived a dc impedance model for a dc/ac converter, where the converter is assumed as a constant power load and the incremental impedance is a negative resistance. In a more recent paper [23], the dc admittance model is developed for a dc/ac converter interfaced permanent-magnet synchronous motor (PMSM). PMSM dynamics are included in the model. However, the converter control dynamics are neglected.

For a VSC-HVDC system, at least two converter stations exist and the control mechanism for each station is different, which implies that the dc impedance models may have different characteristics for each station. Therefore, a comprehensive analysis of dc impedance modeling of a VSC-HVDC system is required to better understand the dc system resonances. In this paper, dc resonance issues will be investigated for a two-terminal VSC-HVDC system. Typical VSC-HVDC controls and a practical dc transmission line will be assumed. Frequency-domain analysis will be applied to examine the characteristics of the derived dc impedance models. The mod-

els will be verified by comparing their frequency responses with the frequency responses obtained from a detailed VSC-HVDC system simulated in a real-time digital simulator. Real-time digital simulations will also be used to validate the analysis results. In the sections that follow, the paper first presents the dc impedance models derivation for both stations of a VSC-HVDC system including controller dynamics in Section II. The derived dc impedance models are verified and resonances are investigated by analysis and real-time digital simulation in Section III. The paper is concluded in Section IV.

## II. IMPEDANCE MODEL DERIVATION

To derive an impedance model seen from the dc terminal, three key relationship equations are used and they are:

- 1) the relationship between the alternating current and alternating voltage of the grid network;
- 2) the relationship between the alternating voltage and current of the VSC. We will give the relationship based on our research work on the ac side of VSC systems in [17];
- 3) the power conservation relationship of the dc side and the ac side of a converter. From this relationship, we can find the relationship between the direct voltage/current and the alternating voltage/current. Further, implementing the knowledge from 1) and 2), we can derive the dc impedance observed from the dc terminal.

In the following subsections, Subsection II-A will give the first relationship in (2) and (3). Subsection II-B will give the dc/ac power balance relationship and its implication. Subsection II-C will use a rectifier converter as an example to give the second relationship. Subsection II-D follows to give an inverter converter example.

### A. Network Model

A two-terminal VSC-HVDC transmission system is shown in Fig. 1. The basic controllers for the rectifier and inverter

stations are depicted in Fig. 1. Since the structure of both stations are identical, each station could operate at either rectifier or inverter mode. Normally, the rectifier station controls the amount of active power transfer, and the inverter station controls DC-link voltage in order to keep power transfer balance. Both stations are able to compensate reactive power to AC grid by directly injecting reactive power or control the AC grid voltage.

An equivalent model of a VSC connecting with an AC voltage source via an inductor is shown in Fig. 2. The alternating voltage source is represented by an ideal voltage source  $v_s$  in series with an impedance  $Z_g(s)$ . The PCC voltage is then represented by  $E$ . The equivalent output voltage (average voltage) of the VSC is called  $v$ . At the DC side of VSC, the DC-link voltage and current are represented by  $v_{dc}$  and  $i_{dc}$ . The capacitor  $C_{dc}$  is used to stabilize the DC voltage, while  $i_{dc1}$  is the net current flowing to the other station. (1) describes the voltage and current relationship between grid and converter in  $dq$  frame. The letter with upper-line represents complex space vector, such as  $\bar{v} = v_d + jv_q$  and  $\bar{i} = i_d + ji_q$ . The angular speed within grid reference frame is  $\omega_1$ , which is a constant throughout this paper.

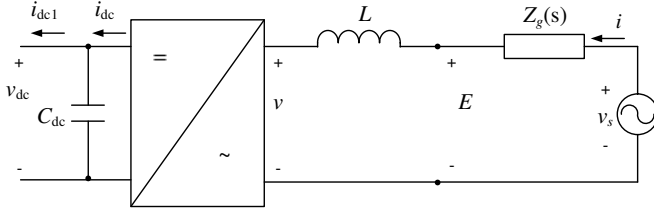


Fig. 2. A model of VSC and grid.

$$L \frac{d\bar{i}}{dt} + j\omega_1 L \bar{i} = \bar{E} - \bar{v} \quad (1)$$

The above equation can be written in the vector and matrix form. Let  $v_{dq} = [v_d \ v_q]^T$  and  $i_{dq} = [i_d \ i_q]^T$ , and  $E_{dq} = [E_d \ E_q]^T$ , and expressing the equation in Laplace domain, we have:

$$E_{dq} = v_{dq} + Z_l(s) i_{dq}, \quad (2)$$

$$\text{where } Z_l(s) = \begin{bmatrix} sL & -\omega_1 L \\ \omega_1 L & sL \end{bmatrix}.$$

Similarly, if we know the impedance matrix of the network  $Z_g(s)$ , we can write another network equation:

$$E_{dq} = v_{s,dq} - Z_g(s) i_{dq}, \quad (3)$$

$$\text{where } Z_g(s) = \begin{bmatrix} r_g + sL_g & -\omega_1 L_g \\ \omega_1 L_g & r_g + sL_g \end{bmatrix}.$$

1) *PCC Voltage Alignment and the Implication*: If we assume that the  $d$ -axis is aligned with the PCC voltage, then we have the following assumption:  $E_q = 0$ . The phase-locked-loop (PLL) in the controller tracks the phase of phase A voltage at PCC. The phase information is then applied for  $abc$ - $dq$  transformation. Throughout this paper, we neglect the impact of PLL dynamics. From this assumption and the

relationship presented in (3), we have the following equation for the  $q$ -axis:

$$0 = v_{sq} - \omega_1 L_g i_d - (r_g + sL_g) i_q. \quad (4)$$

The network voltage keeps a constant magnitude, i.e.,

$$v_{sd}^2 + v_{sq}^2 = \text{constant}.$$

Linearizing this equation will lead to:

$$v_{sd0} \Delta v_{sd} + v_{sq0} \Delta v_{sq} = 0 \Rightarrow \Delta v_{sd} = -\frac{v_{sq0}}{v_{sd0}} \Delta v_{sq}. \quad (5)$$

Based on (5) and (4), we can derive the relationship between the source voltage and the current as follows.

$$\begin{bmatrix} \Delta v_{sd} \\ \Delta v_{sq} \end{bmatrix} = \begin{bmatrix} -\frac{v_{sq0}}{v_{sd0}} \omega_1 L_g & -\frac{v_{sq0}}{v_{sd0}} (r_g + sL_g) \\ \omega_1 L_g & r_g + sL_g \end{bmatrix} \begin{bmatrix} \Delta i_d \\ \Delta i_q \end{bmatrix} \quad (6)$$

With the relationship in (6), we can find the expression of  $\Delta E_d$  in terms of the ac currents:

$$\begin{aligned} \Delta E_d &= \Delta v_{sd} - (r_g + sL_g) \Delta i_d + \omega_1 L_g \Delta i_q \\ &= \underbrace{\left[ -\frac{v_{sq0}}{v_{sd0}} \omega_1 L_g - r_g - sL_g \quad -\frac{v_{sq0}}{v_{sd0}} (r_g + sL_g) + \omega_1 L_g \right]}_{G_{Edi}} \begin{bmatrix} \Delta i_d \\ \Delta i_q \end{bmatrix} \end{aligned} \quad (7)$$

It is also possible to express the converter alternating voltage  $\Delta v_{dq}$  in terms of  $\Delta i_{dq}$  combining (6) and the network relationship in (2) and (3).

$$\begin{aligned} \Delta v_{dq} &= \Delta v_{s,dq} - (Z_l(s) + Z_g(s)) \Delta i_{dq} \\ &= \underbrace{\left[ \begin{array}{cc} -\frac{v_{sq0}}{v_{sd0}} \omega_1 L_g - r_g - s(L + L_g) & -\frac{v_{sq0}}{v_{sd0}} (r_g + sL_g) + \omega_1 (L + L_g) \\ -\omega_1 L & -sL \end{array} \right]}_{Z_{ac,net}} \Delta i_{dq} \end{aligned} \quad (8)$$

## B. DC/AC Power Conservation Relationship

Assuming that there is no loss due to switches, the instantaneous power at the ac side should equal to the instantaneous power at the dc side as shown in (9). Linearizing (9) and rearranging the equation leads to the relation between  $\Delta v_{dc}$  and  $\Delta i_{dc}$  in (10). The variables  $v_{dq}$  and  $i_{dq}$  are ac side quantities, which implies that the derivation should involve both dc and ac side. Hence, in order to get an expression of the dc impedance ( $\frac{\Delta v_{dc}}{\Delta i_{dc}}$ ), the ac side variables ( $\Delta v_{dq}$  and  $\Delta i_{dq}$ ) have to be expressed in terms of  $\Delta v_{dc}$  and  $\Delta i_{dc}$ .

$$v_{dc} i_{dc} = v_d i_d + v_q i_q \quad (9)$$

$$\begin{bmatrix} i_{dc0} \\ v_{dc0} \end{bmatrix}^T \begin{bmatrix} \Delta v_{dc} \\ \Delta i_{dc} \end{bmatrix} = \begin{bmatrix} i_{d0} \\ i_{q0} \end{bmatrix}^T \Delta v_{dq} + \begin{bmatrix} v_{d0} \\ v_{q0} \end{bmatrix}^T \Delta i_{dq} \quad (10)$$

Equation (10) can be simplified considering the relationship between converter voltage  $\Delta v_{dq}$  and the ac current  $i_{dq}$  in (8).

$$\begin{bmatrix} i_{dc0} \\ v_{dc0} \end{bmatrix}^T \begin{bmatrix} \Delta v_{dc} \\ \Delta i_{dc} \end{bmatrix} = \underbrace{\left( \begin{bmatrix} i_{d0} \\ i_{q0} \end{bmatrix}^T Z_{ac,net} + \begin{bmatrix} v_{d0} \\ v_{q0} \end{bmatrix}^T \right)}_{G_{da}(s)} \Delta i_{dq}. \quad (11)$$

## C. Rectifier Station

In this subsection, the ac side of the rectifier will be discussed.

1) *Current Control*: The rectifier station controls the amount of active power transferred to the inverter station and the alternating voltage. The control system of rectifier stations is shown in Fig. 3, where  $P$  is the measured active power sent to inverter station. There are two control loops in Fig. 3, the outer loop controls the active power transfer and grid alternating voltage. The outer control loop generates the reference of  $dq$ -axis currents. The inner control loop regulates the  $dq$ -axis currents and tracks the respective references obtained from the outer control loop. The analysis of the current control is identical to the ac impedance modeling in [17] and the details will be skipped. The current  $i_{dq}$  can be expressed as (12).

$$i_{dq} = \underbrace{\begin{bmatrix} g_c(s) & 0 \\ 0 & g_c(s) \end{bmatrix}}_{G_c(s)} i_{\text{ref}} + \underbrace{\begin{bmatrix} y_i(s) & 0 \\ 0 & y_i(s) \end{bmatrix}}_{Y_i(s)} E_{dq} \quad (12)$$

where  $i_{dq}$ ,  $i_{\text{ref}}$  and  $E_{dq}$  are vectors of  $d$ -axis and  $q$ -axis variables, and

$$\begin{cases} g_c(s) = \frac{k_p s + k_i}{L s^2 + k_p s + k_i} \\ y_i(s) = \frac{s^2(s + 2\xi\omega_0)}{(L s^2 + k_p s + k_i)(s^2 + 2\xi\omega_0 s + \omega_0^2)} \end{cases} \quad (13)$$

The parameters in (13) can be found in the current  $PI$  controller  $F_c(s) = k_p + \frac{k_i}{s}$  and the second-order filter  $F_{2nd}(s) = \frac{\omega_0^2}{s^2 + 2\xi\omega_0 s + \omega_0^2}$ , which is used to feed forward the measured  $PCC$  voltage  $E_d$  and  $E_q$ . The cut-off frequency  $\omega_0$  is chosen at 1000 Hz and damping factor  $\xi$  is  $\frac{1}{\sqrt{2}}$ .

2) *Power Control*: The power conversion efficiency of IGBTs within a two-level VSC-HVDC system is around 98%, and the efficiency increases to 99.5% for a MMC topology [24]. Hence, the active power loss on the IGBTs within a switching station can be neglected. The measured active power can also be expressed as  $P = v_{dc} i_{dc}$ . However, the damping in the system would be lower than the real system during analysis because of the neglecting of power loss. From Fig. 3, the  $d$ -axis current reference can be expressed as (14), where  $F_p(s) = k_{p-p} + \frac{k_{i-p}}{s}$  is the  $PI$  controller.

$$i_{d\_ref} = (P_{\text{ref}} - v_{dc} i_{dc}) F_p(s) \quad (14)$$

Linearizing (14) yields (15).

$$\Delta i_{d\_ref} = [-i_{dc0} F_p(s) \quad -v_{dc0} F_p(s)] \begin{bmatrix} \Delta v_{dc} \\ \Delta i_{dc} \end{bmatrix} \quad (15)$$

The  $q$ -axis current reference can be expressed as (16), where  $F_{ac}(s) = k_{p-ac} + \frac{k_{i-ac}}{s}$  is the  $PI$  controller to track the  $PCC$  voltage magnitude.

$$i_{q\_ref} = (E_{d\_ref} - E_d) F_{ac}(s) \quad (16)$$

Linearizing (16) yields (17).

$$\Delta i_{q\_ref} = -F_{ac}(s) \Delta E_d. \quad (17)$$

Combining (15), (17), and (7) yields:

$$\begin{bmatrix} \Delta i_{d\_ref} \\ \Delta i_{q\_ref} \end{bmatrix} = \underbrace{-F_{ac}(s) \begin{bmatrix} G_{Edi} \\ 0 \end{bmatrix}}_{G_{p1}} \Delta i_{dq} + \underbrace{F_p(s) \begin{bmatrix} -i_{dc0} & -v_{dc0} \\ 0 & 0 \end{bmatrix}}_{G_{p2}} \begin{bmatrix} \Delta v_{dc} \\ \Delta i_{dc} \end{bmatrix} \quad (18)$$

Combining (12), (18) and (7), we have:

$$\Delta i_{dq} = \underbrace{\left( I - G_c G_{p1} - Y_i \begin{bmatrix} G_{Edi} \\ 0 \end{bmatrix} \right)^{-1}}_{M_{i\_dc}(s)} G_c G_{p2} \begin{bmatrix} \Delta v_{dc} \\ \Delta i_{dc} \end{bmatrix}. \quad (19)$$

Now applying the power conservation relationship by combining (19) and (11), the relationship between the direct voltage and the direct current can be found:

$$\begin{bmatrix} i_{dc0} \\ v_{dc0} \end{bmatrix}^T \begin{bmatrix} \Delta v_{dc} \\ \Delta i_{dc} \end{bmatrix} = \underbrace{G_{da}(s) M_{i\_dc}(s)}_{M(s)} \begin{bmatrix} \Delta v_{dc} \\ \Delta i_{dc} \end{bmatrix} = \begin{bmatrix} M_1(s) & M_2(s) \end{bmatrix} \begin{bmatrix} \Delta v_{dc} \\ \Delta i_{dc} \end{bmatrix}. \quad (20)$$

Finally we can have the impedance as:

$$Z_{dc}(s) = -\frac{v_{dc0} - M_2(s)}{i_{dc0} - M_1(s)}. \quad (21)$$

Remarks: Fig. 4 shows the Bode plots of the dc impedance model of the rectifier station with two different grid impedances. The blue trace is the Bode plot with grid impedance of 18.8 mH, and the green trace is the Bode plot with grid impedance of 1.88 mH. Other system parameters can be found in Appendix Tables III, IV, and V. The detailed Bode plot in Fig. 5 demonstrates the impact of grid impedance on dc impedance model is negligible. When the AC system has a low short circuit ratio (SCR), the system becomes unstable. DC impedance-model-based analysis cannot detect the instability. Instead, impedance-model-based analysis for the AC system, as presented in [17], can be used to detect the instability.

Therefore, the simplifying assumption for analyzing DC impedance is that the ac system is well-controlled and remains stable.

#### D. Inverter Station

The inverter station controls dc-link voltage and ensures power transfer balance. Fig. 6 shows control of the inverter station. The only difference between rectifier station is the generation of  $d$ -axis current reference where the dc-link voltage is measured and fed back to the controller, and the error from the reference value is sent to a  $PI$  controller to generate the  $d$ -axis current reference.

Therefore, the  $d$ -axis current reference can be expressed as (22).

$$i_{d\_ref} = (V_{dc\_ref} - v_{dc}) F_{dc}(s), \quad (22)$$

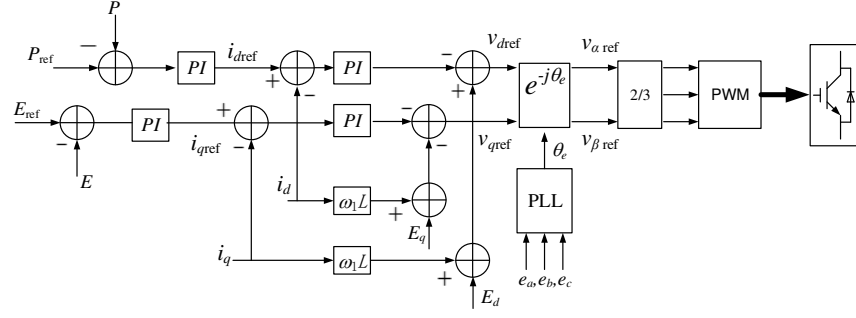


Fig. 3. Control of the rectifier station.

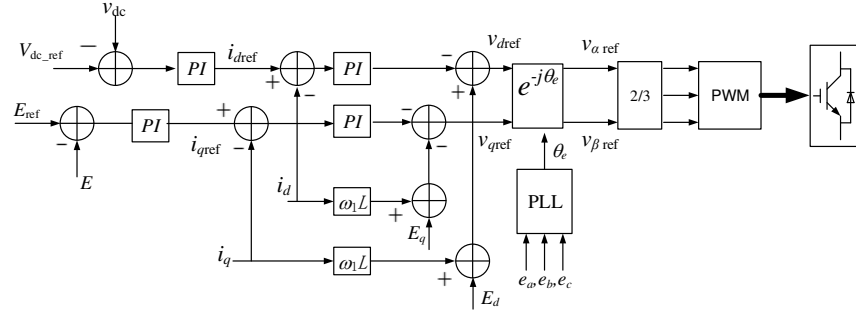


Fig. 6. Control of the inverter station.

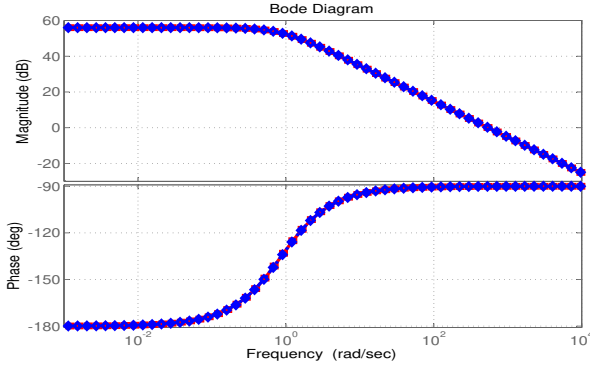


Fig. 4. Bode plots of dc impedance model of rectifier station with different grid impedances (1.88 mH and 18.8 mH). The two plots are seen all together in this Bode plot figure.

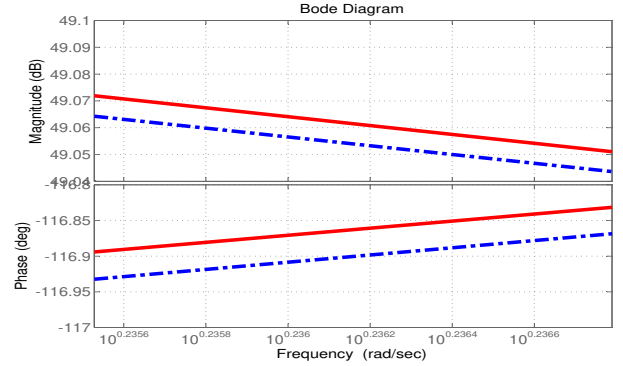


Fig. 5. Detailed Bode plots of dc impedance model of rectifier station with different grid impedance (1.88 mH and 18.8 mH). Here slight difference is shown.

where  $F_{dc}(s)$  is the transfer function of the voltage controller. Linearizing (22) yields the expression of  $\Delta i_{d\_ref}$  as follows.

$$\Delta i_{d\_ref} = \begin{bmatrix} 0 & 0 \end{bmatrix} \begin{bmatrix} \Delta i_d \\ \Delta i_q \end{bmatrix} + \begin{bmatrix} -F_{dc}(s) & 0 \end{bmatrix} \begin{bmatrix} \Delta v_{dc} \\ \Delta i_{dc} \end{bmatrix} \quad (23)$$

Since the inverter station controller also controls ac grid voltage, (16) can be used to describe the  $q$ -axis current reference for the inverter station. Combining (23) and (17) yields:

$$\begin{bmatrix} \Delta i_{d\_ref} \\ \Delta i_{q\_ref} \end{bmatrix} = G_{p1} \Delta i_{dq} + G_{p2} \begin{bmatrix} \Delta v_{dc} \\ \Delta i_{dc} \end{bmatrix}, \quad (24)$$

where  $G_{p1}$  is the same as that in (18) and the new  $G_{p2}$  is

shown in (25).

$$G_{p2} = \begin{bmatrix} -F_{dc}(s) & 0 \\ -\frac{i_{dc0} F_{ac}(s)}{i_{d0}} & -\frac{v_{dc0} F_{ac}(s)}{i_{d0}} \end{bmatrix} \quad (25)$$

The inner current controller structure is identical with that in the rectifier station. Hence, the derivation of impedance model for inverter station can be implemented as the approach shown for rectifier station. Therefore, (21) can be used to calculate the dc impedance for inverter station as well.

### III. RESONANCE ANALYSIS

#### A. Impedance Model Verification

A two-terminal VSC-HVDC system is built in Matlab/Simulink via SimPowerSystems toolbox. The system pa-



rameters and controller settings are listed in Appendix Tables III, IV, and V. In order to verify the dc impedance models derived in Section II, the system was first divided into two isolated parts: a rectifier station and an inverter station.

Fig. 7 shows the setup for the rectifier impedance verification, where the 250 kV dc voltage source is emulating an ideal inverter station. A constant magnitude variable frequency sinusoidal alternating voltage is superimposed to the dc source. The magnitude is set at 5 kV (2% of the dc source magnitude), and the frequency  $f_{sm}$  varies from 1 Hz to 1000 Hz. The dc voltage  $v_{dc}$  and current  $i_{dc}$  are measured and fed into two discrete Fourier transformation blocks. The impedance of the rectifier station at certain frequency then can be expressed as  $Z_{rec}(f_{sm}) = \frac{\Delta V_{dc}(f_{sm})}{\Delta I_{dc}(f_{sm})}$ . The verification setup in Fig. 7 contains a dc capacitor  $C_{dc}$ . However, the derivation in Section II does not take the capacitor into account. Therefore, the complete dc impedance can be found in (26).

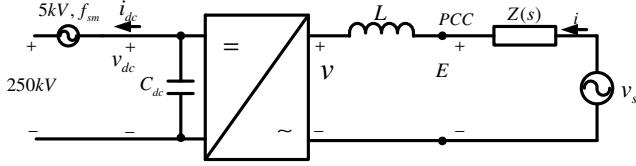


Fig. 7. Rectifier station impedance verification setup.

$$Z_{rec}(s) = \frac{Z_{dc}(s)}{1 + sC_{dc}Z_{dc}(s)} \quad (26)$$

The inverter station verification setup is depicted in Fig. 8, where a dc cable is included. Instead of a 250 kV dc voltage source, a constant dc voltage source with 251 kV is used to emulate an ideal rectifier station. Based on the dc cable parameters, the inverter station will regulate the dc voltage at 250 kV, and the active power sent to inverter station is fixed at 100 MW. A 5 kV variable frequency sinusoidal alternating voltage source is superimposed and is used to calculate the dc impedance of inverter station. Since the dc cable is taken into account, the complete dc impedance of inverter station is (27).

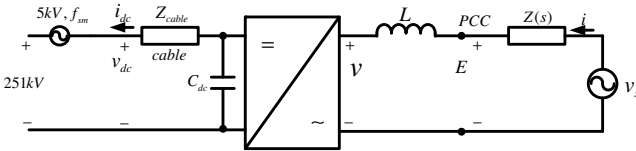


Fig. 8. Inverter station impedance verification setup.

$$Z_{inv}(s) = \frac{Z_{dc}(s)}{1 + sC_{dc}Z_{dc}(s)} + Z_{cable}(s) \quad (27)$$

Fig. 9 shows the verification results of the dc impedance for the rectifier station. The rectifier station is set to send 100 MW constant active power to the dc voltage source. In Fig. 9, the solid trace is the Bode plot of the dc impedance of rectifier station computed via (26), while the discrete squares are the measured dc impedance of rectifier station shown in Fig. 7.

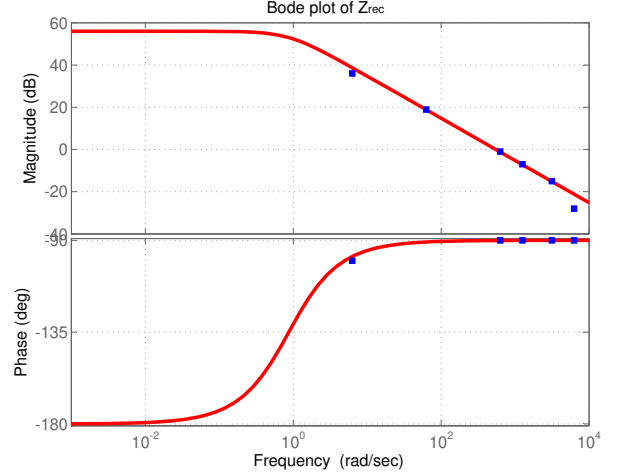


Fig. 9. Bode plot of the dc impedance of the rectifier station.

The following example explains the details of measurement-based impedance extraction procedure. we intentionally impose a 5 kV sinusoidal voltage source with a frequency of 100 Hz on the 250 kV dc voltage source. The ripple parts of dc voltage  $\Delta v_{dc}$  and dc current  $\Delta i_{dc}$  are measured for analysis. The “Discrete Fourier” block in SimPowerSystems toolbox can be used to extract the magnitude and phase of  $\Delta v_{dc}$  and  $\Delta i_{dc}$  at a fundamental frequency (100 Hz). Hence, the dc impedance magnitude is the magnitude ratio of  $\Delta v_{dc}$  and  $\Delta i_{dc}$ , and the dc impedance phase is the phase difference between  $\Delta v_{dc}$  and  $\Delta i_{dc}$ . For the rectifier station verification simulation in Fig. 7, the magnitude ratio of  $\Delta v_{dc}$  and  $\Delta i_{dc}$  is -1.2 dB, and the phase difference between  $\Delta v_{dc}$  and  $\Delta i_{dc}$  is  $-91^\circ$ . Respectively, for the inverter station verification simulation in Fig. 8, the magnitude ratio of  $\Delta v_{dc}$  and  $\Delta i_{dc}$  is 29.3 dB, and the phase difference between  $\Delta v_{dc}$  and  $\Delta i_{dc}$  is  $84.3^\circ$  at 100 Hz. Other frequencies from 1 Hz to 1000 Hz are used to verify the dc impedance model in a broad range.

The results verify a close match obtained and therefore validate the derivation of the dc impedance in Section II. The dc impedance below 1 Hz is not measured since lower frequency components are not easy to be extracted from the large 250 kV dc voltage.

Fig. 10 demonstrates the comparison between the analytical and measured dc impedances for the inverter station. A reasonable agreement can be found for frequencies from 1 Hz to 1000 Hz which validates the inverter dc impedance derivation in Section II.

### B. DC system resonance analysis

1) *Impact of dc capacitor:* Once the dc impedances of rectifier and inverter stations are obtained via (26) and (27), the dc current can be computed as (28)

$$i_{dc}(s) = (v_{dc\_rec}(s) - v_{dc\_inv}(s)) \frac{Y_{rec}(s)}{1 + Y_{rec}(s)Z_{inv}(s)} \quad (28)$$

where  $v_{dc\_rec}$  and  $v_{dc\_inv}$  are the dc terminal voltages of the rectifier and inverter stations respectively. Therefore, in-

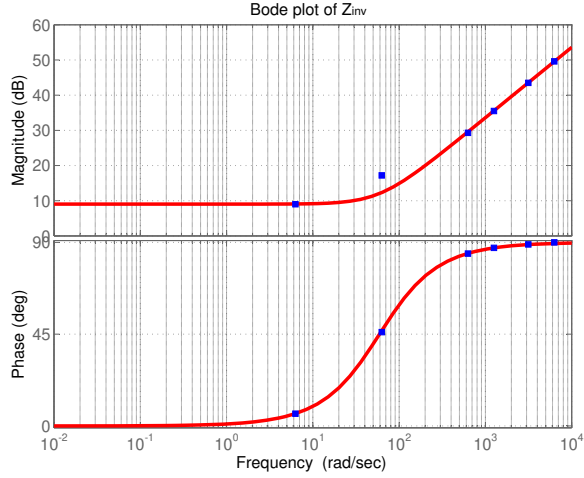


Fig. 10. Bode plot of the dc impedance of the inverter station.

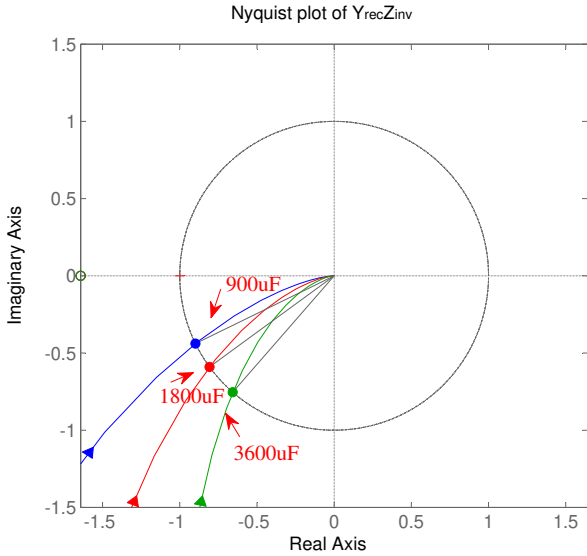


Fig. 11. Nyquist plots of  $Y_{rec}Z_{inv}$ .

vestigating the loop gain  $Y_{rec}Z_{inv}$  can predict dc current characteristics [11], [12], [21].

Fig. 11 demonstrates the Nyquist plots of  $Y_{rec}Z_{inv}$  with different dc capacitor selections, which indicates the impact of the capacitor size on dc current resonance frequencies. The points where the Nyquist traces cross the unit circle indicate the resonance frequencies. For instance, the resonance frequency is 27.7 Hz for 900  $\mu\text{F}$  capacitor, while the resonance frequencies are 18.8 Hz and 12.0 Hz for 1800  $\mu\text{F}$  and 3600  $\mu\text{F}$  respectively. Hence, the resonance frequency decreases while the capacitance increases. The phase margin also increases, **indicating improvement in stability** while the capacitance increases. Table I shows the resonance frequencies and phase margins for different capacitor sizes.

A two-terminal VSC-HVDC model is built in RT-Lab real time digital simulator environment. The RT-Lab real-time digital simulator is a high performance computing platform

TABLE I  
COMPARISON BETWEEN DIFFERENT CAPACITOR SIZES

Capacitance	Resonance frequency (Analysis/Simulation)	Phase margin
900 $\mu\text{F}$	27.7 Hz/28.5 Hz	26°
1800 $\mu\text{F}$	18.8 Hz/19.5 Hz	36.2°
3600 $\mu\text{F}$	12.0 Hz/14.25 Hz	48.9°

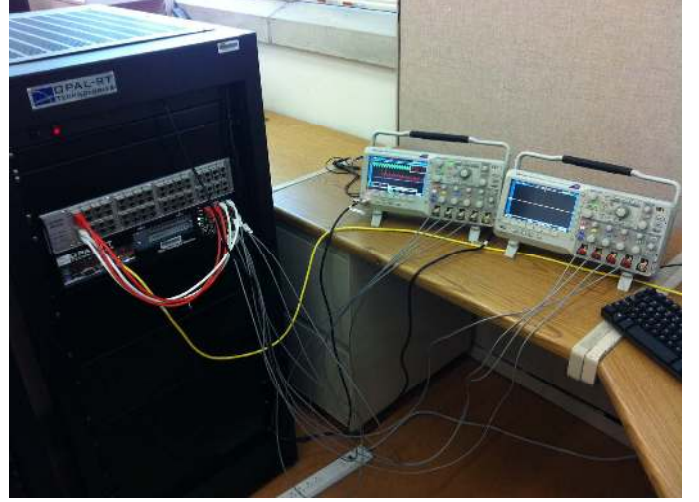


Fig. 12. Real-time digital simulation setup using RT-Lab.

developed by OPAL-RT Technologies, which can simulate power system and power electronics detailed models at real time. Therefore, it can provide precise simulation results and take the switching details of IGBTs into account. Fig. 12 shows the setup of a RT-Lab simulator and the oscilloscopes that monitor simulation signals, such as voltage, current and power.

In the simulation model, the rectifier station is set to send 100 MW active power to the inverter station, and the dc-link voltage is set at 250 kV. The dc capacitor **is varied** to examine the dc current resonance and comparing with the analysis results in Fig. 11. Fig. 13 shows the simulation results for 900  $\mu\text{F}$  capacitor case. For the measurement system in this simulation, power, voltage and current are measured in per unit system, and are displayed on oscilloscope in Volts. For this case, 1V (1pu) represents 100 MW for power, and it also represents 400 A for current and 250 kV for voltage.

Fig. 13 presents the dc current and its discrete Fourier transform (DFT) analysis results. The mean value of the dc current is 1.12 pu. The DFT analysis shows the highest harmonic is at 28.5 Hz and is very close to 27.7 Hz indicated through Nyquist plots in Fig. 11.

Figs. 14 and 15 are the simulation results of 1800  $\mu\text{F}$  and 3600  $\mu\text{F}$  cases. The highest harmonics are at 19.5 Hz and 14.25 Hz respectively. Comparing with the analysis in Fig. 11, a reasonable agreement can be found. According to Table I, phase margin decreases as capacitor sizes becoming smaller. This phenomenon is demonstrated in current ripple magnitudes. With the size increasing, the current ripple magnitudes found in Figs. 13, 14, 15 decrease. The time-domain simulation results verify the analysis.

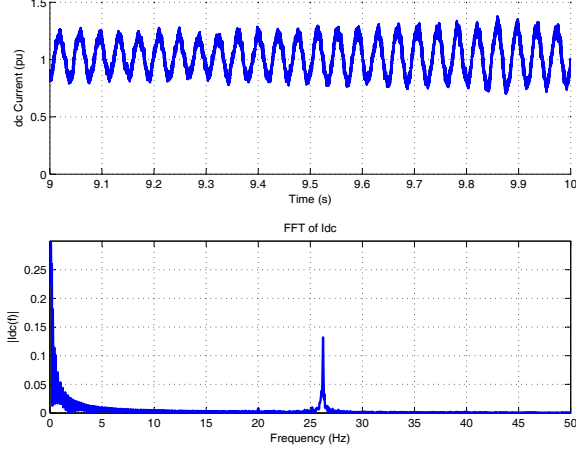


Fig. 13. Simulation results of 900  $\mu\text{F}$  capacitor.

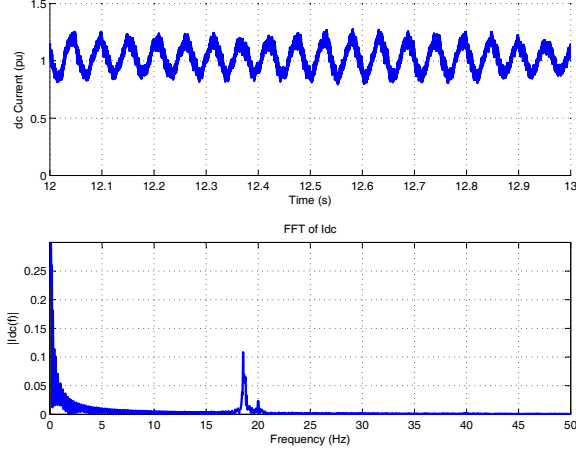


Fig. 14. Simulation results of 1800  $\mu\text{F}$  capacitor.

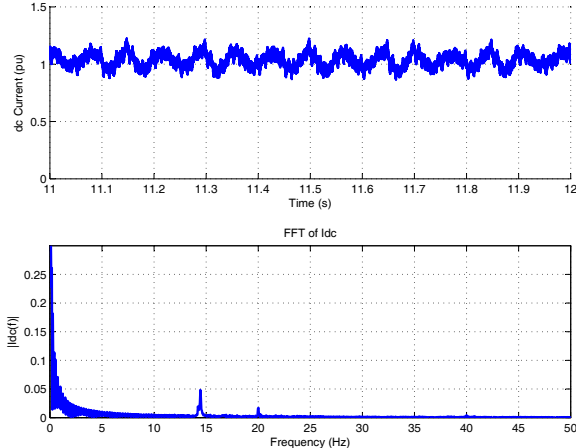


Fig. 15. Simulation results of 3600  $\mu\text{F}$  capacitor.

2) *Impact of power level:* Fig. 16 shows the Nyquist plot of  $Y_{\text{rec}}Z_{\text{inv}}$  at different power levels. The dc capacitor is chosen at 1800  $\mu\text{F}$ . Active power transferred to the inverter station is tested at 100 MW, 200 MW and -100 MW (reverse power flow). The resonance frequency for each power level is almost the same on the Nyquist plot. Table II shows the resonance frequencies and phase margins for different power levels. Although higher power transfer level makes the phase margin decrease small amount, the impact on dc system stability can be neglected.

Figs. 17 and 18 show the real-time simulation results for 200 MW and -100 MW cases. The DFT analysis of dc current indicates resonance frequencies are 20 Hz and 19.5 Hz, which are very close to the 100 MW case shown in Fig. 14.

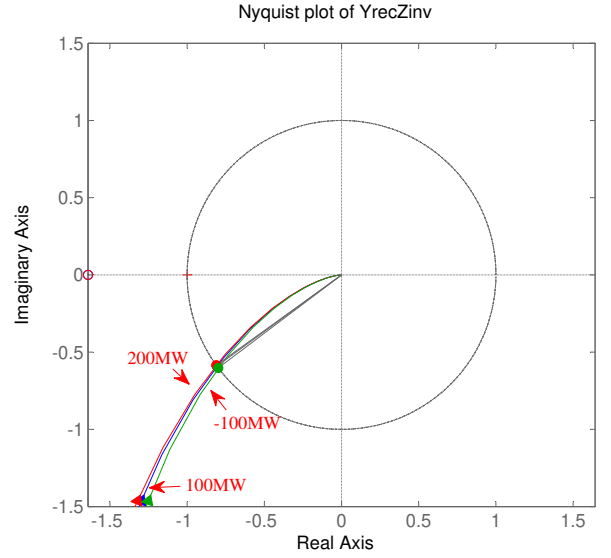


Fig. 16. Nyquist plots of dc current characteristics at different power levels.

TABLE II  
COMPARISON BETWEEN DIFFERENT POWER LEVELS

Power level	Resonance frequency (Analysis/Simulation)	Phase margin
100 MW	18.8 Hz/19.5 Hz	35.8°
200 MW	18.8 Hz/20 Hz	36.2°
-100 MW	18.8 Hz/19.5 Hz	37°

#### IV. CONCLUSION

DC system resonance in a VSC-HVDC system is investigated in this paper. A frequency-domain impedance model is developed by taking the dynamics of the rectifier and the inverter controls into consideration. Nyquist stability analysis is applied to examine resonance characteristics. Impedance-model-based analysis demonstrates that dc-link capacitor size has a significant impact on resonances. Unlike the ac system where power transfer level affects resonance stability significantly, it is demonstrated in this paper that power transfer level has little impact on dc system resonances. Real-time digital simulations in OPAL-RT RT-LAB verify the analysis.



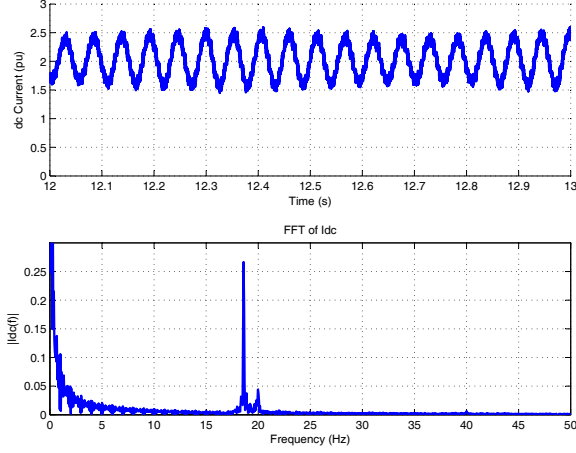


Fig. 17. Simulation results of 1800  $\mu\text{F}$  capacitor at 200 MW.

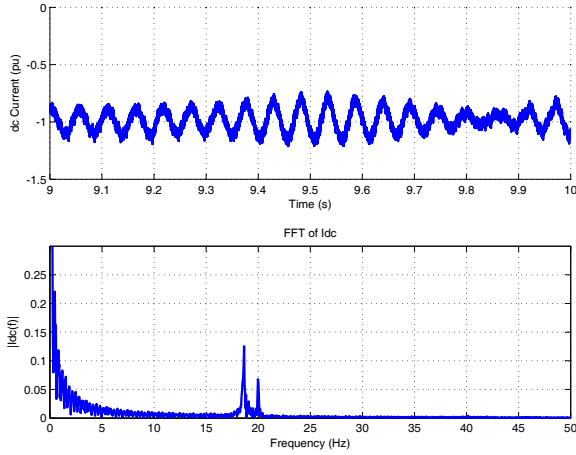


Fig. 18. Simulation results of 1800  $\mu\text{F}$  capacitor at -100 MW.

## APPENDIX

TABLE III  
SYSTEM PARAMETERS OF VSC-HVDC MODEL

Quantity	Value
AC system line voltage	100 kV
AC system frequency	60 Hz
Grid impedance	0.01 $\Omega$ /1.88 mH
Grid filter capacity	18 Mvar
Grid filter tuning frequency	1620 Hz
DC rated voltage	250 kV
DC cable parameters	0.0139 $\Omega$ /km, 0.159 mH/km, 0.231 $\mu\text{F}$ /km
DC cable length	50 km

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TABLE IV  
PARAMETERS OF INDIVIDUAL VSC

Quantity	Value
Switching frequency	1620 Hz
Grid filter	0.01 $\Omega$ /0.02 H
Grid impedance	0.01 $\Omega$ /1.88 mH
DC capacitor	900 $\mu\text{F}$

TABLE V  
PARAMETERS OF CONTROLLERS

Quantity	Value
Current controller	$k_p=50$ , $k_i=100$
DC-link voltage controller	$k_p=0.04$ , $k_i=0.2$
alternating voltage controller	$k_p=0.01$ , $k_i=100$

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