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DC Power Bus Modeling Using a Circuit Extraction Approach based on a Mixed-Potential Integral Equation Formulation and an Iterative Equation Solver

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Abstract

This paper presents a quick and simple approach to perform circuit simulations for an equivalent circuit extracted from a first principles formulation for DC power bus structures. Comparisons between the modeling and measurements demonstrate the application of this approach in DC power bus designs.

Introduction

DC power bus modeling in multi-layer printed circuit board (PCB) or multi-chip module (MCM) substrates is a critical issue in high-speed digital circuit designs. A circuit extraction approach based on a mixed-potential integral equation formulation, denoted CEMPIE, has been developed and successfully applied in various power bus modeling [1], [2]. From a power bus structure, CEMPIE extracts an equivalent passive circuit from a first principles formulation. This circuit is exported to SPICE for circuit simulations. This approach is generally applicable for various power bus studies in the sense that all kinds of SPICE models of IC devices, transmission lines, sources, etc., can be included as lumped circuit models. However, for some simple frequency investigations, the approach is not very computationally efficient on both the simulation speed and the storage memory. Further, some commercial SPICE versions experience a convergence problem for the bias point and DC sweep simulations for a very large-scale {R, L, C} network. A simple approach to perform the swept-frequency $|S_{21}|$ and input impedance simulations by directly solving the system matrix equation using an iterative method is presented in this paper. Some simple lumped circuit elements, such as decoupling capacitors, can be added to the extracted circuit by modifying the system equation. An example demonstrates the effectiveness of this approach.

Formulation

The CEMPIE formulation is similar to the formulation of classical scattering problems. An incident electric field is assumed. The ground plane, and the multi-layer medium in the DC power bus structure are assumed of infinite size, and incorporated into the calculation of the Green's functions. Then, the remaining conducting surfaces, including the planar power plane and vertical surfaces of vias, are replaced by induced surface currents and charges. By enforcing boundary conditions on these conducting surfaces for the vector sum of the incident and induced electric fields, an integral equation results. This equation is discretized and tested using a standard Method of Moments procedure. By further assuming the electric potential over each mesh cell is constant, a final system matrix equation is established as [1]

$$[\mathbf{Y}][\varphi] = -[\mathbf{I}^e], \tag{1}$$

where $[\mathbf{I}^e]$ is the impressed node current vector; $[\varphi]$ is the node scalar-potential vector; and, $[\mathbf{Y}]$ is the system admittance matrix. An equivalent {L, C, R} circuit is extracted from the system admittance matrix $[\mathbf{Y}]$. In the original CEMPIE approach, this extracted equivalent circuit is exported into SPICE where other circuit elements are included and various simulations are performed. The equivalent circuit is extracted in the fashion that they can reproduce the system admittance matrix in SPICE with minimum errors. In the approach presented in this paper, however, the equivalent circuit element values are not calculated. Rather, the system admittance matrix is transferred to the equation solver without changes, assuming it is reproduced with no error at all. Then, external lumped circuit elements, as well as excitations (sources), are added into the system admittance matrix.

Each lumped circuit element or source can be characterized using a simple element admittance matrix or/and a source vector. Most entries of the element admittance matrix and the source vector are zero, except at several special locations, which are related to the circuit nodes where the element or source

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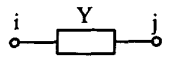
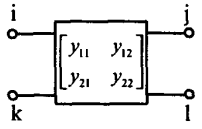
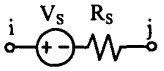
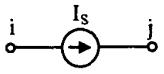
is connected into the circuit model. Typical lumped circuit elements and sources encountered in DC power bus modeling and their corresponding element admittance matrices or/and source vectors are illustrated in Table 1. If one of the nodes is the common ground node, its corresponding row and column is eliminated. All element admittance matrices corresponding to all externally incorporated lumped circuit elements and sources should be added to the system admittance matrix obtained from the CEMPIE approach. Similarly, all source vectors sum up, forming the impressed node current vector. Then, the new system matrix equation becomes

$$[\mathbf{Y}'][\varphi'] = -[\mathbf{I}^{e\prime}]. \tag{2}$$

Note that the number of total circuit nodes may increase after incorporating lumped circuit elements and sources.

Table 1: Typical lumped circuit elements and corresponding element matrices and source vectors.

	Circuit elements	Element matrices and source vectors
1-port admittance		$[Y']:\ \begin{array}{c} \\ i \\ j \end{array}\begin{array}{c} \begin{array}{cc} i & j \end{array} \\ \begin{bmatrix} Y & -Y \\ -Y & Y \end{bmatrix} \end{array}$
2-port admittance network		$[Y']:\ \begin{array}{c} \\ i \\ j \\ k \\ l \end{array}\begin{array}{c} \begin{array}{cccc} i & j & k & l \end{array} \\ \begin{bmatrix} y_{11} & y_{12} & -y_{11} & -y_{12} \\ y_{21} & y_{22} & -y_{21} & -y_{22} \\ -y_{11} & -y_{12} & y_{11} & y_{12} \\ -y_{21} & -y_{22} & y_{21} & y_{22} \end{bmatrix} \end{array}$
Voltage source		$[Y']:\ \begin{array}{c} \\ i \\ j \end{array}\begin{array}{c} \begin{array}{cc} i & j \end{array} \\ \begin{bmatrix} 1/R_S & -1/R_S \\ -1/R_S & 1/R_S \end{bmatrix} \end{array}$ $[I^{e\prime}]:\ \begin{array}{c} \\ i \\ j \end{array}\begin{bmatrix} -V_S/R_S \\ V_S/R_S \end{bmatrix}$
Ideal current source		$[I^{e\prime}]:\ \begin{array}{c} \\ i \\ j \end{array}\begin{bmatrix} I_S \\ -I_S \end{bmatrix}$

$|S_{21}|$ and input impedance are often used for DC power bus studies. They are easy to measure, and are good indications of power bus behavior in the frequency domain. Figure 1 illustrates the setup conditions of source and load for the $|S_{21}|$ and input impedance simulations. In Figure 1(a), a 2-volt voltage source with a 50 Ω source impedance is added at Port 1, while the load at Port 2 is a 50 Ω resistor. Then, voltages at Ports 1 and 2 are

$$V_1 = \sqrt{50}(a_1 + b_1), \tag{3}$$

$$V_2 = \sqrt{50}b_2, \tag{4}$$

where the system impedance is assumed as 50 Ω; a_1 is the incident wave at Port 1, and, b_1 and b_2 are reflection waves at Ports 1 and 2, respectively. Since Port 2 has a matched impedance, its incident wave is zero, namely, $a_2 = 0$. Therefore, according to the definition of scattering parameters [3],

$$S_{21} = (b_2/a_1)_{a_2=0} = b_2/a_1 . \tag{5}$$

The current flowing into Port 1 can be expressed as

$$I_1 = (a_1 - b_1)/\sqrt{50}, \tag{6}$$

$$I_1 = (2 - V_1)/50. \tag{7}$$

Substituting (7) into (6) results:

$$V_1 = 2 - \sqrt{50}(a_1 - b_1). \tag{8}$$

Based on (3) and (8), a_1 can be derived as

$$a_1 = 1/\sqrt{50}. \tag{9}$$

Substituting (4) and (9) into (5),

$$S_{21} = V_2$$

results. Therefore, the voltage at Port 2, which is the potential of the output node, is the desired S_{21}, under the source and load conditions specified in Figure 1(a). The input impedance is a one-port parameter. As shown in Figure 1(b), an ideal unit current source is added at a port. The voltage value at the same port is the desired input impedance looking into that port.

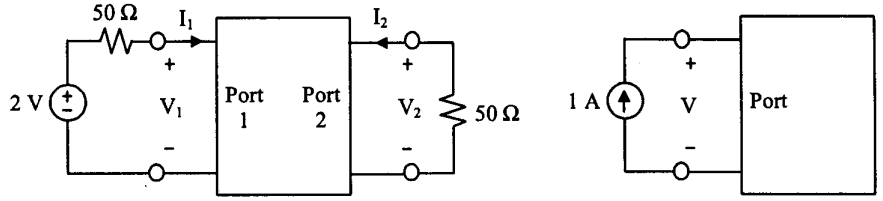


Figure 1: Setups of (a) $|S_{21}|$, and (b) input impedance simulations.

Iterative Equation Solver

The new system equation (2) is established after incorporating lumped circuit elements and specifying source and load conditions. This linear equation can then be solved for unknown node potentials. There are two different classes of methods: direct and iterative methods. Direct methods are usually Gaussian elimination type of methods, such as LU, QR, and Cholesky factorizations [4]. They usually require large storage memory. The algorithms involve access to the individual matrix elements. By contrast, iterative methods obtain an approximate solution through a finite number of steps. The system matrix is involved only indirectly, and no full factorization has to be stored. Therefore much larger scale systems can be handled [5]. However, iterative methods are not universally applicable. Their performance depends on system matrix properties like diagonal dominance or the existence of an underlying differential operator.

DC power bus structures usually result in very large-scale system matrix equations using the CEMPIE formulation, since the whole power plane has to be discretized into small triangular cells. An iterative method, the biconjugate gradient stabilized method, is used to solve the system equation (2), instead of direct methods. The computational complexity of the iterative method is proportional to the number of nonzero elements in the system matrix, though it also depends linearly on the row and column sizes. To improve the computational efficiency, the system matrix $[Y']$ is sparsed. The non-diagonal entries in a row are compared with the diagonal element in that row, which is the dominant element since it represents the field reaction within a mesh cell. If the magnitudes of the non-diagonal entries are 10^{-8} times smaller than the magnitude of the dominant element, the entries are set to be zero.

The convergence rate of iterative methods depends on the system matrix properties. A preconditioner can be used to transform a linear system equation with unsuitable matrix properties into one that has the same solution with the original equation, but has more favorable matrix properties [5]. The incomplete LU factorization is used as a preconditioner in this study. It is found that the preconditioner dramatically increases the convergence speed, although it incurs some initial setup cost as well as the application cost in each step, for the DC power bus modeling problems investigated in this study.

Results

This modeling approach was used to model some PCB DC power bus structures. Figure 2(a) shows an example of a two-layer PCB with two planes representing the power and ground, respectively. Sixteen surface mount technology (SMT) decoupling capacitors were uniformly distributed over the board. One end of every capacitor was directly connected to the top layer, while the other end to the bottom layer through a 24 mil diameter via. The 63 mil dielectric material was FR-4 with a dielectric constant of $\varepsilon_r = 4.7$, and loss

tangent of *tan* $\delta = 0.02$. $|S_{21}|$ between two test ports was investigated both experimentally and using the modeling approach. A network analyzer was used with a full two-port calibration. The reference planes were further rotated to the SMA terminals looking into the power bus. The individual capacitor values were 0.01 μF, with nominal parasitic inductance and resistance values of 820 pH and 120 mΩ. The power bus with the capacitor vias, but no capacitors, was formulated using the CEMPIE approach. The decoupling capacitors were then added into the CEMPIE extracted circuit as series RLC circuits. The modeled and measured results are compared in Figure 2(b). They agree favorably from 100 MHz to 2 GHz.

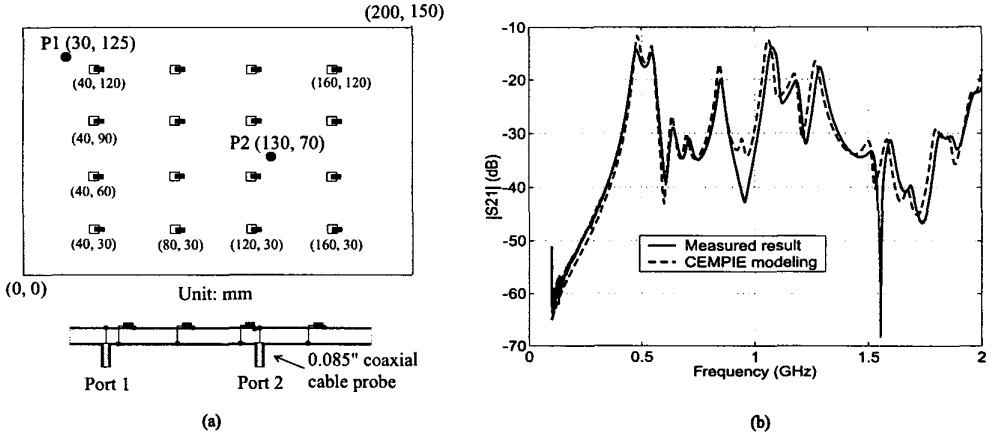


Figure 2: (a) A test PCB power bus geometry; and (b) its modeled and measured results.

Totally 3549 mesh edges and 2422 mesh cells were used in the CEMPIE extraction approach. It took approximately 38 minutes to obtain the system equation (1), and approximately 5 hours 40 minutes to complete the $|S_{21}|$ simulation with 201 frequency points from 100 MHz to 2 GHz using the iterative equation solver, both in a Pentium III PC with a 450 MHz CPU and 512 MB memory. This was a big improvement compared with a direct method. It took approximately 32 hours for the same problem to be solved using an LU factorization on the same computer. Other small-scale power bus modeling examples show that this approach is approximately 20-30 times faster than the full CEMPIE approach.

Conclusion

The approach presented in this paper to perform circuit simulations by solving the system equation using an iterative method is very suitable and computationally efficient for frequency-domain DC power bus modeling. Agreements between modeling and measurements demonstrate its effectiveness.

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