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DC Power Bus Noise Isolation with Power Islands

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Abstract: Segmented power planes are often used for DC power bus noise isolation in multi-layered printed circuit board (PCB) designs. To achieve a desirable noise isolation, different power plane segmentations can be used. A suitable modeling approach, as well as measurements, were employed to study the power bus isolation with several power plane segmentation configurations. The studied geometries included power island designs connected with a conducting bridge, a ferrite bead, and a π -filter. In addition, different conducting bridge widths and power island gap widths were analyzed, and compared. The modeled and measured results show that power plane segmentations with proper designs can result in significant power bus noise isolation.

I. Introduction

Power plane segmentation is an effective method for high-frequency noise isolation on the DC power bus. On a PCB, power bus noise results from switching of IC devices, including CPUs, and ASICs [1], [2]. The switching noise propagates throughout the entire power planes, and results in significant noise problems. In high-speed digital designs that employ multiple layers with entire layers for power and ground, power planes can be segmented using power islands, or totally segmented power areas to achieve a certain degree of noise isolation. A power island is usually employed to provide power supply some fast switching IC devices, while isolating the noise from the rest of the power area. The power island can be connected to the larger power area with a narrow neck, or conducting bridge. The conducting bridge has a considerable impedance at

high frequencies that impedes the noise propagation. Previous studies of the power bus isolation with varying bridge lengths, widths, and locations for two symmetric power areas have been reported [3]. Because of their high impedance at high frequencies, and a very low impedance at DC, ferrite beads can also be used in power island designs. For multi-layered PCBs, the interplane capacitances between the power areas and the reference plane can be considered as shunt capacitors at low frequencies on both sides of the connection bridge. As a result, a conceptual π -filter is formed, which is desirable to contain the noise in the power island. In addition, the performance of this π -filter can be optimized by tuning the parameters. However, in practice, this π -filter does not work out as well as speculated at high frequencies due to the distributed resonances of the power planes. In this study, two lumped capacitors along with a ferrite bead were used to form a lumped π -filter at the neck joining the two power areas, and the resulting power bus noise isolation was studied.

Power plane segmentations can be analyzed with modeling methods for design evaluation. The modeling facilitates the power bus design at early stages. A circuit extraction technique based on mixed potential integral equation, or CEMPIE, is employed herein to model a few power plane segmentation configurations. The CEMPIE formulation is a PEEC-type method based on Maxwell's equations, and similar to the classical scattering problems [4], [5]. One significant advantage of the CEMPIE modeling is that lumped circuit elements can be extracted from the formulation. As a result, this approach has great flexibility to incorporate circuit models, and device models for SPICE simulations in both time and frequency domains. The CEMPIE mod-

eling is a variation of the partial element equivalent circuit (PEEC) modeling method, with the principal difference in the Green's functions [6], [?]. Previous studies have demonstrated the CEMPIE modeling approach is suitable to model the DC power bus structures [8]. The dielectric loss and conductor loss can be included in the modeling. Further, the CEMPIE modeling was developed to model the vertical discontinuities such as via interconnects and test ports [9].

II. STUDYING THE POWER BUS NOISE ISOLATION WITH A POWER ISLAND

A test board was constructed to study the power bus isolation with a power island structure. Measurements were made to investigate the noise isolation between the power island and the larger power area. The test board was a two-sided board, with a dimension of $15\text{ cm} \times 9\text{ cm}$, as shown in Figure 1. The board thickness was 45 mils , and

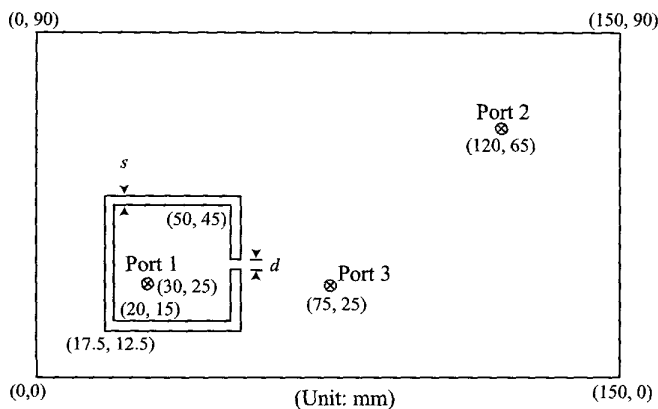


Figure 1. A power island connected to the larger power area with a conducting bridge.

the relative dielectric constant was $\epsilon_r = 4.5$. The top plane was used as the power plane, and the bottom plane was the reference plane. A square power island was constructed in the lower left portion of the power plane. The island was used to mimic the power area of an IC device for studying the noise propagating from the island to the larger power area. The dimension of the power island was $3\text{ cm} \times 3\text{ cm}$, and the power island was isolated from the larger power area with a gap of width 2.5 mm . The right edge of the square power island was connected to the larger power area in the middle with a conducting bridge, or perfect electric conductor (PEC) bridge. The width of the PEC bridge was $d = 2.5\text{ mm}$. Three test ports were built on the test board with SMA connectors. The vias for the SMA connectors had a diameter of 50 mils . Test port 1 was located

in the power island as the incident port. Test ports 2 and 3 were used as far and near observation ports. In the measurements, $|S_{21}|$ were measured with an HP8753D network analyzer between the incident port and one of the observation ports. The other observation port was open. The power island and the test ports were placed in asymmetric locations, as shown in Figure 1, so that all excited wave modes could be observed.

The same test board was also modeled with the CEMPIE approach. First, the Green's functions were determined. In the CEMPIE modeling, the Green's functions in a stratified medium were used, and calculated [10], [11]. The ground plane and the dielectric layers were assumed to be infinite planes. The dielectric loss of the FR-4 material was included in the calculations. The loss tangent ($\tan \delta$) was 0.02 in the studied frequency range. The derived dyadic and scalar Green's functions were attributed to the vector magnetic potentials and scalar electric potentials. Although the dynamic Green's functions were first determined, only the quasi-static Green's functions were used in the modeling to facilitate extraction of an equivalent circuit. Then, the power plane surface was discretized, and the vector basis functions were applied. The vertical interconnects associated with the test ports were discretized as well. The power plane surface was discretized into approximately 780 triangular cells, and each vertical interconnect was discretized into six rectangular cells. The current continuities were enforced between the planar and vertical cells. The scalar potential was assumed to be a constant for each discretized cell in this mixed potential integral equation (MPIE) formulation. A matrix equation was then derived after the testing procedure. The testing functions are the same as the basis functions. The total number of unknowns in this problem was approximately 800. Finally, the matrix equation was solved, and the $|S_{21}|$ was determined based on the port potentials. The $|S_{21}|$ of the studied power bus structure was calculated at 401 frequency points from 10 MHz to 3 GHz to fit the measured points.

The measured and modeled $|S_{21}|$ are shown in Figure 2 for Port 2 as the observation port, and Figure 3 for Port 3 as the observation port. The modeled and measured results agree well in the entire frequency range. Peaks occurred at the board resonances, for example, at 461 MHz for the TM_{10} mode, and 896 MHz for the TM_{11} mode. The peak at 2.3 GHz was a resonance due to the power island dimensions. For a comparison, the test board was modeled again for the entire top plane used as a complete power plane. The CEMPIE modeled $|S_{21}|$ are also shown in Figures 2 and 3. The results indicate the $|S_{21}|$ was somewhat

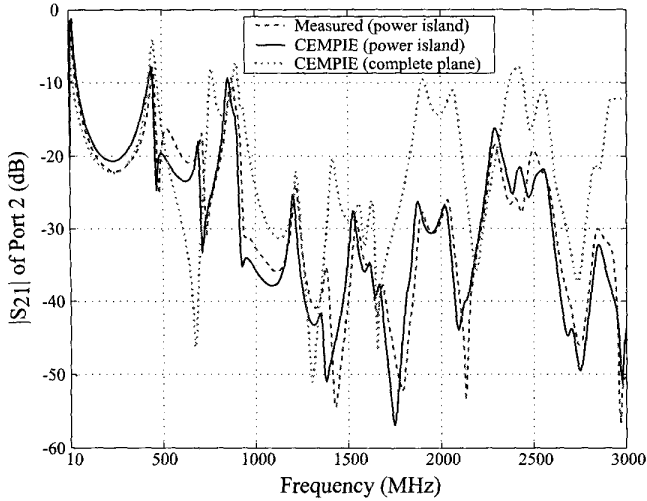


Figure 2. The measured and modeled $|S_{21}|$ at Port 2 for a power island with a PEC bridge connection.

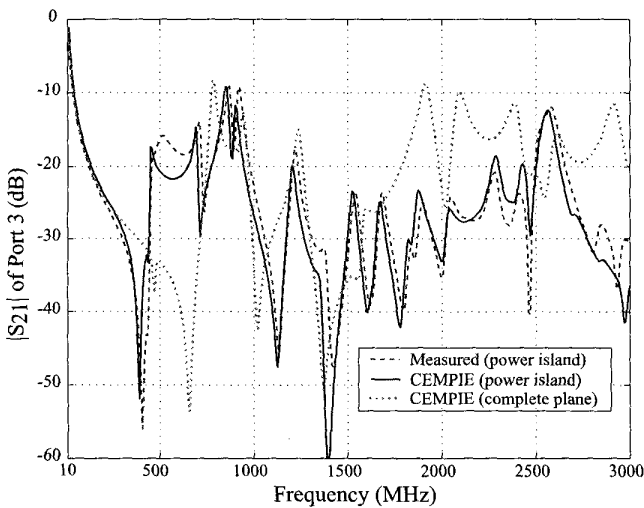


Figure 3. The measured and modeled $|S_{21}|$ at Port 3 for a power island with a PEC bridge connection.

reduced with the use of the power island. Although the decrease of the $|S_{21}|$ peaks below 1.7 GHz was marginal, the peaks beyond 1.7 GHz were reduced by approximately 10 to 20 dB. Therefore, a good noise isolation was achieved for the power island design with a PEC bridge.

The above test board was modeled again with varying PEC bridge widths, and power area isolation widths. Port 2 was used as the observation port in the CEMPIE modeling. First, a wider conducting bridge with a width $d = 5 \text{ mm}$ was modeled. The modeled $|S_{21}|$ is shown in Figure 4 com-

pared with the previous study where $d = 2.5 \text{ mm}$. The

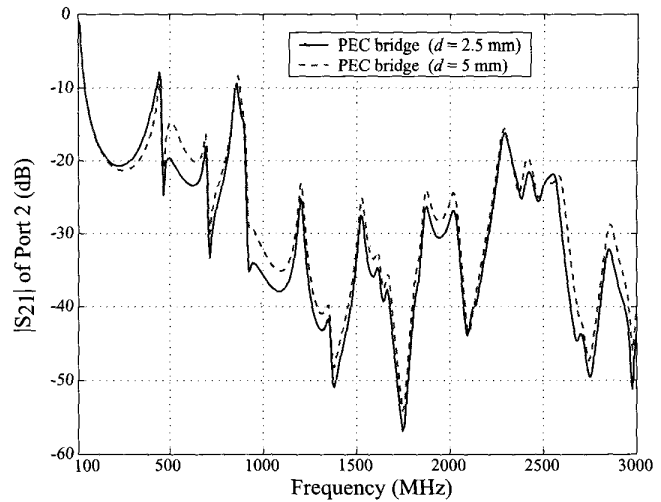


Figure 4. The modeled $|S_{21}|$ for varying bridge width in a power island design.

results indicate the $|S_{21}|$ had only slight increase, although the PEC bridge width was doubled. Therefore, a bridge width between these values had approximately the same power bus noise isolation. Secondly, several gap widths between the power island and the larger power area were chosen to study the resulting power bus noise isolation. The modeled results of $|S_{21}|$ are shown in Figure 5 for the gap width $s = 25 \text{ mils}$, 50 mils , and 100 mils , respectively. Although the $|S_{21}|$ for $s = 25 \text{ mils}$ was approxi-

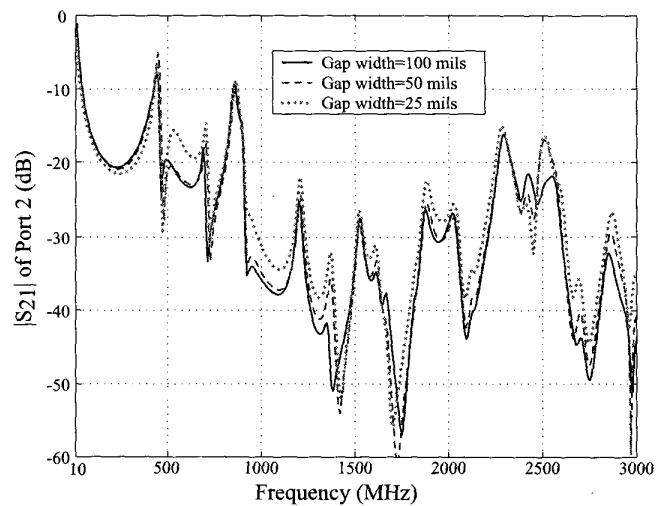


Figure 5. The modeled $|S_{21}|$ for varying gap width in a power island design.

mately 3 dB higher than the other two cases at some peaks,

the differences between these cases were marginal. This study indicates the above values of bridge widths and gap widths achieve approximately the same effects in achieving the power bus noise isolation.

III. STUDYING THE POWER BUS NOISE ISOLATION WITH FERRITE BEAD AND π -FILTER CONNECTIONS

The power island connected to the larger power area with a ferrite bead was also studied with the CEMPIE modeling approach. Two ferrite beads were chosen, and used to replace the PEC bridge in Figure 1. The ferrite beads were a $90\ \Omega$ component (Steward 25Z1206-1) – Ferrite 1, and a $600\ \Omega$ component (Murata BLM31A601S) – Ferrite 2. The ferrite bead impedance was determined by first measuring the $|S_{11}|$ with an HP8753D network analyzer. Then, by converting the S -parameter to the input impedance, the impedance of the components was calculated. The impedance of Ferrite 1 and Ferrite 2 are shown in Figure 6. Further, the ferrite bead impedance as a function of

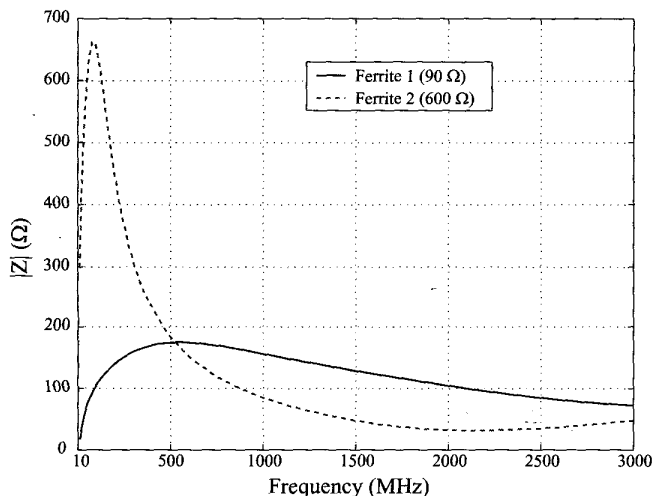


Figure 6. The impedance of the ferrite beads connecting the power island to the larger power area.

frequency was incorporated in the CEMPIE modeling [12], and $|S_{21}|$ calculated. The modeled $|S_{21}|$ using Ferrite 1 and Ferrite 2, as well as the $|S_{21}|$ using the PEC bridge, are compared and shown in Figure 7. Comparing to the case of the PEC bridge, the $|S_{21}|$ of the test board with ferrite beads decreased by approximately 10-20 dB below 2.6 GHz. The high impedance of the ferrite beads at low frequencies had a significant impact on the improvement of the power bus noise isolation. However, although there was an impedance difference between the ferrite parts, similar

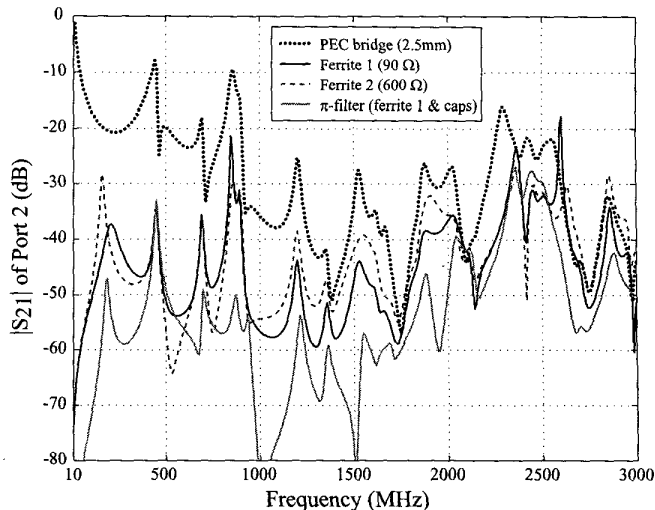


Figure 7. The modeled $|S_{21}|$ for connecting the power island with a PEC bridge, a ferrite bead, and a π -filter.

effects were achieved in the power bus noise isolation.

Lumped elements in a π -network can be used to model the connection bridge using a ferrite bead. Two lumped shunt capacitors on each side of the ferrite bead were inserted between the power and the ground planes. Since the inter-plane capacitances have distributed properties, the lumped capacitors improve the performance of the equivalent π -filter. In this study, two $0.1\ \mu\text{F}$ lumped capacitors were placed at $1.5\ \text{mm}$ on both sides of the connection. The Ferrite 1 was used to connect the power island with the larger power area. The power plane configuration was the same as shown in Figure 1. This configuration was modeled with the CEMPIE approach. The vertical interconnects of the lumped capacitors were included in the modeling. The modeled $|S_{21}|$ is shown in Fig. 7. The results indicate this lumped π -filter connection achieved the best power bus noise isolation with the lowest $|S_{21}|$ values. An additional 10 dB improvement in the power bus noise isolation was achieved at most frequencies compared to the use of a ferrite bead alone. Therefore, placing shunt capacitors in proximity to the connecting bridge to form a π -filter is beneficial.

IV. Conclusions

The use of power islands can result in desirable power bus noise isolation. Comparing with a complete power plane, the power bus noise isolation with a power island is significant at most frequencies. A ferrite bead is beneficial for

the connection of the power island and other power areas. With added lumped capacitors to form a π -filter, the power bus isolation can be improved in an excess of 10 dB over a ferrite bead in a wide frequency range.

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