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DC Power-Bus Noise Isolation With Power-Plane Segmentation

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***Abstract*—Power-plane segmentation is often used for dc power-bus noise isolation in multilayer printed circuit board (PCB) designs. To achieve a desirable noise isolation, different power-plane segmentations can be used. A suitable modeling approach, as well as measurements, were employed in this work to study the noise isolation with several power-plane segmentation designs. The geometries studied include power islands, and totally segmented power planes. The effects of the power-bus noise isolation with different types of power island connections, locations of segmentation, and shapes were analyzed, and compared. The modeled and measured results show that suitable power-plane segmentation can result in significant power-bus noise isolation.**

***Index Terms*—DC power-bus design, noise isolation, power island, power-plane segmentation.**

I. INTRODUCTION

LOGIC transitions of digital integrated circuits (ICs) are a major source of power-bus noise [1], [2]. For PCBs that use complete planes or large area fills as power and ground, this high-frequency noise can propagate throughout the enitre power bus, and result in significant signal integrity (SI) and electromagnetic interference (EMI) problems. In addition to techniques using decoupling capacitors to mitigate the noise, an isolation technique using power-plane segmentation can also be an effective method for minimizing noise propagation. Two types of segmentation, segmented power planes and power islands, are commonly used in high-speed digital designs. A power island can be employed to provide power to some fast switching or noisy IC devices. If these IC devices share a common power supply with the rest of the circuit, a conducting bridge can be employed to connect the power island to the larger power area. However, the low-frequency isolation performance of this topology is relatively poor. Ferrite beads are more suitable for this kind of application due to their frequency-selective loss characteristics. For multilayer PCBs, the parallel interplane capacitances between the power areas and the reference plane are often considered as shunt capacitors on both sides of the connection bridge, and the bridge itself treated as a series inductor. As a result, a simple intuitive model for power islands as a π network can be established. The performance of power islands might then be optimized by tuning the parameters. However, in practice, this π network does not work out as well as speculated at high frequencies due to the distributed resonances of the power planes. An improved π network using two lumped surface-mount-technology (SMT) capacitors and an SMT ferrite bead was found to have a superior performance for noise isolation in this study. The effect of the power island location on the noise isolation was also studied, and found to have little impact.

Segmented power planes are similar to power islands except that they are used to isolate a larger portion of the power plane from the rest. In some applications, PCB layouts are partitioned into different functioning portions, for example, digital and analog circuits. Studies on some geometric dimensions of the segmented power planes with conducting connections using a numerical modeling approach are also reported in this paper. Similar results to the power island were achieved in cases without dc connections. For the complete segmented power planes, although noise can be coupled capacitively between different power areas, or through the modes supported by the parallel power/ground plane pair, the coupling can be reduced by careful design. Previous experimental work on power-plane segmentation has been reported [3], [4]. A hybrid FEM/MoM numerical method was also employed to model totally isolated power planes [5]. This work presents a study on effects of gap shape on board resonances and RF isolation using a *c*ircuit *e*xtraction technique based on a *m*ixed *p*otential *i*ntegral *e*quation (CEMPIE) approach. Further, an approach is developed for isolating power areas at high frequencies, while maintaining a dc connection.

Numerical methods are suitable for modeling power-plane segmentations. A proven modeling approach can greatly facilitate the power-bus design at early stages without the need for prototype hardware. The CEMPIE approach is employed herein to model various configurations of power-plane segmentation. One significant advantage of the CEMPIE approach is that lumped element models can be extracted from the formulation. As a result, the high-frequency power-bus performance can be analyzed with general SPICE simulators. With this approach, other circuit models, and device models can be incorporated. The CEMPIE approach is an application of the partial element

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equivalent circuit (PEEC) method in general multilayer media [6]. Previous studies have demonstrated that the CEMPIE modeling approach is suitable for modeling dc power-bus structures [7].

II. Power–Bus Noise Isolation With Power Islands

The CEMPIE modeling approach is used herein to study the power-bus noise isolation with power islands. The CEMPIE formulation is based on a mixed-potential integral equation approach, and it is similar to the formulation of classic scattering problems [8], [9]. A scattered electric field $\vec{E}^s$ is excited on the exposed conducting surface S as a result of an incident electric field $\vec{E}^{inc}$. The boundary condition on S is

$$\hat{n} \times (\vec{E}^{inc} + \vec{E}^s)|_S = 0 \tag{1}$$

which is the electric field integral equation (EFIE). The scattered electric field results in surface current densities and surface charge densities on the conducting surface. For typical PCB configurations, the conducting surface includes the metal planes, and the interconnects between the planes. In the CEMPIE modeling of power buses, the horizontal power planes are discretized into triangular cells, and the vertical discontinuities, for example, vias, are discretized into rectangular cells. The triangular cells are amenable to model arbitrary power-plane shapes. The induced surface current densities are expanded with vector basis functions. Two types of current vector basis functions are used to facilitate the analysis of the problem. For the triangle surface cells, the Rao, Wilton, and Glisson (RWG) current vector basis functions are anchored by the interior edges [8]. For the vertical rectangular cells, the basis functions are one-dimensional linear functions, and associated only with horizontal edges of the rectangles. This approach neglects the horizontal surface current densities on the vertical discontinuities, which is adequate, since the vertical discontinuities have electrically small dimensions in this study. The surface charge density is assumed as a constant over each discretized cell. When enforcing the boundary conditions, an integral equation results. This integral equation is then tested using testing functions that have the same form as the basis functions. Finally, lumped element models between all basis functions are extracted from the method of moments (MOM) impedance matrix [10]. In the equivalent circuit, each node corresponds to a discretized cell. The interconnecting circuit elements are calculated with some manipulations from the elements of the MOM impedance matrix.

Dyadic and scalar Green's functions for a stratified medium are used in the CEMPIE/PEEC formulation for the vector magnetic and scalar electric potentials, respectively, instead of the free-space Green's function [11], [12]. The dielectric losses of the substrate are included in the scalar Green's functions. The ground plane and the dielectric layers are assumed to have infinite planar extent. To calculate the Green's functions, closed-form expressions of the spectral-domain Green's functions are developed. The complex images of the spectral Green's functions are calculated with a generalized pencil of function (GPOF) method. Then, the spatial-domain Green's

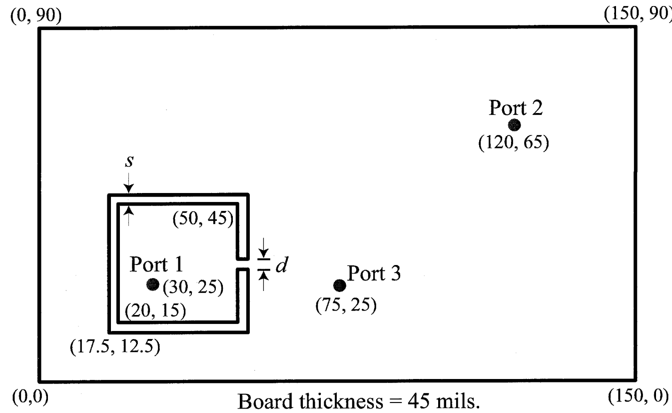

Fig. 1. Test board geometry for a power island connected to the larger power area with a PEC bridge. Units are in millimeters.

functions are determined by taking an inverse Fourier transform with the Sommerfeld identity [13]. For circuit extraction, a quasistatic approximation of the Green's functions is used. This approximation is adequate for suitably defined discretization [9].

A test board was constructed to study the power-bus noise isolation with a power island structure. Measurements were made to corroborate the CEMPIE modeling. The test board was a two-sided board, with dimensions of 9 cm $\times$ 15 cm, as shown in Fig. 1. The board thickness was 45 mils, and the relative dielectric constant was $\epsilon_r = 4.5$. The top plane was designated as the power plane, and the bottom plane was the reference plane. A square power island was constructed in the lower left portion of the power plane, and offset to avoid any symmetry. The island was used to mimic the power area of an IC device for studying the noise propagating from the island to the larger power area. The dimension of the power island was 3 cm $\times$ 3 cm, and the power island was isolated from the larger power area with a gap width of 2.5 mm, which was approximately twice the dimension of the board thickness. The square power island was connected to the larger power area in the middle of the right edge with a conducting bridge, or perfect electric conductor (PEC) bridge. The width of the PEC bridge was $d = 2.5$ mm. Three test ports were built on the test board with SMA connectors. The vias for the SMA connectors had a diameter of 50 mils. Port 1 was located in the power island as the incident port. Ports 2 and 3 were used as remote and near observation ports. In the measurements, $|S_{21}|$ was measured with an HP8753D network analyzer between the incident port and one observation port. The other unused observation port was open-circuited. The power island and the test ports were placed in asymmetric locations, as shown in Fig. 1, so that all excited wave modes could be observed.

The same test board was also modeled with the CEMPIE approach. The power-plane surface was discretized using approximately 780 triangular cells. The vertical interconnects associated with the test ports were discretized as well, and each vertical interconnect was discretized into six rectangular cells. The total number of unknowns in this problem was approximately 800. The dielectric loss of the FR-4 material was included in the modeling with a loss tangent of $\tan\ \delta = 0.02$. Finally, equivalent lumped circuit models were extracted, and the $|S_{21}|$ was

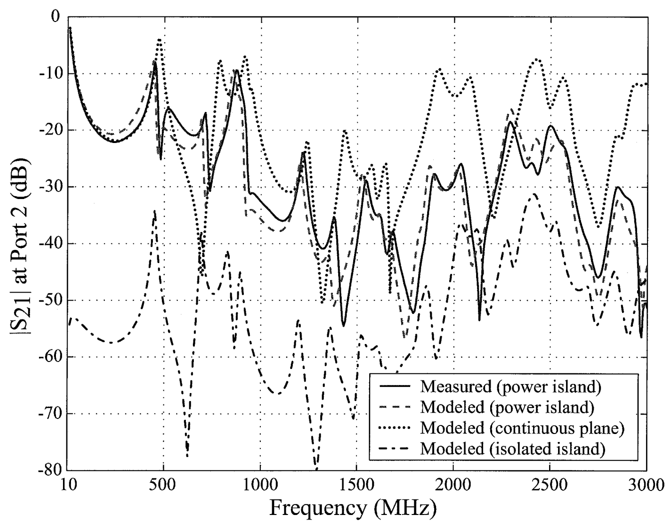

Fig. 2. Measured and modeled $|S_{21}|$ at Port 2 for a power island with a PEC bridge connection.

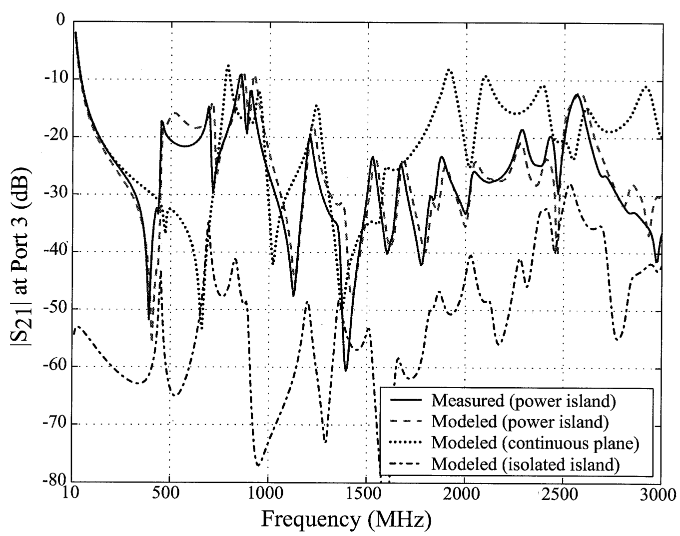

Fig. 3. Measured and modeled $|S_{21}|$ at Port 3 for a power island with a PEC bridge connection.

determined. The $|S_{21}|$ was calculated at the same 401 frequency points from 10 MHz to 3 GHz as in the measurements.

The measured and modeled $|S_{21}|$ are shown in Fig. 2 for Port 2 as the observation port, and Fig. 3 for Port 3 as the observation port. The modeled and measured results agree well over the studied frequency range. Peaks occurred at the board resonances, for example, the peak at 461 MHz is approximately that for the TM_{10} mode of the continuous board, and 896 MHz for the TM_{11} mode. These TM wave modes were excited when the power plane behaved in a microstrip patch antenna fashion [14], [15]. The peak at 2.3 GHz was a resonance due to the power island dimensions. Several factors contributed to the amplitudes at these resonances, including the dielectric loss and skin-effect loss. The dielectric loss was found to be the dominant factor, which was modeled in the CEMPIE modeling approach. For a comparison, the test board was modeled again where the entire top plane was a continuous power plane. The modeled $|S_{21}|$ at Port 2 and Port 3 are also shown in Figs. 2 and 3. The results indicate the $|S_{21}|$ can be dramatically reduced with the use of the power island, though the reduction is very frequency dependent. Although the decrease of the $|S_{21}|$ peaks below 1.7 GHz was marginal for the island with a PEC bridge, the peaks beyond 1.7 GHz were reduced by approximately 10 to 20 dB. The significance of the $|S_{21}|$ spectrum is that a clock harmonic or other noise source that excites the power bus that occurs at a maximum of $|S_{21}|$ will drive the power-plane resonances, and result in appreciable noise on the power bus that can lead to SI and EMI problems.

Studies were then performed using the CEMPIE modeling to investigate the noise isolation effects resulting from different bridge and gap widths, locations of the power islands, and other connection topologies besides the conducting PEC bridge. The same board geometry as shown in Fig. 1 was used. Port 2 was used as the observation port hereafter. First, three cases where the PEC bridge had a width of $d = 1$ mm, 2.5 mm, and 5 mm were modeled. In all cases, the gap width was 2.5 mm, and the board thickness was 45 mils. There was little change of $|S_{21}|$, indicating the PEC bridge width does not significantly impact the noise isolation for practical widths. Next, several gap widths between the power island and the larger power area were chosen. The range of gap widths studied was chosen to conform to practical design limits. The $|S_{21}|$ was calculated with a gap width of $s = 25$ mils, 50 mils, 100 mils, and 200 mils, respectively. In these cases, the PEC bridge width was 2.5 mm, and the board thickness was 45 mils. Although the $|S_{21}|$ for $s = 25$ mils was approximately 3 to 5 dB higher than the other three cases at some peaks, the difference between these cases was marginal. The coupling was dominated by the conducting bridge, and, increasing the gap width resulted in little improvement in the noise isolation.

Connecting the power island to the larger power area with a surface mount ferrite was also studied with CEMPIE modeling. Two ferrite parts were chosen, and used to replace the PEC bridge shown in Fig. 1. The ferrite parts were a 90 Ω (at 100 MHz) component (Steward 25Z1206–1, denoted as Ferrite 1), and a 600 Ω (at 100 MHz) component (Murata BLM31A601S, denoted as Ferrite 2). The impedance of the ferrite beads was determined by measuring the S_{11} from 10 MHz to 3 GHz with an HP8753D network analyzer, and converting S_{11} to input impedance. An SMA-type PCB mounting connector was used in this measurement, and the ferrite component was soldered between the center conductor and the ground. This PCB mounting connector was compensated in the measurements with the same type of connectors that were built as open and short. The measured magnitudes of the ferrite impedances are shown in Fig. 4. Both the magnitude and phase of the ferrite bead were incorporated in the CEMPIE modeling to determine $|S_{21}|$ [13]. The modeled $|S_{21}|$ using Ferrite 1 and Ferrite 2, as well as the $|S_{21}|$ using the PEC bridge, are compared in Fig. 5. Again, the board with the geometry of Fig. 1 was used. As compared to the PEC bridge, the $|S_{21}|$ using ferrite beads decreased dramatically, by approximately 10 to 25 dB below 1.3 GHz. In addition, since Ferrite 2 had a larger impedance than Ferrite 1 from 10 to 350 MHz, the resulting $|S_{21}|$ was smaller, by approximately 13 dB at 200 MHz. Using a ferrite bead of high impedance improved the noise isolation in this frequency range.

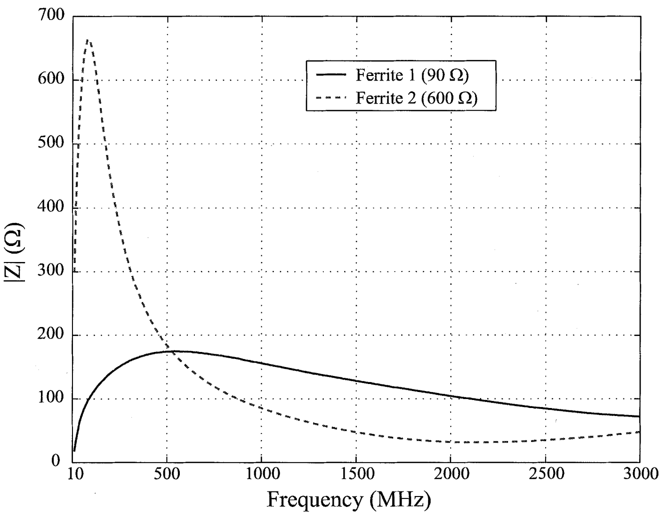

Fig. 4. Measured impedance magnitude of the ferrite beads connecting the power island to the larger power area.

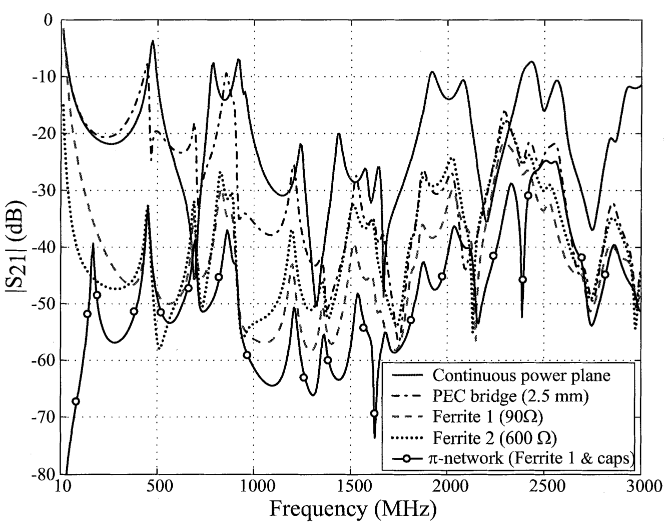

Fig. 5. Modeled $|S_{21}|$ at Port 2 for connecting the power island with a PEC bridge, a ferrite bead, and a π network, as compared to a continuous power plane.

The geometry using a ferrite bead across two power areas is essentially a π network. The parallel plane capacitances between the power and the ground planes on both sides of the ferrite bead behave as shunt capacitors at lower frequencies. Since the interplane capacitances have small values, as well as distributed properties at higher frequencies, lumped capacitors can be placed on each side of the ferrite to improve the low-frequency performance. This configuration was modeled. Two 0805 SMT 0.1 μF lumped capacitors were located 1 *mm* from the gap edges, and on both sides of the connecting ferrite bead, as shown in Fig. 6. Ferrite 1 was used to connect the power island to the larger power area, and the power-plane configuration remained the same as shown in Fig. 1. The vertical interconnects, as well as the equivalent series inductance (ESL) of the lumped capacitors were included in the CEMPIE modeling. The ESL of the capacitors in this study was 0.7 *nH* as determined from component impedance measurements. The vias

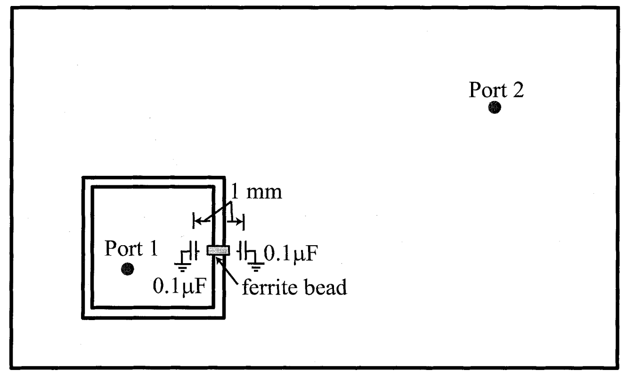

Fig. 6. Modeled configuration for two power areas connected with a π network.

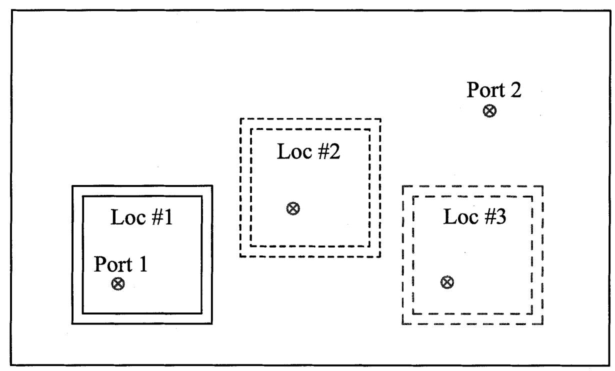

Fig. 7. Three locations tested for a totally isolated power island.

connecting the shunt capacitors to the planes can limit the performance of the π network if the interconnect inductance becomes too large. It is critical to have the ferrite impedance much greater than the impedance of the capacitors and associated interconnect inductance. The modeled $|S_{21}|$ is shown in Fig. 5, and compared with other configurations. The results indicate this lumped π network connection achieved superior noise isolation. Although the two power areas were still connected with dc continuity, there was a significant reduction of $|S_{21}|$ at approximately 10 MHz due to the shunt capacitors. An additional 10 dB improvement in noise isolation was achieved at most frequencies as opposed to the use of a ferrite bead alone. The noise isolation as compared to a continuous plane was approximately 20 to 25 dB.

Noise isolation with regard to island location was studied with a totally isolated power island, i.e., one having no dc connection. For this purpose, three power island locations were chosen, as shown in Fig. 7. The power island on the left portion of the board (Location 1) had the same configuration as in Fig. 1, but had no PEC bridge. Location 2 was in the center of the board. Location 3 was on the right portion of the board, and symmetric to Location 1 with regard to the centerline perpendicular to the long edges of the board. The incident port (Port 1) remained in the same relative location within the power island, and the location of Port 2 was unchanged. The $|S_{21}|$ was determined with the CEMPIE approach, and the results are shown in Fig. 8. For different locations, some of the peaks shifted in frequency due to the change of the modes within the larger power area, and the

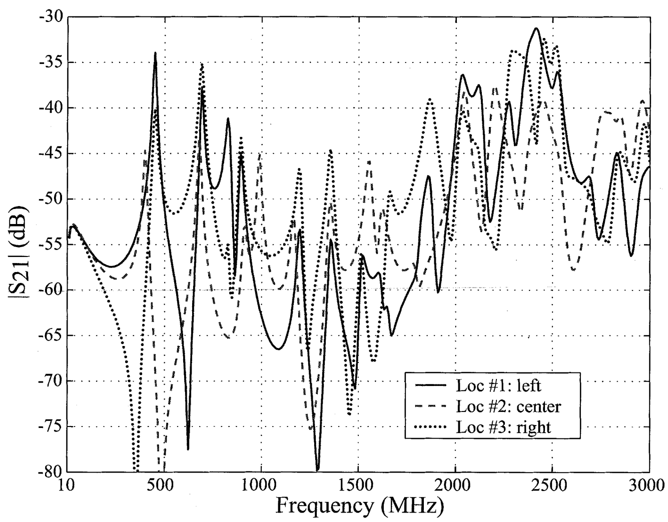

Fig. 8. Modeled $|S_{21}|$ for the totally isolated power island at three locations.

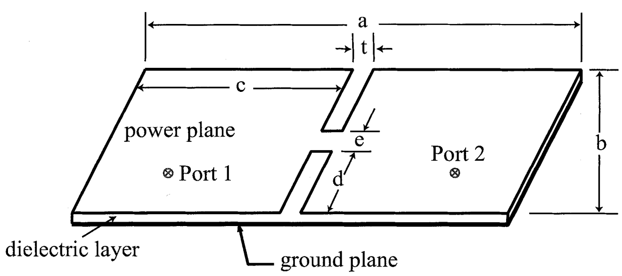

Fig. 9. Test geometry of segmented power plane.

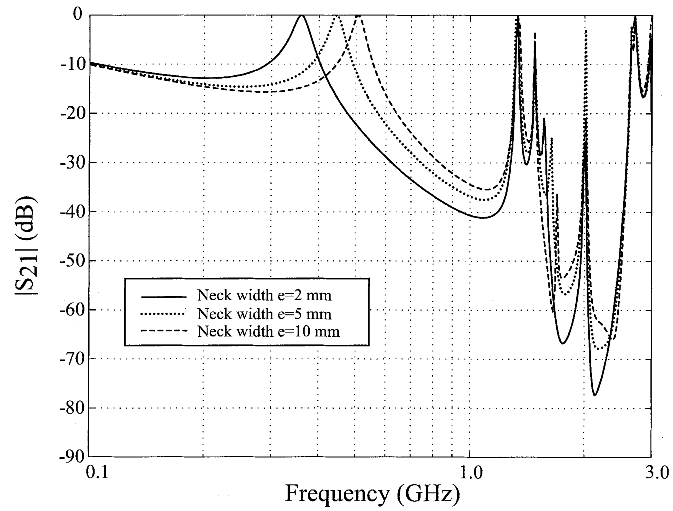

Fig. 10. Power-bus noise isolation versus neck width.

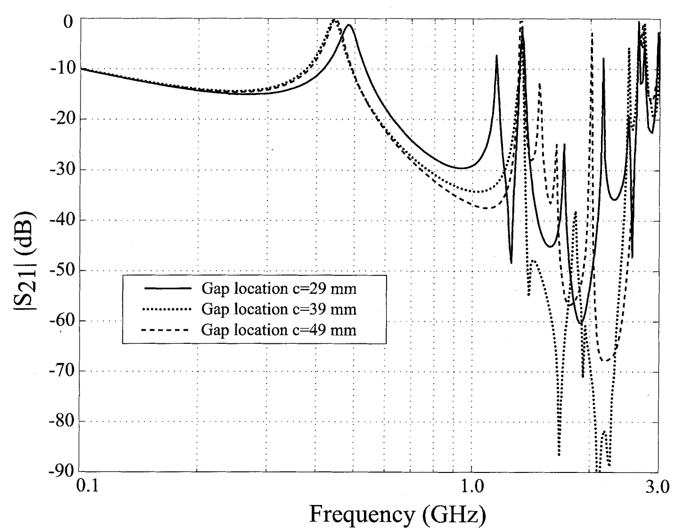

Fig. 11. Power-bus noise isolation versus gap location.

distance between the two test ports. However, no significant difference in the overall envelope resulted between these three locations. It is more helpful to compare the overall envelopes than the resonances at specific frequencies, because the resonances and clock frequencies vary in applications. In these cases, the island location had little impact on the power-bus noise isolation. The shape of the island was also altered by trimming the corners, but this had little impact on the noise isolation as well.

III. Power-Bus Noise Isolation With Segmented Power Planes

Previous results demonstrated the isolation performance of a power island with a π network comprised of a series ferrite and two shunt capacitors. The CEMPIE modeling was also used for examining the isolation of larger board areas as a function of geometry factors such as gap and neck sizes, location, gap type, *etc*. A simple segmented power-plane structure as shown in Fig. 9, with sizes of $a = 100$ mm, $b = 55$ mm, $c = 49$ mm, $d = 25$ mm, $e = 5$ mm, and $t = 2$ mm, was modeled with one geometry factor varying at a time. The board thickness was 43 mils. Fig. 10 illustrates the effect on isolation when changing the neck width. The neck was located in the center of the board, and the neck width was 2, 5, and 10 mm, respectively. The change of neck width affects the series impedance between the two segmented portions in the low frequency band so that a dramatic shift of the first resonance results. A wider neck has a lower inductance, resulting in a higher first resonant frequency. In the high-frequency band, conductive coupling through the neck is no longer dominant, and there is little difference between the three cases when the frequency is higher than 1 GHz.

A change in gap width also results in little difference in the $|S_{21}|$ results. The studied cases included a gap width of $t =$ 1 mm, 2 mm, and 2.5 mm. The gap was located at the center of the board. The effect of changing the neck location was studied as well. In these cases, the neck width was kept unchanged at $e = 5$ mm, while $d = 15$, 20, and 25 mm. The gap was at the center of the board, and $t = 2$ mm. The $|S_{21}|$ results indicated little change for these cases. Another three cases are shown in Fig. 11 where $d = 25$ mm, $e = 5$ mm, $t = 2$ mm, and $c = 29$, 39, and 49 mm. The change of gap location results in a change of the relative sizes of the two segmented portions, thus moving the resonant frequencies associated with these dimensions. The first resonance was a lumped resonance due to the inductance of the bridge with the interplane capacitance of each segmented plane portion (a lumped π network). The change of gap location changed the value of each capacitance. However, when c was changed from 49 mm to 39 mm, the first resonance had little change, which is surmised that the change of the capacitance values might not be significant enough to affect the performance of the π network. And, when c was changed to 29 mm, the two capacitances had such different values that the first resonant frequency started to shift. The second resonant frequencies in all three cases were associated with board dimensions. When $c = 49$ mm, the second resonance was due to the TM_{01} mode, in other words associated with the 55 mm edge. When $c = 39$ mm, the second resonance was associated with the longer edge of the larger segmented plane portion (59 mm), which possibly overlapped with the resonance associated with the TM_{01} mode. The second resonant frequency was close to 1.5 GHz for the test board in these two cases. However, when $c = 29$ mm, the second resonance was associated with a 69 mm edge (the longer dimension of the larger segmented plane portion), which corresponded to 1.2 GHz in frequency. The resonance associated with the TM_{01} mode became the third resonance in this case. The behaviors in all three cases were quite different over a broad frequency range, though the coupling between the two portions was negligibly impacted. Overall, the few cases studied here for a conducting neck indicate that its configuration has insignificant impact on power-bus noise isolation.

A conducting neck is used when the segmented portions have the same logic level. Similar to the power island cases, using a ferrite bead connection, rather than a conducting bridge, results in much better noise isolation, as indicated in the previous power island case. Sometimes, totally isolated power planes are used to provide power supplies that are required by many IC devices. Since there is no direct conducting path for the noise, a considerable power-bus isolation can be achieved, especially at low frequencies. In addition, at higher frequencies, the modal coupling across the gap can be reduced, and some wave modes can be disturbed due to the segmentation. As a result, some board resonances disappear, or move to higher frequencies corresponding to the wave modes excited by the smaller power areas. In general, the structures of the segmentation have a great impact on the power-bus excitation, and noise isolation. For example, the TM_{10} mode cannot be excited on the power plane with a complete gap in the middle, while the same gap does not impact the TM_{20} mode. Therefore, many designs of power areas and gaps have been tested in an attempt to improve the power-bus isolation [4]. An approach using meandering lines for isolating the power areas was also studied herein. Since the currents and charges must satisfy the boundary conditions at the meandering line edges, it is difficult for some wave modes to be established on the power plane, and potentially, the power-bus excitation is minimized, and the noise isolation is improved. However, the method of using meandering gap lines may introduce some difficulties in component placement. As a compromise, the meandering lines can be routed in a small area so that the power-plane segmentation has little impact on the layout.

Three shapes of gap lines were studied with the CEMPIE approach. The test board had the same configuration as in Fig. 1. The test port locations were identical. However, in this study, the top power plane was divided into two totally isolated large power areas. Three gap configurations were modeled, a straight line, a square meander, and a sawtooth meander, as shown in

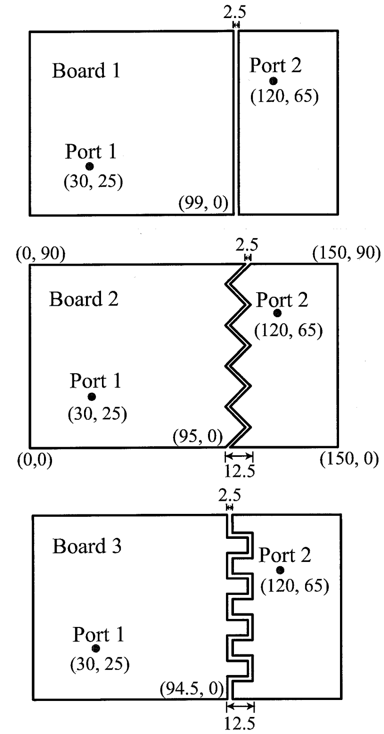

Fig. 12. Two totally isolated power areas with three gap shapes. Units are in mm.

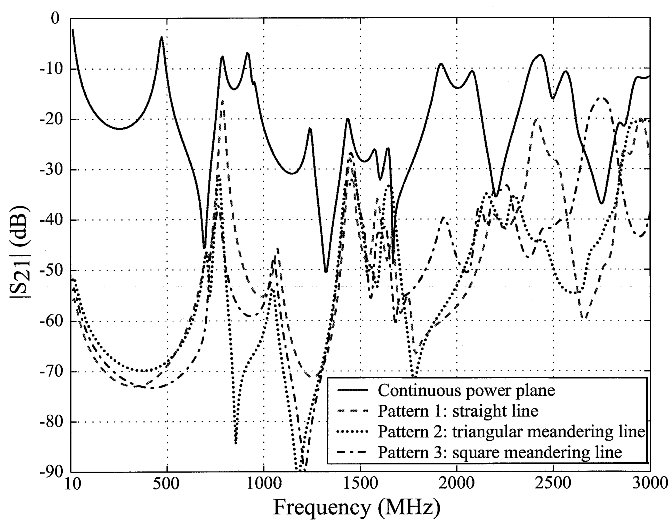

Fig. 13. The modeled $|S_{21}|$ for two totally isolated power areas with three gap shapes.

Fig. 12. The gap width was 2.5 mm in all three cases. In the first design, the two large power areas were isolated by a straight gap. The dimensions of the power areas were 9.9 cm $\times$ 9 cm, and 4.85 cm $\times$ 9 cm. Triangular and square shape meandering lines were used in the other two cases. The meandering lines were confined to a 1.25 cm $\times$ 9 cm area, and the two power areas maintained approximately the same size as in the case of a straight gap. The CEMPIE modeling approach was employed to determine the $|S_{21}|$. The vertical interconnects of the ports were modeled. The modeled $|S_{21}|$ results for these three gap shapes are compared in Fig. 13. There were approximately 10-

and 15-dB decreases of the peaks at 735 MHz with the meandering gap lines as compared to the case of straight gap line. The peaks were resonances due to the short edge dimension of the board (90 mm), and also the long edge of the larger power area (99 mm). The corresponding wave modes were disturbed by the meandering gap lines, and therefore the peak values varied at the same observation port. At frequencies beyond 1 GHz, some peaks shifted in frequency, but the general envelopes of these $|S_{21}|$ peaks were approximately the same. In general, the three studied gap shapes did not show significant difference with regard to the noise isolation. However, comparing the $|S_{21}|$ of a continuous power plane, the reduction of using two totally isolated power areas was more than 10 dB at most frequencies. At low frequencies, the reduction was up to 40 dB. The totally isolated power planes have a high degree of power-bus noise isolation, but the high-frequency noise isolation can also be achieved for power planes with dc continuity using the π network described in the previous section for power islands.

IV. Conclusion

Both segmented power planes and power islands were studied in this paper. Comparing with a continuous power plane, complete segmentation (no dc connection) can achieve significant power-bus noise isolation. A conducting bridge to provide dc connection greatly degrades the isolation at low frequencies. A better approach to provide dc continuity was found to be using a ferrite bead. With added lumped capacitors to form a π network, the power-bus isolation can be improved by an additional 10 dB over a ferrite bead connection in a wide frequency range. The CEMPIE approach is a powerful tool to model the power-plane segmentations, and a design approach was developed with this method to achieve significant noise isolation between different power areas.

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