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DC Transmission Grid with Low Speed Protection using Mechanical DC Circuit Breakers

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***Abstract*--This paper introduces a DC transmission grid with fault tolerant inductor-capacitor-inductor (LCL) voltage source converters (VSCs) and using slow protection system based on mechanical DC circuit breakers (CBs). LCL VSC inherently regulates DC fault current to levels that converter can sustain for prolonged periods which avoids IGBT tripping and brings significant advantage in security and reliability aspects. Simple mechanical DC CBs are used at DC bus bars and connecting points of each DC cable, in the same manner as it is normal practice used with AC transmission protection. The protection logic is based on differential methods which gives excellent selectivity and reliability. The fault clearing time is in the order of *30-60ms* which allows for reliable protection decision making. The simulation results obtained from a four-terminal DC grid modeled on PSCAD platform confirm successful DC fault isolation and grid recovery for a range of severe DC fault scenarios.**

Index Terms-- **HVDC transmission, Protection, Fault Tolerance, Converters, Fault Detection, Circuit Breaker.**

I. Introduction

The DC grid technology is considered as a technical advance obtained from VSC-based HVDC and Modular Multilevel Converter (MMC) HVDC [1, 2]. It provides an attractive approach for offshore renewable energy transmission in Europe. However, both the protection system and DC CBs for the DC grid are much more technically challenging than with the traditional AC system. Low DC impedances make DC fault levels very high and absence of natural zero crossings of fault current implies different technology requirement for fault interrupting equipment [3].

Several DC grid protection schemes have been recently presented in [4-6]. The DC fault can be easily cleared by tripping mechanical AC CBs in the AC switchyard. However, the clearance time is within *50-100ms* and the whole DC grid should be tripped for a single DC fault [4].

A DC CB is required to maintain integrity and security of power transfer in DC grids [3]. Semiconductor-based DC CBs or hybrid ones [5] can interrupt high DC currents within a few milliseconds but their cost is very high. The limited current interrupting capability of semiconductor-based DC CBs implies that protection system must be very fast in order to interrupt fault current on the rising slope within *2-5ms* before it reaches full fault level. This is a challenge for protection system considering that the fault propagation and communication times between several DC CBs would take considerable time in particular for long DC transmission cables [6]. It is also very challenging to develop protection logic without communication because of low DC cable impedance [3].

The importance of limiting DC fault current magnitude has been widely recognized [7-10]. The superconducting fault current limiter approach is a good candidate for DC CB but this technology cost is high, it is immature, and it cannot completely interrupt DC fault currents [7].

Fault tolerant DC/DC converter is another solution proposed to limit DC fault current and isolate the faulty section in a DC grid [8]. In addition, they can provide the capability of voltage stepping and power regulation in a DC grid. Also, the fault isolation is achieved by using only local signals with no need for grid-wide co-ordination [8]. On the downside, the DC/DC converter has higher losses, very high cost and increases the complexity of the whole DC grid.

An alternative approach is to limit DC fault current by developing a fault tolerant VSC. If all DC grid terminals can limit DC fault currents infeed from AC sources, then fault levels will be low in all inner DC cables. Low fault levels imply lower costly DC CBs and also fewer requirements for fast fault clearance. The mechanical DC CBs can then be used which have been demonstrated as 250kV, 8kA prototypes [9] and recently for 80kV, 10kA [10]. Smaller rated versions are commercially available in the market and are normally employed as metallic return transfer breakers to switch mono/bi-polar HVDC operation. Comparing with semiconductor-based DC CB, their cost, loss, and complexity are much lower. It is worthwhile mentioning the fault tolerant VSC can also reduce impact of DC faults on the AC grid.

One method to achieve fault tolerant VSC is using alternate arm multilevel converter or MMC with full bridge or clamp double half bridge sub-modules [11]. Such converters can maintain controllability under AC and DC faults. On the downside, these converters require considerably more power switches than conventional VSCs which increase costs.

The LCL fault tolerant two level VSC has been proposed and studied in depth [12]. The studies show that the converter has capability to limit the DC fault current close to the rated current value in the event of a DC fault.

This article proposes building DC grids using LCL VSCs and mechanical DC CBs. The protection system for selective fault isolation considering fault wave propagation and

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communication delays will be studied. An accurate DC grid and protection model will be developed to study in depth the properties of such protection approach.

II. Fault-tolerant DC Grid Test System

Fig. 1 shows the 1000MW, symmetrical monopole four-terminal DC grid test system model developed in PSCAD (the grid rating is sum of all terminals ratings divided by two).

This is a loop DC grid that can represent any practical offshore DC system such as North Sea DC grid [13]. It includes *±300kV* symmetrical monopole VSCs. They are connected to each other via *600km* DC transmission cables. All four LCL VSCs have two-level topology using sinusoidal pulse width modulation with *1350Hz* switching frequency, which is adopted for convenience of simulation. It is known that MMC half-bridge VSCs have very similar DC fault behavior and we believe that our conclusions equally apply if all terminals use such multi-level VSCs.

Each DC cable has one DC CB at every end. The protection relays and current sensors are located at each CB location. Positive current direction is assumed to be from VSCs towards DC grid for bus bar located sensors, and from bus bars towards middle of DC cable for cable ends current sensors. There is a dedicated communication channel (fiber optic) along each DC cable providing a communication path between the two DC CBs at each cable. The protection system operating times are similar as with AC system protection and similar equipment can be employed.

The DC grid control employs VSC1 terminal to control DC voltage while the active power flow is regulated at all other VSC terminals (with additional DC voltage droop) [14]. In Fig. 1, the positive sign of power indicates sending power from VSC terminal towards DC grid.

III. Fault Tolerant LCL VSC

The fault tolerant LCL VSC topology is shown in Fig. 2. This topology consists of a two-level VSC provided with a passive LCL circuit and detailed design is given in [12]. The converter has all active and reactive control properties as any other VSC. In addition, the converter has capability to limit the DC fault current inherently by appropriate selection of LCL circuit inductors and capacitor. During the DC fault, the voltage depression will cause the grid side current inherent reduction [12]. The LCL circuit parameters design is a trade-off between the optimum efficiency and fault current limitation to reasonable levels.

Assuming that an n-terminal DC grid employs LCL converters at all terminals, the total fault level will be approximately sum of all VSCs rated DC currents. Therefore depending on the fault location the fault current in a cable DC CB will be between zero and the total DC grid fault level. As an example, a 20-terminal DC grid with *1kA* nominal DC current at each terminal will have no more than *20kA* fault current at any point.

The designed values of LCL VSCs passive components are shown in Table I. Note that although large reactors are needed for LCL circuits, no extra ac transformer or series reactors normally used with conventional VSCs are required. The size of LCL components is similar to a comparable transformer. Additionally, the converter archives better efficiency compared to a usual VSC as there would be zero reactive power circulation through the converter [15]. This also implies lower power electronics cost for this converter construction due to lower current rating of the power switches.

IV. Mechanical DC Circuit Breaker

Fig. 1 shows that mechanical DC CBs are located at each DC bus bar (DCCBi, *i=1,2,3,4*) and both sides of each DC cable (DCCBij, *i,j=1,2,3,4*). The breaker model is shown in Fig. 3. The detailed CB design procedure and components are presented in [9]. Fig. 4 shows the circuit breaker parameters for *9kA* peak interrupting currents. This value is obtained for bus bar and cable located DC CBs considering fault current in the test DC grid for worst case pole-pole faults. The value of *9kA* includes fault current and superimposed resonance circuit current. In order to enable breaker commutation, the maximum allowed current derivative is selected as $50A/\mu s$. This leads to breaker auxiliary passive circuit with a capacitor of $6.7\mu F$ and inductor of $6mH$.

The total mechanical DC CBs contact opening time is set to *60ms* in our model. The auxiliary breaker CB2 opening time delay is set to *1.5ms* after main breaker trips.

V. DC Grid Protection Model

The protection system follows the approach proposed in [6], where three protection systems are employed including:

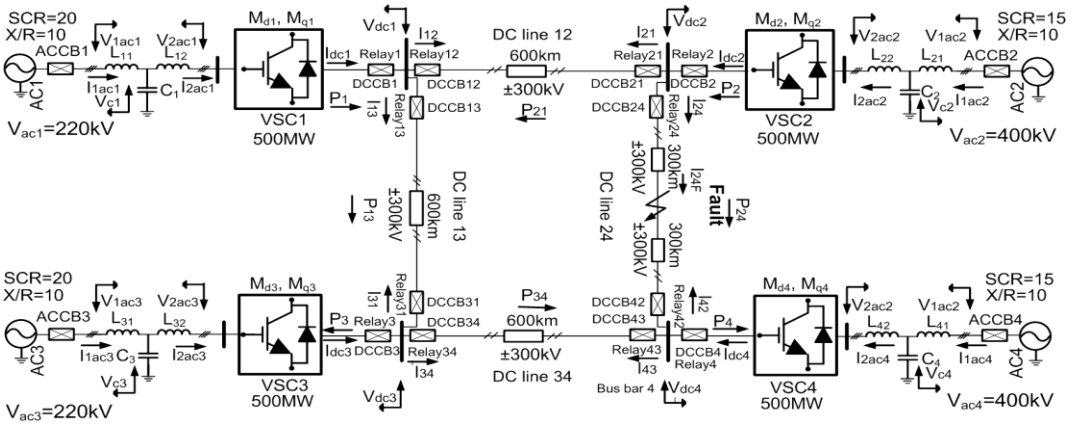

Fig. 1. 1000MW DC grid with DC CBs and fault tolerant VSCs.

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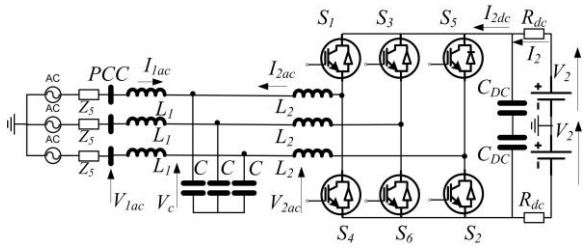

Fig. 2. Fault tolerant LCL VSC [12].

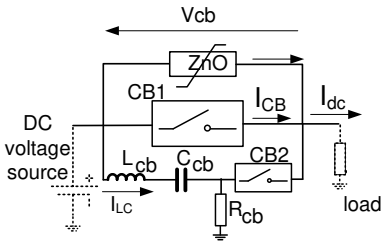

Fig. 3. Mechanical DC circuit breaker [9].

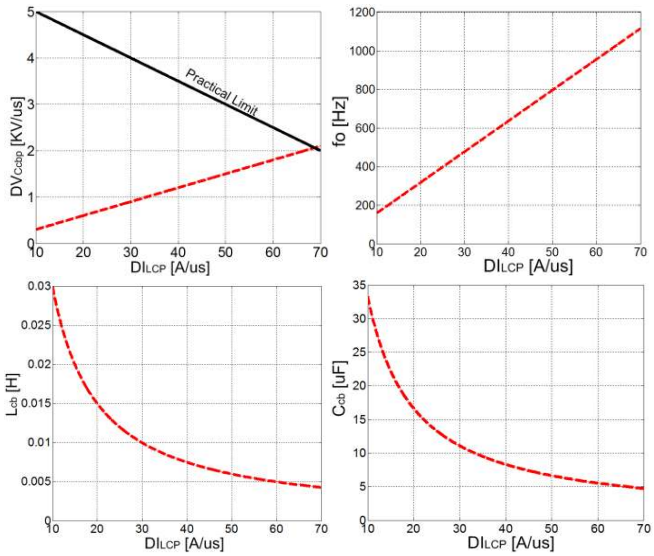

Fig. 4. Mechanical DC CB parameters for a range of resonance current derivative.

- DC transmission cable differential protection (for simplicity we just quote DC cable afterwards),
- DC bus bar protection,
- Backup protection,

The DC transmission cable protection detects a fault occurring on a main DC cable and sends trip signals to DC CBs at each end of the faulty cable. Both cables are tripped in case of symmetrical monopole, while only the faulted pole is tripped if bipole DC grid is considered. The DC bus bar protection isolates any DC fault occurring at a bus bar. It sends trip signals to all cable and bus bar DC CBs connected to the faulty bus bar. Finally, a backup protection is designed to trip appropriately the minimum number of DC CBs in the event of any DC CB failure to operate. While the study in [6] considers semiconductor-based DC CBs, we will assume mechanical DC CBs with detailed models and communication delays.

A. DC transmission cable protection

The DC cable protection consists of fault detection and CB tripping. The selective detection of a fault is based on the evaluation of differential currents obtained at all protection relays. In Fig. 1, the differential currents are defined as:

$$I_{diffij} = I_{ij} + I_{jiD} \quad (i, j = 1,2,3,4, i \neq j) \qquad (1)$$

where subscript D is used to indicate communication delay (signal received at station *i*). It is seen that I_{diffij} is the sum of the two DC currents measured at each end of the DC cable.

When a fault occurs on a DC cable, the DC current flowing through one end of the cable is not the same as the current flowing at the other end. This is a consequence of wave propagation delays from the fault location to the relay locations at the cable ends. Also, VSC terminal arrangements in a DC grid can cause unequal fault currents at faulty cable ends. Considering that all cable current sensors are placed in the adopted direction, the faulty cable differential current increases quickly and reaches a large positive value. This can be used as an indication of the faulty cable since all healthy cables will measure a negative differential current after the fault. The relays on the healthy cables which are closer to the faulty cable will see fault wave earlier than other relays. In addition, at any time the measured currents at the healthy cable's current sensors closer to the faulty cable will be larger than measured values at the other side due to fault wave attenuation over the transmission cable.

Differential currents measured at all cable breakers are then compared with a positive threshold to detect the fault location. In order to detect faults but to avoid unwanted DC CB opening, protection threshold value is selected as *3.5kA*.

Note that wave propagation delay is modeled by using a detailed DC cable model [6]. A relay communication delay is taken into account in this study as a transport delay to model limited speed of optical fiber signal propagation between the two ends of a cable. The communication delay is depicted in Fig. 5. It is seen that the communication delay between Relay 24 and Relay42 is T_c*=3ms* (considering cable length of *600km* and light speed of *200km/ms* through the fiber optic).

TABLE I LCL VSC PASSIVE COMPONENTS DATA

	L_1(mH)	C(μF)	L_2(mH)	C_{DC}(μF)
VSC1	302	10.1	101	100
VSC2	610	11.8	510	100
VSC3	302	10.1	101	100
VSC4	610	11.8	510	100

B. DC bus bar protection

Since the DC cable protection would not detect any bus bar fault, a bus bar protection is also required. The bus bar protection algorithm is also based on evaluation of differential current obtained for each bus bar and its comparison to a threshold value. The bus bar differential currents are calculated as:

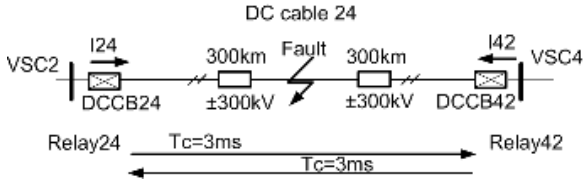

Fig. 5. Communication delay between cable ends relays.

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$$I_{diff\_bi} = I_{dci} - \sum I_{ij} \quad (i, j = 1,2,3,4, i \neq j) \qquad (2)$$

where I_{ij} are the DC cable currents connected to the bus bar i. Given that current sensors are located appropriately as is discussed for the studied grid shown in Fig. 1, the bus bar differential current would be zero in normal operation. When a fault occurs at a bus bar, the differential current (2) increases very fast and exceeds a positive threshold value. This provides an indication for the faulty bus bar, and all DC breakers connected to the faulted bus bar will be tripped immediately (including cable breakers and bus bar breakers). There is no communication delay between these DC CBs because they are installed at the same location.

C. Backup protection

In case of failure of the cable or bus bar protection, a backup protection is required in the grid system. If the cable/bus bar protection operates properly, the cable/bus bar current will drop close to zero after the DC CBs opening time. On the other hand, the current will stay at a large value if the protection fails to operate. Therefore, it is concluded that the protection is failed if the current is still larger than a small threshold value after a specific time, which is set to *20ms* after the trip signal, in this study.

If a cable DC CB failed to open and cable differential protection initiated triggering the breaker, then all the other DC CBs connected to the bus bar will be tripped. On the other hand, if bus bar protection triggered the cable DC CB which failed to open, then the DC CB located at the other end of the cable will be opened. This will require a communication delay between the two cable DC CBs. If bus bar DC CB failed to operate, then the faulted terminal will be isolated using AC CB from AC switchyard.

Note that the backup threshold value is set to a small current of *50A* to avoid misdetection in the test system.

VI. PSCAD Simulation Results and Discussions

A. DC cable model testing

An accurate frequency-dependent (from *0.1 Hz* to *10 kHz*) underground *300kV* DC cable model with distributed parameters is used in this study in order to represent accurately travelling wave propagation. The DC cable involves two layers of insulation with appropriate sheath as is shown in Fig. 6. Each cable is represented as two series segments in order to allow for cable fault simulation.

In order to validate the wave propagation delay in the cable model, a pole-pole DC fault is applied at the middle point of DC cable *24* at *1.5s*. The DC fault is not cleared in this simulation. Fig. 7 shows the measured currents at the healthy end of the cable 24 close to terminal 2 (I_{24} in Fig. 1) and faulty mid-point of cable 24 (I_{24F} in Fig. 1). It can be seen that I_{24} has attenuated transient response with around *1ms* delay compared to I_{24F} (Kirchhoff's Circuit Law is not valid for faulty cable during the transients due to large cable length compared to wavelength of the fault propagating wave).

B. Testing fault current magnitudes in DC grid

In order to determine the required current rating for all cable DC CBs and bus bar DC CBs a range of DC faults is applied and worst case magnitudes are observed at each point. We are further interested to understand how this fault current evolves during the fault period since fault clearing time and protection system logic are not certain in large DC grids. In addition we are interested in fault current value in the VSC converters when they are part of a large DC grid, since [12] only tests a single LCL VSC in isolation.

We study one representative solid DC fault (0.1mΩ), in the middle of cable 24, which is not isolated. The DC fault current through four bus bar DC CBs and the eight cable DC CBs are shown in Fig. 8, where IGBTs are not tripped.

VSCs 2, and 4 capacitors will cause large short transient fault currents as they are close to the fault point, but they rapidly discharge and the fault currents are close to rated currents within *5-10ms* after the fault.

The VSCs 1, and 3 are further away from the fault and they do not see sharp first peak. However it is seen that their DC fault currents have longer time constants, and reduce to *2p.u.* after around *100ms* and settle to *1p.u.* after *200ms*. This implies that worst case situation for bus bar DC CBs dimensioning are remote DC faults. Note however that AC currents (currents in IGBTs) are substantially lower, as shown in Section VI.C and that there is no need for IGBT overrating.

The fault currents in all DC CBs settle to *1-2pu*, after an initial transient with time constant of *150-200ms* and reach the initial peak of *3-12p.u.* depending on location in the grid.

Fig. 8 shows that DC CB interrupting current is inversely dependent on the fault clearance time. A longer fault isolation results in lower fault current interruption.

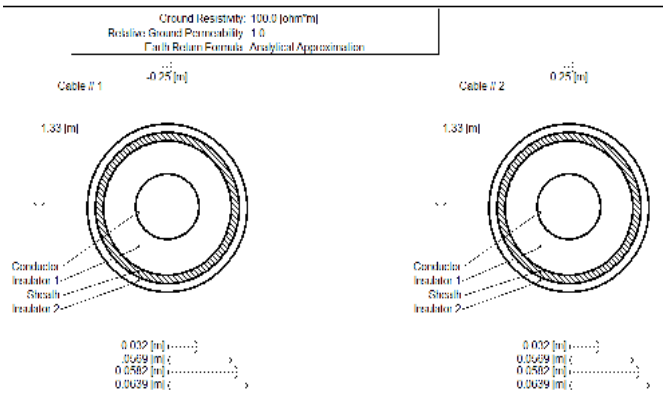

Fig. 6. DC cable model details.

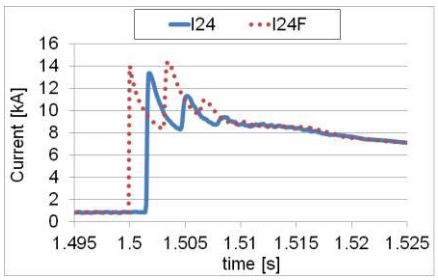

Fig. 7. I_{24} and I_{24F} for a pole-pole fault at the middle point of DC cable 24.

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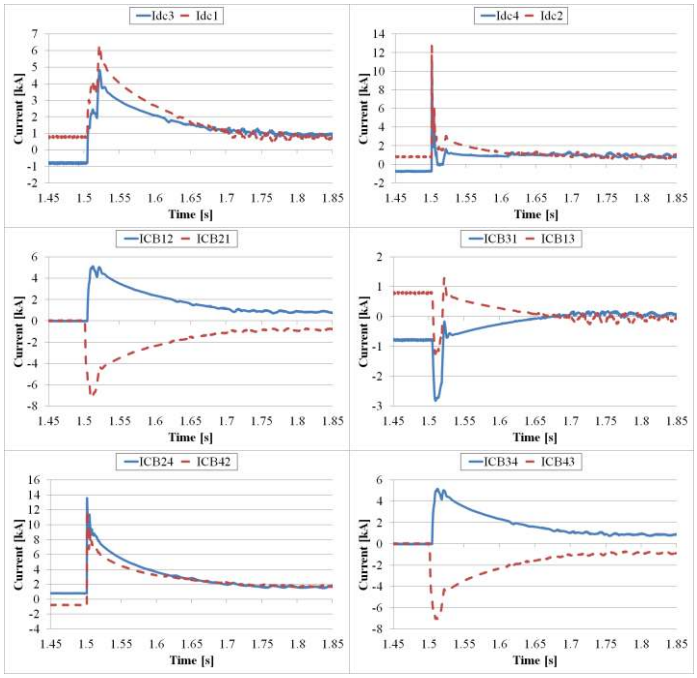

Fig. 8. Currents in VSCs (bus bar DC CBs) and cable DC CBs following a permanent non-isolated DC fault.

C. DC cable protection algorithm testing

In order to evaluate the performance of proposed DC grid protection against DC faults at different locations including faults on bus bars, and to test back up protection, six DC fault scenarios are developed, as shown in Table II.

Fig. 9 shows differential currents obtained for the eight DC CBs relays in case study A. It is seen that only the differential currents on the faulted cable 24 are positive which confirms the selection logic. The DC voltage and power variables at each VSC terminal in case A are shown in Fig. 10. It is seen that the DC voltages (V_{dc1}-V_{dc4} shown in Fig. 1) are recovering to *600kV* at each terminal after fault isolation. The powers (P_1-P_4 shown in Fig. 1) are also regulated at pre-fault values at each terminal and stay unchanged after the fault clearance since power flow is accordingly redirected.

The breakers DCCB24 and DCCB42 variables are shown in Fig. 11. I_{CB24} and I_{CB42} are the main circuit breaker currents. The mechanical DCCB resonance circuit current added to the fault current at the clearance time is shown in this figure. V_{cb24} and V_{cb42} are voltages across the main breaker (as labeled in Fig. 3). It is seen that the fault current at the clearance time is around *4.5kA* while the peak current during the fault reaches up to *14kA*.

TABLE II TEST SCENARIOS OF STUDIED DC GRID

Fault case	Description
A	Pole-pole fault at the middle of DC cable *24*. DCCB24 and DCCB42 are opened.
B	Pole-pole fault at DC cable *24*, *500km* from VSC2, *100km* from VSC4. DCCB24 and DCCB42 are opened.
C	Pole-pole fault at DC bus bar 2. DCCB24, DCCB21 and DCCB2 are opened.
D	Pole-pole fault at the middle of DC cable *24*. DCCB24 failed to operate.
E	Pole-pole fault at DC bus bar 2. DCCB24 failed to operate.
F	Pole-pole fault at DC bus bar 2. DCCB2 failed to operate.

Healthy cables' DCCBs and VSC DC currents are shown in Fig. 12. Large equivalent cable inductance from VSCs 1 and 3 to the fault point leads to slow VSCs 1 and 3 capacitor discharge and causes slow DC CBs current decay. This implies that longer clearance time is preferred which is completely different argument compared to DC grids employing usual VSCs. The only issue with longer clearance time is the AC system stability which could be affected for weak AC systems connected to the DC grid. In this case, mechanical DC CBs can be designed for faster operation with higher cost but the cost still would be much lower than semiconductor-based approaches. In the modelled DC grid, the total fault clearing time is considered as *60ms*.

The currents in DC cables will be equal to those shown in corresponding DCCBs. However, there is no concern for possible cable damage since large mass and heat dissipation area make DC cable thermal constants in the order of minutes.

In [12] all DC faults are applied at VSC DC terminals, and fault current magnitudes are close to rated currents with short transient peaks. In this study it was found that faults on DC cables (further away from VSC DC terminals) will cause much longer transients with high currents, but the steady-state fault current will be around *1pu* as in [12]. As far as DC CB rating is concerned, the faults further away from VSC terminals are worst case conditions (for a given clearance time). Based solely on steady-state fault conditions, each cable DC CB should be rated to around *2kA* (sum of fault currents from two VSCs) in the modeled DC grid, but since trip time is *60ms*, the interrupting current is *4.5kA*.

The AC variables of each VSC converter in case study A are shown in Fig. 13. These results show that the maximum fault currents at VSCs AC sides are within *2 p.u.* as is predicted from converter design. It can be concluded that the maximum IGBTs/diodes currents are lower than double peak

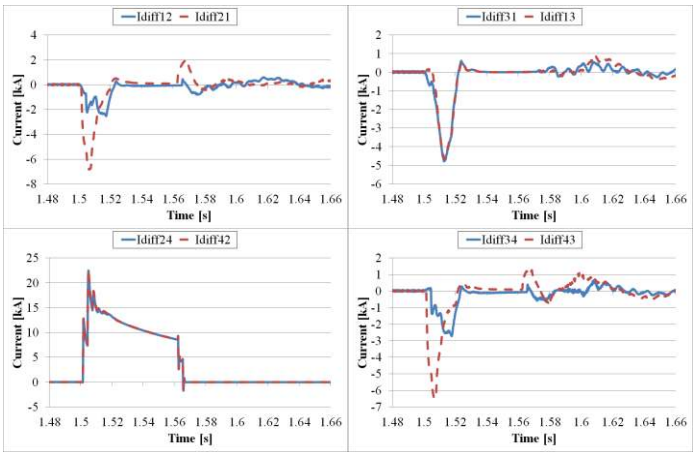

Fig. 9. Differential currents in case A.

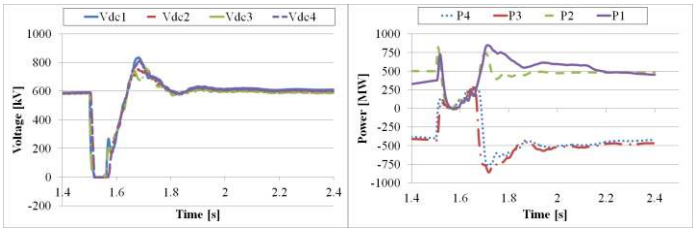

Fig. 10. VSC terminals DC voltages and powers in case A.

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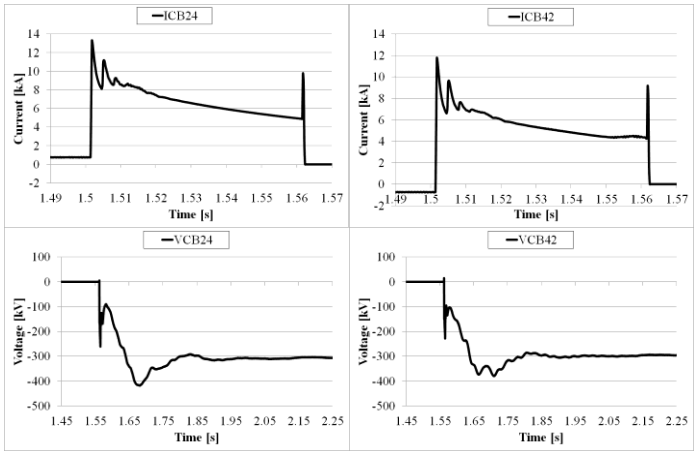

Fig. 11. Cable *24* DC CBs voltages and currents in case A.

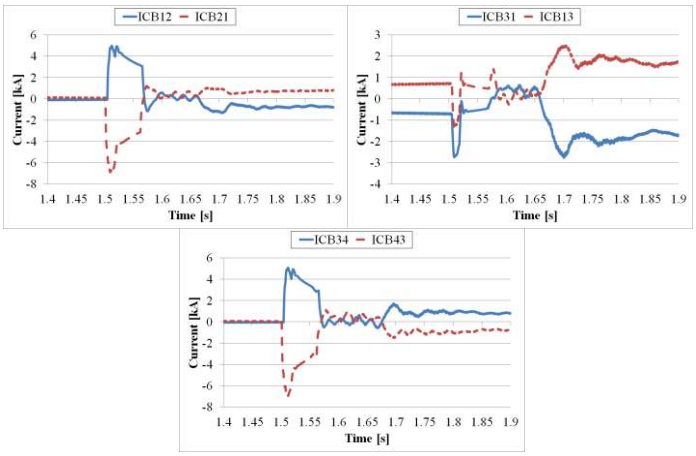

Fig. 12. Currents in CBs in healthy cables for case A.

current in normal operation. This is an important benefit for LCL VSCs and proposed DC grid, because there is no requirements for IGBTs/diodes overdesign.

Additionally, IGBTs are not tripped during DC faults and fault clearing time is not important for the converters. It is further observed that there is no AC voltage depression during the DC fault and the voltages at PCCs stay close to the rated values (DC fault is not transferred to the converters AC side).

There is no high overvoltage on the LCL circuit capacitors either. The results show that the presented DC grid has a good fault tolerant performance under this extreme fault condition.

D. Fault scenario B

The scenario B is introduced to test protection algorithm performance for DC faults at different locations along DC cable. In this case, DCCB42 will receive the trip signal earlier than DCCB24 since fault is closer to VSC4. As a result, DCCB42 will be opened earlier and the fault current is redistributed before DCCB24 opens. Fig. 14 shows the DC cable *24* CBs trip signals and cables differential currents in case B. It is seen that faulty cable CBs are tripped at different times as is expected, whilst other breakers stay closed. Note that due to the lack of space different DCCBs and LCL VSCs detailed variables are just demonstrated for case study A.

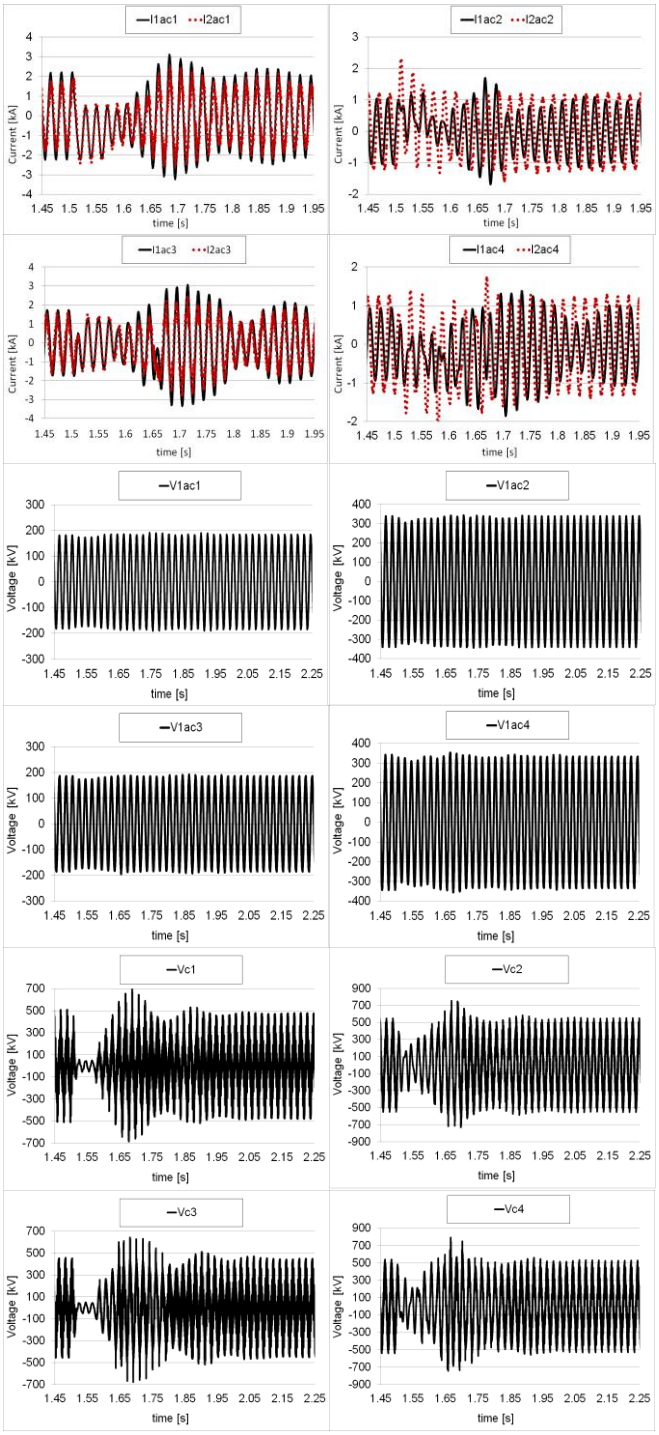

Fig. 13. VSC terminals AC variables in case A.

E. Fault Scenario C

A DC bus bar fault is simulated based on scenario C. Fig. 15 shows the bus bar protection signal generated based on DC bus bars differential currents evaluation.

The DC voltage and power variables at each VSC terminal for DC bus bar fault are shown in Fig. 16. It can be seen that the VSC2 voltage (V_{dc2}) and power (P_2) drop to zero after fault clearance which implies the bus bar protection can isolate the faulty VSC from healthy parts of the grid. The voltages of VSC1, VSC3 and VSC4 recover back to the rated values after the fault clearance.

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The simulation results are shown for worst case when both VSCs 3 and 4 are receiving power while VSC2 has been isolated. It can be seen that VSCs 3 and 4 powers have been accordingly adjusted to new values to provide active power flow balance within the DC grid thanks to the droop control.

F. Fault scenario D

In order to evaluate the backup protection performance, the grid model is tested under scenarios D and E. In case D, a pole-pole fault is applied on cable *24* and DCCB24 fails to operate. Fig. 17 shows cable *24* differential currents as well as backup protection trigger signals generated. It is seen that no trigger signal is generated for DCCB24. However, breakers connected to the bus bar *2* (DCCB21 and DCCB2) are signaled after a *20ms* delay, thanks to the action of designed backup protection.

Fig. 18 shows the voltage and power variables of each VSC terminal and the cable powers in case D.

It is seen that VSC2 voltage and power as well as cables 24 and 21 powers drop to zero after the fault isolation indicating the faulty part is isolated by backup protection. As a result of two cables isolation, cable 13 is slightly overloaded in this case. In order to resolve this issue, VSC terminals reference powers should be accordingly adjusted if the fault is permanent.

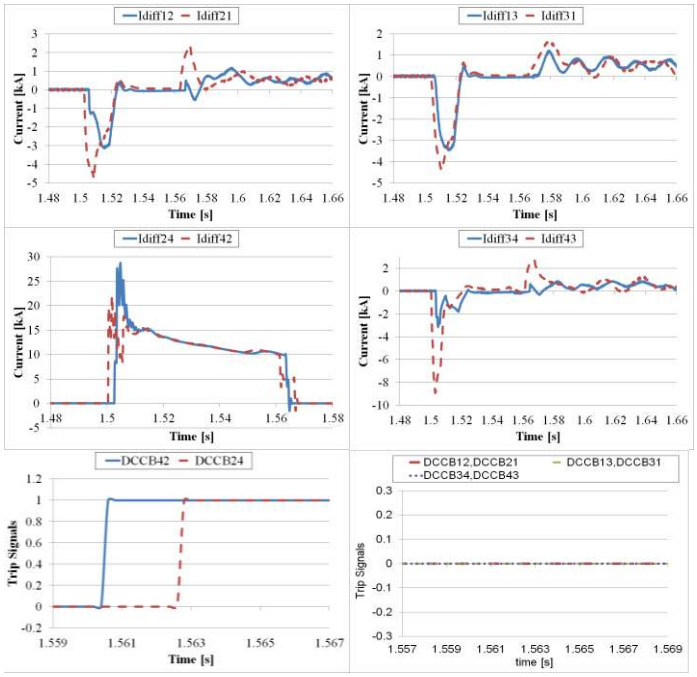

Fig. 14. Differential currents and CB trip signals for case B.

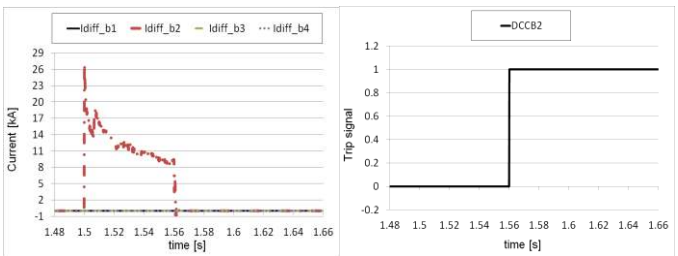

Fig. 15. Bus bars differential currents and DCCB2 trip signal in case C.

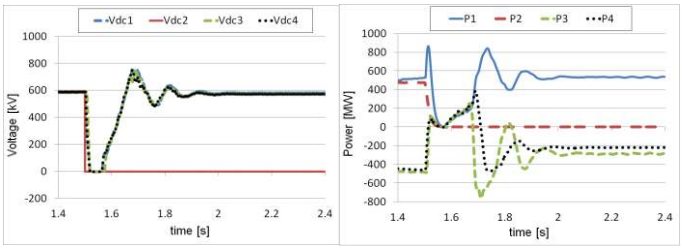

Fig. 16. VSC terminals DC voltages and powers under DC bus bar fault in case C.

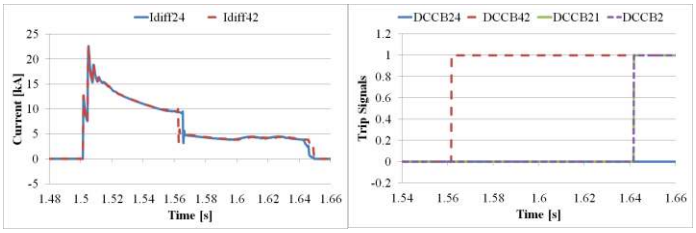

Fig. 17. DC cable *24* differential currents and DC CBs trip signals in case D.

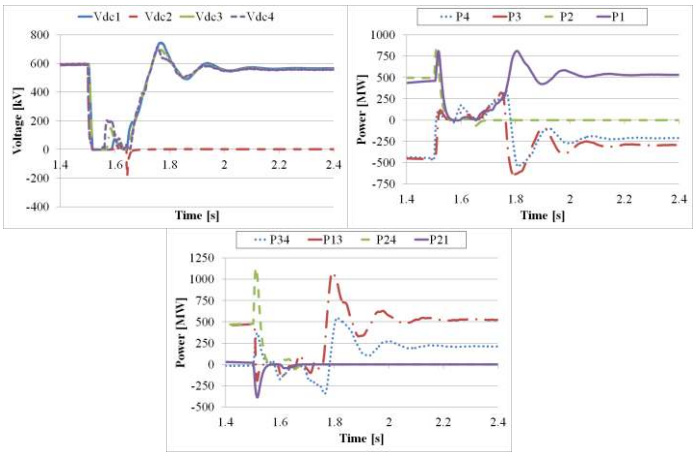

Fig. 18. VSC terminals and DC cables variables in case D.

G. Fault scenario E

To investigate the DC cable backup protection in the event of bus bar DC fault case study E is applied. Fig. 19 shows the DC cables *24*, *12* and DC bus bar *2* breakers trigger signals generated based on bus bar and back up protection. Assuming the DCCB24 fails to open, backup protection triggers the DCCB42 after a *20ms* delay. Since the backup trip signal is sent to the cable opposite end, there is additional *2ms* communication delay for back up breaker DCCB 42.

Fig. 20 shows the DC voltages and powers at each VSC terminal for case E. It is seen that the DC bus bar fault is isolated and the grid power balance is kept within healthy parts of DC grid.

H. Fault Scenario F

Fig. 21 shows the DC voltage and power variables at each VSC terminal in case study F. As is shown in Table II, DCCB2 fails to operate when a solid pole to pole fault is applied on VSC2 DC bus. Note that this is less critical scenario compared

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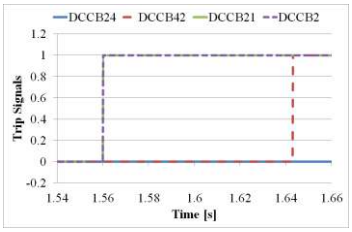

Fig. 19. DC CBs trip signals in case E.

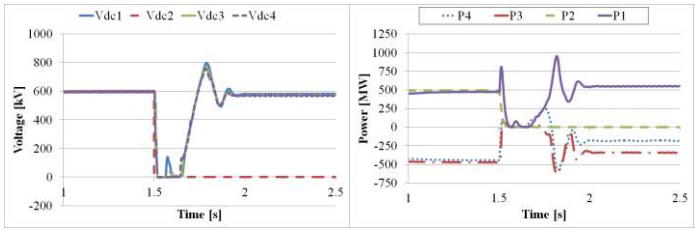

Fig. 20. VSC terminals DC voltages and powers in case E.

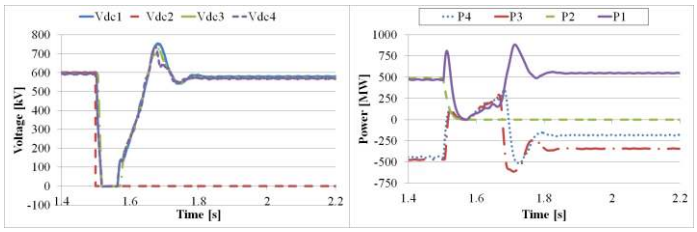

Fig. 21. VSC terminal DC voltages and powers in case F.

to case studies D, and E as the fault is isolated from the DC grid after 60ms. ACCB2 located at AC switchyard isolates VSC2 from AC grid thanks to the designed bus bar back up protection. It is observed that VSC2 voltage and power drop to zero permanently since the terminal is isolated from the grid system, and the remaining system recovers.

VII. Conclusion

A DC grid topology with fault tolerant LCL VSCs and mechanical DC CBs is proposed in this paper. The low cost and high reliability in fault isolation constitute the main advantages of the proposed DC grid. It is concluded that slow protection systems can be used since all grid terminals employ DC fault tolerant topology. Furthermore low DC fault levels imply fewer fault effects on the connected AC systems in the event of DC fault and allow deployment of mechanical DC CBs.

A detailed study on DC grid selective protection including three layers of cable differential protection, bus bar protection, and back up protection is presented.

A four-terminal *1GW* DC grid system is tested under several challenging DC fault scenarios developed on PSCAD platform. The simulation results show that the studied DC grid protection plan works properly and that fault clearance time is not critical.

It is demonstrated that longer fault clearance time results in lower mechanical DCCB total cost with no side effect on DC grid security during the fault. However faults further away from VSC terminals will generally cause higher interrupting currents for a given trip time.

Faster fault isolation is advised for weak AC grids which cannot tolerate power flow interruption for a long time. The protection system selectivity is confirmed for wide range of fault cases. The grid side AC currents at all terminals stay at low values during the faults confirming that proposed DC grid topology will not transfer faults to AC grids, and that VSCs neither need to be overdesigned nor to be tripped for DC faults.

VIII. References

[1] D. Jovcic, D. Van Hertem, K. Linden, J.-P. Taisne, and W. Grieshaber, "Feasibility of DC transmission networks," *in Proc. IEEE ISGT Europe*, Manchester, U.K., pp. 1–8 , Dec. 2011.

[2] J. Dorn, H.Huang, and D.Retzmann. "A new Multilevel Voltage-Sourced Converter Topology for HVDC Applications", *CIGRE 2008*, B4-304, Paris, 2008.

[3] D. Van Hertem, M. Ghandhari, J. B. Curis, O. Despouys, and A. Marzin, "Protection requirements for a multi-terminal meshed DC grid," *in Proc. Cigre Symp.,* Bologna, Italy, Sep. 2011.

[4] T.K. Vrana, S. Dennetière, Y. Yang, J. Jardini, D. Jovcic, and H. Saad, "The CIGRE B4 DC grid Test System," B4-57, 2013.

[5] J. Hafner and B. Jacobson, "Proactive hybrid HVDC breakers – A key innovation for reliable HVDC grids," in *Proc. 2011 CIGRE Bologna conf.*, pp. 1-8.

[6] J. Descloux, B. Raison, and J-B Curis, "Protection strategy for undersea MTDC grids," *in PowerTech, 2013 IEEE*, Grenoble, pp. 1-6, June 2013.

[7] H. Kraemer, W. Schmidt, B. Utz, B. Wacker, H. Neumueller, G. Ahlf, and R. Hartig, "Test of a 1Ka superconducting fault current limiter for DC applications," *IEEE Trans. Appl. Supercond.,* vol. 15, no. 2, pp. 1986-1989, June 2005.

[8] M. Hajian, D. Jovcic, and B. Wu, "Evaluation of Semiconductor Based Methods for Fault Isolation on High Voltage DC Grids," *IEEE Trans. on Smart Grids,* vol. 4, no. 2, pp. 1171-1179, June 2013.

[9] S.Tokuyama, K. Arimatsu, Y. Yoshioka, Y. Kato, and K. Hirata, "Development and Interrupting Tests on 250KV 8KA HVDC Circuit Breaker", *IEEE Transactions on Power Apparatus and Systems*, vol. PAS-104, no. 9, pp. 2453-2459, Sep. 1985.

[10] T. Eriksson, M. Backman, S. Halen "A low loss mechanical HVDC breaker for HVDC Grid applications" B4-303, CIGRE, Paris 2014

[11] M.M.C. Merlin, T.C. Green, P.D. Mitcheson, D.R. Trainer, D.R. Critchley, and R.W. Crookes, "A New Hybrid Multi-Level Voltage-Source Converter with DC Fault Blocking Capability," *9th IET International Conference on AC and DC Power Transmission, London*, pp. 1-5, Oct. 2010.

[12] D. Jovcic, L. Zhang, and M. Hajian, 'LCL VSC Converter for High Power Applications', *IEEE Transaction on Power Delivery,* vol. 28, no. 1, pp. 137-144, Jan. 2013.

[13] D. Van Hertem and M. Ghandhari, "Multi-terminal VSC HVDC for European supergrid: Obstacles," *Renewable and Sustainable Energy Reviews*, vol. 14, no. 9, pp: 3156-3163, Dec. 2010.

[14] A. M. Alsseid, D. Jovcic, and A. Starkey, "Small signal modelling and stability analysis of multiterminal VSC-HVDC," *Power Electronics and Applications*, *Proceedings of the 2011-14th European Conference on*, pp.1-10, 2011.

[15] W. Lin, and D. Jovcic, 'LCL and L-VSC converters with DC fault current limiting property and minimal power losses', IEEE Trans. On Power Delivery, 2014, DOI:10.1109/TPWRD.2014.2314481.

[16] Y. Jiang-Hafner, M. Hyttinen, and B. Paajarvi, "On the short circuit current contribution of HVDC Light," *Transmission and Distribution Conference and Exhibition 2002*: *Asia Pacific. IEEE/PES*, vol.3, pp. 1926-1932, Oct. 2002.

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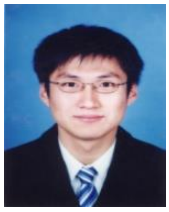

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