DC Voltage Balancing of Flying Converter Cell Active Rectifier

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***Abstract*—In order to reduce input current distortions and improve power factor of a passive three-phase diode bridge rectifier, an active add-on-option circuitry ("Flying Converter Cell") has been introduced recently. A novel voltage balancing concept for such an active three-phase rectifier which is based on the third harmonic injection principle using a Flying Converter Cell (FCC) is proposed in this paper. It is shown that the midpoint voltage of the FCC can advantageously be used for balancing of the DC capacitor voltages without disturbing the input currents. The proposed balancing concept can simply be added to the existing controller structure consisting of current controllers and a voltage controller. Using the proposed active balancing any losses of alternative passive balancing concepts (resistor networks) can be avoided which maximizes the system's efficiency.**

The proposed concept is described in a simple mathematical manner, limitations of the concept are derived and basic operation is verified by simulation results. Measurement results taken from a laboratory prototype with an output power of 10 kW finally demonstrate the good balancing characteristic of the proposed concept.

***Index Terms*—Three-Phase AC-DC Conversion, Input Current Quality, Third-Harmonic Injection, Voltage Balancing, Voltage Control**

I. Introduction

Over the last decades active three-phase rectifier circuits are gaining more and more importance, especially for switch-mode power supplies and AC drives where increasingly (i) low harmonic input/line currents ($\mathrm{THD_i} < 5\%$), (ii) high power factor ($\lambda > 0.99$) and (iii) high efficiency ($\eta > 95\%$) are mandatory ([1]). Numerous active three-phase rectifier topologies have been reported in literature which can achieve the mentioned requirements (e.g. the Vienna Rectifier Topology [2], bidirectional three-phase two level PWM rectifier,...). A very promising implementation of active three-phase rectifier circuits here is the third harmonic injection (THI) principle. A variety of active and passive third-harmonic injection rectifiers have already been discussed (cf., [3]–[12]). One of the mentioned proposed concepts is the topology shown in **Fig. 1**, known as "Flying Converter Cell" (FCC) rectifier ([8], [12]). The topology consists of two half bridges ($S_{\mathrm{cp}\pm}$ and $S_{\mathrm{cn}\pm}$) connected to the positive and negative busbar of the output of the passive diode bridge (D_1-D_6) and a three-level bridge leg (S_{h3}, $D_{\mathrm{h3}\pm}$) which is cyclically connected to one of the three mains phases (which is not conducting current) by three bidirectional switches (S_1-S_3). The FCC can furthermore be used as an extension/add-on-option for an already existing passive three-phase diode rectifier

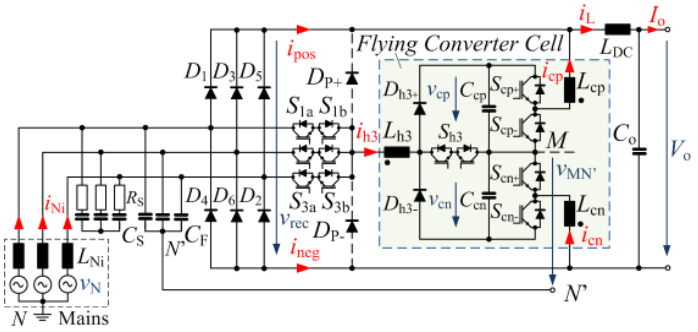


Fig. 1: Active rectifier circuit employing a "Flying" converter cell as proposed in [8] and [12].

(B6) which is one of the major advantages of this topology. As described in [8], the FCC circuitry only has to process about 6% of the rated output power and some amount of reactive power ($\approx 16\% \cdot P_{\mathrm{o}}$), which results in a high efficiency of the overall active system as the main part of the active power has to be drawn by the passive three-phase rectifier diodes.

One of the basic problems of the FCC is the implementation of the voltage control structure. Due to some restrictions (further explained in section III) the voltage controller has to be designed such to merely allow the regulation of the total DC voltage link $v_{\mathrm{cp}} + v_{\mathrm{cn}}$. A dedicated balancing of the cell's DC capacitor voltages v_{cp} and v_{cn} is therefore required. The most common way to assure balanced DC voltages is to add a set of passive balancing resistors in parallel to C_{cp} and C_{cn}. However, this effort will increase the permanent losses of the system. Another promising prospect is given by the use of an active balancing unit as described in [13]. The basic idea is to seperate the leakage current of the capacitor bank from the quiescent current of the voltage divider. This can be realized by either using a high voltage amplifier, bipolar transistors or MOSFETs. This active balancing concept, however, means an increase in complexity and requires additional hardware. The proposed DC voltage balancing concept, which is going to be adapted to an existing control algorithm, takes advantage of all three converter stages, which the FCC already consists of. The following sections describe the proposed DC voltage controller concept and an extended balancing perception considering the DC voltage capacitors C_{cp} and C_{cn} based on the generation of a low-frequency common-mode voltage $v_{\mathrm{MN,avg}}$ (initially

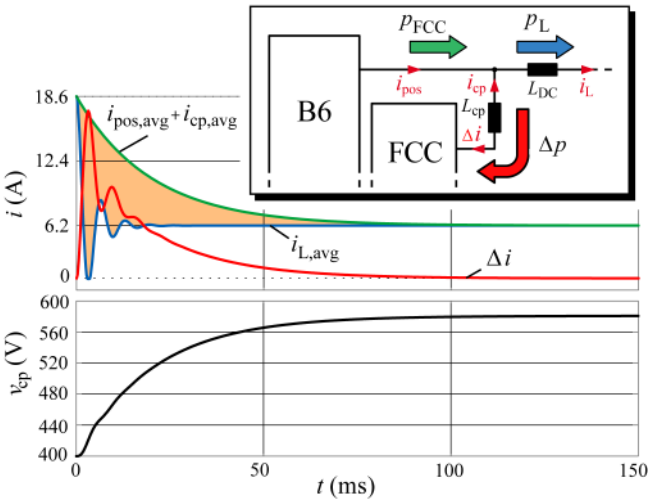


Fig. 2: Load step of the active system from 10 kW to 3 kW rated output power P_o. Due to the low dynamic of the FCC in case of low-pass filtering of the instantaneous power drawn by the diode bridge, the FCC has to deal with the averaged differential power Δp, which leads to an unfavourable increased FCC DC capacitor voltage level (no dedicated voltage controller assumed).

controlled as such to be zero via the three-level bridge leg) of specific shape.

II. DC Voltage Control Structure

The active rectifier system basically consists of two capacitor stages, the uncontrolled DC-link output voltage V_o and the FCC DC voltage $v_{cp}+v_{cn}$. In order to minimize the number of current and voltage sensors the reference current signals for both half bridges are generated by measuring the three mains voltages v_{N1}, v_{N2}, v_{N3} (or the passive rectifier output voltage $v_{rec}(\varphi_N)$) and the DC side smoothing inductor current i_L. By generation of v_{rec} via the mains voltages, the transferred power from the AC input to the DC output can be determined by

$$p(\varphi_N) = v_{rec}(\varphi_N) \cdot i_L(\varphi_N). \tag{1}$$

The given output power $p(\varphi_N)$ is however characterized by a low-frequency 300 Hz ripple component.

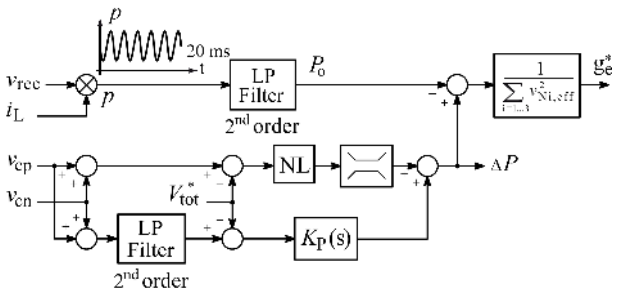
The averaged output power P_o can therefore be calculated by using a digitally implemented low-pass filter structure. The dynamic of the developed low-pass filter defines the performance of the step response considering the FCC.

The step response of the passive rectifier system however is affected by the passive LC output filter which can be described by

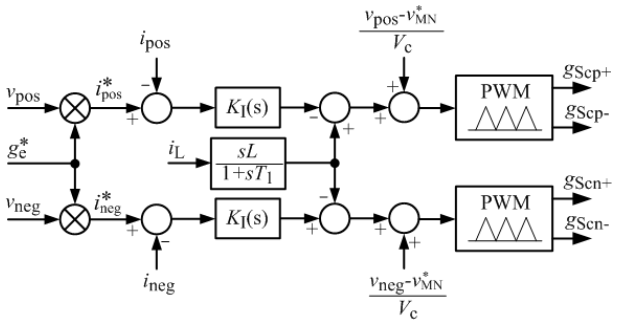
$$G(s) = \frac{i_o(s)}{i_L(s)} = \frac{1 + s2C_oR_{o,ESR}}{1 + s2C_o\left(\frac{R_{DC}}{2} + R_{o,ESR}\right) + s^2C_oL_{DC}} \tag{2}$$

where i_o defines the output current of the LC filter structure, $R_{o,ESR}$ the equivalent series resistance of the output capacitor and R_{DC} the DC resistance of the DC side smoothing inductor L_{DC}.

The required digital low-pass filter hence has to meet two different objectives. On the one hand the digital filter has to be able to compete with the dynamic behaviour of the passive LC filter system and on the other hand has to perfectly reject the



(a)



(b)

Fig. 3: (a) Voltage filtering and simple P-controller structure adapted by a non-linear controlling unit, which generate the mentioned additional output power ΔP further be used in order to evaluate the equivalent electrical conductance value g_e^*, and (b) controller strategies for current controller of i_{pos} and i_{neg}.

300 Hz output power ripple. In case of unsufficient damping, the generated nominal currents and hence the mains input currents will show increased 6th harmonic spectral components and therefore an impaired THD_i has to be expected. Considering lack of FCC system dynamic the FCC DC voltages will highly increase or decrease for load steps of the rectifier systems.

In order to illustrate the discussed issue more accurate, a load step of the active system (**Fig. 2**) is mathematically analyzed. The output filter is defined by $L_{DC} = 2.25\,\text{mH}$, $C_o = 1.1\,\text{mF}$, $R_{o,ESR} = 0.23\,\Omega$ and $R_{DC} = 0.3\,\Omega$. In order to demonstrate the effect on the DC capacitor voltages of the FCC due to a load step appearance, no DC voltage controller and a purely designed 50 Hz PT1 low-pass filter structure (in order to verify the value of the rated output power)

$$G_{PT1}(s) = \frac{1}{1 + sT_c} \tag{3}$$

are assumed. It has to be noted, that the current of the DC voltage capacitor connected to the positive half bridge is defined by $i_{ccp} = -\delta_{cp}i_{cp} + \delta_{h3}i_{Dh3+}$, whereby i_{Dh3+} denotes the current through D_{h3+} (diode of unidirectional three-level bridge leg) and hence only positive current values of i_{Dh3}. Due to the load step characterisitc from 10 kW to 3 kW the passive system immediately reacts with a response time of $\approx 2\,\text{ms}$. If a first order 50 Hz digital low-pass filter structure is assumed the proper output power is set after $\approx 100\,\text{ms}$. Till then the difference of real and fictitious output power

$$\Delta p = p_{FCC} - p_L \tag{4}$$

has to be processed by the FCC which results in an increase of the DC voltages of the FCC capacitor bank (cf. **Fig. 2**), while the DC-link of the passive system remains almost constant (depending on the load characteristic). Similarly, discharging of the FCC DC capacitors applies for an increased load step of the system. A load step can hence be detected by monitoring of the FCC DC voltage levels (v_{cp} and v_{cn}) of the active cell.

In order to guarantee not only a properly filtered output power but also a feasable system dynamic, both a higher order low-pass filter for measuring the rated output power and a nonlinear voltage controller structure in order to improve the dynamic of the FCC is used. The dynamic of the FCC can be improved by implementation of a dedicated voltage controller regarding the FCC DC voltages. The design of the voltage conroller is hence highly dependent on the implemented digital low-pass filter structure which is supposed to obtain the averaged output power P_{o}. The dedicated voltage controller generates some fraction of power ΔP which is added to the measured output power. Therefore, the low-frequency voltage ripple of the DC voltages considering the FCC affects the quality of the mains input currents in the same manner as the previously discussed 300 Hz output power ripple. The voltage controller has therefore be seperated into two parts: A slow responding (due to filtered DC-link voltages) P or PI-controller and a high dynamic (unfiltered DC voltages) nonlinear control structure. Consequently, the nonlinear part of the control strategy has to compensate the poor response behaviour evoked due to digital filtering of the transmitted instantaneous output power of the passive diode bridge. The discussed control solution is depicted in **Fig. 3**. While the nonlinear part of the voltage controller (in order to minimize these deviations especially caused due to load steps) appears to be zero for small variations and is sensitive to demonstrative deviations of the nominal DC voltage level (V_{tot}^{*} calculates to 800 V for the given topology, as discussed in [8]), the additional slow responding P-controller leg accurately adjusts the required DC voltage level of the FCC. Due to passive diode bridge rectification only positive power flow is allowed. Therefore, the overall controller structure has to be limited to

$$P_{\mathrm{o}} - \Delta p > 0\,\mathrm{W}. \tag{5}$$

The maximum limit of the voltage controller highly depends on physical constraints of the passive diode bridge and the FCC semiconductor devices. Focused on the previously discussed considerations the digital filter structure required for evaluation of the averaged output power P_{o} is designed as a second order low-pass filter

$$G\left(\mathrm{s}\right) = \frac{1}{1 + \mathrm{s}T_{\mathrm{c}}\vartheta + \mathrm{s}^{2}T_{\mathrm{c}}^{2}} \tag{6}$$

including a damping part ϑ which mitigates ringing of its appropriate step response (step response similar to bessel filter). The evaluted fractional power (Δp) is added to the computed output power P_{o} which allows the system not only to improve the dynamic of the cell considering load step behaviour, but also to increase or reduce the input power of the overall system in order to charge or discharge the DC voltage capacitor bank, respectively. The equivalent electric conductance g_{e}^{*} can hence be calculated, considering the discussed control structure, by

$$g_{\mathrm{e}}^{*} = \frac{P_{\mathrm{o}} + \Delta p}{\sum\limits_{i=1\ldots3} v_{\mathrm{Ni,eff}}^{2}} \tag{7}$$

The reference currents of the FCC, therefore, can be assessed by

$$i_{\mathrm{pos}} = g_{\mathrm{e}}^{*} v_{\mathrm{pos}}\,; \quad i_{\mathrm{h3}} = g_{\mathrm{e}}^{*} v_{\mathrm{h3}}\,; \quad i_{\mathrm{neg}} = g_{\mathrm{e}}^{*} v_{\mathrm{neg}}\,. \tag{8}$$

The discussed voltage control of the active system is only able to handle the total DC voltage level of the cell $v_{\mathrm{cp}} + v_{\mathrm{cn}}$. In order to prevent imbalance of both voltages a novel DC voltage balancing concept has been developed.

III. DC Voltage Balancing Concept

A possible and very simple approach to assure balanced FCC DC voltages is to use two seperate electric conduction values $g_{\mathrm{e,pos}}^{*}$ and $g_{\mathrm{e,neg}}^{*}$ for the two half-bridge legs generating i_{cp} and i_{cn}. However, this control method thereto causes a DC offset in the mains input currents (i_{Ni}) referred to one mains period and is therefore no suitable solution and hence not further discussed.

Unbalance of DC capacitor voltages typically results due to parasitic effects (e.g. capacitor leakage currents, interlock delay, unsymmetric PWM signals, gate drives etc.) which are generally characterized according to the manufacturers datasheet of the respective component. The leakage current of an electrolytic capacitor, e.g. EPCOS B43501 series is specified by $i_{\mathrm{L}} < 1.4\mathrm{mA}$ for a rated voltage V_{R} of 400 V and C_{R} of 470 μF. In order to evaluate the effect due to unsymmetrical parasitic components (e.g. capacitor ESR) considering unbalanced capacitor voltages, an accurate model of the FCC is given in **Fig. 4(a)**. The extended model includes inductor voltage drops (v_{Lcp}, v_{Lcn}, v_{Lh3}), DC ($R_{\mathrm{DC,cp}}$, $R_{\mathrm{DC,h3}}$, $R_{\mathrm{DC,cn}}$) and equivalent series resistances ($R_{\mathrm{ESR,cp}}$, $R_{\mathrm{ESR,cn}}$) of coils and capacitors, respectively, however, neglects capacitor leakage currents. Inductor voltage drops (v_{Lcp}, v_{Lcn}, v_{Lh3}) have to be considered due to the used rather low switching frequency (10 kHz). Consequently, significantly high inductance values (L_{cp}, L_{cn}, L_{h3}) of approximately 2.6mH are assumed. It has to be noted that design guidelines considering the active rectifier injection inductances are discussed in detail in [8]. Regarding inductor voltage drops, duty cycles for both half bridges and the three-level bridge leg (embracing that the midpoint voltage v_{MN} is controlled to zero) compute to

$$\begin{aligned}
\delta_{\mathrm{cp}}\left(\varphi_{\mathrm{N}}\right) =& \frac{v_{\mathrm{pos}}\left(\varphi_{\mathrm{N}}\right) + L_{\mathrm{cp}}\frac{\mathrm{d}}{\mathrm{d}\varphi_{\mathrm{N}}} i_{\mathrm{cp}}\left(\varphi_{\mathrm{N}}\right) + R_{\mathrm{DC,cp}} i_{\mathrm{cp}}\left(\varphi_{\mathrm{N}}\right)}{V_{\mathrm{cp}}} \\
\delta_{\mathrm{cn}}\left(\varphi_{\mathrm{N}}\right) =& 1 + \frac{v_{\mathrm{neg}}\left(\varphi_{\mathrm{N}}\right) - L_{\mathrm{cn}}\frac{\mathrm{d}}{\mathrm{d}\varphi_{\mathrm{N}}} i_{\mathrm{cn}}\left(\varphi_{\mathrm{N}}\right) - R_{\mathrm{DC,cn}} i_{\mathrm{cn}}\left(\varphi_{\mathrm{N}}\right)}{V_{\mathrm{cn}}} \\
\delta_{\mathrm{h3}}\left(\varphi_{\mathrm{N}}\right) =& 1 - \mathrm{sgn}\left(i_{\mathrm{h3}}\left(\varphi_{\mathrm{N}}\right)\right) \cdot \ldots \\
& \ldots \cdot \frac{v_{\mathrm{h3}}\left(\varphi_{\mathrm{N}}\right) - L_{\mathrm{h3}}\frac{\mathrm{d}}{\mathrm{d}\varphi_{\mathrm{N}}} i_{\mathrm{h3}}\left(\varphi_{\mathrm{N}}\right) - R_{\mathrm{DC,h3}} i_{\mathrm{h3}}\left(\varphi_{\mathrm{N}}\right)}{V_{\mathrm{cp}}}
\end{aligned} \tag{9}$$

where i_{cp} and i_{cn} denote the injection currents of the positive and negative busbar (which can be expressed as a function of i_{pos}, i_{neg} and i_{L} given in [8]) and v_{Lcp},v_{Lcn} the inductor

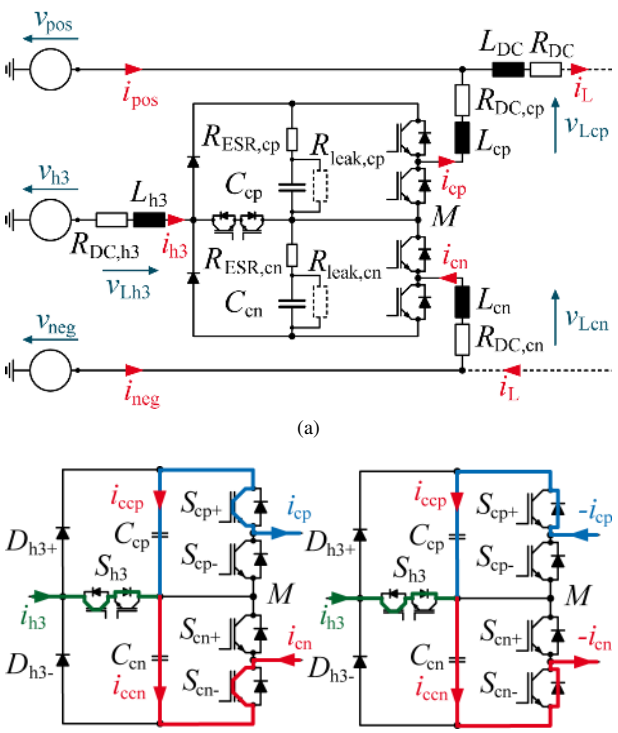


Fig. 4: (a) Model of the FCC considering capacitor leakage current characterized by $R_{\mathrm{leak,cp}}$ and $R_{\mathrm{leak,cn}}$, ESR ($R_{\mathrm{ESR,cp}}$, $R_{\mathrm{ESR,cn}}$) and DC resistances of the passive components (R_{DC}, $R_{\mathrm{DC,cp}}$, $R_{\mathrm{DC,cn}}$) and (b) FCC redundant switching states considering the generation of the AC side input current waveforms for switching states $S_{\mathrm{h3}}=1$, $S_{\mathrm{cp+}}=1$, $S_{\mathrm{cn+}}=0$ for the sector $\varphi_{\mathrm{N}} \in [\frac{\pi}{6} \dots \frac{\pi}{3}]$ ($i_{\mathrm{h3}}>0$, $i_{\mathrm{cp}}>0$, $i_{\mathrm{cn}}>0$) with appropriate midpoint voltage $v_{\mathrm{MN}}=0\,\mathrm{V}$ and capacitor currents $i_{\mathrm{ccp}}(\varphi_{\mathrm{N}}) = -i_{\mathrm{cp}}(\varphi_{\mathrm{N}})$ and $i_{\mathrm{ccn}}(\varphi_{\mathrm{N}}) = -i_{\mathrm{cn}}(\varphi_{\mathrm{N}})$ (left subfigure) and for the sector (right subfigure) $\varphi_{\mathrm{N}} \in [\frac{4\pi}{11} \dots \frac{\pi}{2}]$ ($i_{\mathrm{h3}}>0$, $i_{\mathrm{cp}}<0$, $i_{\mathrm{cn}}<0$) and appropriate midpoint voltage v_{MN}=0 V and capacitor currents $i_{\mathrm{ccp}}(\varphi_{\mathrm{N}}) = i_{\mathrm{cp}}(\varphi_{\mathrm{N}})$ and $i_{\mathrm{ccn}}(\varphi_{\mathrm{N}}) = i_{\mathrm{cn}}(\varphi_{\mathrm{N}})$.

voltage drop of L_{cp},L_{cn}, respectively. Considering the previously discussed equations, the averaged capacitor current I_{ccp} is therefore given by

$$I_{\mathrm{ccp}} = \frac{3}{2\pi} \int_{-\frac{\pi}{3}}^{\frac{\pi}{3}} \Bigg[-\frac{V_{\mathrm{cp}}}{2R_{\mathrm{ESR,cp}}} + \sqrt{\left(\frac{V_{\mathrm{cp}}}{2R_{\mathrm{ESR,cp}}}\right)^2 + \Bigg[i_{\mathrm{Dh3+}}(\varphi_{\mathrm{N}}) \cdot \dots \cdot \left(1 - \delta_{\mathrm{h3+}}(\varphi_{\mathrm{N}})\right) - i_{\mathrm{cp}}(\varphi_{\mathrm{N}})\, \delta_{\mathrm{cp}}(\varphi_{\mathrm{N}}) \Bigg] \frac{V_{\mathrm{cp}}}{R_{\mathrm{ESR,cp}}}} \Bigg] \mathrm{d}\varphi_{\mathrm{N}} \tag{10}$$

for the sector $\varphi_{\mathrm{N}} \in \left[-\frac{\pi}{3} \dots \frac{\pi}{3}\right]$. A calculation of I_{ccp} or I_{ccn} is not possible in an analytical way, due to the definition of the currents i_{cp} and i_{cn}. The averaged capacitor currents I_{ccp} and I_{ccn} have hence been determined numerically. The maximum current that needs to be adjusted using a balancing concept can be assessed numerically by

$$I_{\mathrm{cc,max}} = \frac{I_{\mathrm{ccp}} - I_{\mathrm{ccn}}}{2} \approx 1.5\,\mathrm{mA}\,(P_{\mathrm{o}} = 10\,\mathrm{kW}) \tag{11}$$

for dedicated values $R_{\mathrm{ESR,cp}} = 120\,\mathrm{m\Omega}$, $R_{\mathrm{ESR,cn}} = 180\,\mathrm{m\Omega}$,

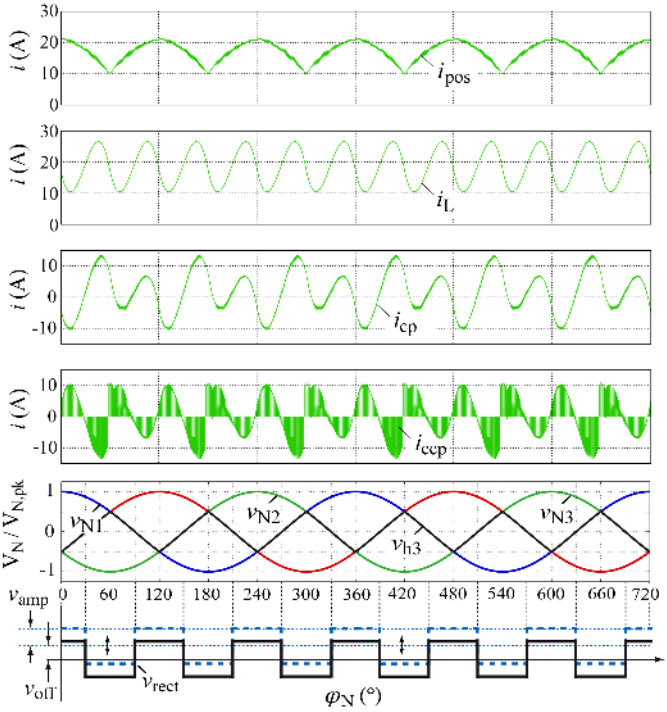


Fig. 5: Proposed active voltage balancing algorithm ($v^*_{\mathrm{MN,avg}} = v_{\mathrm{amp}} \cdot \mathrm{rect}\,(\varphi_{\mathrm{N}}) + v_{\mathrm{off}}$) implemented as rectangular signal $v_{\mathrm{rect}} (= v_{\mathrm{amp}} \cdot \mathrm{rect}\,(\varphi_{\mathrm{N}}))$ with corresponding offset v_{off} and appropriate DC side smoothing inductance current i_{L}, positive DC bus injection current i_{cp} and DC bus input current i_{pos}.

$R_{\mathrm{DC,cp}} = 152\,\mathrm{m\Omega}$, $R_{\mathrm{DC,cn}} = 163\,\mathrm{m\Omega}$ and $R_{\mathrm{DC,h3}} = 157\,\mathrm{m\Omega}$.

It has to be noted that symmetrically chosen DC and ESR values ($R_{\mathrm{ESR,cp}} = R_{\mathrm{ESR,cn}}$ and $R_{\mathrm{DC,cp}} = R_{\mathrm{DC,cn}} = R_{\mathrm{DC,h3}}$) would lead to $I_{\mathrm{cc,max}} = 0\,\mathrm{A}$. Basically, detailed analyses revealed, that the midpoint voltage v_{MN} can be utilized to achieve different currents in both DC-link capacitors C_{cp} and C_{cn} which is explained in the following.

The intention of the proposed balancing concept is to exploit redundant switching states, as depicted in **Fig. 4(b)**, in order to prevent distortions of the generated sinusoidal mains currents, using the midpoint voltage v_{MN} to affect the capacitor currents i_{ccp} and i_{ccn}. Considering both current directions and switching states of all three converter stages, there are 48 $(= 2^3 \times 6)$ different states of the FCC to analyze. As shown in **Fig. 4(b)**(left subfigure) the DC capacitor currents i_{ccp} and i_{ccn} equal $-i_{\mathrm{cp}}$ and $-i_{\mathrm{cn}}$ and v_{MN} remains zero for switching states $S_{\mathrm{h3}}=1$, $S_{\mathrm{cp+}}=1$, $S_{\mathrm{cn+}}=0$ in the sector $\varphi_{\mathrm{N}} \in \left[\frac{\pi}{6} \dots \frac{\pi}{3}\right]$. Changes in sign for both capacitor currents, however, can be observed for the same switching state in a different sector $\left(\varphi_{\mathrm{N}} \in \left[-\frac{4\pi}{11} \dots \frac{\pi}{2}\right]\right)$ (cf., **Fig. 4(b)**(right subfigure)). Since i_{h3} is generated by the FCC injection currents i_{cp} and i_{cn} due to Kirchhoff's law and the midpoint voltage results in the same value for both states ($v_{\mathrm{MN}} = 0\mathrm{V}$ for the given switching states), the AC side input currents will stay undistorted. While modifying (increasing or decreasing) all three duty cycles (δ_{cp}, δ_{h3} and δ_{cn}) by applying a dedicated signal, influencing both capacitor currents can therefore be expected. Basically the easiest way to accomplish the mentioned effect is to use a purely offset in such a manner to intensify or reduce hardly

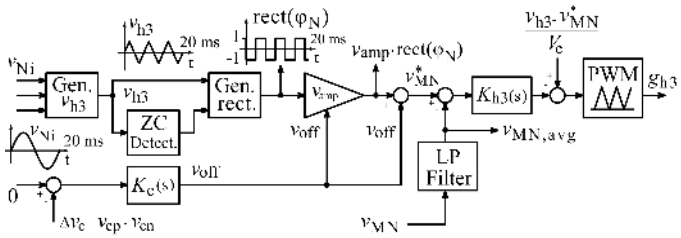


Fig. 6: Modified midpoint voltage controller considering the proposed voltage balancing algorithm $v^*_{\mathrm{MN,avg}}$.

applied switching states. However, adding a simple offset to all three duty cycles does not fit the requirements as δ_{h3} will exceed its limit ("1") for any offset-value. This applies for all continuous functions (sinusoidal, triangular shaped waveforms etc.). Therefore, a square wave signal due to its discontinuity (as shown in **Fig. 5**) is necessary to prevent δ_{h3} from violating its upper boundary. An additional offset can now be added to the rectangular shaped modulation signal which can be used for balancing. The very simple midpoint voltage balancing algorithm (v^*_{MN}) can thus be written as

$$v^*_{\mathrm{MN,avg}} = v_{\mathrm{amp}} \cdot \mathrm{rect}\left(\varphi_{\mathrm{N}}\right) + v_{\mathrm{off}} \tag{12}$$

while v_{amp} denotes the amplitude of the rectangular signal ($\mathrm{rect}\left(\varphi_{\mathrm{N}}\right)$) and v_{off} the appropriate offset. **Fig. 5** depicts the discussed voltage waveforms and appropriate currents i_{pos}, i_{L}, i_{cp} and i_{ccp} of the system. It is of significant importance to note that the chosen waveform using a rectangular signal with appropriate offset does not distort the generation of the input AC currents. The generation of the implemented nominal midpoint voltage is illustrated in **Fig. 6**. The triangular shaped voltage v_{h3} can be generated due to the measured input voltages and calculates to

$$v_{\mathrm{h3}} = -\max\left(v_{\mathrm{N1}}, v_{\mathrm{N2}}, v_{\mathrm{N3}}\right) - \min\left(v_{\mathrm{N1}}, v_{\mathrm{N2}}, v_{\mathrm{N3}}\right). \tag{13}$$

The rectangular shaped signal ($\mathrm{rect}\left(\varphi_{\mathrm{N}}\right)$) has to be formed such, that it has to reverse its sign each time v_{h3} changes in sign ($\frac{\pi}{6}$, $\frac{\pi}{2}$, $\frac{5\pi}{6}$,...).

$$\begin{aligned} &\text{if} \quad v_{\mathrm{h3}}\left(\varphi_N\right) > 0\,\mathrm{V} \;\rightarrow\; \mathrm{rect}\left(\varphi_N\right) < 0 \\ &\text{if} \quad v_{\mathrm{h3}}\left(\varphi_N\right) < 0\,\mathrm{V} \;\rightarrow\; \mathrm{rect}\left(\varphi_N\right) > 0 \end{aligned} \tag{14}$$

A zero crossing detector in order to evalute the roots of v_{h3} is therefore necessary. A seperate controller computes the required voltage offset value (v_{off}) which ideally equals the magnitude of the rectangular signal ($v_{\mathrm{amp}} = v_{\mathrm{off}}$) depending on the DC-link voltage situation ($\Delta v_{\mathrm{c}} = v_{\mathrm{cp}} - v_{\mathrm{cn}}$). The finally generated nominal midpoint voltage $v^*_{\mathrm{MN,avg}}$ is transferred to the voltage controller of the three-level bridge leg which regulates the voltage level v_{MN}.

If for example v_{cp} (instantaneous capacitor voltages of C_{cp}) shall be increased a negative voltage offset has to be applied. Considering v_{cn} a negative DC offset will lead to capacitor (C_{cn}) discharging.

In order to analyze the characteristics of the proposed balancing algorithm a simplified model of the FCC was assumed, neglecting inductor voltage drops (v_{Lcp}, v_{Lcn} and v_{Lh3}), parasitic components and resistances. This leads to an averaged

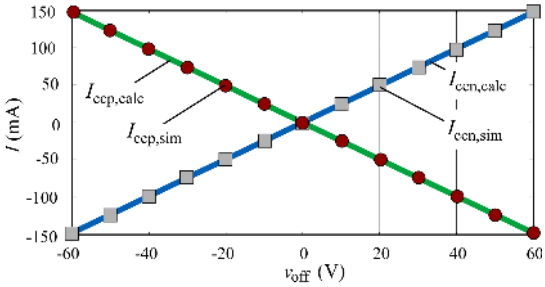


Fig. 7: Evaluated and simulated results of induced DC voltage capacitor currents $I_{\mathrm{ccp,calc}}$,$I_{\mathrm{ccp,sim}}$ and $I_{\mathrm{ccn,calc}}$,$I_{\mathrm{ccn,sim}}$ considering positive and negative FCC capacitor bank C_{cp} and C_{cn}, respectively, due to advantageously exploiting the controlled averaged mitpoint voltage $v_{\mathrm{MN,avg}}$.

current for C_{cp} and C_{cn} as follows.

$$\begin{aligned} I_{\mathrm{ccp}} &= \frac{1}{6} \cdot \frac{\hat{I}_{\mathrm{N}} \cdot v_{\mathrm{off}} \left(-18 + \pi^2\sqrt{3}\right)}{\pi V_{\mathrm{c}}} \\ I_{\mathrm{ccn}} &= -\frac{1}{6} \cdot \frac{\hat{I}_{\mathrm{N}} \cdot v_{\mathrm{off}} \left(-18 + \pi^2\sqrt{3}\right)}{\pi V_{\mathrm{c}}} \,. \end{aligned} \tag{15}$$

Obviously, I_{ccp} and I_{ccn} conform to a linear dependency of v_{off} what could also be confirmed by simulation (**Fig. 7**). It has to be noted that the balancing algorithm is further characterized by the rated output power. The offset v_{off} and the amplitude v_{amp} of the balancing algorithm therefore can not remain fixed for diverging loads due to its linear dependency of $\hat{I}_{\mathrm{N}}$. Assuming e.g. an offset (v_{off}) of 8 V considering 10 kW output power, v_{off} has to be increased for light loads to achieve similar induced capacitor currents due to an decrease of the regarded mains input currents peak value.

In order to guarantee a proper balancing process while achieving undistorted sinusoidal mains currents on the AC side of the passive rectifier, the generated rectangular signal has to comply with a set of constraints. Considering δ_{h3} (cf. **Fig. 8**),

$$v_{\mathrm{amp}} > 0 \qquad (1^{\mathrm{st}}\ \text{constraint}) \tag{16}$$

and

$$v_{\mathrm{amp}} \geq |v_{\mathrm{off}}| \qquad (2^{\mathrm{nd}}\ \text{constraint}) \tag{17}$$

has to be fulfilled. In order to use the maximum balancing capability, the offset v_{off} should be chosen in the same size of the rectangular amplitude v_{amp}

$$v_{\mathrm{off}} = v_{\mathrm{amp}}\,. \qquad (3^{\mathrm{rd}}\ \text{constraint}) \tag{18}$$

Considering the duty cycles of positive and negative half bridges connected to C_{cp} and C_{cn}, respectively, positive and negative limits (neglecting inductor voltage drops) for the offset voltage v_{off} can be assessed by

$$v_{\mathrm{off,lim}} = \pm\frac{V_{\mathrm{c}} - \frac{\sqrt{3}}{2}\hat{V}_{\mathrm{N}}}{2} = 60\mathrm{V}\,. \qquad (4^{\mathrm{th}}\ \text{constraint}) \tag{19}$$

It has to be noted that the maximum offset voltage limit due to applying the proposed rectangular signal waveform is considerably smaller than the rather expected 75 V $\left(= V_c - \hat{V}_{\mathrm{N}}\right)$. In order to analyze the influence of the DC side inductor current due to its considerably high 6^{th} harmonic the inductor voltage

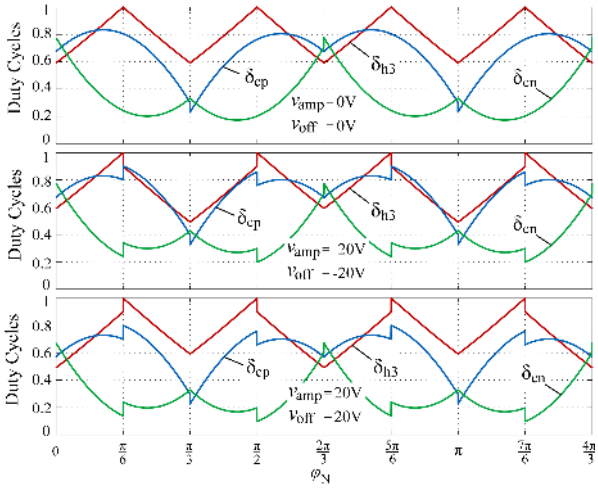


Fig. 8: Adapted duty cycles δ_{cp}, δ_{cn} and δ_{h3} considering injection inductor voltage drops and averaged midpoint voltage $v_{\mathrm{MN,avg}}$.

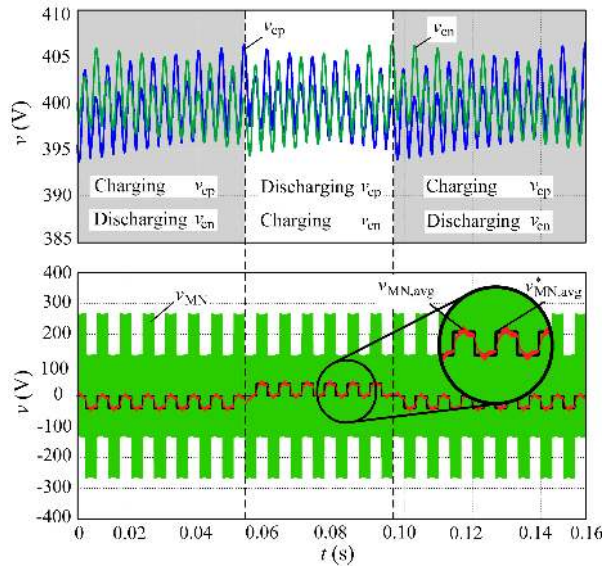
drops (v_{Lcp}, v_{Lcn} and v_{Lh3}) have been added. This results in a considerably high reduction of the previously described constraints for the amplitude and offset of the applied rectangular signal. This problem can be outlined in terms of

$$v_{\mathrm{off,lim}} = \pm \frac{V_{\mathrm{c}} - \sqrt{3}\hat{V}_{\mathrm{N}} \left[\frac{1}{2} + \frac{L_{\mathrm{c}}}{L_{\mathrm{DC}}}\left(1 - \frac{3}{\pi}\right)\right] - \frac{\omega_{\mathrm{N}} L_{\mathrm{c}} \hat{I}_{\mathrm{N}}}{2}}{2} \,. \quad (20)$$

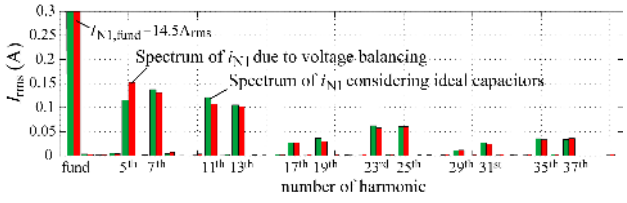
The last term of the equation ($\frac{1}{2}\omega_{\mathrm{N}} L_{\mathrm{c}} \hat{I}_{\mathrm{N}}$) is defined by one fraction of the inductor voltage drop (v_{Lcp}) caused due to the positive busbar current i_{pos} for the sector $\varphi_{\mathrm{N}} \in \left[0 \ldots \frac{\pi}{3}\right]$

$$L_{\mathrm{c}} \frac{\mathrm{d}}{\mathrm{d}\varphi_{\mathrm{N}}} i_{\mathrm{pos}}\left(\varphi_{\mathrm{N}}\right) = -\omega_{\mathrm{N}} L_{\mathrm{c}} \hat{I}_{\mathrm{N}} \sin\left(\varphi_{\mathrm{N}}\right) \,. \quad (21)$$

Considering a rated output power of $P_{\mathrm{o}} = 10\,\mathrm{kW}$, an injection inductance L_{c} of 2.6 mH, a DC side smoothing inductor of 2.25 mH and 400 V FCC DC voltage levels (V_{c}) the maximum midpoint voltage offset $v_{\mathrm{off,lim}}$ yields approximately 40 V. Equation (20) indicates that even for no load mode of the active system, the maximum voltage level is merely enlarging to 44 V, which is caused due to the still applying 300 Hz current ripple. However, side effects of the active system considering no load mode are not discussed within this paper. As previously mentioned, a rectangular shaped signal is necessary to prevent δ_{h3} from violating its upper boundary. The occurring step characteristic (in all three duty cycles) however causes small deviations of modulation values for i_{pos}, i_{neg} and i_{h3} as the voltage controller of the three-level brdige leg can not ideally follow the implemented step and is therefore only able to increase or decrease the midpoint voltage of the FCC with a diminutive delay for a switching frequency of only 10 kHz. It is therefore mandatory to keep the amplitude of the rectangular shaped signal as small as possible. The maximum positive and negative adjustable average currents are, furthermore, very small, neglecting additional ripple due to PI-controller, etc., however, still sufficient for the given topology. The discussed algorithm complies with the adapted midpoint voltage and therefore has to be considered as feed forward signal for both



(a)



(b)

Fig. 9: (a) Simulation results regarding DC voltage control and balancing (v_{cp},v_{cn}) and appropriate nominal ($v^*_{\mathrm{MN,avg}}$) and real signal waveforms of the midpoint to neutral point voltage v_{MN} and $v_{\mathrm{MN,avg}}$. (b) Mains input current (i_{N1}) spectrum in order to verify undistorted mains input currents due to the proposed balancing concept.

current controllers and the midpoint voltage controller (**Fig. 3(c)** and **Fig. 6**). The midpoint voltage v_{MN} can hence no longer be assumed to be 0 V. The corresponding duty cycles (δ_{cp}, δ_{cn}, δ_{h3}) for the dedicated current and voltage controllers, regarding the deactivated voltage controller ($v_{\mathrm{off}} = v_{\mathrm{amp}} = 0\,\mathrm{V}$), generation of a positive ($v_{\mathrm{off}} = v_{\mathrm{amp}} = 20\,\mathrm{V}$) averaged midpoint volate v_{MN} and causing a negativ offest value ($v_{\mathrm{off}} = -20\,\mathrm{V}$, $v_{\mathrm{amp}} = 20\,\mathrm{V}$), are depicted in **Fig. 8**. In contrast to [8] where inductance voltage drops are neglected, the duty cycles illustrated in **Fig. 8** are considering the injection inductances ($L_{\mathrm{cp}} = L_{\mathrm{cn}} = L_{\mathrm{c}}$) potential difference which are mandatory side effects for low switching frequency (10 kHz) applications. The previously discussed balancing controller limitation issue ($v_{\mathrm{off,lim}}$), now becomes much more obvious.

Fig. 9(a) depicts simulation results of the implemented balancing concept. In order to verify proper operation of the proposed concept, both DC voltages v_{cp} and v_{cn}, the averaged ($v_{\mathrm{MN,avg}}$ - red), the nominal averaged ($v^*_{\mathrm{MN,avg}}$ - blue) as well as the instantious (v_{MN} - green) midpoint voltage are illustrated. The spectrum of one mains phase input current (i_{N1}) regarding the implemented balancing concept compared to implemented ideal capacitors ($C_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}}} = \infty$) is finally visualized in **Fig. 9(b)**. The $\mathrm{THD_i}$ considering the ideal capacitor case was simulated to

TABLE I: Design Specifications of the Built Three-Phase Rectifier using a FCC.

Mains voltage:	$V_{\mathrm{LL}} = 400\,\mathrm{V_{rms}}$
Mains frequency:	$f_{\mathrm{N}} = 50\,\mathrm{Hz}$
Switching frequency:	$f_{\mathrm{s}} = 10\,\mathrm{kHz}$.
FCC dc-link voltage:	$V_{\mathrm{cp}} = V_{\mathrm{cn}} = 400\,\mathrm{V}$
Output power:	$P_{\mathrm{o}} = 10\,\mathrm{kW}$

TABLE II: Power Devices Selected for Implementation of the FCC Prototype.

$S_{\mathrm{ia,b}}$	1200 V/40 A IGBT, IKW40T120, Infineon
$S_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}}\pm}$	600 V/20 A IGBT, IKW20N60H3, Infineon
$D_{\mathrm{h3}\pm}$	1200 V/15 A, STTH1512W, ST-Microelectronics
$C_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}}}$	470 μF/400 V, EPCOS B43501-type
L_{cp}=L_{cn}=L_{h3}	3.2 mH, Iron core 3UI60a, N = 123 turns
C_{F}, C_{S}	6.8 μF/275 $\mathrm{V_{AC}}$, MKP X2, Arcotronics
C_{o}	2.2 mF/400 V, Felsic CO 39 A728848
L_{DC}	2.25 mH, Iron core 2 x UI60a
$D_1 - D_6$	35 A/1600 V, 36MT160, Vishay

1.85% and regarding voltage controller and balancing concept yields 1.86%. No nameable distortions examining the input current frequency spectrum for a range between 50 Hz and 2 kHz hence could be observed. What can be noticed from **Fig. 9(a)** is that a relatively high DC voltage capacitor ripple of approximately 8 V occurs for v_{cp} and v_{cn}, respectively. This voltage ripple is primarily defined due to the 3$^{\mathrm{rd}}$ order harmonic component of i_{cp} (cf. **Fig. 5**) and i_{cn}. The magnitude of the ripple is generally defined by the capacitance of the passive component. In order to reduce the volume of the DC voltage capacitor bank, a relatively high peak-to-peak voltage $\Delta V_{\mathrm{c,pkpk,max}}$ ripple of $2-3\% \cdot V_{\mathrm{c}}$ has been taken into account. As discussed in a previous section the zero crossings of i_{cp},i_{cn} have to be evaluated numerically. An analytical form regarding the design of the DC voltage capacitor is hence not possible.

IV. Experimental Results

The implemented 10 kW/10 kHz active rectifier employing a flying converter cell has been discussed in [12] considering its basic operation principle for different load conditions, efficieny η, power factor λ and total harmonic distortion of input currents $\mathrm{THD_i}$. Detailed specifications of the active system, applied power semiconductor devices and passive components are given in TABLE I and TABLE II. Based on the previous derivations the proposed balancing concept has been implemented in a digital signal processor (TI 320F2808). **Fig. 10(a)**-**Fig. 10(c)** facilitate the previously discussed significance of a non-linear voltage controller. **Fig. 10(a)** depicts a load step from 5 kW to 10 kW while implemented a purely P-controller in addition to a second order low-pass pre-filter for DC voltage input signals (v_{cp} and v_{cn}). As can be seen, the low dynamic of the FCC leads to a voltage deviation ($V_{\mathrm{DC,dev}}$) of 160 V with respect to the required 800 V DC voltage level. **Fig. 10(a)** and **Fig. 10(b)** illustrate an increasing (5 kW to 10 kW) and a decreasing (10 kW to 5 kW) load step, respectively, while taking advantage of an implemented nonlinear voltage controller structure. It can be observed that the deviation could be reduced significantly to

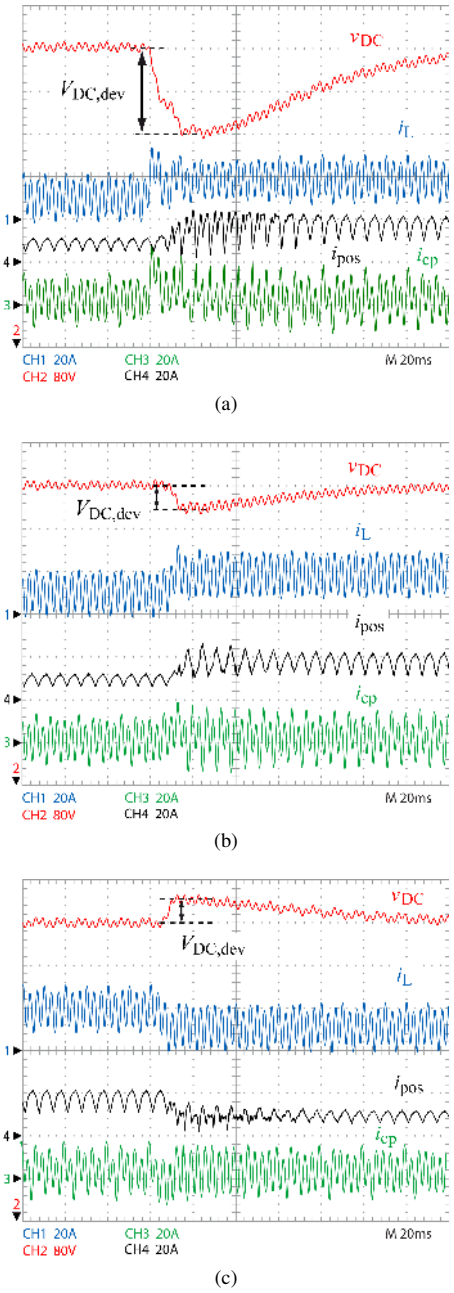
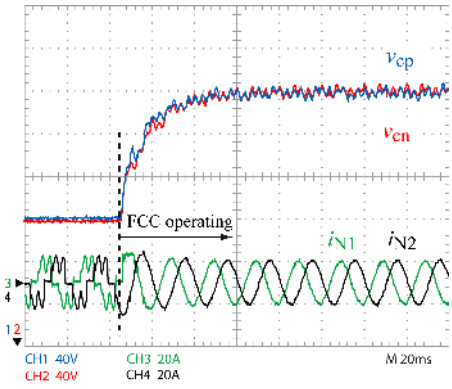


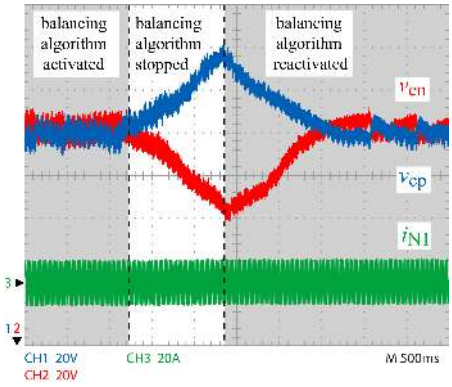
Fig. 10: Measurement results of the FCC DC voltage $v_{\mathrm{DC}} = v_{\mathrm{cp}} + v_{\mathrm{cn}}$ considering load steps of the active rectifier system, comparing the discussed voltage controller strategies. (a) Load step from 5 kW to 10 kW using a merely P-controller voltage regulation structure. (b) 5 kW to 10 kW load step with additional nonlinear controller leg. (c) 10 kW to 5 kW load step considering nonlinear voltage controller.

approximately 40 V which is about 10% of the rated voltage level (depending on the chosen voltage controller gain).

The DC voltage balancing concept is verfied in **Fig. 11**. **Fig. 11(a)** shows the transition from passive to active diode bridge mode and the appropriate charging of the FCC DC voltage from 280 V (pre-charged) to 400 V required for proper generation of injection currents for each half bridge switching leg. After the DC voltages are set to the dedicated 400 V limit



(a)



(b)

Fig. 11: Measurement results taken from the laboratory prototype for a rated output power of 10 kW. (a) Transition from passive diode mode operation to active current shaping using the proposed voltage balancing concept ($v_{\mathrm{off}} = \pm 10\,\mathrm{V}$, $v_{\mathrm{MN}} = \pm 10\,\mathrm{V}$). (b) Steady state operation while deactivating the voltage balancing controller and reactivating it after 1 s.

they are perfectly balanced ($V_{\mathrm{cp}} = 399.8\,\mathrm{V}$, $V_{\mathrm{cn}} = 400.1\,\mathrm{V}$). **Fig. 11(a)** furthermore illustrates a smooth transition of both FCC DC voltages v_{cp} and v_{cn} without any perceivable overshoot, while active voltage balancing is operating. In **Fig. 11(b)** voltage control of v_{cp} and v_{cn} using the active voltage balancing controller (grey area in **Fig. 11(b)**) can be observed. For the proposed balancing concept both DC voltages of the FCC are perfectly aligned. After deactivating (white area in **Fig. 11(b)**) the balancing algorithm ($v_{\mathrm{amp}} = v_{\mathrm{off}} = 0\,\mathrm{V}$) v_{cp} and v_{cn} are starting to drift off the required voltage level of 400 V ($V_{\mathrm{cp}} = 435\,\mathrm{V}$, $V_{\mathrm{cn}} = 365\,\mathrm{V}$). Reactivating the balancing concept finally regulate the FCC DC voltages to the expected 400 V voltage level.

V. Conclusion

In this paper a novel DC voltage balancing concept and a dedicated voltage controller for active three-phase rectifiers based on third harmonic injection principle employing a FCC are discussed. The proposed concept is theoretically and mathematically analyzed and proven using simulation software. The voltage controller for adjusting the overall FCC DC voltage $v_{\mathrm{cp}} + v_{\mathrm{cn}}$ is discussed while adressing emerging problems (low-frequency distortions regarding $\mathrm{THD_i}$ and lack of dynamic compared to a conventional passive rectification system with LC output filter) due to inappropriate digital filtering concepts considering the measured output power and FCC DC voltages.

A novel voltage balancing concept is described which advantageously uses the midpoint voltage v_{MN} of the FCC to charge or discharge the DC voltage capacitors. The implementation of the required square wave signal ($v^*_{\mathrm{MN,avg}} = v_{\mathrm{amp}} \cdot \mathrm{rect}\,(\varphi_{\mathrm{N}}) + v_{\mathrm{off}}$) is discussed and its boundaries considering offset (v_{off}) and amplitude (v_{amp}) are mathematically derived.

The voltage balancing and voltage controller concept has been adapted to the existing current (half bridges) and voltage controller (three-level bridge leg) structures of the FCC and furthermore implemented in a digital signal processor of a 10 kW/10 kHz laboratory prototype. The illustrated results reveal that the concept is well suited for the proposed converter topology as the midpoint voltage $v_{\mathrm{MN,avg}}$ of the FCC can be advantageously used to affect the DC voltage capacitor currents I_{ccp} and I_{ccn} in order to smoothly balance the appropriate voltages v_{cp} and v_{cn} while AC side input currents stay undistorted.

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