DCM Forward-Flyback converter with Cockcroft-Walton Voltage Multiplier: steady-state analysis considering the influence of the parasitic capacitances at very low power and very high voltage gain

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***Abstract*— Electrohydrodynamic (EHD) cooling systems are becoming a feasible solution to replace rotary fans from electronic products, leading to more robust solutions with lower weight. High voltage power supplies are an essential part of the system. In general, EHD loads require very low current to produce the corona discharge and the air flow [1]. The Forward-Flyback converter with Cockcroft-Walton Voltage Multiplier (FF-CWVM) is presented in this paper as a suitable candidate to supply an EHD load. Under very low power (1.5W) and high voltage gain (1:250) conditions, the FF-CWVM is very sensitive to the influence of the parasitic capacitances, leading to new operation stages. Then, the steady-state operation of the converter is analyzed and the most representative equivalent circuits and waveforms are presented. Finally, the theoretical analysis is validated with simulation and experimental results and the importance of achieving ZVS is highlighted.**

Keywords—Cockcroft-Walton voltage multiplier; Flyback; very low power; very high voltage gain; parasitic capacitances; new operation stages; ZVS; efficiency; Electrohydrodynamic (EHD) load;

I. INTRODUCTION

The design of the power supply is critical for the behavior of the EHD cooling system. Several topologies have been analyzed in combination with the Cockcroft-Walton Voltage Multiplier (CWVM): the non-resonant Half-Bridge [2], the Boost [3] and the Flyback [4,5]. Additionally, the resonant Half-Bridge topology, without CWVM, has also been considered. However, the effect of the parasitic capacitances prevents that circuit from operating as expected.

The selected topology is the Forward-Flyback converter with CWVM due to the very low power specifications. The cost, weight and size of the converter are also determining factors, because the final goal is to achieve a very compact and robust power supply in order to replace the current cooling systems (rotary fans and heatsinks) available nowadays in the industry.

In this type of application, the influence of the parasitic capacitances must be analyzed in detail [6]. Therefore, properly measuring and calculating the transformer parameters [7,8] is critical to understand the behavior of the circuit.

The steady-state of the converter is analyzed and some design guidelines are given in this paper. The ideal output voltage gain equation is presented and the CWVM voltage drop issue, explained in [9], is also addressed in this paper. The impact of the Flyback topology in the CWVM voltage drop is also taken into consideration and a more accurate expression is obtained. Thus, a global equation to calculate the output voltage is presented in this paper.

The effect of the parasitic capacitances and the analysis of the Zero Voltage Switching (ZVS) are the main contributions of this paper. Some important features regarding the influence of the parasitic capacitances are analyzed. New operation stages, some of their equivalent circuits and the main waveforms are presented, considering the parasitic effects.

Simulation and experimental results are provided to validate the theoretical approach of the paper. The waveforms are compared with the theoretical ones and the efficiency of the power stage is measured. The impact of the ZVS is quantified and the importance of achieving it is highlighted.

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II. STEADY-STATE ANALYSIS OF THE FF-CWVM

The steady-state operation of the Forward-Flyback with CWVM topology, depicted in Figure 1, is analyzed along this section. The ideal voltage gain and the CWVM voltage drop equations are presented, as well as the operation stages of the converter. Based on the results, the expression of the real output voltage is obtained and some design guidelines are stated. The influence of the parasitic capacitances on the behavior of the circuit and the equivalent circuits are analyzed in detail, highlighting the new operation stages.

A. Energy flow of the FF-CWVM

When the Flyback topology and the CWVM are used together, the performance of the converter changes. Unlike a conventional Flyback, the energy is delivered to secondary side in two different ways:

(1) During the magnetization of the transformer (when the switch is ON), some energy is also sent to secondary side, charging the C_i capacitors. This occurs because the diodes subscripted with odd numbers are forward-biased. This is described as 'Forward' energy in this paper.
(2) The energy stored in the magnetizing inductance of the transformer is delivered to secondary side when the switch turns off, as in a conventional Flyback, charging the C_{Oi} capacitors and supplying the load. This is called 'Flyback' energy along this paper.

A more detailed description of the operation of the circuit is provided throughout this section.

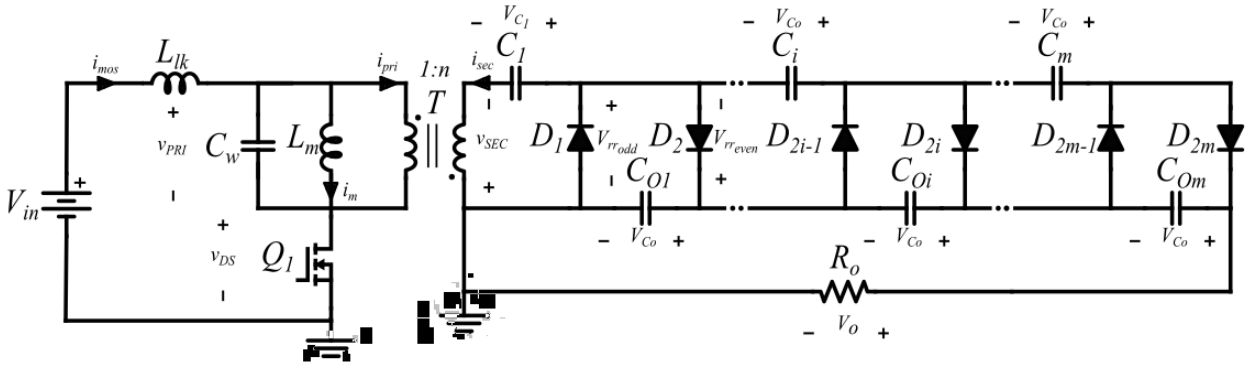


Fig 1 Forward-Flyback with CWVM circuit

B. *Voltage gain analysis in DCM*

A general analysis of the DCM FF-CWVM topology is performed in [4], where the theoretical voltage gain (1) is obtained, considering the ideal circuit. The DCM condition (2) is met due to the very light load specifications and the high turn ratio of the transformer.

$$\frac{V_o}{V_{in}} = \frac{nm}{2}\left[1 + \sqrt{1 + \frac{2R_o}{L_m f_{sw}}\left(\frac{D_1}{nm}\right)^2}\right] \quad (1)$$

$$L_m \leq \frac{R_o}{2f_{sw}}\frac{D_1}{nm}\frac{V_{in}}{V_o} \quad (2)$$

Therefore, the voltage gain of the converter depends on the number of voltage multiplier (VM) stages (m), the turn ratio (n), the duty cycle (D_1) when the switch is ON, the magnetizing inductance (L_m), the switching frequency (f_{sw}) and the output resistance (R_o).

The theoretical voltage across the capacitor C_1 (V_{C_1}) is equal to the secondary voltage of the transformer when the switch is ON (3). The relationship between V_{C_1} and the voltage across the remaining output capacitors (V_{C_o}) (4) is calculated by stablishing the volt-second balance in the transformer primary voltage. In these calculations, the output capacitors are supposed to be large enough that the voltage across them is essentially constant. The voltage drop across the diodes when they are forward biased is also neglected.

$$V_{C_1} = n\,V_{in} \quad (3)$$

$$V_{C_o} = n\,V_{in}\cdot\left(1 + \frac{D_1}{D_2}\right) \quad (4)$$

D_2 is defined as the duty cycle when the switch is OFF and the magnetizing energy stored in the transformer is delivered to the secondary side.

According to the previous equations, some design guidelines can be stablished to determine the value of some parameters of the converter. The input and output voltage are given as requirements of the power supply. Some design steps are discussed next:

(1) The number of VM-stages is defined by the voltage ratings of the available capacitors.
(2) Considering deratings for safety, the desired voltage across the output capacitors (except for C_1) is determined.
(3) The relationship between D_1 and the turn ratio is calculated depending on the values of the magnetizing inductance and the rest of parameters explained in Equation (1).
(4) Then, the turn ratio is fixed and D_1 is calculated, as well as the ratio $\frac{D_1}{D_2}$. If this values are not valid, the turn ratio must be changed and D_1 and D_2 must be recalculated and checked again.

In this circuit, the voltages across the output capacitors are:

$$V_{C_1} = \frac{V_{Co}}{2} \quad (5)$$

which implies that $D_1 = D_2$. The remaining values of the parameters, given in Table I, will be shown in the validation section (Section IV).

B. *CWVM voltage drop*

The general performance of the CWVM is explained in [9], but the influence of the Flyback stage is included in this paper, as well as a different arrangement of the secondary side capacitors. The output voltage is obtained as the addition of the voltage across each C_{Oi} capacitor. The key concepts are summarized next:

(1) The energy flows through the CWVM capacitors prior to being delivered to the load. When this happens, the charge of each consecutive capacitor is reduced, depending on the VM-stage to which it belongs (6).
(2) During the Forward interval, the C_i capacitors are charged, and the voltage across them depends on the voltage across the $C_{O(i-1)}$ capacitors (except for C_1).
(3) On the other hand, the C_{Oi} capacitors are charged during the Flyback interval, and the voltage across them depends on the voltage across the C_i capacitors.

$$\Delta Q_{C_i} = \Delta Q_{C_{Oi}} = (m - i + 1)\frac{I_o}{f_{sw}} \quad (6)$$

These dependences imply that the capacitors get slightly discharged when they deliver energy to the load, which directly affects the voltage across the rest of the capacitors of the CWVM. In conclusion, the output voltage is affected by the charge reduction in each consecutive capacitor.

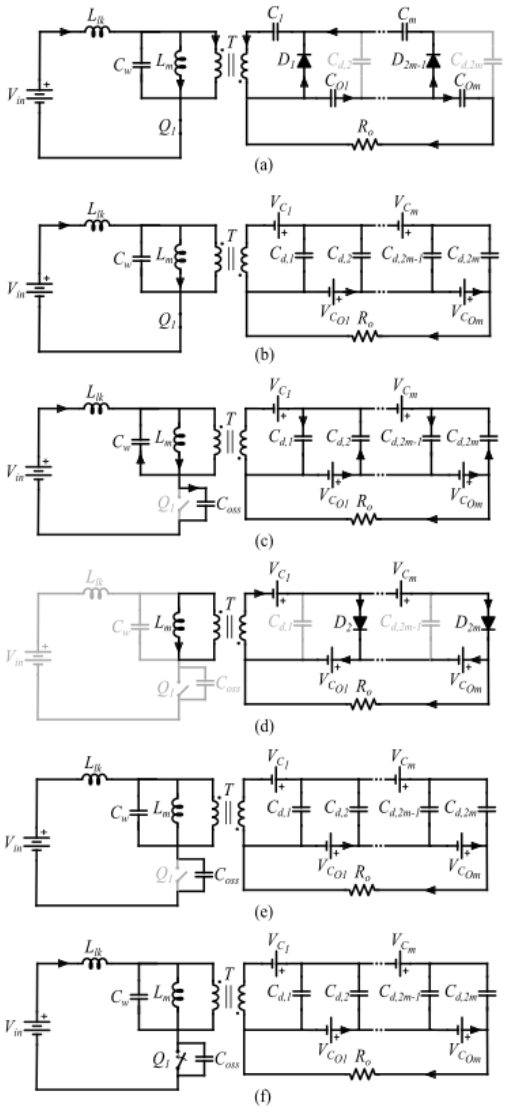


Fig 2 Operation stages of the DCM FF-CWVM (a) St1; (b) St2; (c) St3; (d) St4; (e) St5; (f) St6

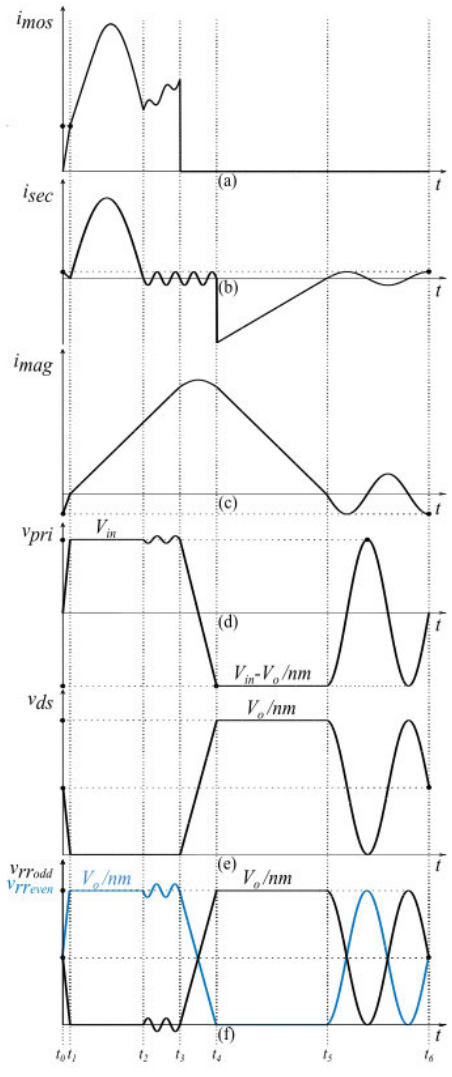


Fig 3 Waveforms considering the parasitic capacitances (a) MOSFET current; (b) Transformer secondary current; (c) Magnetizing current; (d) Transformer primary voltage; (e) MOSFET drain-source voltage; (f) Odd diodes (black) and even diodes (blue) reverse voltage

Then, following the method proposed in [9], the output voltage is calculated as the addition of the voltages across the C_{Oi} capacitors. Assuming that all the output capacitors are equal ($C_i = C_{Oi} = C_o$), the output voltage expression is obtained (7). Simplifying the summation, the output voltage is calculated (8) and two terms are clearly identified: the ideal value (9), based on the design guidelines explained previously, and the CWVM voltage drop (10).

$$V_o = 2nmV_{in} - \frac{I_o}{f_{sw}C_o}\sum_{i=1}^{m}(m-i+1)^2 \quad (7)$$

$$V_o = 2nmV_{in} - \left(\frac{2m^3+3m^2+m}{6}\right)\frac{I_o}{f_{sw}C_o} \quad (8)$$

$$V_{o,ideal} = 2nmV_{in} \quad (9)$$

$$\Delta V_{o,CWVM} = \left(\frac{2m^3+3m^2+m}{6}\right)\frac{I_o}{f_{sw}C_o} \quad (10)$$

As a conclusion, the FF-CWVM voltage drop adversely affects the voltage gain and its value depends on some parameters of the converter, as well as the output current (I_o). This effective output voltage loss can be compensated by increasing the duty cycle and/or decreasing the switching frequency (increasing the ON-time of the switch) in order to reach the specified value for the output voltage.

C. *Operation stages*

In order to properly understand the behavior of the FF-CWVM under very light load and very high voltage gain conditions, the influence of the parasitic capacitances must be taken into account since the waveforms, the voltage gain and the performance of the circuit are significantly affected by them. Compared to the ideal analysis reviewed in [4], new operation stages (Figure 2) must be considered. Also, the most representative waveforms are shown in Figure 3.

- Stage 1 ('St1' – Fig.2(a)) from t_1 to t_2: the MOSFET is ON and the 'Forward' diodes (subscripted with odd numbers)

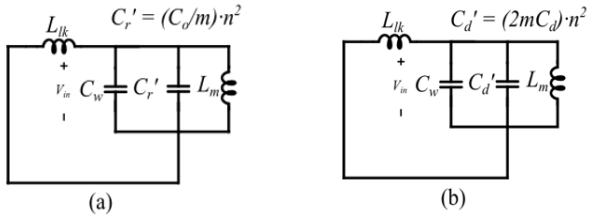


Fig 4 Equivalent resonant circuits of the DCM FF-CWVM (a) St1; (b) St2

are polarized. The Forward energy flows through the secondary side, charging the C_i capacitors. Figure 4(a) shows the equivalent resonant circuit during 'St1'. As explained in [4], the resonant capacitance (C_r') depends on the secondary side capacitors and it is estimated based on the behavior of the CWVM. The resonance occurs between C_r' and the leakage inductance (L_{lk}) because the winding capacitance of the transformer (C_w) is negligible compared to C_r'. Simultaneously, the magnetizing current rises and the Flyback energy is stored in the transformer.

- Stage 2 ('St2' – Fig.2(b)) from t_2 to t_3: when the previous resonance ends, the Forward diodes are turned OFF. The MOSFET remains conducting and the energy is still being stored in the magnetizing inductance. A resonant current is overlapped in the waveforms, as shown in Figure 3, and the equivalent circuit during 'St2' is depicted in Figure 4(b). The leakage inductance and the parasitic capacitances C_w and C_d' (the parasitic capacitance of the diodes referred to primary side) form the resonant circuit.

- Stage 3 ('St3' – Fig.2(c)) from t_3 to t_4: the MOSFET is turned OFF. Before delivering the energy stored in the magnetizing inductance to the voltage multiplier, the parasitic capacitances of the circuit (C_w, C_d' and the MOSFET C_{oss}) must be either charged or discharged. This voltage transition must always be accomplished, even though it is performed almost immediately in most of the converters. However, at very low power and very high voltage gain specifications, the influence of the parasitic capacitances becomes relevant, resulting in a very slow voltage transition.

The energy stored in the magnetizing inductance must perform this slow voltage transition in a Flyback converter. In principle, in order to compensate this effect, the duty cycle must be increased to allow a bigger energy storage in the transformer, which reduces the effective duty cycle of the converter. Therefore, the voltage gain is affected by this issue and Equation (1) is no longer met. The impact of the slow voltage transition on the gain and the efficiency of the converter will be discussed in Section III.

- Stage 4 ('St4' – Fig.2(d)) from t_4 to t_5: the 'Flyback' diodes (subscripted with even numbers) are polarized and the remaining magnetizing energy is delivered to the voltage multiplier, charging the C_{Oi} capacitors. The operation along this stage is also explained in [4] and corresponds to a conventional Flyback converter.

- Stage 5 ('St5' – Fig.2(e)) from t_5 to t_6: the Flyback diodes are turned OFF. Another resonant stage is defined, as depicted in Figure 3. The equivalent resonant circuit between the parasitic capacitances and the magnetizing inductance is illustrated in Figure 5(a). In order to save this resonant energy,

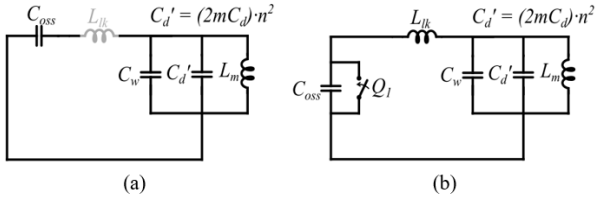


Fig 5 Equivalent resonant circuits of the DCM FF-CWVM (a) St5; (b) St6

ZVS must be achieved, increasing the efficiency and improving the behavior of the converter. This feature will be analyzed in detail in Section III. The impact in the waveforms when ZVS is not achieved is explained in the next operation stage.

- Stage 6 ('St6' – Fig.2(f)) from t_0 to t_1: the MOSFET is just turned ON and the current demanded by the parasitic capacitances to be either charged or discharged must flow through the MOSFET. Then, the initial condition of the current through the leakage inductance (equal to the MOSFET current) at the beginning of 'St1' is not zero, as expressed in (11). Therefore, if ZVS is not achieved at the end of 'St5', the behavior of the circuit during the 'St1' is affected and the current waveforms become distorted. The energy required to perform this hard-switching operation depends on the value of the parasitic capacitances and the voltage across them when the MOSFET is turned ON.

$$i_{lk}\,(t{=}t_1) = i_{mos}\,(t{=}t_1) \neq 0 \tag{11}$$

III. ZVS AND SLOW VOLTAGE TRANSITION

A. ZVS considerations

The ZVS is critical since it significantly improves the behavior and the efficiency of the converter. The higher the charge of the parasitic capacitances when the MOSFET turns ON, the higher the peak in the MOSFET and the secondary currents. The advantages will be summarized along this section and will be validated in Section IV.

In order to achieve ZVS, the MOSFET must be turned ON when the voltages across every parasitic capacitances have reached the 'St1' voltage levels. Taking the v_{ds} waveform as a reference (Figure 3(e)), the MOSFET must be turned ON when the minimum of the 'St5' resonance is reached. Therefore, the switching frequency and the duty cycle must be adjusted to obtain the desired voltage gain of the converter while achieving ZVS.

When this feature is achieved, the resonant energy flowing through the parasitic capacitances and the magnetizing inductance during stage 'St5' is saved and the waveforms of the converter are similar to the theoretical ones. This implies that the peak currents through the MOSFET, the transformer and the diodes are minimized, reducing their RMS values and the EMI noise. Then, the ZVS feature increases significantly the efficiency and improves the behavior of the converter.

B. Slow voltage transition: impact on the circuit

The slow voltage transition occurs because the parasitic capacitances must be either charged or discharged before the transformer is able to send the energy stored in the magnetizing inductance to the secondary side. The time to perform this transition (t_{SVT}) is calculated in Equation (12),

where C_{par} is the total parasitic capacitance in primary side (13) and $I_{m,pk}$ is the peak value of the magnetizing current.

$$t_{SVT} = \frac{C_{par} V_o}{n m I_{m,pk}} \tag{12}$$

$$C_{par} = C_w + C_d{}' + C_{oss} \tag{13}$$

As a result, this extra t_{SVT} must be added to the switching period, which was not included in Equation (1). Therefore, the slow voltage transition does not negatively affect the voltage gain but it must be take into account when calculating the switching frequency and the duty cycle of the converter to obtain ZVS. In conclusion, it influences the voltage gain but can be corrected by adding the t_{SVT} to the period.

On the other hand, the impact of the slow voltage transition on the efficiency can be separated in two terms:

(1) The maximum magnetizing current flows through the transformer during a longer time, compared to the ideal operation, in order to charge and discharge the parasitic capacitances, causing additional losses.

(2) The drain-source voltage across the MOSFET cannot instantaneously increase, so a 'quasi' Zero Current Switching (ZCS) is naturally achieved, saving some turn-off losses as a result.

IV. Validation and Experimental Results

The specifications of the circuit are illustrated in Table I. As explained in the previous section, the switching frequency and the duty cycle are adjusted in order to achieve ZVS. Simulation and experimental results are provided to validate the theoretical analysis accomplished along this paper.

TABLE I. Specifications of the Circuit

Parameter	*Symbol*	*Value*
Input voltage	V_{in}	12V
Output voltage	V_o	3kV
Output power	P_o	1 5W
Transformer turn ratio	n	1:25
Number of VM-stages	m	5
Switching Frequency	f_{sw}	55kHz

A. Simulations

In order to compare the behavior of the circuit under ZVS and hard-switching conditions, as well as the remaining features analyzed along this paper, the following simulations are performed. The MOSFET current and drain-source voltage waveforms, with and without achieving ZVS, are depicted in Figures 6 and 7, respectively.

The comparison between the MOSFET current waveforms clearly shows the impact of achieving 'quasi' ZVS. Although a perfect ZVS operation cannot be performed, the MOSFET is turned ON when the drain-source voltage reaches the minimum of the resonance that occurs in the stage 'St5'. On the other hand, the slow voltage transition during the stage 'St3' can also be observed in the MOSFET drain-source voltage waveforms.

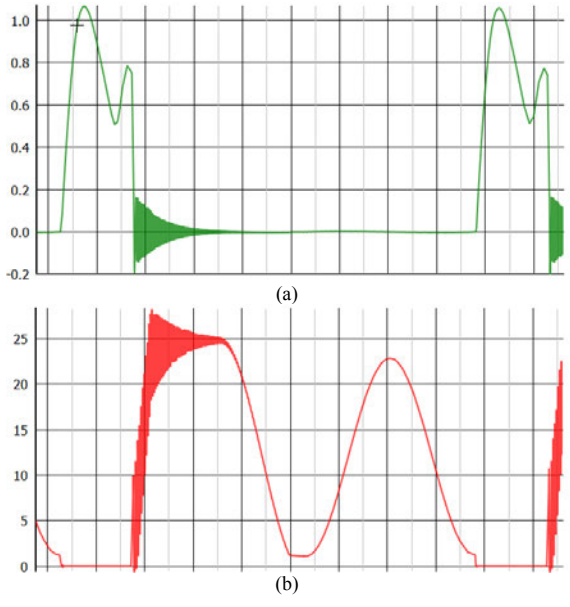


Fig 6 ZVS waveforms: (a) MOSFET current; (b) MOSFET drain-source voltage

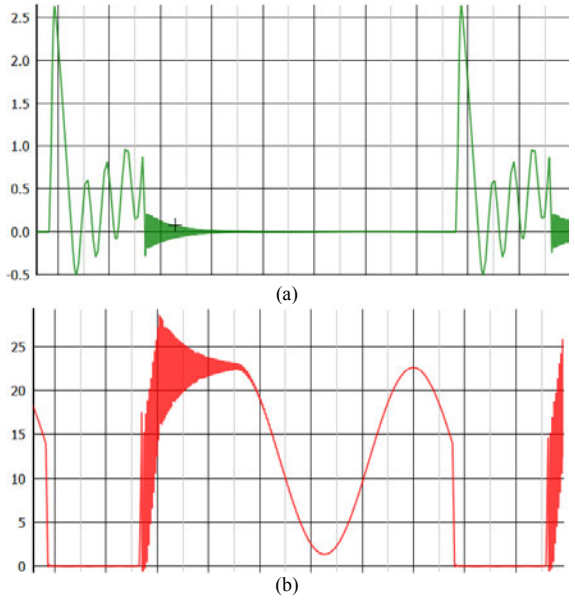


Fig 7 No ZVS waveforms: (a) MOSFET current; (b) MOSFET drain-source voltage

B. Experimental Results

The theoretical analysis of the parasitic capacitances has been verified by testing a 5-stages CWVM Forward-Flyback prototype. A picture of the PCB is illustrated in Figure 8 and the converter specifications were shown in Table I. The transformer measurements have been performed following the method proposed in [7], and the parasitic capacitances have been calculated according to [8]. This parameters are depicted in Table II, as well as the value of the output capacitance. This one is calculated after the leakage inductance is measured in order to properly set the resonant frequency of the current through the MOSFET during stage 'St1'.

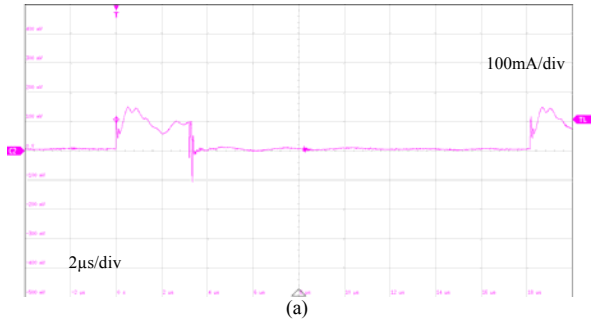
Fig 8 FF-CWVM prototype with 5 VM-stages

TABLE II. MEASUREMENTS AND CALCULATIONS OF THE PARAMETERS OF THE TRANSFORMER

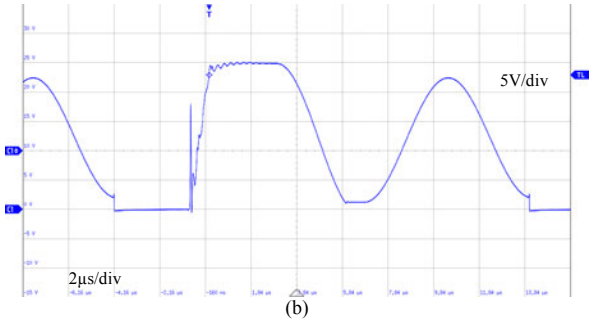
Parameters of the transformer	*Symbol*	*Value*
Magnetizing inductance	L_m	46 5µH
Leakage inductance	L_{lk}	510nH
Total winding parasitic capacitance	C_w	20nF
Diode parasitic capacitances	C_d	0 2pF
Output capacitances	C_o	22nF

In order to check the non-ideal behavior of the converter under very low power and very high voltage gain conditions, the drain-source voltage and the current through the MOSFET are also measured in the prototype. These waveforms are illustrated in Figures 9 and 10, with and without achieving 'quasi' ZVS, respectively. In both cases, the secondary current (i_{sec}) is also measured to check the most representative waveforms in the prototype.

Resistive and EHD loads are both tested to check their performance. The only difference between them is that the EHD load behaves as a capacitor until the corona discharge occurs, generating the plasm and ionizing the air between the electrodes [1]. This ions are attracted by the electric field, creating an air flow that can be used to cool electronic devices. At 3kV, the EHD load has been characterized to demand 1.5W to the converter, behaving as a resistive load.



(a)



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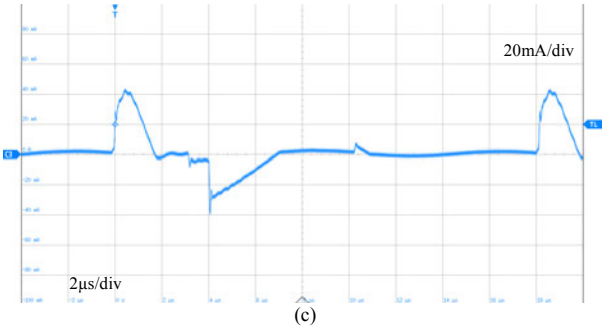
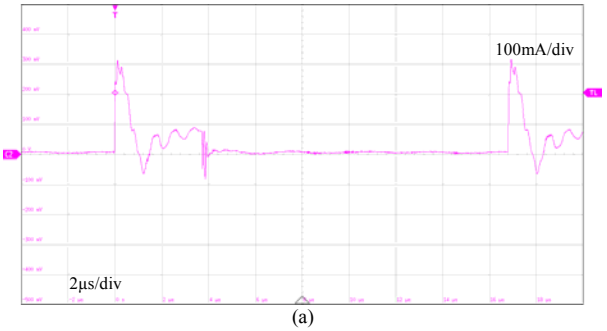
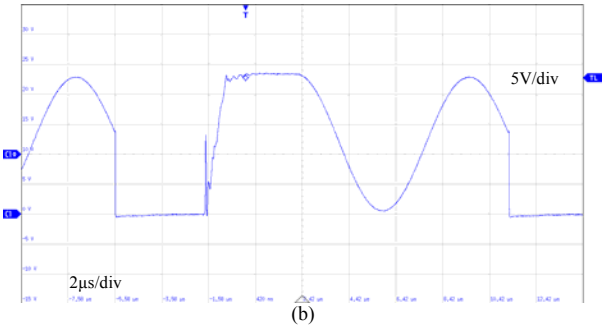


(c)

Fig 9 ZVS experimental waveforms (a) MOSFET current (i_{mos}); (b) MOSFET drain-source voltage (v_{ds}); (c) Secondary current (i_{sec})



(a)



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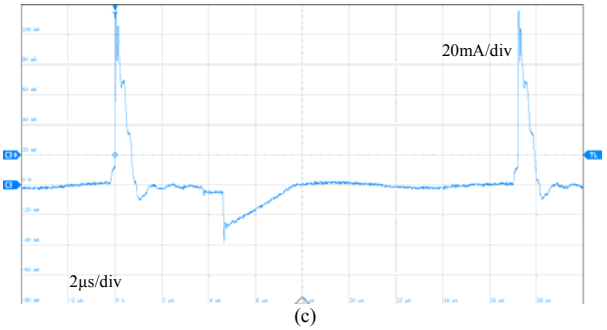

(c)

Fig 10 No ZVS experimental waveforms: (a) MOSFET current (i_{mos}); (b) MOSFET drain-source voltage (v_{ds}); (c) Secondary current (i_{sec})

The differences between the waveforms when 'quasi' ZVS is achieved and when the MOSFET is hard-switched are notorious. In order to describe this feature, the v_{ds} waveforms are used as example in Figures 9(b) and 10(b). Although a perfect ZVS cannot be achieved, the MOSFET is turned ON when the voltage across the parasitic capacitances is only 10% of its maximum value ($v_{ds,max}$). On the other hand, the hard-switching operation is tested when that voltage is 60% of $v_{ds,max}$. The main benefits of achieving 'quasi'

ZVS in terms of the behavior of the converter, which are illustrated in the Figures 9 and 10, are summarized next:

(1) The drain-source voltage of the MOSFET shows the voltage at which the MOSFET is turned ON, which is the minimum of v_{ds}. This way, the resonant energy flowing through the parasitic capacitances and the magnetizing inductance is almost entirely saved and the current waveforms of the converter are not distorted.
(2) The current through the MOSFET and the secondary current are similar to the theoretical ones. This decreases their RMS values and reduces the EMI noise. In addition, the resonant current is almost sinusoidal and its frequency is the desired one.

On the other hand, the current waveforms when the ZVS is not achieved are distorted, due to the reasons explained previously. The peak values of said currents are huge and very dangerous for the semiconductors of the circuit, mainly for higher output power specifications.

Regarding the impact of the ZVS on the efficiency of the converter, measurements have been taken for both cases, which are depicted in Table III. The obtained efficiency is 93.44% when 'quasi' ZVS is achieved and 90.02% when it is not. Gate driver losses are not included in this measurements.

TABLE III. MEASUREMENTS

Parameter	***Symbol***	***Value***
Input voltage	V_{in}	12 0 V
Output resistance	R_o	6 1 MΩ
With ZVS		
Output current	$\boldsymbol{I_o}$	500 μA
Output voltage	V_o	3050 V
Output power	P_o	1 525 W
Input power	P_{in_ZVS}	1 632 W
Efficiency (ZVS)	η_{ZVS}	93 44 %
Without ZVS		
Output current	$\boldsymbol{I_o}$	500 μA
Output voltage	V_o	3050 V
Output power	P_o	1 525 W
Input power (ZVS)	P_{in_NoZVS}	1 694 W
Efficiency (ZVS)	η_{NoZVS}	90 02 %

V. CONCLUSIONS

A deep analysis of the DCM Forward-Flyback converter with CWVM for very high voltage gain (1:250) and very low power (1.5W) applications has been performed. The influence of the parasitic capacitances has been analyzed in detail, highlighting the impact of the 'quasi' ZVS and the slow voltage transition on the operation stages and the efficiency of the converter. The main contributions of this paper have been validated, obtaining a good matching between the simulation and the experimental results. The obtained efficiency is η = 93.44% when 'quasi' ZVS is achieved and η = 90.02% without ZVS at very low load (1.525W, 500μA, 3050V output).

The 'quasi' ZVS operation is accomplished by turning the MOSFET ON when the voltage across the parasitic capacitances is 10% of its maximum value, while the hard-switching operation is tested when that voltage is at 60% of that maximum value. Although the converter is operated in open loop, a variable switching frequency control is needed to assure the MOSFET is turned ON at the minimum of the resonance that occurs in the stage 'St5' between the parasitic capacitances and the magnetizing inductance. The design of the control stage will be analyzed in detail in the future.

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