Hindawi Publishing Corporation
Active and Passive Electronic Components
Volume 2009, Article ID 987304, 4 pages
doi:10.1155/2009/987304

Research Article

DDCC-Based Quadrature Oscillator with Grounded Capacitors and Resistors

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Received 2 October 2008; Revised 24 November 2008; Accepted 19 January 2009

Recommended by Krishnamachar Prasad

A new voltage-mode quadrature oscillator using two differential difference current conveyors (DDCCs), two grounded capacitors, and three grounded resistors is presented. The proposed oscillator provides the following advantages: the oscillation condition and oscillation frequency are orthogonally controlled; the oscillation frequency is controlled through a single grounded resistor; the use of only grounded capacitors and resistors makes the proposed circuit ideal for IC implementation; low passive and active sensitivities. Simulation results verifying the theoretical analysis are also included.

1. Introduction

Second-generation current conveyors (CCIIs) have been found very useful in many applications. This is attributed to their higher signal bandwidths, greater linearity, and larger dynamic range than those of the operational-amplifiers (op-amps) based ones. Recently, Chiu et al. [1] proposed a new current conveyor circuit called the differential difference current conveyor (DDCC). The DDCC has the advantages of both the CCII and the differential difference amplifier (DDA) (such as high input impedance and arithmetic operation capability) [1].

A quadrature oscillator typically provides two sinusoids with 90° phase difference for a variety of applications, such as in telecommunications for quadrature mixers, in single-sideband generators, in direct-conversion receivers, or for measurement purposes in vector generators or selective voltmeters [2, 3]. As a result, a number of circuits have been presented in technical literature [4–8].

In this paper, a new voltage-mode quadrature oscillator based on DDCCs is presented. The proposed circuit employs two DDCCs, two grounded capacitors, and three grounded resistors. The proposed circuit enjoys independent oscillation control through a single grounded resistor and independent frequency control through another single grounded resistor. The use of grounded capacitors and resistors makes the proposed circuit suitable for integrated circuit implementation [9]. The theoretical results are verified by PSpice simulation.

2. Proposed Circuit

The electrical symbol of DDCC is shown in Figure 1. It was proposed in 1996 by Chiu et al. [1], and it enjoys the advantages of CCII and DDA such as larger signal bandwidth, greater linearity, wider dynamic range, simple circuitry, low power consumption, and high input impedance [1]. The DDCC has three voltage input terminals: $Y1$, $Y2$, and $Y3$, which have high input impedance. Terminal X is a low-impedance current input terminal. There is a high-impedance current output terminal Z. The input-output characteristics of the DDCC is described as [1]

$$\begin{pmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ I_Z \end{pmatrix} = \begin{pmatrix} 1 & -1 & 1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{pmatrix} \begin{pmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ I_X \end{pmatrix}. \quad (1)$$

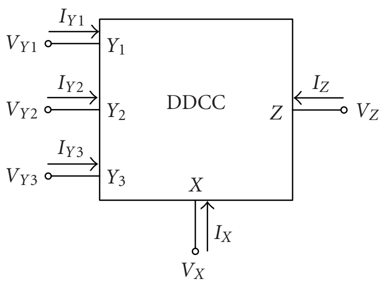

FIGURE 1: Electrical symbol of DDCC.

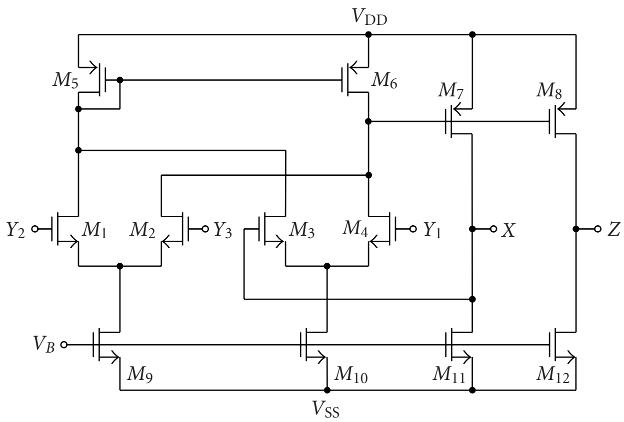

FIGURE 2: The CMOS implementation of DDCC.

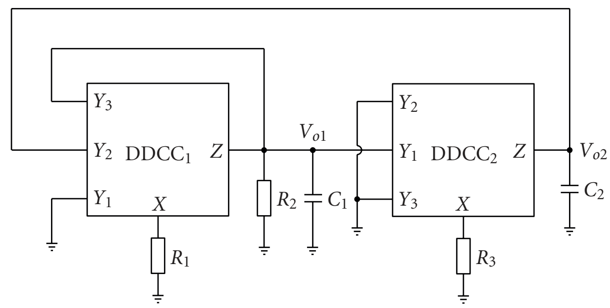

FIGURE 3: Proposed voltage-mode quadrature oscillator.

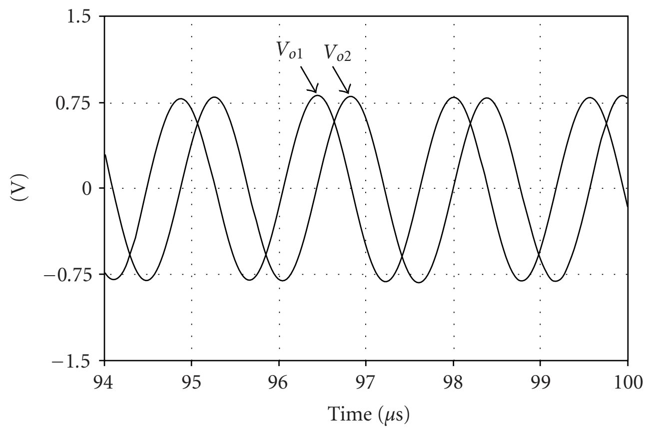

FIGURE 4: The simulated quadrature output waveforms.

The CMOS realization of the DDCC used in this paper for the quadrature oscillator circuit is shown in Figure 2.

The proposed quadrature oscillator is shown in Figure 3. It is composed of two DDCCs, two grounded capacitors, and three grounded resistors. The characteristic equation of the circuit can be expressed as

$$s^2 C_1 C_2 R_1 R_2 R_3 + s C_2 R_3 (R_1 - R_2) + \frac{R_2^2}{R_1} = 0. \tag{2}$$

The oscillation condition and oscillation frequency can be obtained as

$$R_1 \leq R_2, \tag{3}$$

$$\omega_o = \sqrt{\frac{R_2}{C_1 C_2 R_3 R_1^2}}. \tag{4}$$

It can be seen from (3) and (4) that the oscillation condition can be adjusted by grounded resistor R_1 or/and R_2 and the oscillation frequency can be controlled by varying the grounded resistor R_3 without disturbing the oscillation condition. This means that the oscillation frequency and oscillation condition are orthogonaly controlled. By using a JFET to replace R_3, a voltage-controlled oscillator can be obtained [10]. From (4), the passive sensitivities of proposed quadrature oscillator are low. From Figure 3, DDCC$_2$ along with C_2 and R_3form the lossless integrator. Hence, the phase difference ϕ between V_{o1} and V_{o2} is given by

$$\phi = \pi - \tan^{-1}(\omega R_3 C_2). \tag{5}$$

At $\omega = \omega_0$, (5) can be obtained as $\phi = \pi/2$, ensuring that the currents V_{o1} and V_{o2} are in quadrature.

3. Nonideal Effects

To consider the nonideal effect of a DDCC, taking the nonidealities of the DDCCs into account, the relationship of the terminal voltages and currents can be rewritten as [11]

$$\begin{pmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ I_Z \end{pmatrix} = \begin{pmatrix} \alpha_{k1} & -\alpha_{k2} & \alpha_{k3} & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \beta_k \end{pmatrix} \begin{pmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ I_X \end{pmatrix}, \tag{6}$$

where $\alpha_{k1} = 1 - \varepsilon_{k1v}$ and ε_{k1v} ($|\varepsilon_{k1v}| \ll 1$) denotes the voltage tracking error from V_{Y1} terminal to V_X terminal of the kth DDCC, $\alpha_{k2} = 1 - \varepsilon_{k2v}$ and ε_{k2v} ($|\varepsilon_{k2v}| \ll 1$) denotes the voltage tracking error from V_{Y2} terminal to V_X terminal of the kth DDCC, $\alpha_{k3} = 1 - \varepsilon_{k3v}$ and ε_{k3v} ($|\varepsilon_{k3v}| \ll 1$) denotes the voltage tracking error from V_{Y3} terminal to V_X terminal of the kth DDCC, and $\beta_k = 1 - \varepsilon_i$ and ε_i ($\varepsilon_i \ll 1$) denotes the output current tracking error of the kth DDCC. The characteristic equation of Figure 3 becomes

$$s^2 C_1 C_2 R_1 R_2 R_3 + s C_2 R_3 (R_1 - R_2 \alpha_{13} \beta_1) + \frac{R_2^2 \alpha_{12} \alpha_{21} \beta_1 \beta_2}{R_1} = 0. \tag{7}$$

Table 1: CMOS model used in simulation.

.MODEL NMOS LEVEL = 3 UO = 460.5 TOX = 1.0E-8 TPG = 1 VTO = +0.62
JS = 1.08E-6 XJ = 0.15U RS = 417 RSH = 2.73 LD = 0.04U VMAX = 130E3 NSUB = 1.71E17
PB = 0.761 ETA = 0.00 THETA = 0.129 PHI = 0.905 GAMMA = 0.69 KAPPA = 0.10 CJ = 76.4E-5
MJ = 0.357 CJSW = 5.68E-10 MJSW = 0.302 CGSO = 1.38E-10 CGDO = 1.38E-10
CGBO = 3.45E-10 KF = 3.07E-28 AF = 1 WD = +0.11U DELTA = +0.42 NFS = 1.2E11 DELL = 0U
LIS = 2 ISTMP = 10 TT = 0.1E-9
.MODEL PMOS LEVEL = 3 UO = 100 TOX = 1.0E-8 TPG = 1 VTO = −0.58
JS = 0.38E-6 XJ = 0.10U RS = 886 RSH = 1.81 LD = 0.03U VMAX = 113E3 NSUB = 2.08E17
PB = 0.911 ETA = 00 THETA = 0.120 PHI = 0.905 GAMMA = 0.76 KAPPA = 2 CJ = 85E-5
MJ = 0.429 CJSW = 4.67E-10 MJSW = 0.631 CGSO = 1.38E-10 CGDO = 1.38E-10
CGBO = 3.45E-10 KF = 1.08E-29 AF = 1 WD = +0.14U DELTA = 0.81 NFS = 0.52E11 DELL = 0U
LIS = 2 ISTMP = 10 TT = 0.1E-9

Table 2: Transistor aspect ratios of the used DDCC.

MOS transistor	W/L
M_1–M_4	1.6/1
M_5-M_6	8/1
M_7-M_8	20/1
M_9-M_{10}	29/1
M_{11}-M_{12}	90/1

The modified oscillation condition and oscillation frequency are

$$R_1 \le R_2\alpha_{13}\beta_1, \quad (8)$$

$$\omega_o = \sqrt{\frac{R_2\alpha_{12}\alpha_{21}\beta_1\beta_2}{C_1C_2R_3R_1^2}}. \quad (9)$$

From (7) and (8), the tracking errors slightly change the oscillation condition and oscillation frequency. However, the oscillation condition and oscillation frequency still can be orthogonally controllable.

4. Simulation Results

To verify the theoretical prediction of the proposed circuit, Figure 3 has been simulated using PSpice simulation program. The DDCC in Figure 2 was simulated using the 0.5 μm MIETEC as tabulated in Table 1 [12]. The transistor aspect ratios of DDCC are listed in Table 2 [12], and the supply voltages were $V_{DD} = -V_{SS} = 2.5$ V. The biasing voltage V_B was taken as −1.7 V. The quadrature oscillator was designed with $C_1 = C_2 = 50$ pF, $R_1 = R_3 = 5$ kΩ, and $R_2 = 5.2$ kΩ for the oscillation frequency of $f_0 = 649$ kHz that where R_2 was varied with R_1 by (3) to ensure the oscillator will start. The simulation results are shown in Figure 4. In this figure, the oscillation frequency of 640 kHz is obtained. The oscillation frequency is 640 kHz instead of 649 kHz owing the effect described in Section 3. According to (9), this drop-off would be caused by voltage and current tracking errors. Figure 5 shows the simulated frequency spectrums of V_{o1} and V_{o2} in Figure 4. The result of the V_{o2} total harmonic distortion analysis is 1.02%. Figure 6 shows the simulation results of the proposed quadrature oscillator in Figure 3 by varying the values of the resistor R_3 with $C_1 = C_2 = 50$ pF, $R_1 = 5$ kΩ, and $R_2 = 5.2$ kΩ. The nonidealities may be due to the ignored tracking errors of the DDCC.

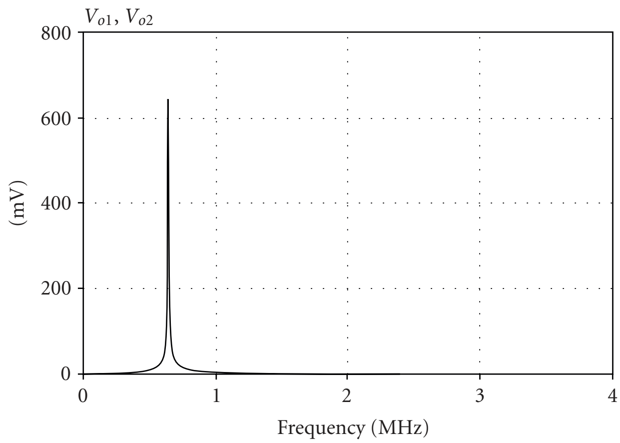

Figure 5: The simulated frequency spectrum of V_{o1} and V_{o2}.

5. Conclusions

In this paper, a new DDCC-based voltage-mode quadrature oscillator circuit has been presented. The proposed circuit employs two DDCCs, two grounded capacitors, and three grounded resistors. The proposed circuit enjoys independent oscillation control through a single grounded resistor and independent frequency control through another single grounded resistor. The use of grounded capacitors makes the circuit attractive for integration, and the use of grounded resistor for independent control of the oscillation frequency makes the circuit attractive for the realization of voltage-controlled oscillators. The active and passive sensitivities are

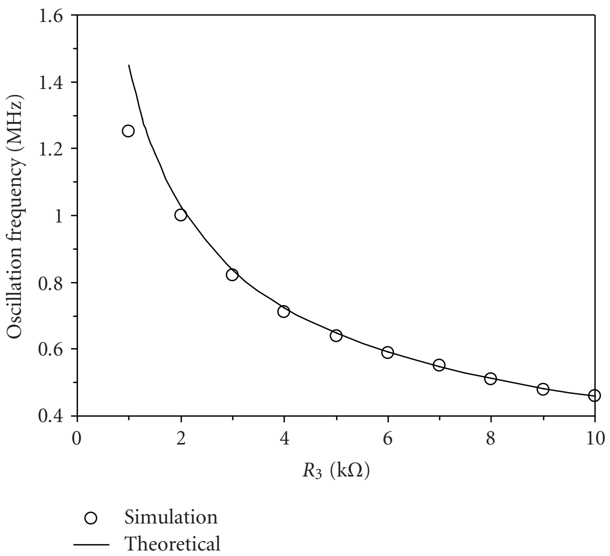

Figure 6: Simulated results of the oscillation frequency.

no more than unity. Simulation results, which confirm the theoretical analysis, are obtained.

Acknowledgment

The authors would like to thank the anonymous reviewers for their valuable comments.

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