IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received December 5, 2018, accepted January 18, 2019, date of publication January 25, 2019, date of current version February 22, 2019.

Digital Object Identifier 10.1109/ACCESS.2019.2895388

DDS-PLL Phase Shifter Architectures for Phased Arrays: Theory and Techniques

GIULIO D'AMATO[1], GIANFRANCO AVITABILE[1], GIUSEPPE COVIELLO[1], AND CLAUDIO TALARICO[2]

[1]Dipartimento di Ingegneria Elettrica e dell'Informazione, Politecnico di Bari, 70125 Bari, Italy
[2]Department of Electrical and Computer Engineering, Gonzaga University, Spokane, WA 99258, USA

Corresponding author: Giulio D'Amato (giulio.damato@poliba.it)

ABSTRACT The main purpose of this paper is to review the framework behind direct digital synthesizer phase-locked loops (DDS-PLLs), as well as to provide a set of novel techniques that can be used during the development and the deployment of phased arrays based on local oscillator (LO) phase shifting approaches. A beam steering transmitter prototype employing our revised DDS-PLL architecture and the experimental results obtained during its characterization are presented. The main contribution of the proposed implementation consists in showing that the output phase increments of the DDS-PLL are unaffected by the frequency multiplication operated by the PLL. The proposed prototype is centered at 3.350 GHz and allows to independently set the phase of its four LOs at 2.453 GHz with an 8-bit resolution. The DDS-PLL architecture is frequency-independent, and the modular structure of its phase control units allows to achieve different phase resolutions with a very small redesign effort.

INDEX TERMS Beam steering transmitter, DDS-PLL, direct digital synthesizer (DDS), phase-locked loop (PLL), phase shifter.

I. INTRODUCTION

Phased arrays are antennas made up of at least two stationary elements whose radiation pattern can be shaped and steered by assigning a convenient phase and amplitude relation to the currents fed to each of its radiators [1]. Although phased arrays were first conceived in the early 1900s and have been used in warfare applications since World War II, over the years their technology has steadily evolved, and nowadays there is a renewed interest in their application to consumer electronics. This is because they provide, compared to single element antennas, many advantages, including the opportunity to focus and steer the beam without the need to move their individual elements.

There is a large body of work describing circuits and systems that are capable of driving electronically scanned arrays, a.k.a. beam steering units (BSUs). A common classification consists of considering the BSUs according to the physical principle and devices used to implement the required phase shifts at the antennas. Common examples are the BSUs based on transmission lines. The basic idea is to implement phase shifts exploiting propagation delay mismatches arising in electrical [2], [3], microelectromechanical [4], [5] or optical [6], [7] circuits. With this approach, the signal is routed through paths characterized by different electrical lengths. This can be achieved either through the fabrication of paths whose physical length is different or by locally altering the electrical properties of the medium where the propagation of the signals is taking place. A second common classification is made by considering the portion of the circuit where the phase shifts are implemented (Fig. 1), namely Radio Frequency (RF), Intermediate Frequency (IF), Baseband (BB) and Local Oscillator (LO) paths. To date, RF phase shifting architectures are the ones that have been most commonly used to implement phased arrays. In these architectures, phase shifting is performed near the antennas, either after the signal up-conversion for the transmitter or before the down-conversion for the receiver. These architectures are characterized by one LO distribution point and the use of a single mixer. RF phase shifting architectures can be designed for intrinsic resilience to strong interferers. This is because unwanted contributions captured by the antennas can be canceled before any other signal conditioning takes place, which is where the desired signal risks to be distorted by the

The associate editor coordinating the review of this manuscript and approving it for publication was Bora Onat.

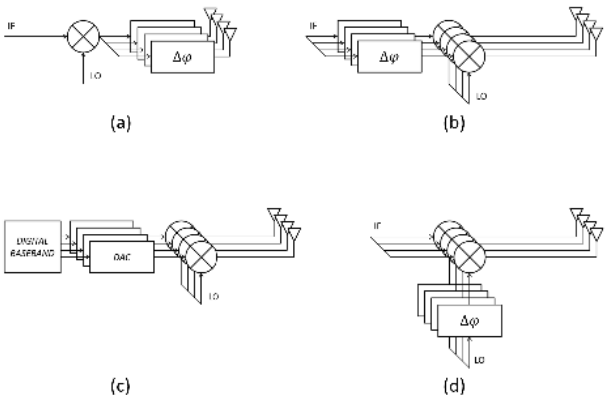

FIGURE 1. (a) RF phase shifting; (b) IF phase shifting; (c) BB phase shifting; (d) LO path phase shifting.

saturation of the input dynamic range. However, having phase shifters in the RF path means that they must be rated for high frequencies, where non-idealities cannot be neglected. This causes most designs to occupy a large on-chip area and to require expensive technology processes for their fabrication. In the case of IF phase shifting architectures, phase shifting is performed before the up-conversion or after the down-conversion stage. These solutions operate at a much lower frequency than the ones that have just been discussed, and thus their requirements are more relaxed. However, the complexity of the overall circuit topology is higher: IF phase shifting architectures require one frequency conversion stage for each antenna of the array. This also means that an LO distribution network capable of guarantying phase coherency at its output ports must be designed. Since filtering is done after the frequency conversion, these architectures can become non-functional in presence of strong interferers. Phase shifting architectures working in BB are frequently developed through all-digital beamforming [8]. In such systems, beamforming in the transmit path is accomplished by imposing phase shifts and amplitude weights to digital streams of samples ultimately converted to analog signals through a DAC. This means that to implement a transceiver, each antenna must be equipped with an ADC and a DAC. Additionally, the bandwidth of the involved signals must be small enough so that all the required computations can be performed in real time by a DSP. Digital phased arrays can synthesize multiple beams, perform adaptive enhancements to the radiation pattern, and estimate directions of arrival. Unfortunately, these advantages have a considerable cost, both in terms of power consumption and increased complexity of the system. In LO phase shifting architectures, the LO is the only component that has to be phase shifted in order to perform beam steering [9], [10]. In these architectures, phase shifts are indirectly imposed to signals during frequency conversion. For this reason, typical performance degradations (e.g. losses, non-linearity, and noise) due to the insertion of phase shifters can be neglected. Since phase shifts are applied to single tones (rather than across the whole signal bandwidth), special techniques, that are about to be discussed, can be employed for their implementation. It must be noted that the LO phase shifting approach implements an approximation of the linear phase shifts ideally required to drive a phased array. In fact, they merely add a constant phase offset to each frequency component of the output signal, thus introducing a deterministic phase distortion.

Among the many solutions that have been reviewed, the LO phase shifting approach is the most promising. This is especially true when phase shifts are implemented during the very synthesis process of the LO, as it happens in direct digital synthesizer phase-locked loops (DDS-PLLs). DDS-PLLs are well recognized [11] as a solution to implement economic, compact and lightweight BSUs for phased arrays, and are characterized by an exceptional phase resolution and a frequency independent theory of operation. Since the steering resolution is a function of the phase shifters' resolution, it becomes extremely beneficial in large phase arrays with narrow main lobes.

Considered the above state of the art, the focus of our work has been to review and expand the framework behind DDS-PLLs and to disclose a set of techniques we prepared during the development of our prototypes. Moreover, we present a beam steering transmitter based on our revised DDS-PLL architecture along with the experimental results obtained during its characterization. In this paper, for the first time, we demonstrate why, in certain circumstances, the output phase increments of DDS-PLLs are unaffected by the frequency multiplication operated by the PLL, and we show the measured results of beam steering for our transmitter acquired in multiple angular positions and for different steering angles.

The rest of the paper is organized as follows. Section II reviews the theory of operation of conventional and revised DDS-PLL phase shifters. Section III presents a set of techniques that can be used during the development and the deployment of phased arrays based on the proposed phase shifting approach. Section IV presents a beam steering transmitter prototype employing a revised DDS-PLL architecture. Finally, Section V discusses the experimental results collected during the characterization of the prototype.

II. THEORY OF OPERATION OF DDS-PLL PHASE SHIFTERS

DDS-PLLs are electronic circuits that can be used to synthesize LOs whose phase can be adjusted in fine-grained steps. This is done through a PLL synthesizer, whose output phase and frequency is controlled by the output phase and frequency of a DDS.

Fig. 2 shows a simple schematic representation of the DDS-PLL structure. According to a well-established theory [12], the DDS signal along with the feedback output signal generates an error voltage that, suitably filtered, forces the voltage-controlled oscillator (VCO) instantaneous phase divided by an integer factor, N, to be equal to the DDS reference phase. Thus, in DDS-PLLs, the DDS block allows, under the control of a digital Phase Tuning Word (PTW),

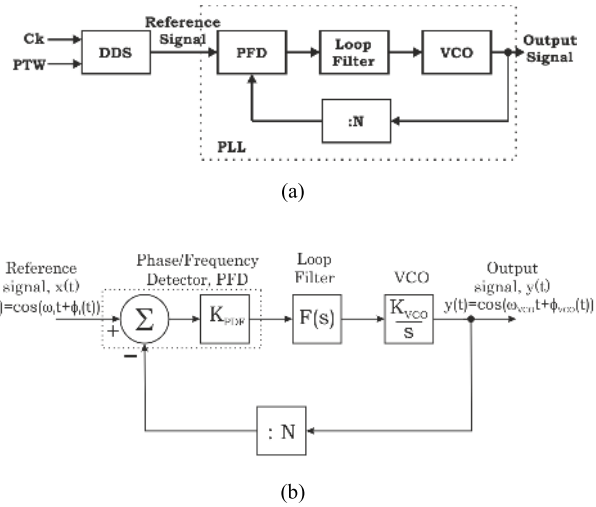

FIGURE 2. (a) DDS-PLL phase shifter's block diagram; (b) Simplified linear model of the PLL.

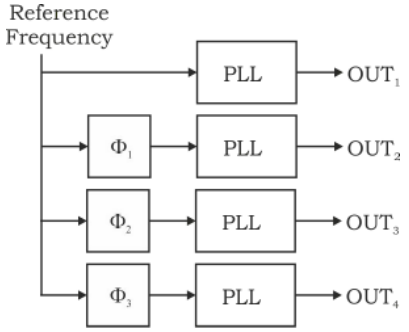

FIGURE 3. Mutual phase-shift between multiple channels.

to continuously vary the reference phase produced at its output, and therefore it acts as the phase control unit (PCU) of the PLL output. This allows combining the PLLs' ability to generate stable high-frequency tones with the exceptionally high phase resolution of DDSs.

For a system with multiple output channels, the phase shift associated with each signal requires the definition of one of the channels as a reference. Fig. 3 illustrates how, thanks to the properties of the PLL, different phase shifts of the same reference signal determines the required corresponding mutual shifts in the output signals.

The DDS, in our case, feeds the phase shifted reference signal to the second, third and fourth channel by retrieving time-shifted replicas of the same stored waveform. The main difference between this and other approaches to phase shifting is that in this case phase shifts are introduced during the synthesis process of the LO. This means that the LO is directly synthesized with the desired phase, rather than having the phase shifts applied after the generation of the LO. Three alternative architectures can be used to implement DDS-driven PLLs. They differ from the role assigned to the DDS into the loop. For example, one can put the DDS in the feedback path of the PLL, in order to implement a fractional divide-by-N stage [13]. Alternatively, the DDS can be used to generate the offset frequency in an offset-PLL [14]. Finally, one can use the DDS to generate the reference signal of the PLL. This last option is the simplest DDS-PLL architecture that can be implemented (Fig. 2).

Our revised-approach allows to further simplify the aforementioned DDS-PPL architecture because it does not need a traditional full DDS. Indeed, our structure does not require a sine wave but, rather, the reference signal can be a square wave with a relative delay between the various channels of Fig. 3 [15]. This provides a very important advantage: it allows to completely avoid the well-known spur issues usually associated with DDS-based sinusoidal synthesis [16], [17] thus ensuring a better spectral purity. For a more thorough theoretical analysis, the reader is encouraged to refer to [12], [17], and [18].

Given these premises and assuming phase locking has occurred, it is now evaluated in detail how, in this latter scheme, the output phase of the PLL is controlled by a phase shift at the DDS output. Let's assume that the DDS is synthesizing a sine wave. If $\Delta\varphi_{MIN}$ is the smallest phase shift that the DDS can apply to its output signal, its corresponding minimum time delay (Δt_{MIN}) is:

$$\Delta t_{MIN} = \frac{\Delta\varphi_{MIN} \cdot T_{REF}}{2\pi}$$

where T_{REF} is the period of the DDS's output sine wave (that will be used as the reference signal of the PLL). The phase shift at the PLL's output ($\Delta\varphi_{OUT}$) due to the above time delay is:

$$\Delta\varphi_{OUT} = \frac{\Delta t_{MIN}}{T_{OUT}} 2\pi = N \frac{\Delta t_{MIN}}{T_{REF}} 2\pi = N \cdot \Delta\varphi_{MIN}$$

where T_{OUT} is the period of the PLL's output waveform.

When phase-lock is achieved [12], T_{OUT} is equal to T_{REF} divided by the integer division factor, N (see Fig. 2). As it will be explained in the remainder of this section, due to the periodicity of the PLL's output, even if $\Delta\varphi_{OUT}$ is greater than $\Delta\varphi_{MIN}$, this does not mean that the phase resolution of the DDS-PLL phase shifter will be less than the one of the DDS. Since in modern phase frequency detectors (PFDs) the phase and frequency mismatch detection are operated by converting an analog input signal into a digital signal, several revised topologies have been proposed to decrease the complexity and power consumption of these DDS-PLLs [15], [19]. In fact, the DDS can be completely replaced by an all-digital PCU that, without any degradation of the PLL performance, feed square waves rather than sine waves to its PFD input. As a result, these architectures do not require a digital-to-analog conversion at the DDS output and therefore help to significantly reduce both the complexity of the circuit and its power consumption. The DAC block is usually the largest contributor [14] to the power consumption of a DDS, and thus the interest in revised DDS-PLL implementations seems more than justified.

It is important to remark that in DDS-PLLs (and their variants) the output of the PLL is locked to the one of the PCU,

but its frequency can be N times higher when acting as a frequency multiplier. This means that the relationship between the PCU's and the PLL's output phase is not trivial, even if it depends only on the phase tuning word (PTW) assigned to the PCU (namely a k-bit word, whose permutations correspond to linearly spaced angles in the [0°, 360°] range). When N is greater than 1, the sequence of output phases becomes scrambled, following a law that is now illustrated. To this end, one can quantify the output phase difference due to the assignment of two different PTWs ($\Delta PTW = PTW_1 - PTW_0$):

$$\frac{2\pi}{2^k} \cdot N \cdot \Delta PTW = \frac{2\pi}{2^k} \cdot \beta + 2\pi x \tag{1}$$

where $2\pi/2^k$ is the phase resolution of the PCU, and $\beta\epsilon\ [0 \ldots 2^k]$ and x are integer numbers. The right side of equation (1) simply decomposes the obtained phase difference into two convenient terms, namely an effective phase difference and an integer number of turns around the phase wheel. Since this latter contribution can be neglected in the case of LO synthesis, one can rewrite equation (1) as follows:

$$\left(\frac{2\pi}{2^k} \cdot N \cdot \Delta PTW\right) mod\ 2\pi = \frac{2\pi}{2^k} \cdot \beta \tag{2}$$

For a generic design, the output phase difference of two consecutive PTWs can be greater than $2\pi/2^k$; however, this does not necessarily imply a degradation of the output phase resolution. When a given output phase ($\Delta\varphi_{out} = [2\pi/2^k] \cdot \beta$) has to be synthesized, the above equation must be inverted. For example, this can be done through a lookup table.

It is now shown how, in a DDS-PLL phase shifter, as long as N is an odd number, the output phase resolution is equal to the phase resolution of the PCU. Let's assume that $N = 2m + 1$ and that the effective output phase difference is 0 (namely that two PTWs would return the same effective output phase, and thus the phase resolution would not be maintained). Equation (1) would become:

$$\Delta PTW = \frac{x}{(2m+1)} \cdot 2^k \tag{3}$$

Keeping in mind that ΔPTW must be an integer number (constraint A), that ΔPTW must be less than 2^k (constraint B), and that all the dividers of 2^k are powers of 2, the only possible solution for which the equation derived would respect the constraint A is x equal or multiple of $(2m + 1)$. However, this solution would violate constraint B, because ΔPTW would have to be equal to 2^k. In other words, two different PTWs cannot produce an effective phase difference equal to 0, therefore if N is an odd number the output phase resolution of a DDS-PLL is preserved. Let's now assume that $N = 2m$ and that the effective output phase difference is again 0. Equation (1) would become:

$$\Delta PTW = \frac{x}{m} \cdot 2^{k-1} \tag{4}$$

Keeping in mind the previously defined constraints A and B, and that all the dividers of 2^k are powers of 2, there are two possibilities for which the above equation respects constraint A. The two possibilities are that x is equal to m with m being an odd number, or that m is an even number. If m is an odd number, two PTWs would return the same effective output phase, and as a byproduct, the output phase resolution is halved. If m is an even number, more than two PTWs would return the same effective output phase, depending on the greatest common divisor (GCD) of m and 2^{k-1}. The above considerations demonstrate that the output phase resolution (OPR) of a DDS-PLL is preserved if, and only if, m is an odd number, and that:

$$OPR = \frac{2^k}{GCD(N, 2^k)} \tag{5}$$

III. TECHNIQUES FOR DDS-PLL IMPLEMENTATIONS

The reviewed theory of operation is not sufficient to implement and characterize beam steering transmitters based on DDS-PLLs (and their variants). This is because some practical issues must be carefully controlled. The following set of techniques have been developed to address these practical issues.

First, mismatches due to fabrication tolerances must be compensated for. This is because they lead to unpredictable phase offsets among the output channels of the DDS-PLLs, even if they were assigned the same PTW. A calibration procedure is necessary to phase align the LOs, and thus put the phased array into a known state from which predictable mutual phase shifts can be assigned following the previous formulations. This can be achieved by exciting the IF port of the transmitter with a sine wave and then aligning adjacent outputs in pairs. Following are the steps that can be adopted:

1) Every PTW is set to 0 to put the array into its reset state.
2) One channel of the array is arbitrarily assumed as calibrated (and thus as the first reference channel).
3) All channels are muted, except for the current reference channel and the one that is going to be calibrated.
4) The two unmuted channels must be placed at an equal electrical distance from the receiver (whether we use antennas or coaxial cables and a power combiner).
5) The PTW for the phase alignment of the non-reference channel is obtained adding 2^{k-1} to the PTW corresponding to the minimum received signal strength (RSS) at the receiver and then performing a modulus 2^k operation. Thus, the PTW we look for is the one corresponding to the antiphase condition, from which the PTW for phase alignment is calculated.
6) At this point, the last calibrated channel is elected as the new reference, and its adjacent output becomes the new channel to be calibrated.
7) Steps 3 to 6 are repeated for every adjacent pair of outputs that must be calibrated.

The above steps return a vector of PTWs that ensures phase alignment. After calibration, beam steering can be accomplished using the above PTWs as offset values to be added to the theoretical PTWs obtained inverting equation (2). It is useful to note that different strategies can be used to find the PTW corresponding to the minimum RSS of each channel.

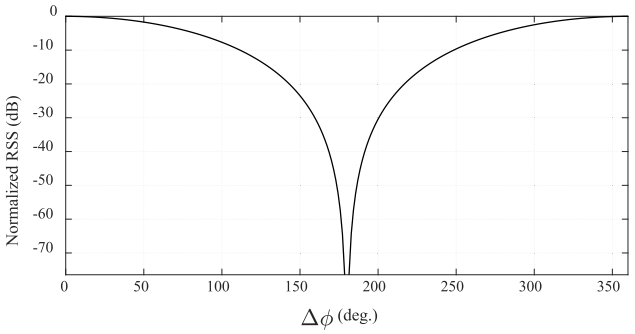

FIGURE 4. Theoretical normalized curve of the RSS when the mutual phase shift among two active output channels is varied.

One option is to inspect all PTWs to choose the one corresponding to the minimum RSS. Unfortunately, this solution can become too onerous if the resolution of the phase shifter is high or if the number of radiating elements is large. An effective workaround is to exploit the fact that the theoretical normalized RSS curve has just one minimum point (Fig. 4), as it follows from its equation:

$$RSS(\Delta\varphi) = dB(1 + cos\,(\Delta\varphi)) \tag{6}$$

A final consideration concerns the repeatability of the proposed technique and the applicability of its results. Any perturbation on the signal path affects the output phase of its corresponding channel. However, it is the PCU to PLLs interface the one that is most sensitive to mismatches. The reason lies in the previously derived theory of operation.

An alternative way to measure mutual phase shifts among the output channels is to sample the waveforms in the time domain with an oscilloscope. One can interconnect the LOs under test to an oscilloscope and measure the time difference among the zero-crossings of the acquired signals, and quantify mutual phase shifts by studying the cross-correlation function of these same signals. It is important to note that the precision of the measurement is affected by the time-base and gain settings of the instrument. To obtain consistent results, time-base and gain must be kept the same for the whole measurement process.

In an RF quiet environment, the system-level characterization of the transmitter can be performed using a simple setup consisting of a spectrum analyzer interconnected to an antenna (acting as a receiver). A 1-D characterization of the beam steering can be performed by sampling the RSS at multiple angular positions and for different steering angles assigned to the transmitter. For example, for a given steering angle, one can sample data for a full revolution of the transmitter through a motorized rotating pedestal. It is important to emphasize that, to obtain meaningful results, the distance between the phased array and the receiving antenna must be chosen in such a way that the far-field condition is satisfied, that is:

$$R_{far} = \frac{2 \cdot D^2}{\lambda} \tag{7}$$

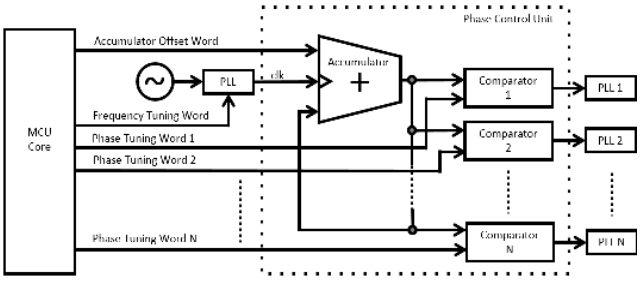

FIGURE 5. PCU architecture used to implement the revised DDS-PLLs.

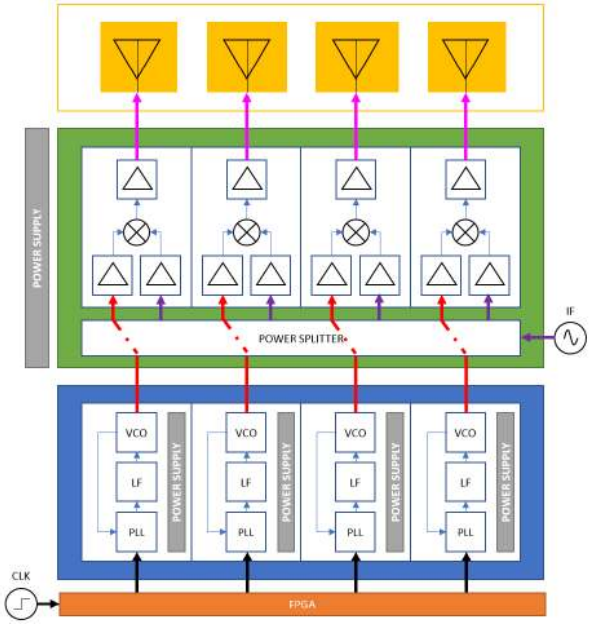

FIGURE 6. System architecture of the proposed phased array transmitter.

Moreover, it should be noted that the RSS is not per se an index of the quality of a wireless link. This is especially true for phased arrays based on the LO phase shifting approach, where a linear phase distortion across the signal bandwidth is always present, and whose magnitude increases for higher steering angles. A measurement of the error vector magnitude (EVM) of a test communication, following any of the many well-known protocol standard, must be conducted to get a clear picture of the actual capability of the apparatus to transmit intelligible information contents.

IV. BEAM STEERING TRANSMITTER PROTOTYPE

To prove the validity of the theory and techniques presented, we fabricated a beam steering transmitter prototype. The prototype uses the PCU architecture introduced in [20] (Fig. 5). In this architecture, the PCU is implemented through an accumulator register and a set of comparators and has been synthesized into an FPGA evaluation board. The comparators are implemented in such a way that, depending on their assigned PTW, the output is a square wave with a different phase.

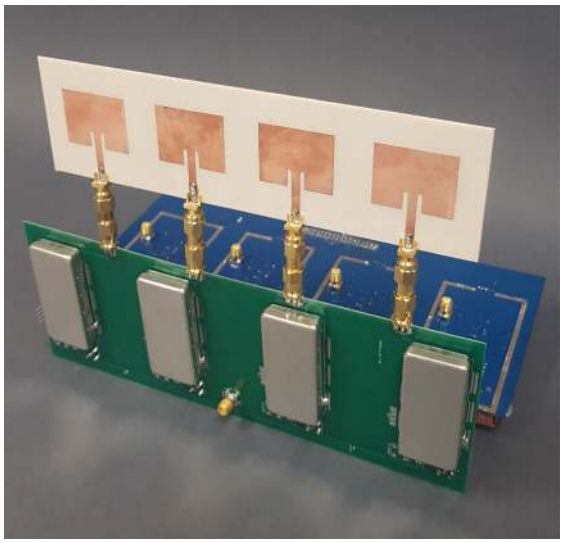

FIGURE 7. Phased array transmitter prototype.

The system architecture is depicted in Fig. 6 [21]. The transmitter is made up of four identical channels equipped with a LO synthesizer, an active up-conversion stage, and an antenna. In this implementation, the design has been partitioned into three Printed Circuit Boards (PCBs), one for each of the cited subsystems. The three PCBs have been designed in such a way that they could be assembled together as demonstrated in Fig. 7. The design of the LO synthesizers and their PCB implementation have been presented in [22]. Its size is 240x100-mm^2 and its reference inputs and RF outputs are spaced apart by 61.15-mm. The PCB is made up of four integer-N PLLs based on an Analog Devices' integrated circuit (ADF4118) and a voltage-controlled oscillator (VCO190-2453TY) from Sirenza (Fig. 8). The mutual phase shifts among the channels are implemented by the previously cited PCU. The PCU and an open-source microcontroller IP-core [23] with the function of assisting the configuration of the PCU and PLLs have been synthesized onto a single Altera's EP4CE225F29C7 FPGA. The PCU outputs four 1-MHz square waves. Their phase can be changed with an 8-bit resolution over the [0°, 360°] range. The PCU's clock signal has a frequency of 256-MHz and is conditioned through a low noise clock jitter cleaner integrated circuit from Texas Instruments (LMK04806B). The spectral purity of this clock is crucial to obtain high-quality LOs.

The up-conversion PCB is made up of four sub-circuits based on the ADE-35MH from Mini Circuits, as well as LO, IF and RF path gain blocks from Analog Devices and passive filters and attenuators from Mini Circuits (Fig. 9). The size of the board is 80x215-mm^2. LO inputs are spaced apart by 61.15-mm whereas RF outputs are spaced apart by 44.75-mm.

The antenna array's PCB is made up of four patch antennas designed with Keysight's ADS and lays on a 0.060-in thick RO4003C laminate from Rogers Corporation (Fig. 10). The antennas have been centered at 3.350-GHz and are spaced

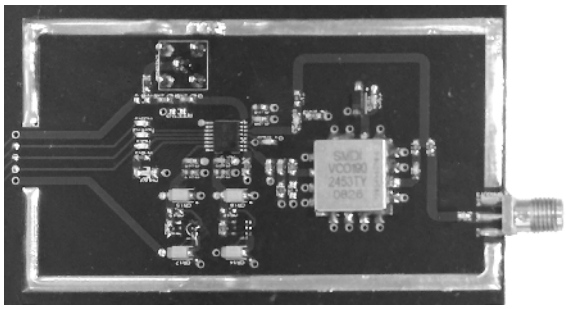

FIGURE 8. LO synthesizers PCB (one channel).

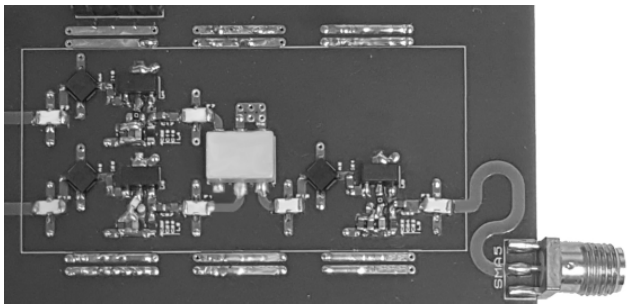

FIGURE 9. Active up-conversion PCB (one channel).

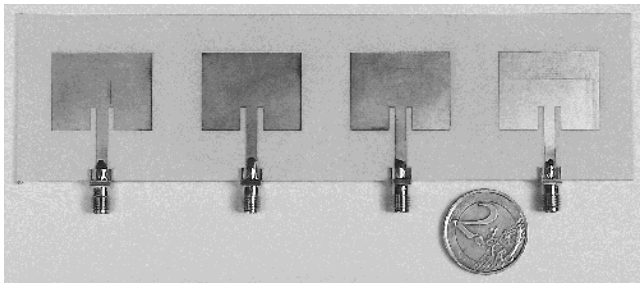

FIGURE 10. Antenna array PCB (four patch antennas).

apart by $\lambda/2$. The size of the PCB is 185x50-mm^2 and the SMA connectors on it are spaced apart by 44.75-mm. Fig. 11 shows the 3D reconstruction of the radiation patterns for 4 different mutual phase shifts configurations ($\Delta\varphi = 0°$, 30°, 60°, 90°) whereas Fig. 12 shows the 3-dB angular width, main lobe magnitude, sidelobe level (SLL) and main lobe direction for ten $\Delta\varphi$ configurations. The obtained scan angle is ±54°, however, the shape of the radiation pattern may require limiting this range. For example, if the specification of the system requires an SLL better than −10-dB, the scan angle must be restricted to ±27.4°. The above results have been simulated through CST.

V. EXPERIMENTAL RESULTS

The performance of the described prototype has been evaluated both at the block- and system-level in an RF quiet environment. Our test bench included the following instruments: i) an N9010A vector signal analyzer (VSA) from Keysight; ii) an HDO9404 oscilloscope from Teledyne LeCroy; iii)

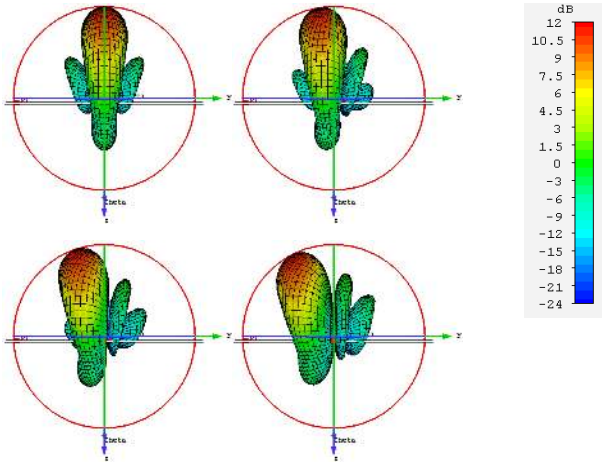

FIGURE 11. 3D reconstruction of radiation patterns for 4 different mutual phase shifts configurations ($\Delta\varphi = 0°, 30°, 60°, 90°$).

an E4433B and an N5182A vector signal generator (VSG) from Keysight; iv) an N5242A vector network analyzer (VNA) from Keysight. During the tests, the interconnections were made through semi-rigid coaxial cables secured through a torque meter wrench. This was done to ensure that the measurements were repeatable, that the losses introduced were controlled, and that undesired couplings were minimized.

The first test was to validate the LOs generation and mutual phase shifting capabilities among the channels. The validation process was conducted on the LO synthesizers PCB and was performed in the frequency domain to assess the spectrum at each output, and in the time domain, by sweeping the phase of one output and comparing it against all the others, to find the phase error of complete set of mutual phase shifts (256 steps). The PFD frequency of the PLLs was set to 1-MHz, whereas the loop bandwidth was set to 10-kHz through a second-order passive filter. The measured phase noise matches the expected RMS jitter of 0.6° simulated through ADIsimPLL. The RMS phase error is less than 1° and was measured through the cross-correlation method described in the previous section using a window of 10k periods sampled at 20-GSPS.

The second test has been conducted on the up-conversion PCB. This test was performed, channel by channel, in the frequency domain by inputting known LO and IF signals generated through the VSGs, and measuring the output power and the EVM of a QPSK transmission following the WCDMA protocol. The LO frequency was 2.453-GHz and the IF center frequency was 897-MHz. These values should produce, after mixing, an upper-sideband signal centered at 3.350-GHz. The measured RSM of the EVM was within 1% of the theoretical value.

Finally, we tested the reflection coefficient of the antenna elements used in the design (Fig. 13). For a bandwidth of 10-MHz centered around 3.350-GHz, the signal's power transferred to the antenna exceeds 99%. Fig. 14 shows the normalized radiation pattern for the single antenna.

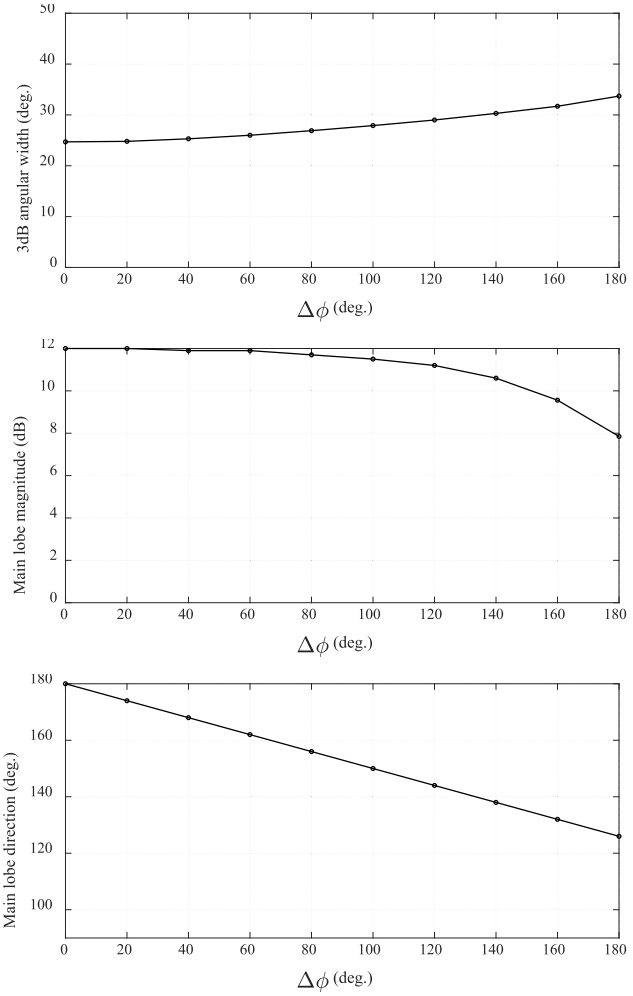

FIGURE 12. 3-dB angular width, main lobe magnitude with SLL, and main lobe direction vs. mutual phase shift assigned to adjacent antennas ($\Delta\varphi$).

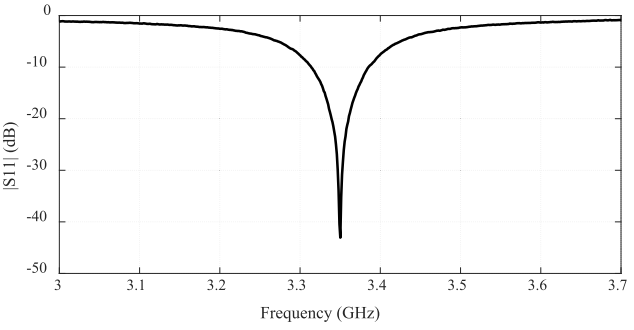

FIGURE 13. Measured reflection coefficient at input ports.

The purple lines demarcate the limits of the main lobe, whose Half Power Beam Width (HPBW) measures 85°.

At the system level, the overall architecture has been tested attaching a patch antenna to our VSA and probing the received signal strength (RSS) for different directions and for various scan angles. The signal and frequency configuration of this test was the same as the one from the up-conversion

TABLE 1. Normalized values of the radiation pattern for $\Delta\varphi$ equal to 0°, 22.5°, 45° and 90°, sampled at various angular positions $\Delta\theta$ (dB).

$\Delta\varphi$	$\Delta\theta = 0°$	$\Delta\theta = 10°$	$\Delta\theta = 20°$	$\Delta\theta = 30°$	$\Delta\theta = 40°$	$\Delta\theta = 50°$	$\Delta\theta = 60°$	$\Delta\theta = 70°$	$\Delta\theta = 80°$	$\Delta\theta = 90°$
0.0°	0.00	-1.93	-8.84	-30.91	-14.65	-15.38	-20.43	-26.31	-25.73	-24.90
22.5°	-0.88	-0.21	-3.30	-11.53	-27.35	-16.40	-17.05	-20.76	-25.72	-30.11
45.0°	-3.85	-0.31	-0.79	-4.74	-13.37	-28.07	-19.00	-18.92	-21.08	-23.68
90.0°	-28.98	-6.91	-1.32	-0.48	-2.571	-7.02	-13.56	-20.38	-21.89	-21.58

$\Delta\varphi$	$\Delta\theta = -90°$	$\Delta\theta = -80°$	$\Delta\theta = -70°$	$\Delta\theta = -60°$	$\Delta\theta = -50°$	$\Delta\theta = -40°$	$\Delta\theta = -30°$	$\Delta\theta = -20°$	$\Delta\theta = -10°$	$\Delta\theta = 0°$
0.0°	-24.93	-25.77	-26.36	-20.45	-15.38	-14.65	-30.90	-8.85	-1.93	0.00
22.5°	-21.22	-20.83	-22.15	-27.79	-20.46	-13.95	-13.99	-27.23	-6.10	-0.88
45.0°	-21.79	-20.02	-18.70	-19.43	-28.14	-19.64	-12.71	-14.76	-16.36	-3.85
90.0°	-24.96	-26.40	-27.90	-19.98	-15.18	-15.06	-27.22	-14.89	-11.41	-28.98

TABLE 2. Comparison of state of the art phase shifting architectures.

Reference	Technique	Technology	Resolution	Frequency
[2]	RF path	Discrete PIN diodes	6-bit	1.030- to 1.090-GHz
[3]	RF path	Liquid crystals	Continuous	12-GHz
[4]	RF path	Monolithic LC circuits	5-bit	6- to 18-GHz
[5]	RF path	Monolithic MEMS	4-bit	DC to 40-GHz
[6]	RF path	Fiber-based photonic circuit	Continuous	20- to 30-GHz
[7]	RF path	Integrated optics	Continuous	10.7- to 12.75-GHz
[8]	IF path	FPGA-based hybrid circuit	-	-
[9]	LO path	Monolithic 40-nm CMOS	6-bit	44- to 54-GHz
[10]	LO path	Monolithic 0.18-µm SiGe BiCMOS	4- to 5-bit	24-GHz
This work	LO path	Revised DDS-PLL architecture	8-bit	3.350-GHz

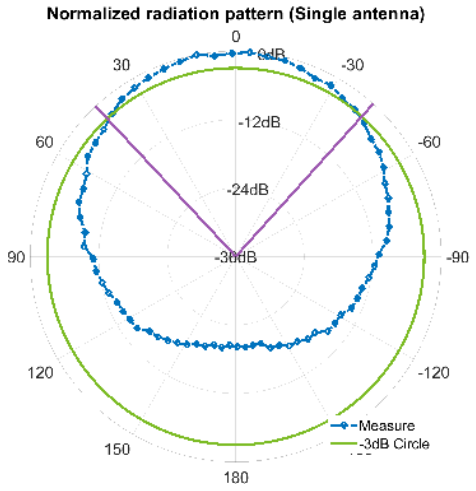

FIGURE 14. Normalized radiation pattern for the single element antenna.

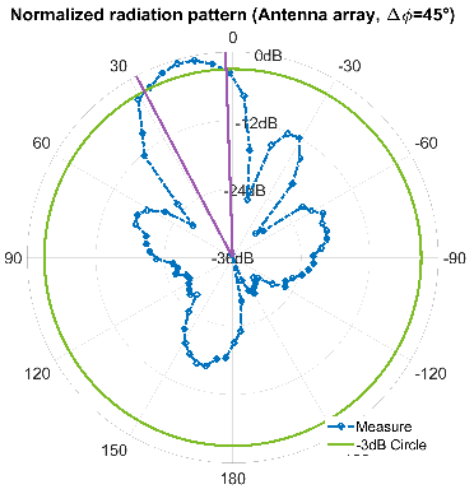

FIGURE 15. Normalized radiation pattern for the antenna array ($\Delta\varphi = 45°$).

PCB. However, our proposed transmitter architecture is not bound to this particular configuration. In fact, it can be employed to transmit any modulation scheme with any LO and IF frequency configuration. This is because all DDS-PLL architectures and their revised variants are frequency independent. Frequency independence is achieved thanks to the fact that the aforementioned architectures implement the same quantized phase shifts across the whole synthesis bandwidth of the PLLs.

Fig. 15 shows the normalized radiation pattern for the antenna array when the mutual phase shift assigned to adjacent antennas ($\Delta\varphi$) is equal to 45°. The purple lines demarcate the limits of the main lobe, whose HPBW measures 26°. The beam steering is clearly recognized. In this case, the main lobe direction points away from the broadside of 14°. TABLE 1 provides normalized values of the radiation pattern for $\Delta\varphi$ equal to 0°, 22.5° , 45°, and 90°, sampled

at various angular positions $\Delta\theta$. The experimental results illustrate how our revised DDS-PLL architecture can be successfully employed to implement a beam steering transmitter for phased arrays. TABLE 2 [22] compares our solution with other state-of-the-art phase shifting architectures. It is important to note that improving the resolution of the phase shifts is more beneficial when the 3-dB angular width of the main lobe is small, that is when the number of elements in the phased array is large. In this case, the angular resolution of the array becomes comparable to the beam width, and thus an exceptionally fine-grained spatial selectivity can be achieved.

VI. CONCLUSIONS AND FUTURE WORKS

This work presented a review of the framework behind DDS-PLLs, as well as a set of techniques that can be used during the development and the deployment of phased arrays based on LO phase shifting approaches. A beam steering transmitter prototype employing a revised DDS-PLL architecture has been presented, together with the experimental results obtained during its characterization. The proposed prototype, centered at 3.350-GHz, allows to independently set the phase of its four LOs at 2.453-GHz with an 8-bit resolution and has been used to implement a successful WCDMA wireless link. The DDS-PLL architecture is frequency independent, and the modular structure of the presented PCU can be exploited to achieve different phase resolutions with very small redesign effort. The achieved phase shift resolution is especially useful in large phased arrays, where the 3-dB angular width of the main lobe is small, and thus exceptionally fine-grained spatial selectivity can be achieved.

Future works will focus on: i) the implementation of a larger phased array, to take full advantage of the achieved phase resolution; ii) the implementation of a beam steering receiver prototype and its integration towards a full-featured transceiver.

REFERENCES

[1] R. J. Mailloux, "Phased array theory and technology," *Proc. IEEE*, vol. 70, no. 3, pp. 246–291, Mar. 1982.

[2] K. Sharma, A. Basu, and S. Koul, "High power 6-bit digital phase shifter for airborne IFF application," in *Proc. Asia-Pacific Microw. Conf. (APMC)*, Dec. 2016, pp. 1–4.

[3] O. H. Karabey, F. Goelden, A. Gaebler, S. Strunck, and R. Jakoby, "Tunable loaded line phase shifters for microwave applications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Baltimore, MD, USA, Jun. 2011, pp. 1–4.

[4] K. Miyaguchi *et al.*, "A 6-18 GHz 5-bit phase shifter MMIC using series/parallel LC circuit," in *Proc. 32nd Eur. Microw. Conf.*, Milan, Italy, Sep. 2002, pp. 1–4.

[5] M. Kim, J. B. Hacker, R. E. Mihailovich, and J. F. DeNatale, "A DC-to-40 GHz four-bit RF MEMS true-time delay network," *IEEE Microw. Wireless Compon. Lett.*, vol. 11, no. 2, pp. 56–58, Feb. 2001.

[6] H. Y. Jiang *et al.*, "Microwave photonic phase shifter using a phase modulator and a fiber Bragg grating in a round-trip," in *Proc. CLEO*, San Jose, CA, USA, Jun. 2013, pp. 1–2.

[7] M. Burla *et al.*, "CMOS-compatible integrated optical delay line for broadband Ku-band satellite communications," in *Proc. IEEE Int. Top. Meeting Microw. Photon.*, Noordwijk, The Netherlands, Sep. 2012, pp. 120–123.

[8] D. Digdarsini, M. Kumar, and T. V. S. Ram, "Design & hardware realization of FPGA based digital beam forming system," in *Proc. 3rd Int. Conf. Signal Process. Integr. Netw. (SPIN)*, Feb. 2016, pp. 275–278.

[9] C. Lu *et al.*, "A 48 GHz 6-bit LO-path phase shifter in 40-nm CMOS for 60 GHz applications," in *Proc. ESSCIRC*, Bucharest, Romania, Sep. 2013, pp. 73–76.

[10] H. Hashemi, X. Guan, A. Komijani, and A. Hajimiri, "A 24-GHz SiGe phased-array receiver-LO phase-shifting approach," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 2, pp. 614–626, Feb. 2005.

[11] L. Li, W. Hong, Y. Zhang, Z. Chen, and P. Chen, "Design and implementation of an active array antenna with remote controllable radiation patterns for mobile communications," *IEEE Trans. Antennas Propag.*, vol. 62, no. 2, pp. 913–921, Feb. 2014.

[12] F. M. Gardner, *Phaselock Techniques*. Hoboken, NJ, USA: Wiley, 2005.

[13] J. Juyon, I. Burciu, T. Borr, S. Thuries, and E. Tournier, "A low spurious level fractional-N frequency divider based on a DDS-like phase accumulation operation," in *Proc. 18th Int. Conf. Mixed Design Integr. Circuits Syst.*, Gliwice, Poland, Jun. 2011, pp. 417–421.

[14] A. Bonfanti, F. Amorosa, C. Samori, and A. L. Lacaita, "A DDS-based PLL for 2.4-GHz frequency synthesis," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 50, no. 12, pp. 1007–1010, Dec. 2003.

[15] G. Avitabile, F. Cannone, and G. Coviello, "Low-power Tx module for high-resolution continuous programmable phase shift," *Electron. Lett.*, vol. 44, no. 18, pp. 1052–1053, Aug. 2008.

[16] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge, U.K.: Cambridge Univ. Press, 2003.

[17] "A technical tutorial on digital signal synthesis," Analog Devices, Norwood, MA, USA, Appl. Note, 1999.

[18] J. A. Crawford, *Advanced Phase-lock Techniques*. Norwood, MA, USA: Artech House, 2008.

[19] G. D'Amato, G. Avitabile, G. Coviello, and C. Talarico, "A beam steering unit for active phased-array antennas based on FPGA synthesized delay-lines and PLLs," in *Proc. Int. Conf. Synth., Modeling, Anal. Simulation Methods Appl. Circuit Design*, Istanbul, Turkey, Sep. 2015, pp. 1–4.

[20] G. D'Amato, G. Piccinni, G. Avitabile, G. Coviello, and C. Talarico, "An integrated phase shifting frequency synthesizer for active electronically scanned arrays," in *Proc. 21st Int. Symp. Design Diagnostics Electron. Circuits Syst. (DDECS)*, Budapest, Hungary, Apr. 2018, pp. 91–94.

[21] G. D'Amato, G. Avitabile, G. Coviello, and C. Talarico, "A beam steering transmitter prototype for IOT communications," in *Proc. 3rd Int. Conf. Smart Sustain. Technol.*, Split, Croatia, Jun. 2018, pp. 1–5.

[22] G. D'Amato, G. Avitabile, G. Coviello, and C. Talarico, "A modulator-less Beam Steering Transmitter based a revised DDS-PLL Phase Shifter Architecture," *J. Commun. Softw. Syst.*, vol. 14, no. 1, pp. 1–9, Mar. 2018.

[23] G. D'Amato, G. Avitabile, G. Coviello, and C. Talarico, "Toward a novel architecture for beam steering of active phased-array antennas," in *Proc. 59th Int. Midwest Symp. Circuits Syst. (MWSCAS)*, Abu Dhabi, UAE, Oct. 2016, pp. 1–4.

GIULIO D'AMATO was born in Bari, Italy, in 1989. He received the Laurea degree in electronics engineering from the Politecnico di Bari, Italy, in 2014, where he is currently pursuing the Ph.D. degree in electric and information engineering. His research interests include circuits and systems for phased arrays.

GIANFRANCO AVITABILE received the Laurea degree in electronics from Florence University, Italy, in 1992. He was with the Department of Electronics, University of Florence, as an Assistant Professor. Since 1998, he has been with the Department of Electronics, Politecnico di Bari, as an Associate Professor. His current research interests include high-frequency circuits for both civil and military applications.

GIUSEPPE COVIELLO was born in Bari, Italy, in 1981. He received the Laurea degree in electronics engineering and the Ph.D. degree in electric and information engineering from the Politecnico di Bari, Italy, in 2006 and 2015, respectively. Since 2006, he has been a Researcher with the Dipartimento di Ingegneria Elettrica e dell'Informazione. His current research interests include digital phase shifter systems and power amplifier pre-distortion techniques.

CLAUDIO TALARICO received the B.S. and M.S. degrees in electrical engineering from the University of Genoa, Italy, and the Ph.D. degree in electrical engineering from the University of Hawaii. He is currently a Professor of electrical and computer engineering with Gonzaga University. Before joining Gonzaga University, he was with Eastern Washington University, the University of Arizona, and with industry, where he held both engineering and management positions at Siemens Semiconductors, IKOS Systems, and Marconi Communications. His research interests include digital and mixed analog/digital integrated circuits and systems, computer-aided design methodologies, and design and analysis of systems-on-chip.