Dead-Time Issues in Predictive Current Control

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***Abstract*—Current control in inverter-driven machine systems is the inner most component of the hierarchy of control loops. If the control of current in the machine is not fast and accurate then it is difficult, if not impossible, to build a high-performance drive system.**

Unfortunately, the implementation of current control in power electronic systems is not ideal. Practical effects can have a significant influence on its performance. This paper examines one of these effects, dead time, and considers the influence it has on the performance of predictive current controllers (PCCs).

The paper presents analysis that shows that a PCC implicitly compensates for voltage loss due to dead time. Also, a modified PCC is introduced that reduces the zero-current-clamp problem caused by dead time. Simulation and experimental results are presented to verify the analysis and confirm the performance of the new algorithm.

***Index Terms*—Current clamp, inverter dead time, predictive current controller (PCC), pulsewidth modulation (PWM).**

I. Introduction

CURRENT control in inverter-driven machine systems is arguably the most important part of the system. If accurate and rapid current control is achieved, then, given the correct reference currents, fast and accurate torque control can be achieved.

Real implementations of current control are far from ideal, with practical effects introduced by the inverter power electronics and the digital control systems producing, in some circumstances, significant departures from ideal behavior. This paper considers one of these effects—dead time—and especially its influence on the performance of predictive current controllers (PCCs).

Dead time is the term used to refer to the fact that, in an inverter, there must be a time delay between turning off one of the transistors in an inverter leg and turning on the other transistor in the same leg. This time is required so that the stored charge that is present in minority-carrier-based semiconductor switches [such as the popular insulated gate bipolar transistor (IGBT)] has time to disappear before turning on the other device. If this gap is not present, then the device being turned off is still able to conduct current when the other device is turned on. The result is that there is a short circuit across the dc link, and catastrophic failure of the inverter leg can occur.

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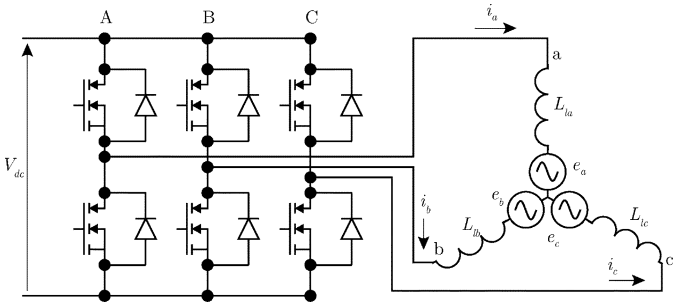

Fig. 1. Schematic of a conventional six-switch inverter.

It is well known that the insertion of dead time into the switching regime causes a number of undesirable effects on the output voltage of an inverter. A large number of papers have appeared in the literature that analyze this problem and propose various minimization techniques [1]–[9]. These papers have mostly concentrated on minimizing the voltage distortion (and by implication the current distortion) for inverters being controlled using triangular-wave pulsewidth-modulation (PWM) generation techniques. However, there are no papers (known by the authors) that consider the effects of dead time on the performance of inverters under the control of a PCC.

II. Dead-Time Effects on Space-Vector PWM

It may be beneficial at this stage to briefly review the effects that dead time has on the performance of inverters. These effects can be grouped into two categories—voltage error effects and zero-current-clamping effects.[1]

Let us firstly consider voltage error effects for a conventional PWM inverter connected to the simplified model of an induction machine. Fig. 1 is a schematic of a conventional three-phase inverter feeding the simplified model of an induction machine. Fig. 2 shows the well-known PWM space-vector diagram for the same inverter, where a "1" denotes that the top transistor of a leg is turned on, and by implication that the bottom transistor is turned off. If one is trying to produce a voltage vector in Sector 0 of Fig. 2, then the switching pattern shown in Fig. 3 is developed (assuming that symmetric PWM is being employed). This switching pattern assumes that current is flowing out of Leg *A* and into Legs *B* and *C*. A leg will experience a dead-time lag effect if the transistor in the leg is not conducting at the time of the switching (i.e., the parallel diode is conducting). The dark grey section in this diagram indicates loss of volt-second area due to dead time, and the light grey area indicates an increase in volt-second area. The dashed lines indicate the desired switching point, and the solid line the actual switching point.

[1]We are *not* considering the interactions that dead time may have on the dynamic performance of a machine.

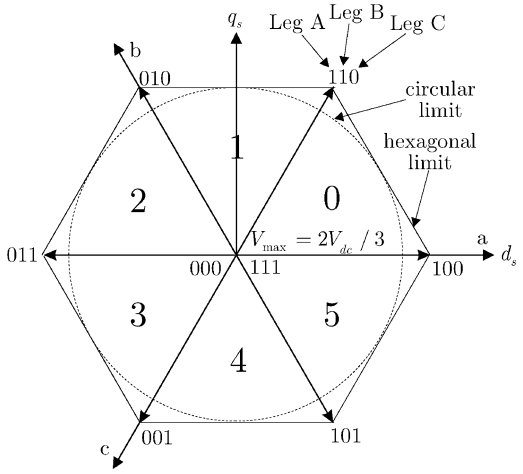

Fig. 2. Switching vectors for a six-switch PWM inverter.

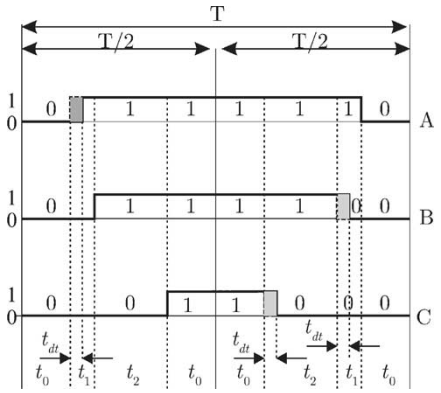

Fig. 3. Switch patterns for symmetric PWM with and without dead time.

One can see that for Leg *A* this results in a loss of area, and for Legs *B* and *C* a gain in area.

Remark 1: One will note from Fig. 3 that if t_1 and t_2 are very small (i.e., a small length space vector) then the effect of the dead time becomes relatively larger. Therefore, dead time becomes a more significant problem at low output voltages.

Remark 2: One can also see that another effect of dead time is that the PWM is no longer symmetric about the center of the control period.

Remark 3: The net result of the effect of dead-time on the voltage is the following.

1) The magnitude of the voltage space vector is in error.
2) The voltage space vector angle is different due to dead time.

Remark 4: The magnitude of the previous two effects is very dependent on the desired voltage magnitude, with the dead time having a relatively larger effect for low voltage magnitudes.

The other major effect produced by dead time is the so-called zero-current-clamp effect [5]. When the current in a phase attempts to go through zero (i.e., change of current direction), there can be long periods (sometimes tens of control cycles) when the current stays at or near zero. Distortion from the phase whose current is attempting to reverse is reflected in the other phases.

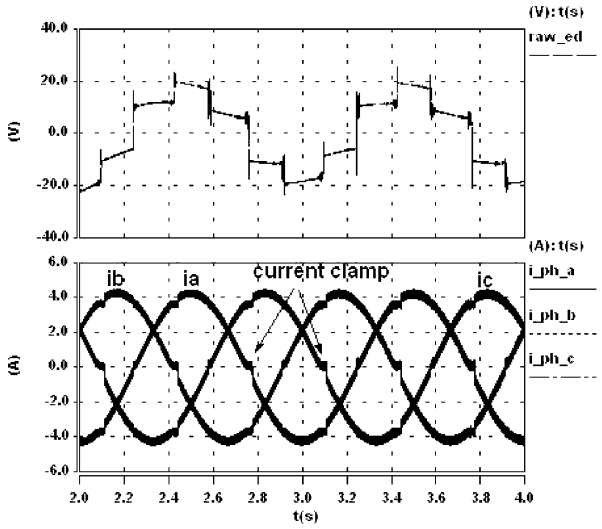

Fig. 4. Dead-time effects with a predictive current controller—simulation results. Switching frequency 5 kHz.

Remark 5: The zero current clamp is again particularly bad at very low voltages, which corresponds to low frequencies when the inverter is feeding a machine.

The current-clamp phenomena occurs when the initial condition for a phase current is near zero. When current clamp occurs, all these near-zero initial conditions go to zero current during the dead-time period of the particular phase leg. At the end of the dead-time period, when the complementary switch in the leg is switched, the phase current will follow the same trajectory, regardless of the initial condition, since all the initial conditions map to a zero current during the dead time. This event, in itself, is only a necessary condition for clamping, but it is not sufficient. The clamp will occur, if at the end of the control interval the current ends up in the band of initial conditions that again lead to zero current during the phase leg dead time [5]. Obviously, this will mean that the process will again repeat. Implicit in this explanation is that the switching sequence from one control cycle to another does not vary much, which in turn implies that one must be operating at a very low output frequency and with low reference currents. Current clamping results in undesirable distortion in the output currents from the inverter. This can be particularly bad for low-speed and position-control applications.

This paper is primarily concerned with the operation of PCCs with dead time. If we run a simple PCC simulation with an induction machine load and a reference current of $i^* = 4.2\sin(2\pi t)$ with 4-μs dead time, then the plot shown in Fig. 4 results. This diagram shows the estimated back electromotive force (EMF) and the phase currents. The estimated back EMF is highly distorted by the presence of the current clamp in the phases, and each phase has disturbances in it from the zero crossing of the currents in the other phases.

Remark 6: It should be noted that there is feedback in the PCC via the estimated back EMF. This effect will be one of the subjects studied in this paper.

The remainder of this paper will discuss predictive current control and the influence of dead time on its performance.

III. Predictive Current Control and Dead Time

Predictive current control can be implemented on each phase of a three-phase system (taking appropriate account of the influence of the star point) [10], or alternatively on a two-phase system (after a three-phase-to-two-phase transformation). It is the later approach that will be considered here. It is beyond the scope of this paper to present the predictive current control algorithm—details can be found in [11]–[13].

The predictive current control end-point-control equations for each of the two phases, in discrete form, can be shown to be [11], [13], [14]

$$v^*_{k+1} = \frac{L_l}{T}(i^*_{k+1} - i_k) + \hat{e}_k \tag{1}$$

$$\hat{e}_k = v^*_k - \frac{L_l}{T}(i_k - i_{k-1}) \tag{2}$$

where L_l is the total machine leakage inductance, v^*_{k+1} is the desired next applied voltage, v^*_k is the current desired applied voltage, $\hat{e}_k$ is the current estimated back-EMF voltage, and i^*_{k+1} is the desired current at the end of the control interval. This algorithm is essentially a dead-beat or one-step-ahead algorithm. It is also called predictive because it uses the machine model to predict the control voltage required to take the current from its present value to the desired value in one control interval (if possible subject to voltage limitations). The predictive current control has received attention recently by the drives community because it is particularly amenable to digital implementation, it is computationally simple, allows control of the switching frequency, has a very fast transient response, requires minimal machine parameter knowledge and has parameter error robustness.

If the total leakage inductance of the machine is known, and if the desired output voltage is accurately produced then predictive current control works very well [11]–[13]. However, the presence of dead time results in voltages being applied that are different from the desired voltage. It should be noted that this occurs even if one has perfect knowledge of all the parameters in the system. This voltage error is then propagated into the estimated back EMF via the v^*_k value in (2). The resultant error in $\hat{e_k}$ then affects the desired voltage for the next control interval via (1). Counter intuitively, we shall see that the errors in the back-EMF estimate have very positive effects on the performance of the algorithm. Zero current clamping also occurs when predictive current control is used. The back-EMF errors also help reduce (but do not eliminate) this effect.

A. Dead-Time Voltage Compensation

In conventional PWM strategies the applied voltage error created by dead time can be compensated for by a number of techniques. For example, one can sample the inverter leg output current, and this together with knowledge of the active switch in the leg determines whether the switching time needs to be compensated. Another technique is to augment the reference waveform to overcome the applied voltage error [1].

Let us consider the situation with predictive current control. Before doing this, we shall introduce the following definitions:

$$v^*_k \triangleq \text{command voltage from the control algorithm at } k \tag{3}$$

$$v^a_k \triangleq \text{actual voltage applied to the machine at } k \tag{4}$$

$$v^{a*}_k \triangleq \text{desired machine voltage at } k \tag{5}$$

$$e_k \triangleq \text{back EMF calculated using } v^a_k \tag{6}$$

$$\hat{e}_k \triangleq \text{calculated back EMF using } v^*_k \tag{7}$$

$$\Delta v_k \triangleq \text{voltage error } = v^a_k - v^*_k. \tag{8}$$

It should be emphasised that, if there is no dead time, then $v^*_k = v^{a*}_k = v^a_k$—that is, the control algorithm commanded voltage will be equal to the voltage that one desires on the terminals of the machine, and this voltage will actually be impressed on the machine. If dead time is present, then the commanded voltage from the control algorithm is not the voltage that actually appears on the machine terminals.

Using this new notation, let us rewrite (2) as follows:

$$e_k = v^a_k - \frac{L_l}{T}(i_k - i_{k-1}). \tag{9}$$

The term e_k can be considered to be an "accurate" back EMF.[2] We shall assume up to interval k that there has been no dead time in the inverter, hence, the $v^*_k = v^a_k$. In interval $k+1$ dead time is introduced. Rewrite (1) to give the commanded voltage as follows:

$$v^*_{k+1} = \frac{L_l}{T}(i^*_{k+1} - i_k) + e_k. \tag{10}$$

Equation (10) gives the voltage that we wish to apply in interval $k+1$. Under the condition of no dead time the commanded voltage is equal to the desired machine terminal voltage, i.e., $v^*_{k+1} = v^{a*}_{k+1}$. However due to dead time we will have an error and v^a_{k+1} is the voltage that will actually be applied, which will in general be different from v^*_{k+1}.

During interval $k+1$ we calculate the control for interval $k+2$. However, because of the dead-time error in the applied voltage the calculation of the back EMF will be at variance with the "accurate" back EMF during this interval. The relevant back-EMF equation is

$$\hat{e}_{k+1} = v^*_{k+1} - \frac{L_l}{T}(i_{k+1} - i_k) \tag{11}$$

where $v^*_{k+1} \neq v^a_{k+1}$ due to dead time.

The commanded voltage for the next control interval $k+2$ is given by

$$v^*_{k+2} = \frac{L_l}{T}(i^*_{k+2} - i_{k+1}) + \hat{e}_{k+1}. \tag{12}$$

Remark 7: It should be noted that v^*_{k+2} has a different value because $\hat{e}_{k+1}$ is not correct due to $v^*_{k+1} \neq v^a_{k+1}$.

Using definition (8) we can write the voltage error due to dead time as

$$\Delta v_{k+1} = v^a_{k+1} - v^*_{k+1}. \tag{13}$$

[2]It should be noted that even this expression for the back EMF is, in fact, an estimate made from current measurements and an approximate machine model.

From the definition of e_k in (6) we can write the following expression for the "accurate" back EMF:

$$e_{k+1} = v^a_{k+1} - \frac{L_l}{T}(i_{k+1} - i_k). \tag{14}$$

Using (14) and (11) we can write

$$\begin{aligned} e_{k+1} - \hat{e}_{k+1} &= v^a_{k+1} - \frac{L_l}{T}(i_{k+1} - i_k) \\ &\quad - v^*_{k+1} + \frac{L_l}{T}(i_{k+1} - i_k) \\ &= v^a_{k+1} - v^*_{k+1} \qquad (15) \\ \therefore \Delta v_{k+1} &= e_{k+1} - \hat{e}_{k+1} \qquad (16) \\ \Rightarrow \hat{e}_{k+1} &= e_{k+1} - \Delta v_{k+1}. \qquad (17) \end{aligned}$$

Using (12) and substituting (17) we can write

$$v^*_{k+2} = \underbrace{\frac{L_l}{T}(i^*_{k+2} - i_{k+1}) + e_{k+1}}_{v^{a*}_{k+2}} - \Delta v_{k+1} \tag{18}$$

where v^{a*}_{k+2} is the desired machine terminal voltage that would be calculated if we have e_{k+1}.

It is easily seen from (18) that

$$v^*_{k+2} = v^{a*}_{k+2} - \Delta v_{k+1}. \tag{19}$$

In other words, the commanded voltage for the next control interval is augmented by the dead-time error voltage from the previous interval.

If the current directions in the phases remain the same from one control interval to another then the dead-time voltage error will be the same in succeeding intervals. Therefore,

$$\Delta v_{k+2} = v^a_{k+2} - v^*_{k+2} = \Delta v_{k+1}. \tag{20}$$

Substituting (19) into (20) we can write

$$\begin{aligned} v^*_{k+2} - v^{a*}_{k+2} + \Delta v_{k+1} &= \Delta v_{k+1} \qquad (21) \\ \therefore v^a_{k+2} &= v^{a*}_{k+2}. \qquad (22) \end{aligned}$$

Remark 8: Equation (22) indicates that the actual applied machine voltage is equal to the desired machine terminal voltage one would apply if the accurate back EMF were calculated. This actual desired machine voltage must be applied in order for the current to go the the desired current. This has been achieved because the algorithm has generated an augmented commanded voltage that automatically compensates for the fact that the commanded voltage is not the applied voltage due to the dead time.

Remark 9: The autocorrection phenomena shown in (22) carries on for subsequent control intervals while the phase currents remain in the same direction. When the currents change direction, there will be one control interval where an applied voltage error may be made, and then the autocorrection will be reset and continue.

In order to quantify the voltage error due to dead time consider the case of a purely inductive load, with ideal switches and diodes, and phase currents which obey the conditions $\mathrm{sgn}(i_a) > 0$, $|i_a| \approx 0$, $\mathrm{sgn}(i_c) > 0$, $\mathrm{sgn}(i_b) < 0$, and a switching pattern which is selected to move the current more negative.

This situation is illustrated in Fig. 5 where PWMA, PWMB, and PWMC are the firing patterns for the top switches in legs A, B, and C, respectively, of the inverter. That is, the desired switching sequence is – 000 → 001 → 101 → 111. The ia1 plot is the *a*-phase current waveform that would be obtained if it were possible to have perfect switches and no dead time. The ia2 trace is the current waveform obtained when the *a*-phase current does not change sign during the switching interval but the effects of dead time are included. On the other hand, ia3 is the waveform obtained when the current does change sign during the control interval. The v1, v2, and v3 traces are the *a*-phase voltage waveforms corresponding to ia1, ia2, and ia3, respectively, and dv1 and dv2 are the error voltages obtained by the difference between the ideal voltage v1 and v2, and v1 and v3, respectively. The voltage V is defined as $(1/3)V_{\mathrm{dc}}$, where V_{dc} is the dc-link voltage. In all cases, the current-clamp effect has been ignored.

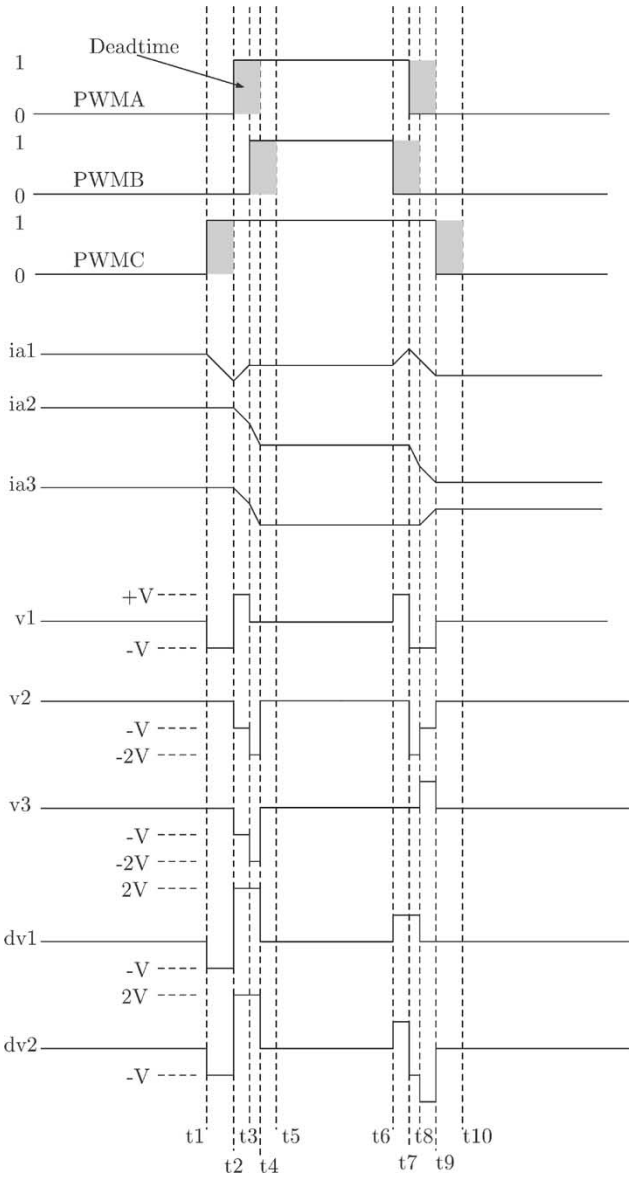

Fig. 5. Ideal waveforms for a purely inductive load.

If we consider trace ia1 then at time $t1$ the top switching device in the *c*-phase leg of the inverter bridge is switched on and the bottom switching device of the same leg is switched off. A circuit configuration as shown in Fig. 6(a) is obtained where

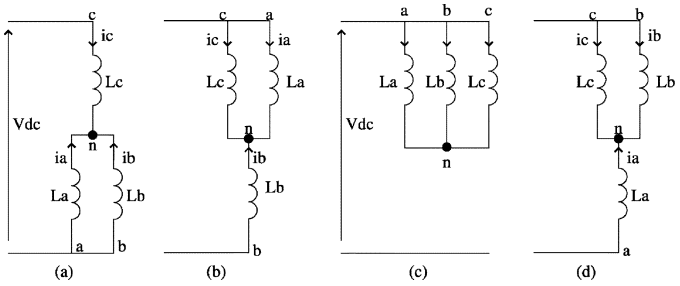

Fig. 6. Effective circuit configuration for different switch patterns.

point "c" has a potential of $V_{\rm dc}$ with respect to points "a" and "b." If $L_a = L_b = L_c = L$ then,

$$i_c(t)|_{t1\le t<t2} = \frac{V_{\rm dc}}{\frac{3}{2}L}t + i_c(t1). \tag{23}$$

Consequently,

$$i_a(t)|_{t1\le t<t2} = -\frac{\frac{1}{3}V_{\rm dc}}{L} + i_a(t1) \tag{24}$$

and

$$v_{an}|_{t1\le t<t2} = -\frac{1}{3}V_{\rm dc} = -V. \tag{25}$$

At time $t2$ the top switching device in the a-phase leg is switched on. The circuit configuration for this case is shown in Fig. 6(b). Thus,

$$i_a(t)|_{t2\le t<t3} = \frac{V}{L}t + i(t2) \tag{26}$$

$$\Rightarrow v_{an}|_{t2\le t<t3} = V. \tag{27}$$

At $t = t3$, when all of the top switching devices are turned on, which corresponds to Fig. 6(c), the voltage across the inductors is zero. This means that the rate of change of current is zero and

$$i_a(t)|_{t3\le t<t6} = i_a(t3) \tag{28}$$

$$\Rightarrow v_{an}|_{t3\le t<t6} = 0. \tag{29}$$

Similar analysis can be applied to the second half of the control interval.

For trace ia2, dead -time is considered but the current in the a phase does not change sign. As the c-phase current is defined to be positive, there is a time delay between the bottom switching device of the c-phase leg switching off and the phase being connected to $V_{\rm dc}$(i.e., a volt-second loss). Consequently, the c-phase leg of the load does not become connected to $V_{\rm dc}$ until time $t2$ instead of time $t1$ as was the case previously. Also, there is a volt-second loss in the a phase at time $t2$ as the a-phase current is also positive. At time $t2$ then, the circuit configuration becomes as per Fig. 6(a) and equations for current and voltage for the a phase are

$$i_a(t)|_{t2\le t<t3} = -\frac{V}{L} + i_a(t2) \tag{30}$$

$$v_{an}|_{t2\le t<t3} = -V. \tag{31}$$

At time $t3$ there is no volt-second loss as the b-phase current is defined to be negative. The circuit configuration becomes as per Fig. 6(d), giving

$$i_a(t)|_{t3\le t<t4} = -\frac{2V}{L} + i_a(t3) \tag{32}$$

$$v_{an}|_{t3\le t<t4} = -2V. \tag{33}$$

The a-phase leg is connected to $V_{\rm dc}$ at time $t4$ corresponding to Fig. 6(c). This situation will remain until the top a-phase switching device turns off (there is a volt-second gain for the b phase as the b-phase current is negative) giving

$$i_a(t)|_{t4\le t<t7} = i_a(t4) \tag{34}$$

$$v_{an}|_{t4\le t<t7} = 0. \tag{35}$$

Similar analysis, accounting for volt-second gain or loss in individual phases, leads to the remaining waveforms in Fig. 5.

With Δv_k defined as per (8), then it is easily shown for the a phase (which is the same as the d phase by the alignment chosen) that $\Delta v_k = 2Vt_d/T$ for no change from positive current, 0 if the current changes half way during the interval, and $-2Vt_d/T$ for no change from negative current. The variable t_d is the dead time.

In terms of algorithm performance, if the current does change sign, from positive to negative, during interval k for example, then from (13),

$$v_k^a = v_k^* - 2V\frac{t_d}{T} + 0 \tag{36}$$

$$v_{k+1}^a = v_{k+1}^* - 0 - 2V\frac{t_d}{T} \tag{37}$$

$$v_{k+2}^a = v_{k+2}^* + 2V\frac{t_d}{T} - 2V\frac{t_d}{T} = v_{k+2}^*. \tag{38}$$

That is, the compensation applied in interval k will be in error by $-2(V)t_d/T$ and in interval $k+1$ by the same amount. The implicit compensation applied during interval $k+2$ and following intervals, however, will be correct. A similar argument applies when the current direction goes from negative polarity to positive polarity. This error over two control intervals, which effectively creates a "dingle" in the applied voltage from the desired, does not have a significant effect on the algorithm performance. In fact, the error in voltage tends to push the current waveform away from zero, decreasing the chances of the current-clamp effect which is discussed in the next section. Similar results can be obtained via the same method for the q-phase currents.

Simulation results, for a purely inductive load, obtained using the SABER simulation package, are shown in Fig. 7. The inverter is assumed to have a dead time of 4 μs, and has a switching frequency of 4 kHz. The two plots in the figure are for the cases where we use the known zero back-EMF value in the algorithm, and when we use the back-EMF estimation as in (2). The reference current for the controller is a 4.2-A amplitude sine wave. The results show that the voltage error has been compensated for when the back-EMF estimate is used, and the current reaches its desired peak-to-peak value. Note the distortion in the current if the known back EMF is used.

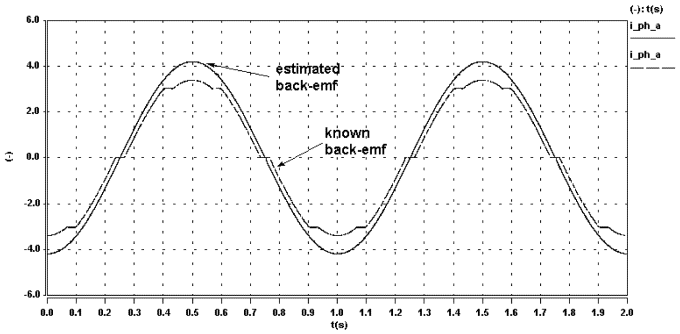

Fig. 7. Simulation results—algorithm performance with purely inductive load and $i^* = 4.2\sin(2\pi t)$.

B. PCC and Zero-Current Clamping

The PCC suffers from the zero-current-clamp problem discussed in Section I. One can view a one-step-ahead controller, as defined by (1) and (2), to be an algorithm that generates a sequence of i_k's that move toward some desired value of current (the sequence is only one value in length under the condition that the current can be achieved with the available voltage, and the parameters in the controller are exact). There is no explicit feedback that takes into account the error between the obtained current and the desired current in the previous control interval. Therefore, if the current at the end of a control interval lies in the band of currents that will map to zero during the dead time of a leg then the sequence of inverter firings will repeat until the $i^*_{k+1} - i_k$ error becomes large enough to force a significantly different switching pattern.[3] A technique to minimize the current clamp phenomena is to provide some auxiliary feedback in the PCC that will cause an augmented voltage to be applied that will move the current toward the desired current.

Heuristically, one can think of this as applying an additional voltage boost, above that required to overcome dead-time voltage loss, in order that the regular pattern of applied voltages is broken and thus the current may be forced through zero earlier than it normally would.

There is a choice as to whether this auxiliary feedback is proportional or also involves integration.

One can augment (1) to form an expression of the form

$$v^*_{k+1} = \frac{L_l}{T}(i^*_{k+1} - i_k) + \hat{e}_k + K_p(i^*_k - i_k) + K_i\Sigma\Delta i_k \quad (39)$$

where $\Sigma\Delta i_k = \Sigma\Delta i_{k-1} + (i^*_k - i_k)$ and $\Delta i_k = (i^*_k - i_k)$.

Remark 10: The integral sections of (39) would only be active if the desired voltage vector magnitude is less than the maximum voltage that can be produced by the inverter.

Clearly, the additional terms in the algorithm will substantially modify the dynamics of the algorithm. To determine the stability of the algorithm with auxiliary feedback terms a similar approach to that taken in [14] is applied to (39).

If we assume that the voltage error due to deadtime effects is zero (i.e., $\Delta v_{k+n} = 0, n \in \mathbb{I}$) then from (13), and the realization that under zero dead time that $v^a_{k+1} = v^{a*}_{k+1} = v^*_{k+1}$, (39), can be written as

$$v^a_{k+1} = \frac{L_l\Delta L}{T}(i^*_{k+1} - i_k) + \hat{e}_k + K_p(i^*_k - i_k) + K_i\Sigma\Delta i_k \quad (40)$$

[3]This increase in $i^*_{k+1} - i_k$ would result if the reference is changing. If the reference remained constant then the current clamp could occur indefinitely.

where ΔL is the multiplicative error in L_l. v^a_k can be written as

$$v^a_k = \frac{L_l}{T}(i_k - i_{k-1}) + e_k \quad (41)$$

from the simplified model of the induction machine shown in Fig. 1. Thus,

$$\frac{L_l}{T}(i_{k+1} - i_k) + e_{k+1} = \frac{L_l\Delta L}{T}(i^*_{k+1} - i_k) + \frac{L_l}{T}(i_k - i_{k-1}) + e_k - \frac{L_l\Delta L}{T}(i_k - i_{k-1}) + k_p\Delta i_k + k_i\sum\Delta i_k. \quad (42)$$

Collecting terms gives

$$\frac{L_l}{T}(i_{k+1} - i_k) + \frac{L_l\Delta L}{T}i_k - \frac{L_l}{T}(i_k - i_{k-1}) + \frac{L_l\Delta L}{T}(i_k - i_{k-1}) + k_p i_k + k_i\sum i_k = \frac{L_l\Delta L}{T}i^*_{k+1} + k_p i^*_k + k_i\sum i^*_k + (e_k - e_{k+1}). \quad (43)$$

Dividing both sides of (43) by L_l/T we get

$$\begin{aligned}&(i_{k+1} - i_k) + \Delta L i_k - (i_k - i_{k-1}) + \Delta L(i_k - i_{k-1}) + \frac{T}{L_l}k_p i_k + \frac{T}{L_l}k_i\sum i_k \\ &= \Delta L i^*_{k+1} + \frac{T}{L_l}k_p i^*_k + \frac{T}{L_l}k_i\sum i^*_k + \underbrace{\frac{T}{L_l}(e_k - e_{k+1})}_{\text{disturbance}}\end{aligned} \quad (44)$$

where $T/L_l(e_k - e_{k+1})$, the scaled difference between the true values of the back EMF at the end of successive control intervals, can be considered as a disturbance term and may be ignored for this analysis [14]. Looking at the terms $\sum i^*_k = i^*_k + i^*_{k-1} + i^*_{k-2} + \cdots$ we notice the following:

$$\begin{aligned}y_k &= \sum i^*_k = i^*_k + y_{k-1} \\ \therefore y_k - y_{k-1} &= i^*_k \\ \therefore y[z-1] &= i^* z \\ \therefore y &= \frac{z}{z-1}i^*.\end{aligned} \quad (45)$$

Using (45), (44) becomes in z-transform form

$$\left(z^2 - z + \Delta L z - z + 1 + \Delta L z - \Delta L + K_p z + K_i\frac{z}{z-1}\right)i = \left(\Delta L z^2 + K_p z + K_i\frac{z}{z-1}\right)i^* + \text{disturbance} \quad (46)$$

where $K_i = k_i T/L_l$ and $K_p = k_p T/L_l$. Ignoring the disturbance term, the augmented system transfer function from i^* to i is

$$\frac{i}{i^*}(z) = \frac{\text{num}(z)}{\text{den}(z)} \quad (47)$$

where

$$\text{num}(z) = (\Delta L z^2 + (K_p - \Delta L)z + K_i - K_p)z$$

and

$$\text{den}(z) = z^3 + (2\Delta L - 3 + K_p)z^2 + (3 - 3\Delta L - K_p + K_i)z + (\Delta L - 1).$$

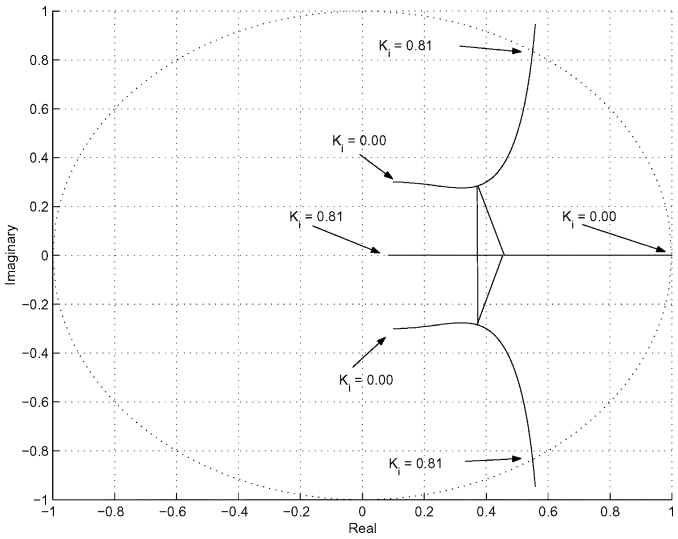

Fig. 8. Root locus of poles of linearized transfer functions given by (47).

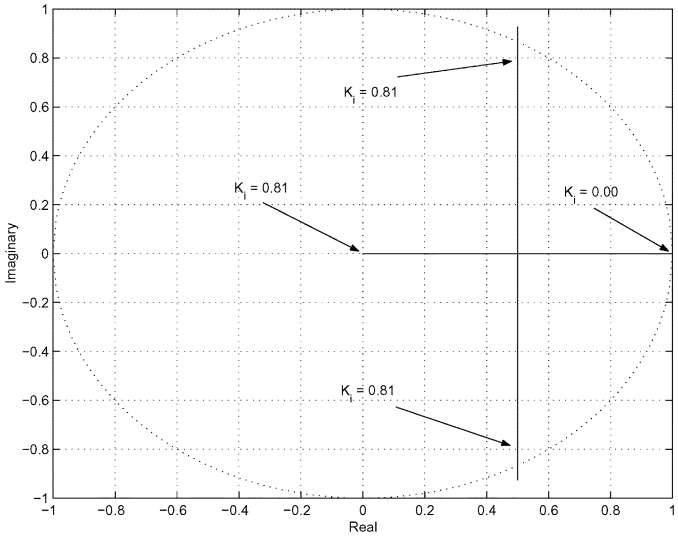

Fig. 9. Root locus of the zeros of linearized transfer function given by (47).

Jury's stability test [15] when applied to the characteristic equation

$$\mathrm{den}(z) = 0 \tag{48}$$

gives the limits on integral gain K_i such that stability is ensured to be

$$0 < K_i < \Delta L(K_p + \Delta L). \tag{49}$$

Figs. 8 and 9 show root locus plots of the poles and zeros of (47), respectively, for $\Delta L = 0.9$, $K_p = 0$, and $0 < K_i < 1$. These plots confirm the stability limit given by (49) and show that the transfer function is minimum phase for K_i within the stability limits. It is not necessary to consider the effect of the proportional term due the undesirable effect that this term has on current ripple as explained in the next section.

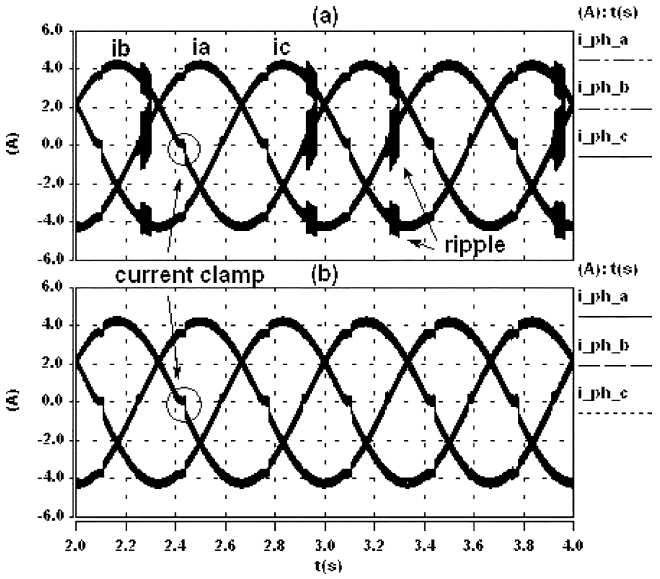

Fig. 10. Current waveforms for purely proportional feedback. (a) $k_p = 10$. (b) $k_p = 0$.

IV. Simulation Results

Simulation studies have shown that the use of proportional feedback leads to unacceptable current ripple especially at times where one of the phase currents crosses zero.

Fig. 10(a) and (b) shows simulated three-phase current waveforms when proportional feedback gains, k_p, of 10 and 0, respectively, and a reference of $i^* = 4.2\sin(2\pi t)$ is applied. While there is a demonstrated reduction in the length of time that the current remains clamped around zero the increase in ripple that is shown more than offsets any benefit. If k_p is less than 10, the amount of ripple decreases but the clamp time increases. If k_p is increased significantly above 10, then the algorithm becomes unstable. There is no perceived benefit from the addition of a proportional feedback term to the algorithm.

The use of integral feedback though is shown to reduce both the amount of ripple observed on the waveform and the length of time that the current remains in its clamped state. Fig. 11(a) and (b) shows phase current waveforms for gains of $k_i = 10$, $\Delta L = 0.9$, and $k_p = 0$. A close-up of the a-phase current waveforms (Fig. 12) reveals a reduction of the time that current is clamped of approximately 40%; further, there is no appreciable increase in ripple over the noncompensated waveform. Care must be taken when choosing the integral gain so as to not exceed the stability limit.

V. Experimental Results

The algorithm has been tested on a system comprised of a 38-kW inverter and a three-phase inductive load (three 5.6-mH inductors connected in a star configuration) to demonstrate the effect of error in back-EMF estimation. A 7.5-kW induction machine was also used as the load in order to demonstrate the effect of additional integral feedback on the algorithm. All of the

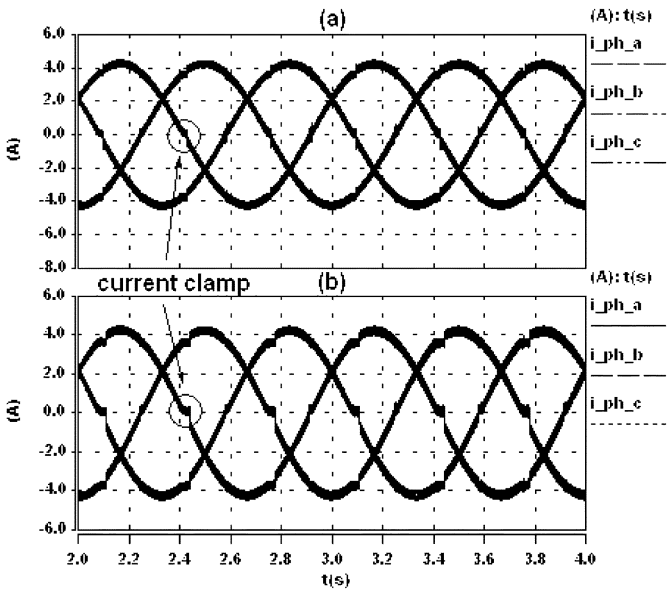

Fig. 11. Current waveforms for purely integral feedback. (a) $k_i = 10$. (b) $k_i = 0$.

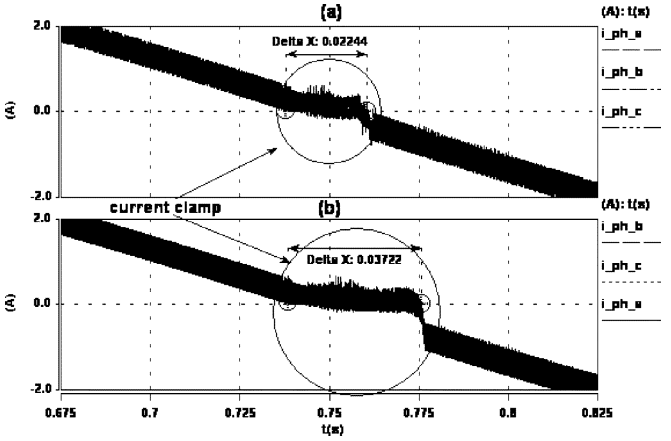

Fig. 12. Zoomed current waveforms for purely integral feedback. (a) $k_i = 10$. (b) $k_i = 0$.

TABLE I
LOAD PARAMETERS

Induction Machine	
7.5kW	$r_s = 1.0\ \Omega$
415V	$r_r = 0.855\ \Omega$
I A	$L_s = 0.1194\ H$
50 Hz	$L_r = 0.1194\ H$
1450 rpm	$L_m = 0.1144\ H$
Static Load	
$L_s = 5.6mH$	$R_s = 0.5\Omega$

experimental results have been generated with a switching frequency of 4 kHz.

The parameters of the induction machine and inductive load are given in Table I.

The current sampling system is designed so that precise sampling of the currents is achieved at the beginning and middle of each control interval. It uses serial A/D converters positioned right next to the Hall-effect transducers, and transmits the digital data at rate of 2.5 Mbits/s, which corresponds to a sampling rate of 125 kSa/s. The PCC algorithm only requires samples at twice the control rate (which is approximately 4 kHz). The extra samples are used for online protection for over current. There is also a dc-link voltage sampling system that works in a similar fashion. Precise synchronization of the samples so that they align with the beginning and the middle of the control interval is achieved by precisely controlling the sample hold. The digital value of the samples for these times are available to the processor after the serial link digital transmission delay (which is approximately 8 μs).

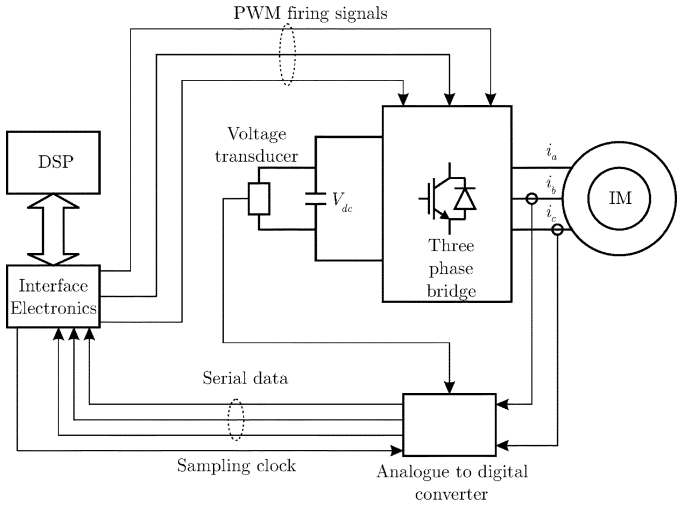

Fig. 13. Experimental setup.

A block diagram of the experimental setup is shown in Fig. 13.

Figs. 14 and 15 show the a-phase (d-phase) output current waveforms obtained from a reference of $i^* = 4.2\sin(2\pi(0.95)t)$. A moderately high dc-link voltage of 475 Vdc was used for these plots so that the voltage loss effect due to dead time would be more evident. The reduction in amplitude of the load current due to dead-time effects is clearly evident in Fig. 15 as compared to Fig. 14. It has also been found that while zero current clamp is still present it is less significant for the waveform when the back EMF is estimated, as compared to the known back-EMF case. These results are consistent with those obtained by simulation.

Figs. 16 and 17 show the reduction in zero current clamp duration with the introduction of an integral term to the basic algorithm. The dc-link voltage used for these plots was 240 Vdc. The integral gain used to generate Fig. 17 was $k_i = 10$ which gave a reduction in clamping time of approximately 30%–40% which is again consistent with the simulation result.

Remark 11: The current clamp evident in these plots appears to be displaced from the zero crossing. High-frequency ripple on the waveforms, which cannot be observed accurately due to sampling and memory limitations of the oscilloscope at this relatively low fundamental frequency, are, in, fact causing current excursions to the zero crossing.

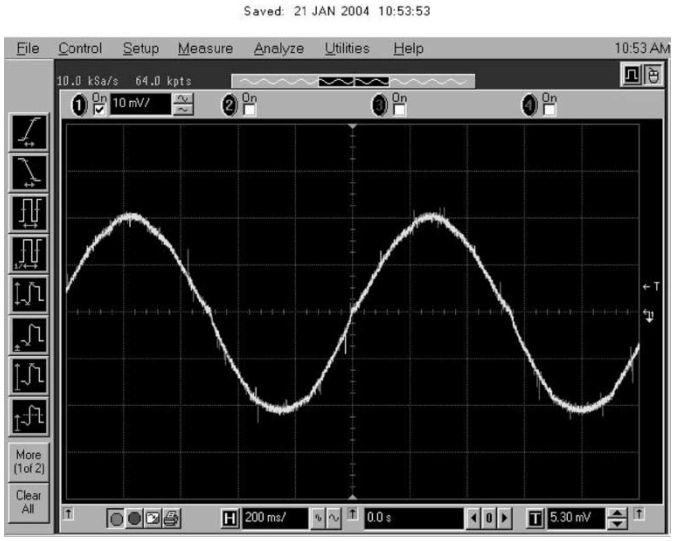

Fig. 14. The *a*-phase current waveform for static inductive load with estimated back EMF (1 div = 2 A).

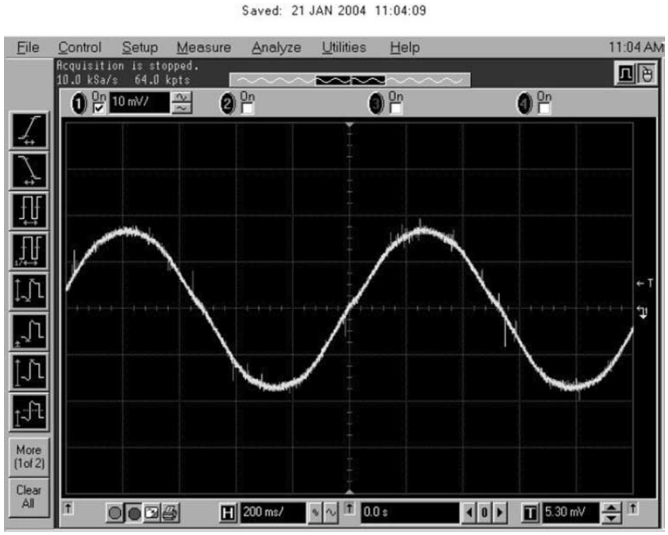

Fig. 15. The *a*-phase current waveform for static inductive load with known (zero) back EMF (1 div = 2 A).

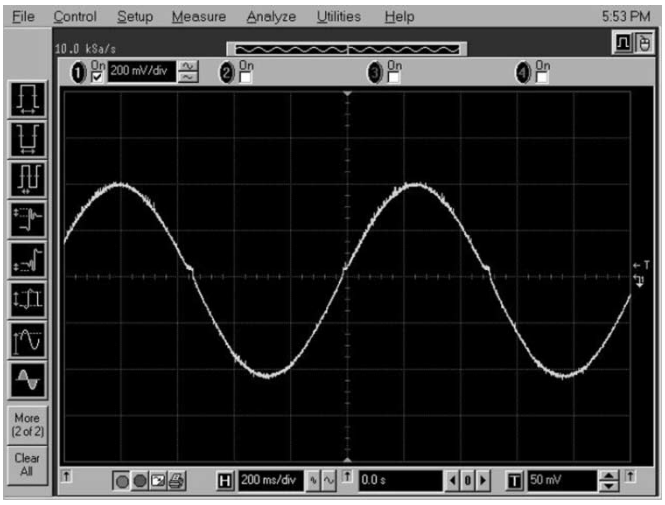

Fig. 16. The *a*-phase current waveform for induction machine load—back EMF estimated (1 div = 2 A).

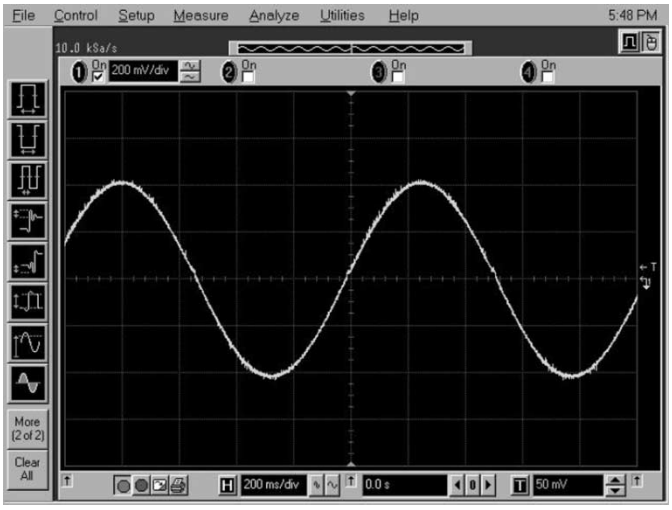

Fig. 17. The *a*-phase current waveform form induction machine load—additional integral feedback term included (1 div = 2 A).

VI. Conclusion

The PCC is a fully digital, computationally efficient, high-performance, parameter-insensitive current control algorithm for induction machines. However, the influence of dead time on the performance of the algorithm has not been previously investigated. This paper has demonstrated that voltage error due to dead time is implicitly compensated for by the predictive control algorithm and that the inclusion of an additional feedback term into the algorithm significantly reduces the zero-current-clamp effect. The stability boundaries of the augmented PCC have been calculated. The augmented algorithm does not require any additional hardware, and only a marginal increase in computational effort. The excellent performance of the augmented PCC algorithm has been verified experimentally.

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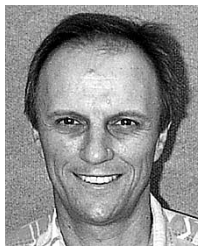

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