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## Introduction

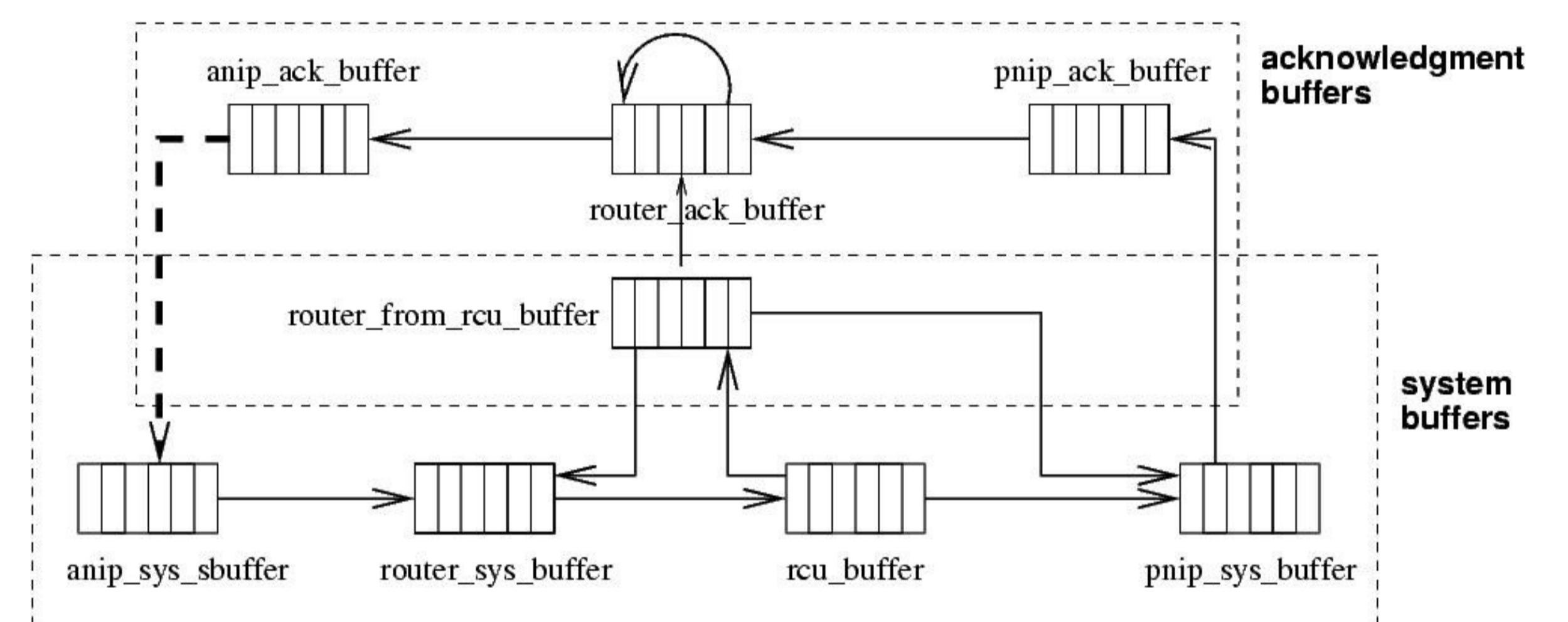
Network on Chip(NOC) is an alternative means of communication between individual blocks inside a chip [Hermani et al. 2000].

- It uses packet-switching communication, like TCP/IP.
- It solves the problem of scalability that is present in the traditional point-to-point communication.
- Packet-switching may lead to deadlock.



## Results

- Complete and formal model (in PVS) of NOC and ÆTHEREAL.
- A systematic way of keeping track of the design alternatives (modularity of the model).
- A proof that the system is deadlock free. Done in an abstracted version of the model.



## What is ÆTHEREAL protocol?

ÆTHEREAL protocol is a protocol that is designed to realize correct functionality of NOC and avoid any circumstance that lead to deadlock [Goossens et al. 2000].

This is done by providing:

1. Best effort service (BE), and
2. Guaranteed-throughput service (GT)

GT connections are established by BE packet transfer between the sender (ANIP) and the receiver (PNIP) blocks.

## Research problem

**Is ÆTHEREAL protocol deadlock free?**

## Deadlock prevention criteria

1. Use separate buffers for ANIP-to-PNIP and PNIP-to-ANIP communications.
2. Do not allow ANIP to send more packets than it can accommodate their acknowledgment packets.

%when ever there is a packet coming to anip\_sys\_buffer,  
%there will be always a space to accommodate it.

```
Inv1(s):bool = ee(s) + g(s) + m(s) + l2(s) <= C(l2(s))
property1: LEMMA reachable_path(sl) IMPLIES
(FORALL i: i < length(sl) IMPLIES Inv1(nth(sl,i)))
```

Formal specification is useful to document complex designs, force designers to clarify design choices, and resolve problematic inconsistencies in the early stage of the design process.