Decoupling Capacitance Allocation for Power Supply Noise Suppression

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ABSTRACT

We investigate the problem of decoupling capacitance allocation for power supply noise suppression at floorplan level. Decoupling capacitance budgets for the circuit modules are calculated based on the power supply noise estimates. A linear programming technique is used to maximize the allocation of the existing white space in the floorplan for the placement of decoupling capacitors. An incremental heuristic is proposed to insert more white space into the existing floorplan to meet the remaining demand required for decoupling capacitance fabrication. Experimental results on six MCNC benchmark circuits show that the white space allocated for decoupling capacitance is about 6% – 12% of the chip area for the $0.25\mu m$ technology, and the power supply noise can be kept below $10\%Vdd$.

1. INTRODUCTION

Signal integrity is emerging as an important issue as VLSI technology advances to deep submicron regime. Of particular importance among the signal integrity issues is the power supply noise. In today's deep sub-micron CMOS technology, devices are of smaller feature size, faster switching speed, and higher integration density. Large current spikes due to a large number of "simultaneous" switching events in the circuit within a short period of time can cause considerable IR drop and Ldi/dt noise over the power supply network [5]. Power supply noise degrades the drive capability of transistors due to the reduced effective supply voltage seen by the devices. Power supply noise may also introduce logic failures and jeopardize the reliability of high performance VLSI circuits, since the noise margin gets lower as the supply voltage scales with the technology. Recently, many research efforts [6][18][17][12][15][16] have been directed toward power supply noise analysis and power supply network optimization. Topology optimization [11], wire sizing [10], on-chip voltage regulation [3], and decoupling capacitance deployment [6][14] are the most widely used techniques to relieve power supply noise. In the past, decoupling capacitance optimization has been investigated at circuit level or system level [14][4] with the assumption that there is always white (empty) space available for decoupling capacitance.

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In this paper, we investigate the problem of on-chip decoupling capacitance (decap) deployment at floor planning level. Given a floorplan with the placement information and the worst case switching activity profile of each circuit module, we want to find an area efficient scheme to deploy the decap such that the power supply noise at each module is suppressed to below a specified limit. We estimate the worst case noise in the power supply network experienced by each module according to the placement information and switching profiles. Based on the worst case power supply noise, we calculate decoupling capacitance budget for each circuit module. We allocate white (empty) space for decoupling capacitors in two steps. Existing white space is first allocated to the neighboring blocks using a linear programming technique to maximize the utilization of the existing white space in the floorplan. Additional white space, if needed, is inserted into the floorplan using a heuristic method to meet the total decoupling capacitance demand of the whole circuit.

The rest of the paper is organized as follows. Power supply noise estimation for each circuit module is presented in Section 2. Decoupling capacitance budgets for the circuit blocks are calculated in Section 3. White space allocation for these decoupling capacitances is addressed in Section 4. Experimental results are presented in Section 5. Finally, conclusions are drawn in Section 6.

2. POWER SUPPLY NOISE ESTIMATION

Decoupling capacitance is allocated to each module based on its switching profile and the power supply noise it experiences. To determine the decap demand of each module, we must estimate the power supply noise at each module in the floorplan. In the following subsections, we will discuss power supply network modeling, switching current distribution, and noise estimation.

2.1 Power Supply Network Modeling

In today's VLSI technology, most power supply networks are of a mesh structure as illustrated in Fig. 1. We make the following assumptions: (i) All the segments of the mesh grids are of the same physical dimensions. (ii) The connection points of the circuit modules to the power grids are determined by the locations of the centers of the modules. We model each segment of the power grids as a lumped *RLC* element, and the whole mesh as a pseudo-distributed *RLC* network as illustrated in Fig. 2. The GND node in Fig. 2 should be regarded as a GROUND network with a similar mesh structure as illustrated in Fig. 2. The unit length parasitics r, l, and c are technology dependent. The package parasitics of the power pins are R_P and L_P. The unit length inductance l should be regarded as the average inductance per unit length in the power supply grids. The circuit blocks are modeled as time-varying current sources that draw current from the VDD sources through their con-

nection points in the power supply grids. Since the circuit should operate correctly even under the worst case scenario, we use the worst case switching activity profiles of the circuit blocks to deduce the current waveforms for power supply noise estimation.

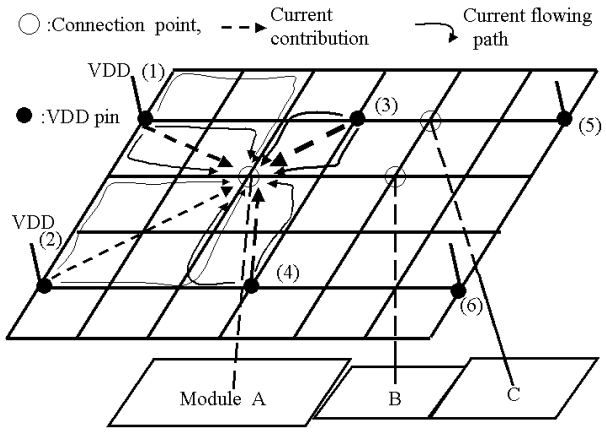

Figure 1: Power Supply Network–Mesh Structure

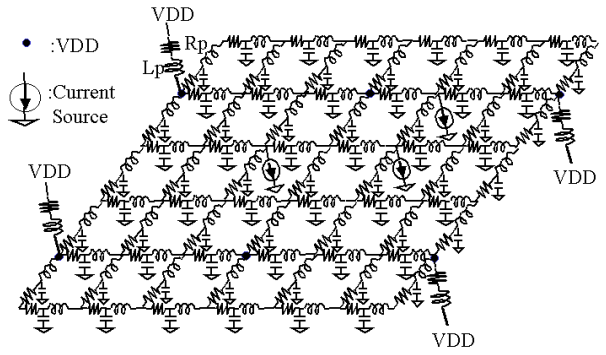

Figure 2: Model of power supply network

2.2 Current Distribution

Given the mesh topology and the switching current waveforms of the circuit modules, we can approximately determine the distribution of those switching currents among the power supply network. A key observation is that currents follow the least-impedance paths when flowing from the *VDD* source to the destination sink. In other words, if there are multiple paths from a *VDD* source to a destination sink, the current flowing along each path is inversely proportional to the impedance of the path. Based on this observation, we make the following assumption: The switching current drawn by a sink comes from only the neighboring *VDD* sources; the contributions from remote *VDD* sources are negligibly small, and therefore can be ignored. This assumption significantly simplifies the current distribution analysis without compromising the validity of the results. The direct consequence of this assumption is that currents flowing along the neighboring grids of the sinks are slightly overestimated, and consequently the power supply noise at the connection points will be overestimated. With that assumption in mind, the question comes down to how the current drawn by a sink is split among the neighboring *VDD* sources, or in other words, how much current each neighboring *VDD* pin is contributing.

Suppose that there are N ($N = 4$ in most cases) neighboring *VDD* sources surrounding a sink. Let $Z_1, Z_2, \ldots, Z_N$ be the impedances between the current sink to the N neighboring *VDD* pins, respectively. Let I be the current a sink is sourcing from the power network. Let $I_1, \ldots, I_N$ be the currents contributed by the N neighboring *VDD* pins, respectively. $I_1, \ldots, I_N$ are given by the following equations:

$$\begin{aligned} & I_1 + I_2 + \ldots + I_N = I && (a) \\ & Z_1 I_1 = Z_2 I_2 = \ldots = Z_N I_N && (b) \\ & Y_j = \tfrac{1}{Z_j} \quad j = 1, 2, \ldots, N && (c) \\ \Rightarrow \quad & I_j = \tfrac{Y_j}{\sum_{i=1}^{N} Y_i} I, \quad j = 1, 2, \ldots, N, && (d) \end{aligned} \tag{1}$$

where Y_j is the admittance from the sink to *VDD* source j. Eqn. (1.a) states that the contributions from the neighboring *VDD* pins sum up to the total current the sink is sourcing. Eqn. (1.b) states that the voltage differences from the sink to different neighboring *VDD* pins are the same. Solving equations $(1.a) - (1.c)$ gives the solution to $I_1, \ldots, I_N$ as shown in equation $(1.d)$.

The impedance between a sink and a *VDD* pin in the power mesh is mainly determined by the least-impedance paths that link them. The impedance of a path can be calculated based on its length and the unit length parasitics of the wire segments in the power grids. The equivalent impedance of the shortest paths, the second shortest paths, ..., and so on, connected in parallel, will be a reasonable estimate of the impedance between the two points. Clearly, the accuracy of the approximation improves as more paths are considered. Experimental results show that it is sufficient to consider only the shortest paths and the second shortest paths. The error (compared with SPICE results) is less than 10%.

Once the component currents I_j $(j = 1, 2, \ldots, N)$ from the neighboring *VDD* sources are determined, we distribute I_j among the dominant paths from *VDD* source j to the sink as illustrated in Fig. 3. Let $\{P_1, P_2, \ldots, P_w\}$ denote the set of the shortest paths and

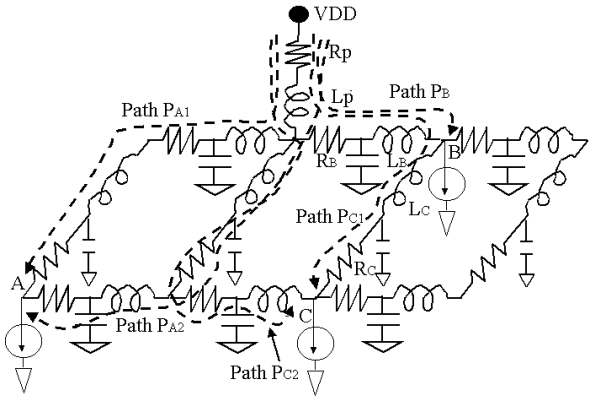

Figure 3: Current paths in power supply mesh.

the second shortest paths under consideration. Let $Y_{P_1}, Y_{P_2}, \ldots, Y_{P_w}$ be the admittance of these paths. By a similar derivation used in Eqn. (1), the current I_j can be distributed among these paths, denoted by $i_{P_1}, i_{P_2}, \ldots, i_{P_w}$, as follows:

$$\begin{aligned} & i_{P_1} + i_{P_2} + \ldots + i_{P_w} = I_j, \\ & i_{P_k} = \tfrac{Y_{P_k}}{\sum_{i=1}^{w} Y_{P_i}} I_j, \quad k = 1, 2, \ldots, w. \end{aligned} \tag{2}$$

2.3 Noise Estimation

To estimate the power supply noise that a circuit block experiences, we calculate the voltage variation at the connection point

of the block in the power supply grids, which is the voltage difference between the connection point and its neighboring power supply pins [18]. Suppose P_k is a dominant current path between the connection point of circuit module k and the VDD pin closest to it. Let $T^{(k)} = \{P_j : P_j \cap P_k \neq \emptyset\}$ be a collection of the current paths in the power supply mesh that overlap with path P_k (including P_k itself). Let $P_{jk} = P_j \cap P_k$ denote the overlapping part between path P_j and path P_k, $R_{P_{jk}}$ denote the resistance of P_{jk}, and $L_{P_{jk}}$ denote the inductance of P_{jk}. Let $V_{noise}^{(k)}$ denote the power supply noise at module k. $V_{noise}^{(k)}$ can be calculated using Kirchhoff's Voltage Law (KVL):

$$V_{noise}^{(k)} = \sum_{P_j \in T^{(k)}} (i_j R_{P_{jk}} + L_{P_{jk}} \frac{di_j}{dt}), \quad (3)$$

where i_j is the current flowing along path P_j. One should note that not only the switching current of module k contributes to $V_{noise}^{(k)}$, other modules that draw current from the same VDD pins as module k contribute as well, as long as their current distribution paths overlap with P_k. Since there are potentially several paths leading to a module from a VDD pin, we choose the path of the worst current load to calculate the noise.

3. DECOUPLING CAPACITANCE BUDGET

In this section, we estimate the decap budget for each circuit module in the floorplan based on (i) the power supply noise the module experiences, and (ii) the upper limit of the power supply noise, denoted $V_{noise}^{(lim)}$, that the circuit can tolerate. $V_{noise}^{(lim)}$ is technology dependent, and is usually set to be $10\%Vdd$. Suppose there are M modules in the floorplan, and the switching current of module k is $I^{(k)}$, $k = 1, 2, \ldots, M$. Let $C^{(k)}$ be the decoupling capacitance required for circuit module k. Let $Q^{(k)}$ be the total charge that module k will draw from the power supply network during the worst case switching process. $Q^{(k)}$ is given by the following equation:

$$Q^{(k)} = \int_0^{\tau} I^{(k)}(t)dt,$$

where τ is the duration that the switching process lasts. The upper limit of $C^{(k)}$ is $Q^{(k)}/V_{noise}^{(lim)}$, which assumes that $C^{(k)}$ will provide most of the switching current of module k. The decoupling effect will diminish when $C^{(k)}$ is increased beyond the limit.

An apparent budget scheme is $C^{(k)} = Q^{(k)}/V_{noise}^{(lim)}$, $k = 1, 2, \ldots, M$. This scheme is suboptimal in the sense that it will result in a larger decap budget than required. We refer to a solution produced by this scheme a "Greedy Solution". Although the "Greedy Solution" method is not optimal, it is commonly used in practice and cited in research literatures [5][14].

In this paper, we take a different approach to compute $C^{(k)}$. The decap required for each circuit module can be initially estimated as follows:

$$\begin{aligned} &\theta = max(1, \tfrac{V_{noise}^{(k)}}{V_{noise}^{(lim)}}), \\ &C^{(k)} = (1 - 1/\theta)Q^{(k)}/V_{noise}^{(lim)}, \quad k = 1, 2, \ldots, M, \end{aligned} \quad (4)$$

Suppose the estimated power supply noise (before considering decap) of module k is θ times the tolerable noise limit $V_{noise}^{(lim)}$. In order to reduce the power supply at module k to $V_{noise}^{(lim)}$, we need to scale the noise at module k by a factor of θ, which is achievable if we scale down all the currents that contribute to $V_{noise}^{(k)}$ by a factor of θ according to Eqn. (3). The current flowing through the network can be reduced to $1/\theta$ of its value by adding enough decap to buffer $(1 - 1/\theta)$ portion of the current load. Since the decap at module k is only responsible for providing the switching current of module k, the decap $C^{(k)}$ should be such that when its voltage is lowered from Vdd to $Vdd - V_{noise}^{(lim)}$, it will release $(1 - 1/\theta)Q^{(k)}$ amount of charge to supply the demand of module k during the switching process, which leads to $C^{(k)}V_{noise}^{(lim)} = (1 - 1/\theta)Q^{(k)}$. When $V_{noise}^{(k)} \leq V_{noise}^{(lim)}$, no decap is required.

When $C^{(k)}$ is added to module k, we update the power supply noises at module k and all the modules that draw currents from the same VDD pins as module k according to Eqn. (3). Since the switching current at module k also contributes to the power supply noise at those modules, when the current drawn by module k is reduced due to decoupling effect of $C^{(k)}$, the noise at those affected modules will also be relieved to some extent as dictated by Eqn. (3). Due to the contributions by the switching current of the neighboring modules, the updated $V_{noise}^{(k)}$ may still be above $V_{noise}^{(lim)}$ after adding decap $C^{(k)}$. However, $V_{noise}^{(k)}$ will be further relieved as we add decap to the neighboring modules.

After the initial decap budgets are calculated for all the modules in the floorplan, we verify the updated power supply noise at each module to make sure it is indeed below $V_{noise}^{(lim)}$. If $V_{noise}^{(k)}$ is still above $V_{noise}^{(lim)}$ for some module k, we will increase $C^{(k)}$ by an adequate amount (without exceeding its upper limit) such that $V_{noise}^{(k)}$ goes below $V_{noise}^{(lim)}$. If $C^{(k)}$ is increased to the limit and $V_{noise}^{(k)}$ is still above the limit, we need to increase the decap of its neighboring modules until $V_{noise}^{(k)}$ goes below $V_{noise}^{(lim)}$. This process is guaranteed to converge (since the "Greedy Solution" is the worst case solution of this approach).

The decap budgets generated with our procedure can be significantly smaller than the "Greedy Solution" (Please refer to Table 2 in Section 5). The procedure for decap budgets calculation is summarized in Fig. 4.

Remark 1. The added on-chip capacitance may change the resonance condition of the chip. If the clock frequency (or it harmonics) coincides the resonance frequency of the chip, a large voltage fluctuation can build up in the power supply network and cause circuit failure. Simulation must be performed to identify the potential resonance frequencies [5] and the power supply network may need to be redesigned to prevent resonance.

4. WHITE SPACE ALLOCATION FOR DECOUPLING CAPACITANCES

On-chip decaps are usually fabricated as MOS capacitors. The unit area capacitance of a MOS capacitor is given by $C_{ox} = \varepsilon_{ox}/t_{ox}$, where t_{ox} is the oxide thickness and ε_{ox} is the permittivity of SiO_2. The decoupling capacitance budget for each circuit module is converted to the area of silicon required to fabricate the decap as follows:

$$S^{(k)} = C^{(k)}/C_{ox}, \quad k = 1, 2, \ldots, M, \quad (5)$$

where $S^{(k)}$ is the white space required to fabricate $C^{(k)}$.

Decaps need to be placed in the close neighborhood of switching activities to effectively relieve the power supply noise. Decaps located far from the noisy spot are not effective due to longer RC delay time and IR drop [6]. The decoupling capacitances allocation problem really boils down to white space (WS) allocation in the existing floorplan. Due to timing and routing constraints, it is best not to make dramatic changes to the given floorplan. Decap allocation

Decoupling Capacitance (decap) Budget( )

Input: Floorplan with placement information, power supply noise of all circuit modules.

Sort all circuit modules according to the power supply noise;

For each module in the sorted list–starting with the module with the worst noise – **do**

Calculate its decap budget using Eqn. (4);

Update power supply noise of the modules affected due to the decap added using Eqn. (3);

For each module in the sorted list (after initial run) **do**

Check to see if its power supply noise is below $V_{noise}^{(lim)}$;

If power supply is not below $V_{noise}^{(lim)}$ **then**

Increase its decap until noise goes below limit or the decap reaches its limit;

If the power supply noise is still above $V_{noise}^{(lim)}$ **then**

Increase the decap of neighboring modules until noise goes below limit;

Output: Decoupling capacitance budget for each module.

Figure 4: Procedure: *Calculating decoupling capacitance budget for each module in the floorplan.*

can be done as a post-placement refinement to the existing floorplan in an incremental manner [9]. There are two issues in decap allocation: First, we must allocate $S^{(k)},\ k = 1,2,\ldots,M$, amount of WS to module k. Second, the amount of WS $S^{(k)}$ must be in the vicinity of module k in order for the decap to be effective. The WS allocation are carried out using a two-step approach as follows.

4.1 Allocation of Existing WS

The isolated WS's in the original floorplan are treated as WS modules and can be used for decap fabrication. Since decap (or equivalent WS) must be placed close to the target circuit module, WS modules located far from a circuit module are considered inaccessible. When we allocate an existing WS module to its neighboring circuit modules, it is possible that after the white space demands of all its neighboring circuit modules has been met, there is still some WS left, and the remaining WS is not neighboring to any circuit blocks and therefore considered as inaccessible WS. We must allocate the existing WS judiciously such that the inaccessible WS is minimized.

The problem can be solved using the linear programming (LP) technique. Suppose there are H isolated WS modules with area $A_k,\ k = 1,2,\ldots,H$, in the existing floorplan.
Let $N_k = \{j : module\ j\ is\ adjacent\ to\ WS\ module\ k\}\ k = 1,2,...,H$, denote a set of circuit modules neighboring WS module k. Let $x_k^{(j)}$ be the amount of WS allocated to circuit module j from WS module k. The WS allocation problem can be formulated as follows:

$$\begin{aligned}
maximize \quad & S = \sum_{k=1}^{H} \sum_{j \in N_k} x_k^{(j)}, \\
subject\ to \quad & \sum_{j \in N_k} x_k^{(j)} \le A_k,\ \ k = 1,2,\ldots,H, \\
& \sum_{k=1}^{k=H} x_k^{(j)} \le S^{(j)},\ \ j = 1,2,\ldots,M, \\
& x_k^{(j)} \ge 0, \quad \forall k, \forall j, \qquad (6)
\end{aligned}$$

where S is the total WS allocated. The first set of constraints guarantee that the total WS allocated from a WS module k is less than or equal to its area A_k. The second set of constraints guarantee that the WS allocated to a circuit module j is less than or equal to its WS demand $S^{(j)}$, because there is no need to over-supply its WS demand. The third set of constraints guarantee that all the allocations are positive.

After we solve the LP problem, we know exactly how the existing WS modules are allocated to the circuit modules and how much WS is inaccessible. We compute the updated white space demand $\tilde{S}^{(j)},\ j = 1,2,...,M$, for all circuit modules after the WS allocation as follows:

$$\tilde{S}^{(j)} = S^{(j)} - \sum_{k=1}^{H} x_k^{(j)}, \quad j = 1,2,\ldots,M.$$

The additional amount of WS $S_{(A)}$ that needs to be inserted into the floorplan is determined as:

$$S_{(A)} = \sum_{j=1}^{M} \tilde{S}^{(j)} = \sum_{j=1}^{M} S^{(j)} - S.$$

If $S_{(A)} = 0$, allocation process is complete; Otherwise, we need to insert $S_{(A)}$ into the floorplan such that the WS can be used for decoupling capacitance allocation.

4.2 Insertion of Additional WS into Floorplan

We use a heuristic to insert $S_{(A)}$ into the floorplan. The WS is inserted by extending the floorplan dimensions in both x-direction and y-direction. Suppose α portion of the additional WS $S_{(A)}$ is obtained by extending the floorplan in y-direction, and $(1-\alpha)$ portion of $S_{(A)}$ is obtained by extending the floorplan in x-direction. Let $LayoutX$ and $LayoutY$ be the width and height of the original floorplan. The extensions of the floorplan in x-direction and y-direction, denoted by $ExtX$ and $ExtY$, are given as follows:

$$ExtY = \frac{\alpha S_{(A)}}{LayoutX};\ \ ExtX = \frac{(1-\alpha)S_{(A)}}{(LayoutY + ExtY)}.$$

The heuristic works as follows: The modules in the floorplan are

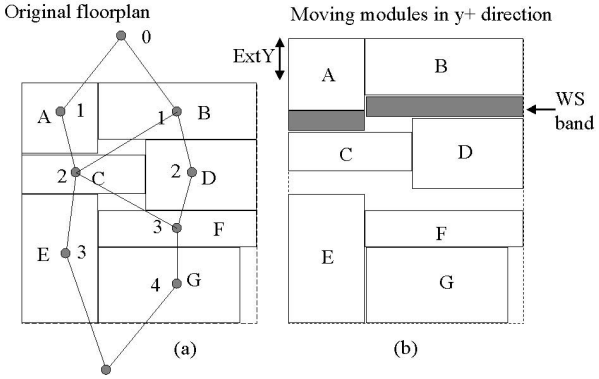

Figure 5: Moving modules in y-direction in the order $\{(A,B),\ (C,D),\ (E,F),\ (G)\}$ to make WS for decoupling capacitance.

arranged into rows according to their levels in the constraint graph [13][6] with the level of the source node in the graph set to 0. First we move the circuit modules in y-direction row by row. We move the modules in the top row by $ExtY$, then the rows below it will be moved subsequently as illustrated in Fig. 5. We insert WS

bands between the rows by shifting the adjacent rows by different amounts in y-direction. The width of the WS band is determined by the WS demand of the circuit modules in the previous row. The width of the WS band inserted between row $j-1$ and row j, denoted by $B_{WS}^{(j-1)}$ is given as follows:

$$B_{WS}^{(j-1)} = \frac{\sum_{i \in row\ (j-1)} \alpha \tilde{S}^{(i)}}{LayoutX}.$$

The inserted WS band provides α portion of the WS demanded by the circuit modules in row $j-1$.

Similarly, WS bands are inserted between columns by moving the modules in x-direction.

$$B_{WS}^{(k-1)} = \frac{\sum_{i \in column\ (k-1)} (1-\alpha) \tilde{S}^{(i)}}{LayoutY + ExtY}.$$

Our heuristic inserts the additional WS required into the existing floorplan in an incremental manner. Since modules in the same row (or column) are shifted by the same amount of distance in our algorithm, our heuristic preserves the topology of the original floorplan.

5. EXPERIMENTAL RESULTS

The proposed decoupling capacitance budget and allocation algorithms are implemented in C. The linear programming part of the algorithm is solved using Matlab by invoking a system call to Matlab in our C program. Experiments are performed on six MCNC [1] benchmark circuits implemented in $0.25\mu m$ technology.. The pitch for the metal lines in the power supply mesh is $333.3\mu m$, and the pitch for VDD pins is $1000\mu m$. The parameters such as unit length parasitics of the metal grids in the power supply network are provided by a leading semiconductor company. The technology parameters are listed in Table 1. The initial floorplans of the MCNC benchmark circuits used for this work were obtained from [7]. These floorplans were generated by running simulated tempering with an improved Monte-Carlo technique [8]. The worst case switching current profiles for the circuit modules are generated as follows. The worst case current density j_s is estimated for $0.25\mu m$ technology based on the technology parameters, such as integration density, transistor channel length, obtained from ITRS'97 Roadmap [2]. The peak switching current for a circuit module k is $I^{(k)} = j_s A_k$, where A_k is the area of module k. The overall switching current waveform of module k is approximated with a triangular waveform with peak value $I^{(k)}$, and duration of the switching current waveform (τ) is assumed to be half the clock cycle. Our method is, however, not limited to the triangular waveform assumption, and more sophisticated piece-wise linear waveforms can be used to represent the switching current waveforms of the circuit modules. In our experiments, j_s is set to $0.35\mu A/\mu m^2$, and τ is set to $1ns$. The power supply noise limit $V_{noise}^{(lim)}$ is set to be $0.25V$.

The experimental results are presented in Table 3. The total decoupling capacitance budgets for the benchmark circuits vary significantly depending on the size of the modules and the dimensions of the floorplan. Large circuits like *playout* and *apte* suffer serious power supply noise and require considerable amount of WS for decoupling capacitance fabrication. The WS used for decoupling capacitance is about 12% of its chip area for *apte*, and about 10% of its chip area for *playout*.

To compare our method with the "Greedy Solution" method (see Section 3), the decoupling capacitance budgets obtained with the two methods are listed in Table 2. It is clear our method generates smaller decoupling capacitance budgets. For circuit *ami49*, the decoupling capacitance generated with our method is only 41.5% of that generated using "Greedy Solution" method.

Table 1: Technology parameters

Parameters	Description	Value
r	wire resistance per unit length ($\Omega/\mu m$)	0.0125
l	wire inductance per unit length ($pH/\mu m$)	0.8
c	wire capacitance per unit length ($fF/\mu m$)	20
L_P	package inductance per VDD pin (nH)	0.1
R_P	package resistance per VDD pin (Ω)	0.2

Table 2: Comparison of decap budgets: Ours vs "Greedy Solution"

Circuit	decap Budget (our method) (nF)	decap Budget ("Greedy Solution") (nF)	Percentage (%)
apte	27.73	32.64	85.0
xerox	8.00	13.5	59.3
hp	3.45	6.18	55.8
ami33	0	0.8	0.0
ami49	10.28	24.8	41.5
playout	42.91	61.67	69.6

Data on the existing WS in the original floorplan, the inaccessible WS, and the added WS are also collected for each benchmark circuit as shown in Table 3. The percentage in the parentheses is the percentage of the total chip area for WS. To determine the effectiveness of decoupling capacitance placement, the peak noise data before and after decoupling capacitances deployment are collected and compared. It is evident that peak noise is indeed suppressed to within the noise limit of $0.25V$. As an example, the floorplan of benchmark circuit *playout* is shown in Fig. 6 (a) (before WS insertion) and Fig. 6 (b) (after WS insertion), respectively. α value (see Section 4.2) used in the experiment is 0.5. It is clear the modification to the floorplan is minor and the topology of the floorplan is preserved.

6. CONCLUSION

A methodology for decoupling capacitance allocation at floorplan level is proposed. The proposed methodology can be used to estimate the decoupling capacitance budget for each circuit module in the floorplan. A linear programming technique and a proposed heuristic are incorporated into the methodology for decoupling capacitance placement. Experimental results on six MCNC benchmark circuits show that our methodology produces significantly smaller decoupling capacitance budgets than the "Greedy Solution" method commonly used in practice and research. The algorithm implemented for decoupling capacitance allocation modifies the floorplan incrementally without dramatically changing the topology of the original floorplan.

7. ACKNOWLEDGMENT

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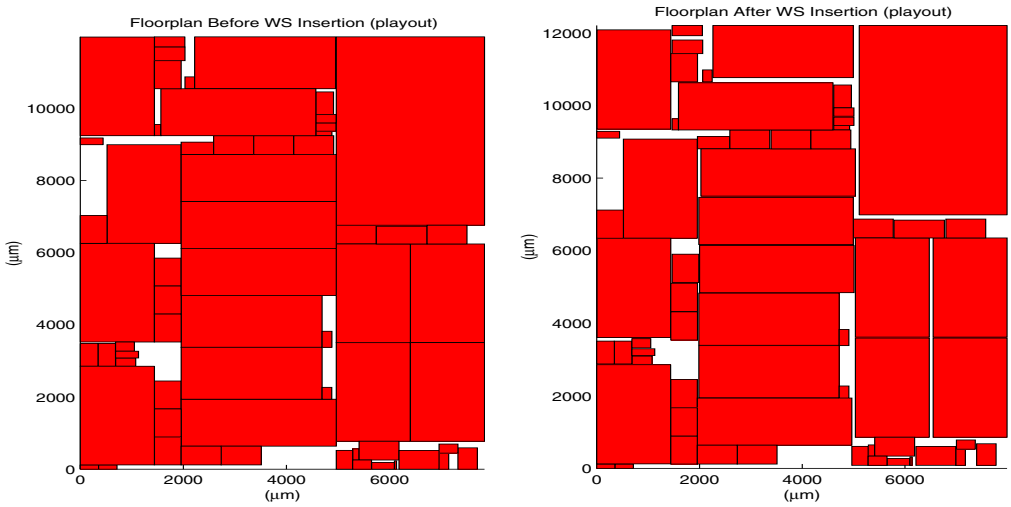
Table 3: Experimental results for MCNC benchmark circuits

Circuit	Modules	Existing WS (μm^2) (%)	decap Budget (nF)	Inaccessible WS (μm^2) (%)	Added WS (μm^2) (%)	Peak Noise (V)(before)	Peak Noise (V)(after)
apte	9	751652 (1.6)	27.73	0 (0)	4794329 (10.3)	1.95	0.24
xerox	10	1071740 (5.5)	8.00	0 (0)	528892 (2.7)	0.94	0.20
hp	11	695016 (7.8)	3.45	306076 (3.5)	300824 (3.4)	1.09	0.23
ami33	33	244728 (21.3)	0	N/A	0	0.16	0.16
ami49	49	2484496 (7.0)	10.28	891672 (2.5)	463615 (1.3)	1.45	0.25
playout	62	5837072 (6.6)	42.91	792110 (0.9)	3537392 (4.0)	1.23	0.24



(a) Before (b) After

Figure 6: Floorplan of benchmark circuit *playout* before (a) and after (b) WS insertion

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