Deep reactive ion etching as a tool for nanostructure fabrication

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Deep reactive ion etching (DRIE) is investigated as a tool for the realization of nanostructures and architectures, including nanopillars, silicon nanowires or carbon nanotubes on Si nanopillars, nanowalls, and nanonetworks. The potential of combining top-down fabrication methods with the bottom-up synthesis of one-dimensional nanocomponents is assessed. The field-emission properties of carbon nanotubes/Si pillars hybrid structures are measured, as well as the transport properties of large-area nanowires obtained via nanowire lithography. The potential of DRIE for the fabrication of three-dimensional nanostructures is also revealed. © *2009 American Vacuum Society.*
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I. INTRODUCTION

Nanosize vertical silicon structures with high aspect ratio are crucial for many applications, such as photonics, optical waveguides, microfluidics, DNA separation, heat dissipation, etc.[1–3] Two approaches are generally followed to fabricate them. The first relies on bottom-up methods, the most popular being the catalyst-assisted growth of vertical silicon nanowires (SiNWs).[4,5] The second relies on top-down manufacturing, namely, high-aspect-ratio anisotropic etching of silicon wafers.[4,5] So far, these two approaches have progressed on two parallel tracks, and their independent development could be seen as a competition to set a single nanofabrication standard.

Amongst top-down methods, deep reaction ion etching (DRIE) is regarded as a powerful method to fabricate vertical silicon structures or pillars.[2,3,6,7] The DRIE process is a key silicon micromachining technique, and in microelectromechanical system (MEMS) device fabrication, anisotropic DRIE of silicon is a mature process technology that is used for creating three-dimensional (3D) mechanical structures.[8,9] Recently, DRIE has been also successfully applied to through-wafer etching for advanced packaging.[10] A typical DRIE process involves the use of a high-density plasma and comprises a sequence of alternating steps (no more than a few seconds long) of silicon etching and polymer deposition to protect the already-carved features from further lateral etching. As cycles go on, the micromachining proceeds via a series of "bites" into the silicon, each on the order of 0.5–5.0 μm deep. These are usually called "scalloping" [or "ripple," see Figs. 1(a) and 1(b)].[8–10] For nanostructure etching, however, scalloping can become a serious problem.[6,7] As feature size and scallop size become comparable, the process conditions have to be adjusted to minimize the ripple, in order to ensure smooth sidewalls at the nanoscale. This can be achieved by optimizing source power, bias power, gas flow rate, flow cycle time, substrate temperature, and chamber pressure.

In this study, we illustrate an optimized DRIE process for the fabrication of smooth silicon nanostructures, including nanopillars, nanowires, and nanowalls. We also show that we can favorably exploit and control the scalloping effect to realize novel three-dimensional nanostructures. We then devise advanced mask-engineering solutions that allow us to combine the advantages of both top-down and bottom-up fabrication methods. These include the possibility of using etching masks for DRIE that can later catalyse the growth of individual or multiple NWs or nanotubes. Further, we show that bottom-up nanostructures themselves (such as nanoparticles, NWs, or nanospheres) can be used as etching masks

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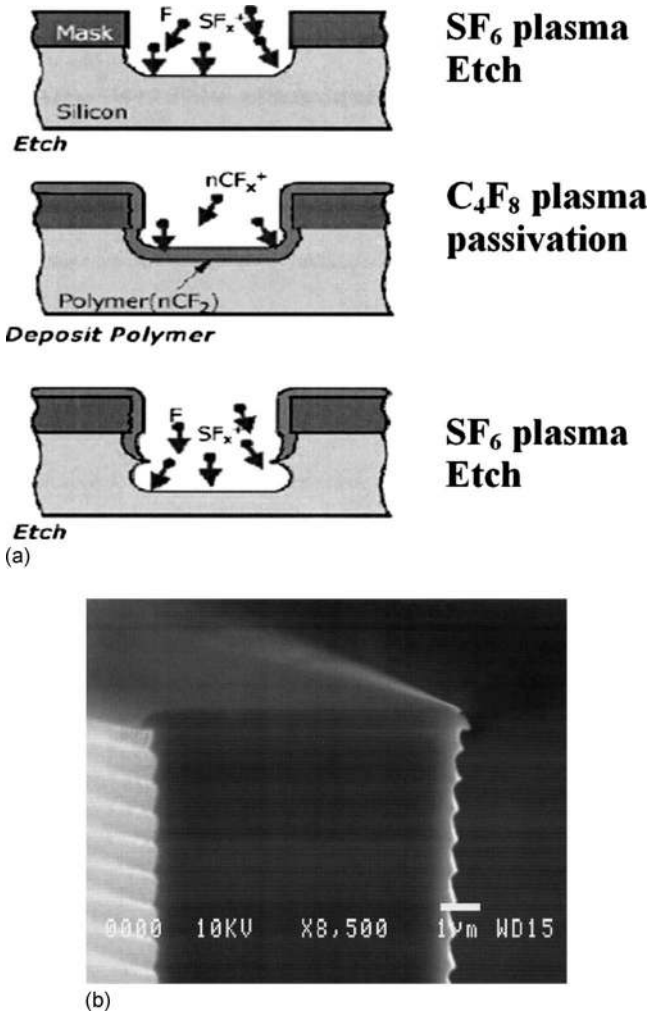


FIG. 1. (a) Illustration of two alternative DRIE processes of etching and passivation; (b) SEM micrograph of a typical scalloping pattern.

for top-down micromachining.[11–13] These hybrid solutions highlight a broad fabrication potential, where lithography-free nanostructures organized by self-assembly merge with well-established and commercially compatible top-down processing methods.

II. EXPERIMENTAL DETAILS

Dry etching of silicon wafers was carried out in an inductively coupled plasma reactive ion etching (ICP-RIE) system (Alcatel, AMS100). The coil rf power was varied from 500 to 800 W, while the platen power was set to 50 W. Alternated etching/passivation cycles with gas flows of SF_6 [250 SCCM (SCCM denotes cubic centimeter per minute at STP) and 1 s], C_4F_8 (200 SCCM and 1 s), and O_2 (100 SCCM and 0.5 s) were used with a three-step process (etching silicon, passivation, and etching the passivation layer). The substrate temperature was kept at 0 °C by means of a helium-cooled sample holder. Samples were examined by scanning electron microscopy (SEM) to investigate the relationship between etch rate and aspect ratio of the resulting structures.

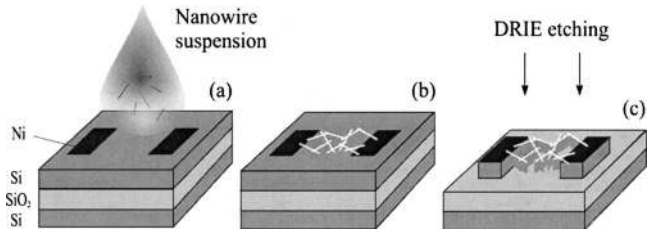


FIG. 2. Fabrication of NW networks via NWL. (a) Spin-casting of NW suspension. (b) NW masks form a network connecting the electrodes. (c) The conformal structure is etched into the SOI layer via DRIE.

Micron and submicron dot patterns were prepared using conventional photolithography and AZ5214 photoresist. e-beam lithography was used to pattern nanodot masks, with dimensions down to 50 nm. Si etching was also performed using a mask of Au or Co nanoparticles.[14,15] Two methods were used to prepare nanoparticles on silicon. The first consists of spin-coating a solution of Au colloids 20–40 nm in diameter. The second is to evaporate a patterned thin metal layer, followed by thermal annealing to form nanodots. After DRIE etching, as-prepared Au or Co particles are used to grow SiNWs (Ref. 15) or carbon nanotubes (CNTs),[16] respectively. Alternatively, oxidized SiNWs were prepared as selective masks for DRIE.[13,15,16] As-grown SiNWs were oxidized in a furnace at 1100 °C, then ultrasonically dispersed in isopropyl alcohol (IPA).[13,15,17] Ni electrodes were prepared on commercial Si structures or silicon-on-insulator (SOI) structures (100 nm Si/150 nm SiO_2/500 μm Si). The NW suspension was then spin-coated on the Si surface with a sufficiently high density to create percolation paths between the metal terminals. A conformal netlike structure was then carved into the SOI substrate to form a nanostructured film,[13] as shown schematically in Fig. 2.

Electrical measurements on SiNW networks were then taken by means of a Cascade Microtech probe station coupled to a Keithley 4200 device analyzer. The doped Si substrate acts as back-gate. Field emission measurements on Si nanopillars and CNT/Si pillars were done in a vacuum system using the sample as the cathode and a Cu sphere as the anode. The gap between cathode and anode is 200 μm, and the sample area is ~0.6 cm^2. The chamber was pumped down to 1.5×10^{-4} Pa prior to measurements.

III. RESULTS AND DISCUSSIONS

We first calibrated our DRIE etching conditions to minimize the scalloping of silicon pillars obtained with lithographically defined masks. Figure 3 shows SEM micrographs of Si pillar arrays patterned with different densities. The estimated etch rates are between 14 and 720 nm/min depending on the process conditions. Pillars ~1 μm in diameter and with heights of 30–40 μm can be fabricated to yield aspect ratios larger than 60. By using short cycle times

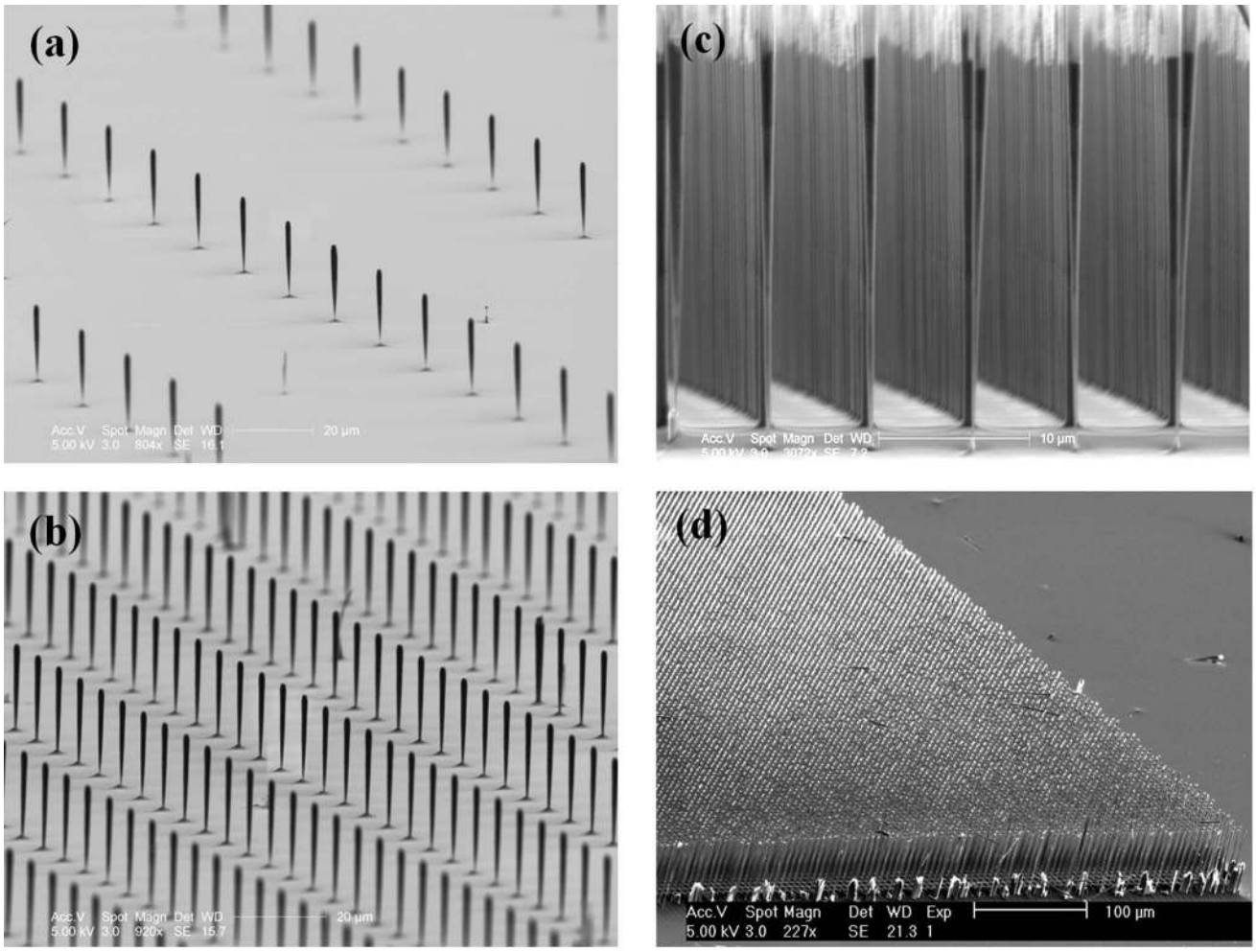


FIG. 3. Micron or submicron silicon pillar arrays with different densities using masks fabricated by UV photolithography.

(see Sec. II), the sidewall roughness can be reduced below 6 nm (peak-to-peak). By means of e-beam lithography, dots with dimensions of 50–500 nm are prepared. Using these dots as masks we produced the silicon nanopillars shown in Fig. 4. The height of these nanopillars is about 5–20 μm, thus obtaining aspect ratios of 40 and above. We observed that pillars and nanopillars tend to taper at the base, which is often thinner than the top of the structure. Yet, this effect does not weaken the stiffness and mechanical stability of the nanopillar array. Lastly, no undesired silicon grass is found on the background of all our samples.

We now combine top-down and bottom-up nanofabrications using Au both as an etching mask and as catalyst for NW growth. Figure 5(a) shows a silicon nanopillar etched by DRIE using a single Au colloid as an etch mask. Since the Au particle still remains at the nanopillar tip, it can be used to trigger the synthesis of further SiNW branches.[13] Figure 5(b) shows that individual SiNWs grown from Au particles can create bridges between etched Si nanopillars. We note that some pillars are larger than the average colloid size, with rough tips [Fig. 5(b)]. We believe that this is a consequence of colloid agglomeration during dispersion, which results eventually in a non-ideal mask geometry.

With a similar procedure, it is also possible to grow dense NW forests. In this case, patterned Au layers were used instead of colloids. After DRIE etching, a thermal annealing treatment splits the Au layer into Au nanoparticles for NW growth.[13,15] This results in thick NW forests on top of Si pillars, as shown in Fig. 6(a) and 6(b).

Following the same approach, but using Co as mask/catalyst, we demonstrate the growth of vertically aligned CNTs on silicon nanopillars. The SEM images in Fig. 7 verify the formation of large scale arrays of CNTs/Si-nanopillars. Such a geometry could be favorable for field emission applications.[18] Field emission measurements showed that a current density of 6.7 mA/cm^2, with a turn-on field of 1.82 V/μm. As expected, field emission is detected for a much lower anode voltage than for samples made only of Si pillars (see Fig. 8). One of the motivations of using nanopillars or nanotubes for field emission is the large geo-

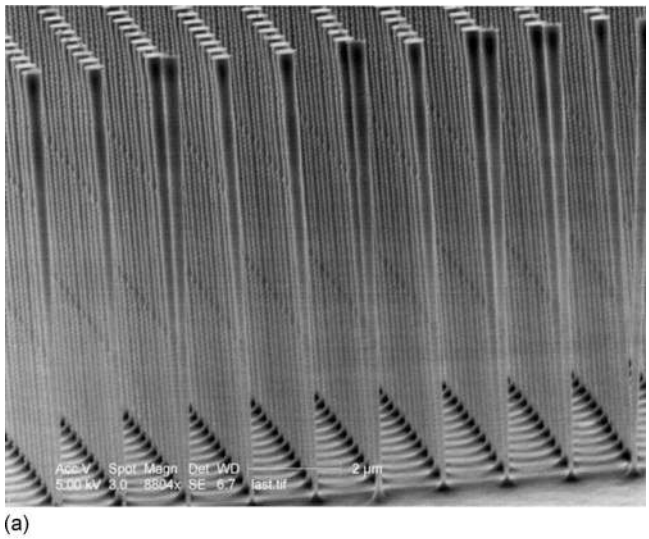


FIG. 4. Silicon nanopillars fabricated from mask patterned by e-beam lithography.

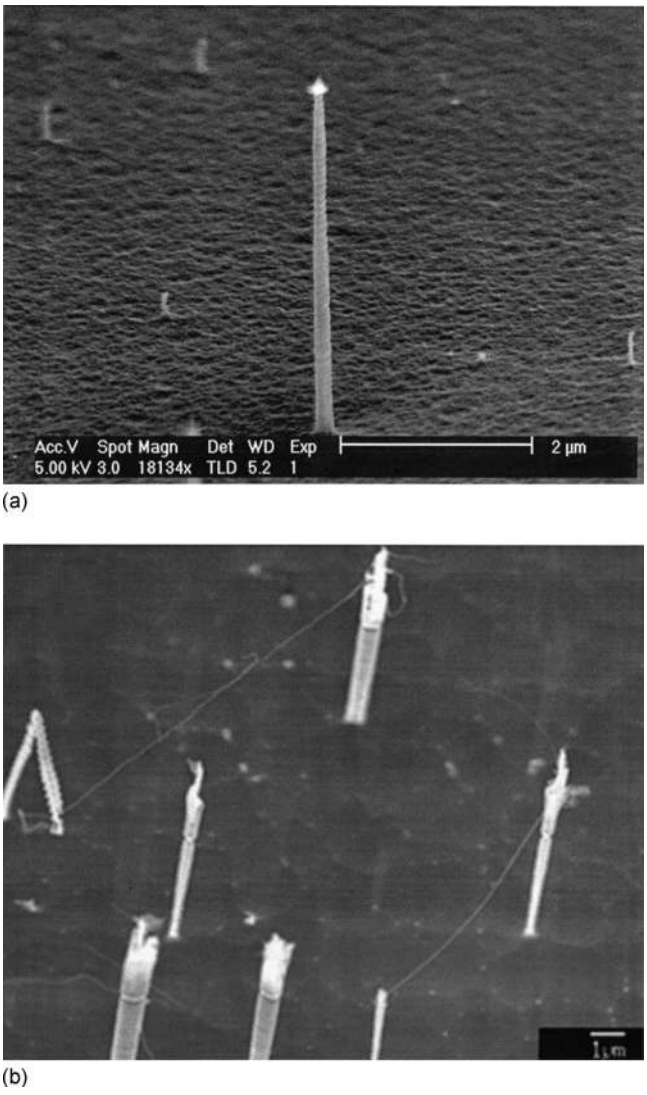
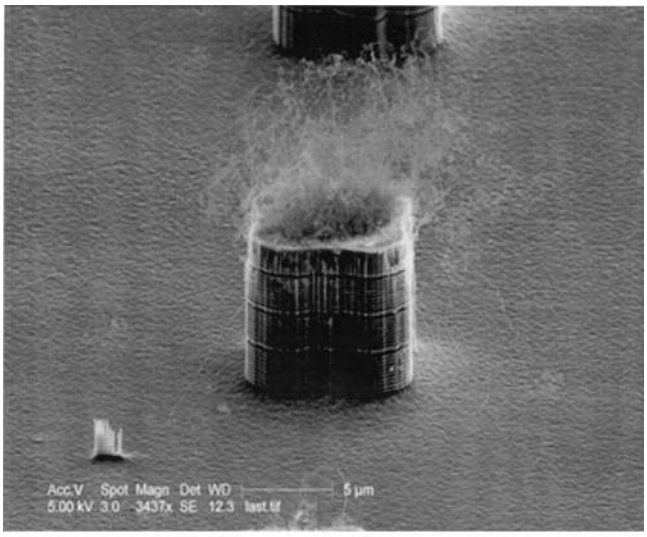


FIG. 5. (a) Individual Si nanopillar fabricated from a Au nanoparticle, still present at the top of the structure. (b) Silicon nanowires grown on Si nanopillars using the Au particle shown in (a) as the catalyst.

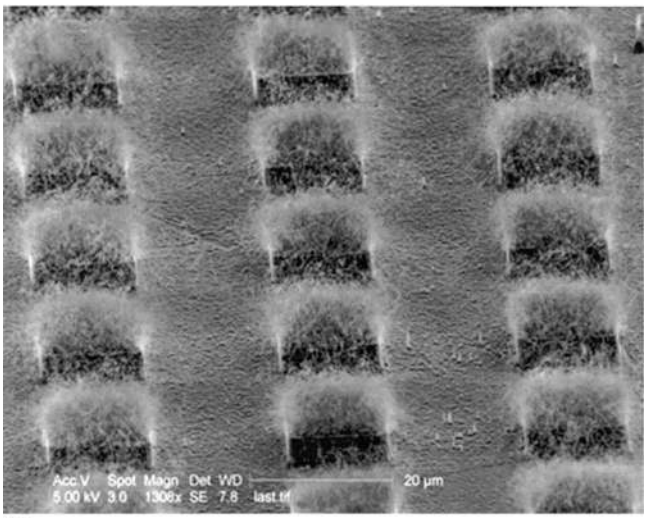
metric field enhancement factor, which can provide lower turn-on voltages.[19,20] The sample in Fig. 8 shows high current densities of tens of mA cm^{-2} and low turn-on electrical fields of a few V μm^{-1}. The good field emission performance is attributed to the morphology of our CNT/Si-nanopillars, especially the formation of a sharp and vertically aligned CNT array. These CNT/Si nanopillar arrays might be an ideal candidate cathode for potential applications in flat panel displays, which need a low-power, low-temperature, and high-current electron emitter. These nanotube coated silicon pillars could also be used as sensors, whereby the tubes could lead to a more sensitive detection of chemicals, gases, etc.

The use of chemically synthesized NWs as masks for top-down etching is called nanowire-lithography (NWL).[13,21] Figure 9(a) shows an SEM image of a typical large-area device obtained via NWL, following a similar procedure as in Ref. 13, illustrated in Fig. 2. Even with contact separations of several tens of microns, a monolithic multibranched path connecting the pads is always achieved. At higher magnifications [inset in Fig. 9(a)] we observe single-crystalline bulk junctions below the oxidized NW masks. Figure 9(b) shows a representative transfer curve for the NW device in Fig. 9(a). Given that the original SOI was not intentionally doped, the resulting SiNW network exhibits ambipolar behavior. The hysteresis observed in Fig. 9(b) and the fact that electron conduction seems to dominate is consistent with our former results for long-channel NW devices.[13] Indeed, trapping of positive charges occurs at the NW surfaces, which results in a preferential *n*-type doping of the SOI-NW channels.[13]

Finally, the flexibility of DRIE can also achieve more complex 3D nano-architectures. By introducing a controlled nanoscale scalloping, we can produce periodically modulated features and, eventually, vertical arrays of suspended

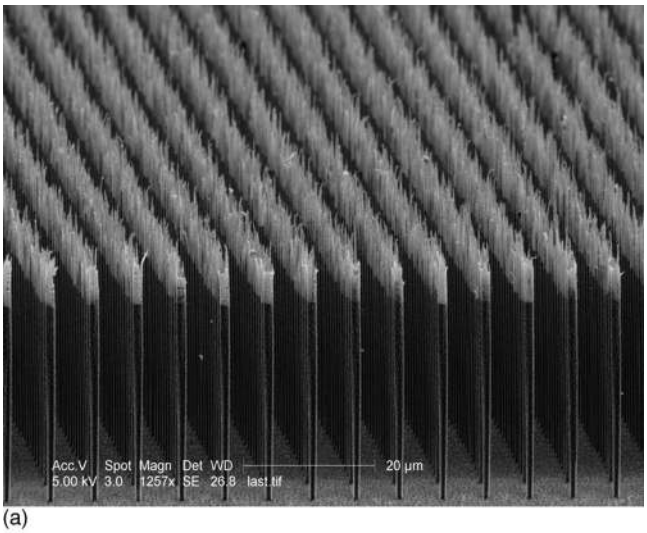


(a)

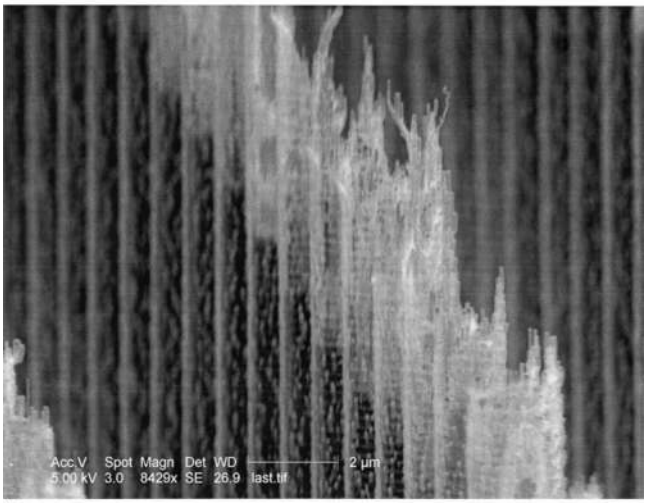


(b)

FIG. 6. (a) Forestlike silicon nanowires grown on the top of silicon pillars and (b) an array of silicon pillars with Si nanowires on top.



(a)



(b)

FIG. 7. Carbon nanotubes grown on silicon pillars: (a) on an array of Si nanopillars and (b) higher magnification showing the vertical aligned carbon nanotubes.

nanostructures.[13] Using oxidized SiNWs as masks [Fig. 10(b)], a controlled undercutting yields a sequence of vertically stacked NWs carved into the Si substrate. Their height and separation (few tens of nanometers) reflect the periodicity of the etching cycles. Such structures do not collapse if the original NW mask is clamped at one or both ends by a supporting metal pad. On the other hand, when using nanoparticles as masks, an incomplete undercutting produces nanopillars with bamboolike structure [Figs. 10(c) and 10(d)]. The constrictions forming along the column can be as small as 10–20 nm, yet the pillar remains self-supporting. These structures could be used for single-electron transport experiments through multiple quantum dots, as for chemically synthesised Si nanochains.[22] Compared to the nanochains of Ref. 22, DRIE allows to produce Si structures with well-defined doping concentrations (given by the

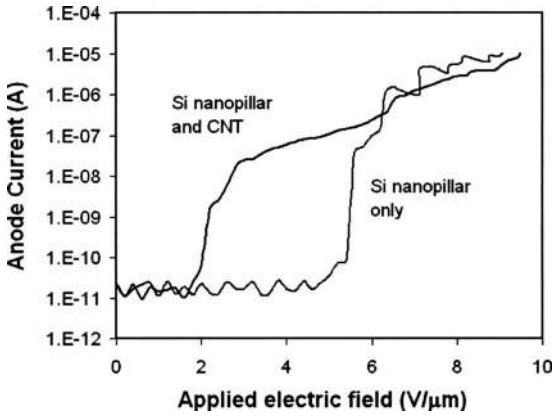


FIG. 8. Field emission test result: anode current vs applied voltage for sample of Si nanopillar and Si nanopillar/CNT.

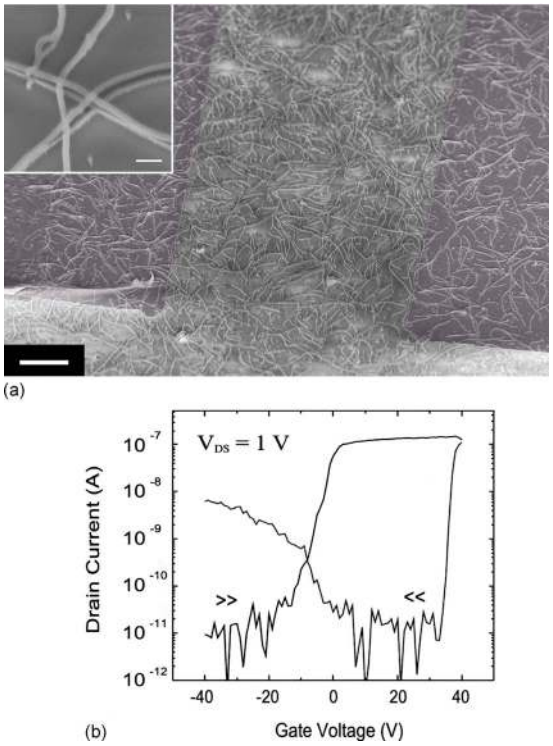


FIG. 9. (a) SEM image of a typical large-area device obtained via NWL. Scale bar: 10 μm. Inset: crystalline bulk junctions forming at the crossing points of overlapping NW masks. Scale bar: 200 nm. (b) Representative transfer curve for the NW device in (a).

original properties of the Si wafer). Alternatively, the doping could be modulated by postgrowth ion implantation.[23]

IV. CONCLUSIONS

We demonstrated the versatility of deep reactive ion etching to create a variety of Si nanostructures and architectures (including nanopillars, SiNWs/CNT on Si nanopillars, nanowalls, nanonetworks, etc.). Photolithography, e-beam lithography, nanoparticles, and NWs have also been used to prepare masks with features down to 20 nm. The use of nanoparticles as masks enables the further growth of SiNWs or CNTs by vapor-phase methods on Si pillars arrays. CNTs-on-Si nanopillars have enhanced field emission performance compared to bare Si pillars. With a thorough control over scalloping effect, nanowire lithography can produce large-area semiconductor NW films as well as vertical arrays of aligned NWs. All these results emphasize the great potential of DRIE for ultrasmall, large-area and 3D nanofabrication.

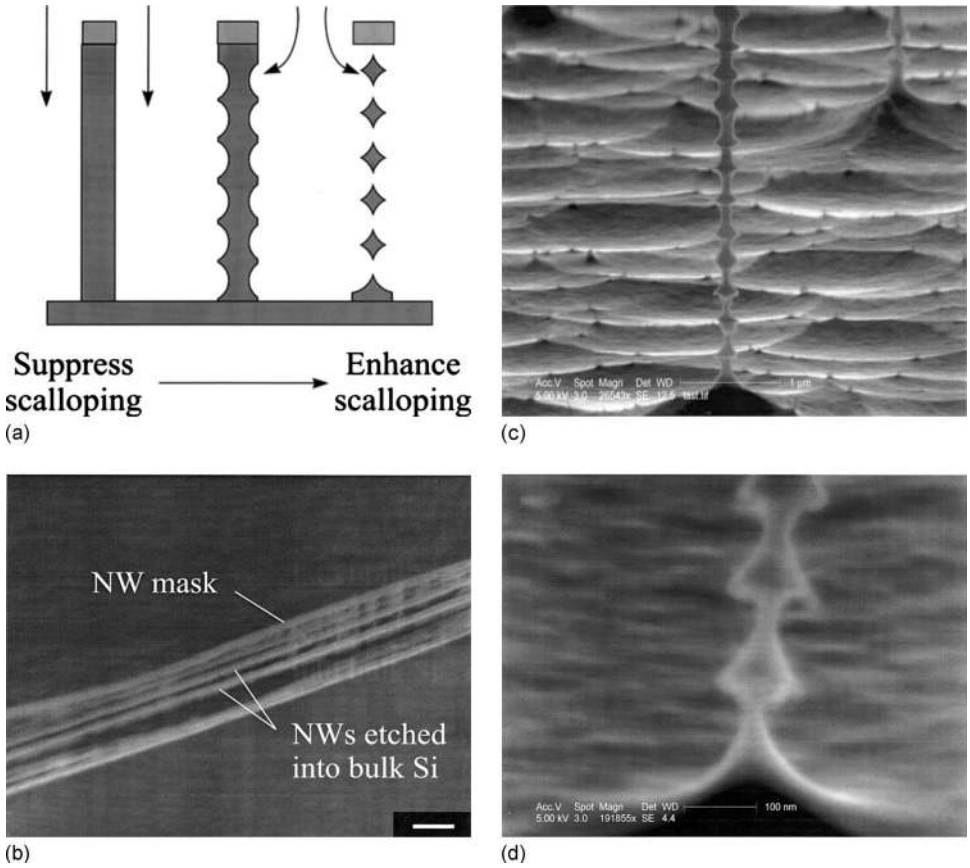


FIG. 10. (a) Illustration of fabrication of nanostructures by controlling scalloping effect; (b) SEM image of vertically stacked NW scale bar: 200 nm. [(c) and (d)] Nanopillars with bamboo structure.

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