SLAC-PUB-12924
October 2007

Deep sub-micron FD-SOI for front-end application

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Abstract

In order to confirm benefits of a deep sub-micron FD-SOI and to identify possible issues concerning front-end circuits with the FD-SOI, we have submitted a small design to Oki Electric Industry Co., Ltd. via the multi-chip project service of VDEC, the University of Tokyo. The initial test results and future plans for development are presented.

1. Introduction

The silicon-on-insulator (SOI) complementary metal–oxide-semiconductor (CMOS) process has long been employed for special uses in such areas as military and/or space instrumentations. The development of a bulk CMOS process, however, significantly advanced over the SOI CMOS, and, then, the SOI CMOS have not been widely employed in commercial use. Entering into the late 1990s, the trend curve of bulk CMOS processes has tended to be behind Moore's law, and, hence, manufacturers are eager to find a way to recover development speed. SOI CMOS is revisited to exhibit its performance over existing bulk CMOS processes; the SOI CMOS eventually shows up as a successor to the CMOS process inheriting well-matured fabrication technologies for bulk CMOS.

SOI devices are free from parasitic PNPN structure, and, hence, intrinsically immune to single event latch-ups. Moreover SOI devices are located on a very thin silicon layer, the energy deposit by an impinging particle is relatively small, and, then, it appears that we can automatically mitigate the single event upsets (SEU) and/or single-event transients (SET). The reality is that the SEU and/or SET effects are not necessarily eliminated even in an advanced SOI process [1,2] without adoption of an appropriate hardening-by-design technology.

When designing front-end circuits with a fully-depleted (FD) SOI, we can use benefits such as small floating-body effects, superior sub-threshold characteristics and small temperature coefficients as well as the common nature of SOI devices, i.e. small parasitic capacitance, low junction leakage, decrease in substrate coupling noise, and reduction

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Submitted to Nucl.Instrum.Meth.A

Work supported in part by US Department of Energy contract DE-AC02-76SF00515

of the silicon area. Compared with a partially depleted (PD) SOI, the FD-SOI employs a thinner silicon layer, and, then, the silicon layer underneath the gate electrode is completely depleted. The kink effect, which is revealed in the PD-SOI, is moderated in the FD-SOI. An improvement in the threshold slope parameter assists us in employing a low threshold-voltage (VT) transistor for an analog circuit design.

In order to confirm benefits of a deep sub-micron FD-SOI and to identify possible issues concerning front-end circuits with the FD-SOI, we have submitted a small design to Oki Electric Industry Co., Ltd. via the multi-chip project service of VDEC, the University of Tokyo, as a part of the joint effort of the SOI pixel-detector R&D program [3].

The aspect of total dose effects for the FD-SOI is reported by Ikegami et al. in an accompanying paper in this proceedings [4].

2. Circuit description

The fabrication process for our test-element-group (TEG) design is a 0.15μm FD-SOI CMOS process from Oki Electric Industry Co., Ltd., which provides a shuttle service for the 0.15 μm process, via VDEC or directly. We can use a metal–insulator–metal (MIM) capacitor with five metal layers for wiring traces. Three types of transistors are available: thick oxide transistors for I/O circuit, high VT transistors for logic circuits, and low VT transistors for analog circuits. The voltage tolerance is 1.8 V for I/O circuits, and 1 V for core circuits.

The chip size employed is 2.6 mm by 2.6 mm referring to a scribe line. The TEG chip includes four types of front-end circuits: CHAIN1, CHAIN2, CHAIN3 and CHAIN4. Each circuit is equipped with a preamplifier circuit, test pulse circuit and multiplexed analog monitor output. Discriminator circuits accompany CHAIN2, CHAIN3 and CHAIN4.

Since it was observed that the $I-V$ characteristics behaved better for a body-tie transistor than for a body-float transistor as shown in Fig. 1, the body-node was connected to the source-node for all transistors employed.

The amplification element employed in the preamplifier circuit is depicted in Fig. 2. The input signal, AIN, is fed into a common source nMOS transistor. The size of the transistor is $W/L = 5/0.5$ with $M = 360$. $W = 5$ μm comes from the design rule for a body-tie transistor. The drain current of the input transistor is adjustable over a range of 100−500 μA. The trans-conductance for the drain current of 500 μA is about 10 mS. A gain-boost scheme is employed for the cascode transistor. Two outputs, AOUT and CAS, are provided: AOUT is with a source follower, and CAS is without a source follower. By employing a relatively large, and multi-fingered input transistor, we try to identify the gate-edge leakage current due to radiation, which still exists even in an advanced SOI process unless a special hardening-by-design technology is taken.

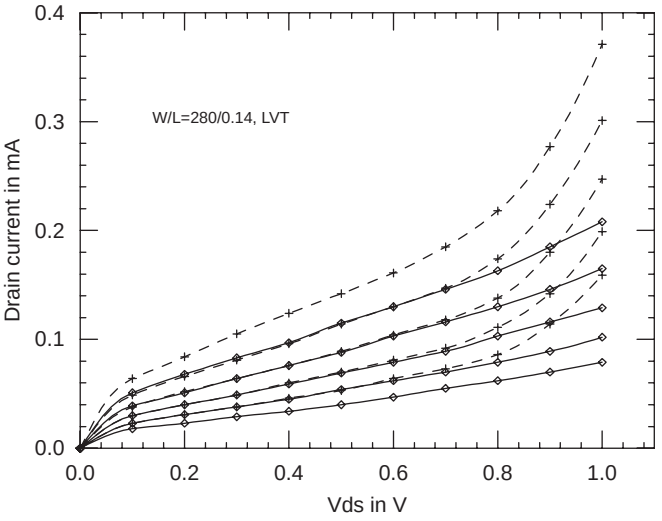

Fig. 1. $I-V$ characteristics for a low VT nMOS transistor with $W/L = 280/0.14$. The curves are for $V_{gs} = 0.2$, 0.21, 0.22, 0.23 and 0.24 V. The dotted lines are for a body-float transistor, and the solid lines for a body-tie transistor.

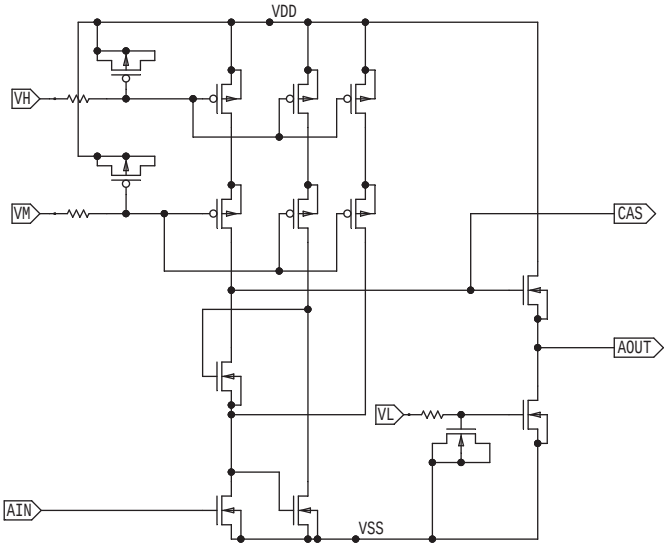

Fig. 2. Schematic of the amplification element.

CHAIN1 is accompanied by a trans-conductor circuit as shown in Fig. 3 together with a feedback capacitor of 0.1 pF. CHAIN1 has a configuration traditionally employed for a radiation detector readout. CHAIN1 can be operated with either a small current in the order of 1 nA or a larger current in the order of 100 nA, but with a short decay time. Fig. 4 shows the waveform of CHAIN1 for operations with a small current (1 nA).

CHAIN2 is accompanied by a circuit as shown in Fig. 5 with a feedback capacitor of 0.04 pF. CHAIN2 provides a time-over-threshold (TOT) scheme that enables an A-to-D conversion at the side of a front-end chip and is compatible with a low V_{DD} voltage. The circuit works properly only with a positive charge input. The feedback element of these

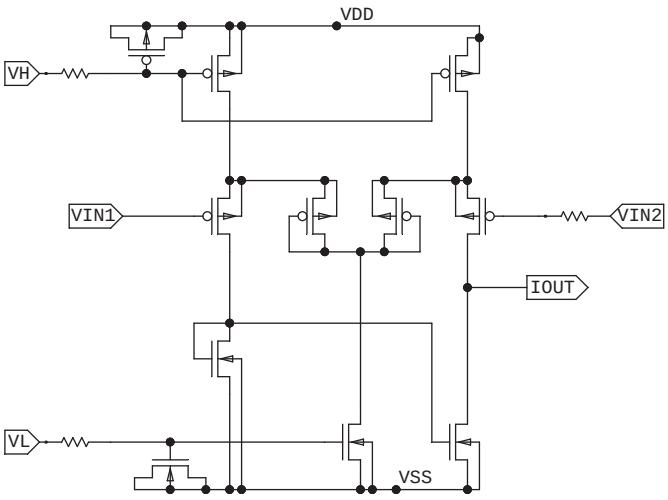

Fig. 3. Schematic of the feedback element for CHAIN1.

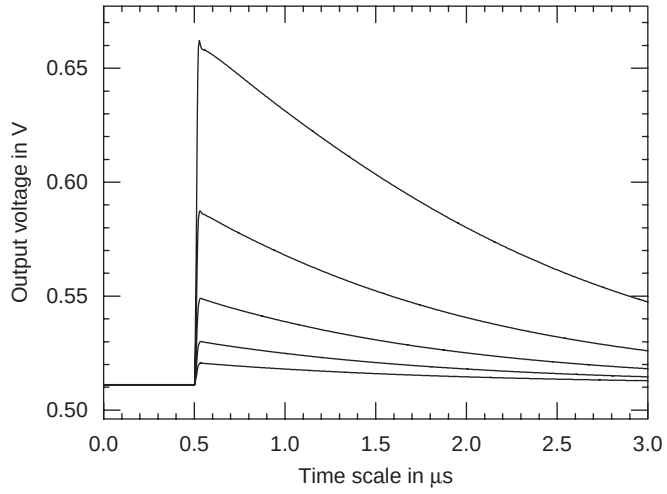

Fig. 4. Waveform for a slow tail operation of CHAIN1. The feedback circuit is operated with a bias current of 1 nA. The curves are for input charges of 16, 8, 4, 2 and 1 fC. An additional capacitance of 10 pF is attached at the input node.

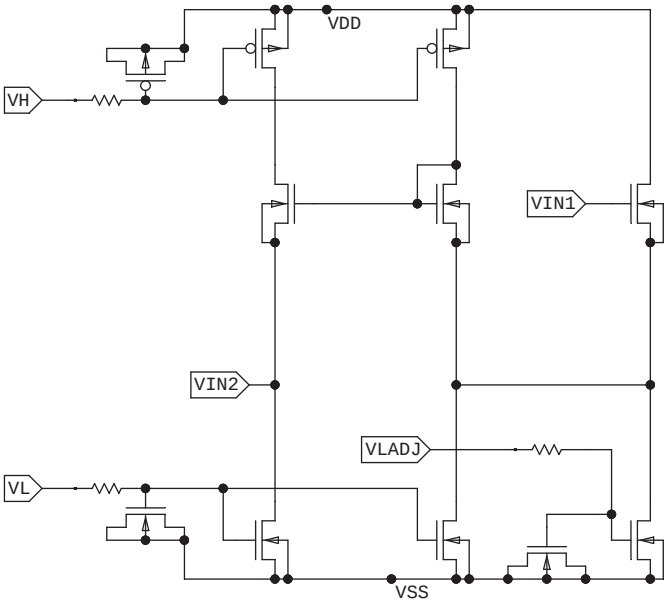

Fig. 5. Schematic of the feedback element for CHAIN2.

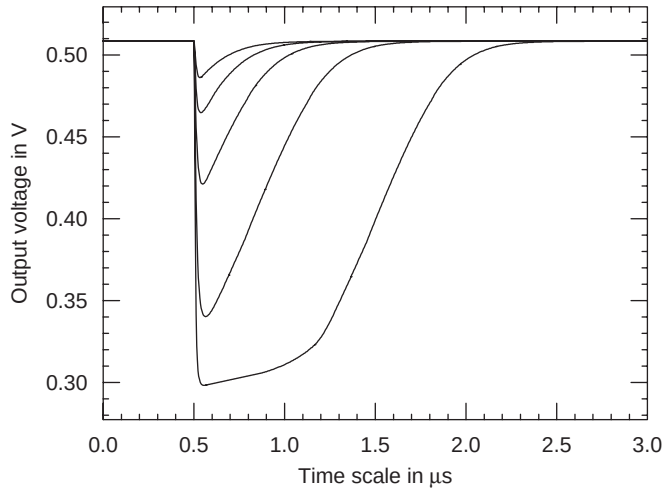

Fig. 6. Waveform of CHAIN2. The feedback circuit is operated with a bias current of 5 nA. The curves are for input charges of 16, 8, 4, 2 and 1 fC. An additional capacitance of 10 pF is attached at the input node.

circuits is operated with a very small current in the order of 5 nA, and is vulnerable to a leakage current of the constant current source. Fig. 6 shows the waveform of CHAIN2 for an operation with a bias current of 5 nA for the feedback circuit.

CHAIN3 is accompanied by a circuit as shown in Fig. 7 with a feedback capacitor of 0.04 pF. The feedback element has just a minor modification from that of CHAIN2 to employ a capacitor of 0.04 pF for the mirror part of the feedback circuit, which introduces a small overshoot before settling to a base line, and, hence, helps operation of the discriminator circuit located downstream.

CHAIN4 is accompanied by a circuit as shown in Fig. 8. CHAIN4 works as a trans-impedance amplifier [5] and is compatible with a high flux environment. Fig. 9 shows the waveform of CHAIN4 for an operation with a bias current of 100 nA for the feedback circuit. The feedback circuit for CHAIN4 is operated with a relatively larger current to be robust against the leakage current.

3. Circuit evaluation

At the first step of the circuit evaluation it turned out that the electro-static-discharge (ESD) protection circuit was leaky, and the preamplifier became saturated. We identified that the ESD circuit was fabricated with a thin oxide transistor. Nominal value of the leakage current of the low VT transistor is 10 nA/μm, which can kill the preamplifier circuit. In order to reduce the leakage current of the ESD transistor, we raised the V_{SS} power rail of the

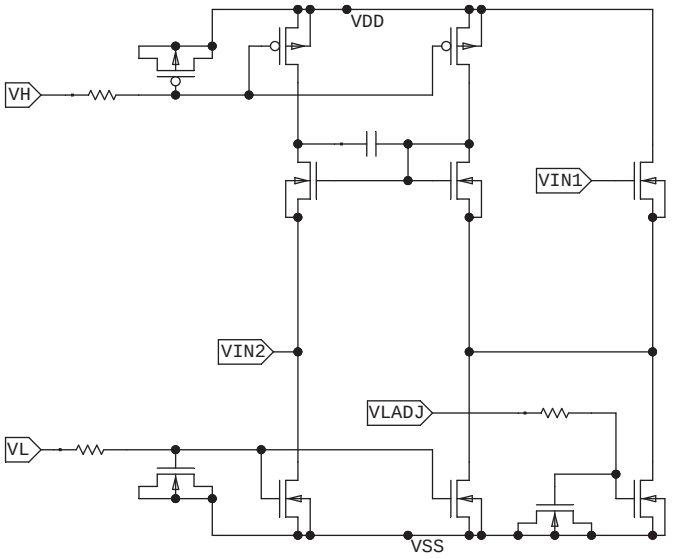

Fig. 7. Schematic of the feedback element for CHAIN3.

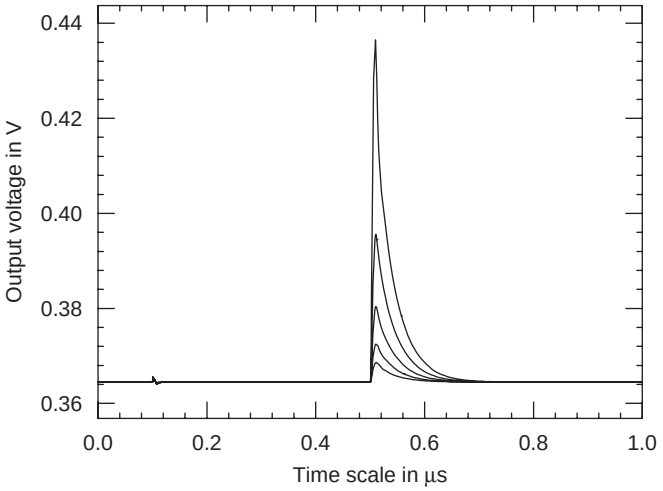

Fig. 9. Waveform of CHAIN4 for negative charge. The feedback circuit is operated with a bias current of 100 nA. The curves are for input charges (negative) of 16, 8, 4, 2 and 1 fC. An additional capacitance of 10 pF is attached at the input node.

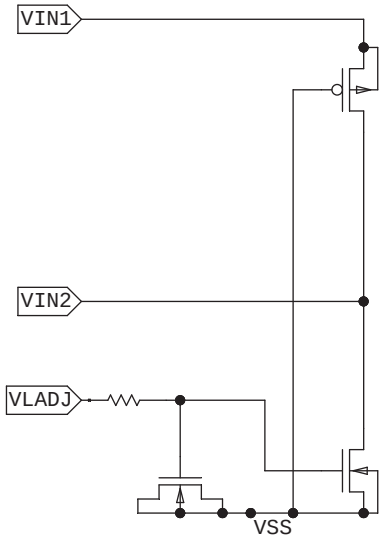

Fig. 8. Schematic of the feedback element for CHAIN4.

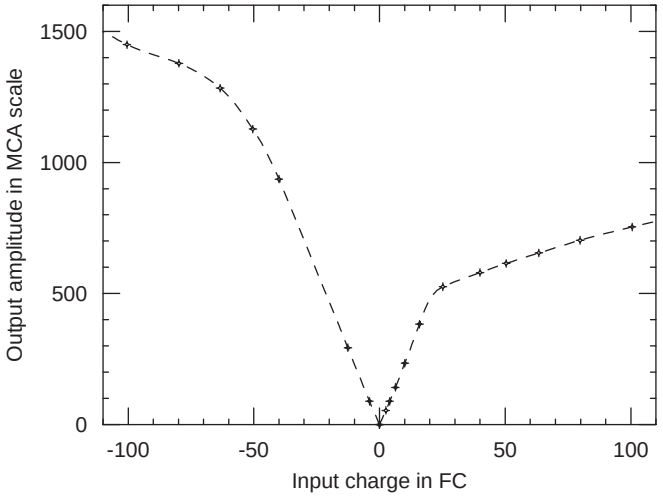

Fig. 10. Response of CHAIN1. The peaking time employed is 500 ns. The vertical scale comes from the channel number of the MCA employed. Actual voltage swings are positive for negative charge inputs, and negative for positive charge inputs.

ESD transistors, and, then, the preamplifier circuit was recovered.

Fig. 10 shows the response of CHAIN1 circuit chain. CHAIN1 shows a good linearity for the input charge of 20 to −50 fC; the voltage swings were −200 mV, and 500 mV, respectively. In order to characterize the performance, we employed an external shaping amplifier, Ortec 571, and a multi-channel analyzer (MCA). The decay time constant of the preamplifier could be slowed down to 20 μs, but was limited by a leakage current of the feedback circuit.

The upper three lines in Fig. 11 show the equivalent noise charge in terms of peaking time for an original design. The noise level at the peaking time of 500 ns was 800–900 electrons, and increased monotonically for 1, 2 and 3 μs of the peaking time. The tendency was little affected by the drain current of the input FET of the preamplifier. This behavior is understood as coming from the leakage current of the ESD transistors located at the input node of the preamplifier.

We quickly submitted a revised design with thick oxide ESD transistors in place of the leaky transistors. Then the electronic noise charge went down to 400 electrons or less with the peaking time of 500 ns as drawn by the solid line in Fig. 11.

The dot-dash line in Fig. 12 shows the equivalent noise charge for the original design in terms of external capacitance attached at the input node of the preamplifier. The excess noise for low capacitance region is understood as coming from the leakage current of the ESD transistors.

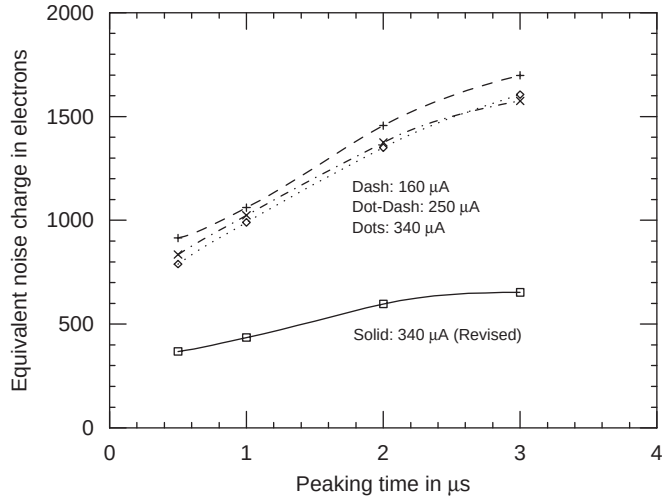

Fig. 11. Equivalent noise charge of CHAIN1 in terms of peaking time. The dash, dot-dash, and dotted lines are for the original design with the drain currents for the input FET 160, 250 and 340 μA, respectively; the solid line for the revised design with the drain current for the input FET 340 μA.

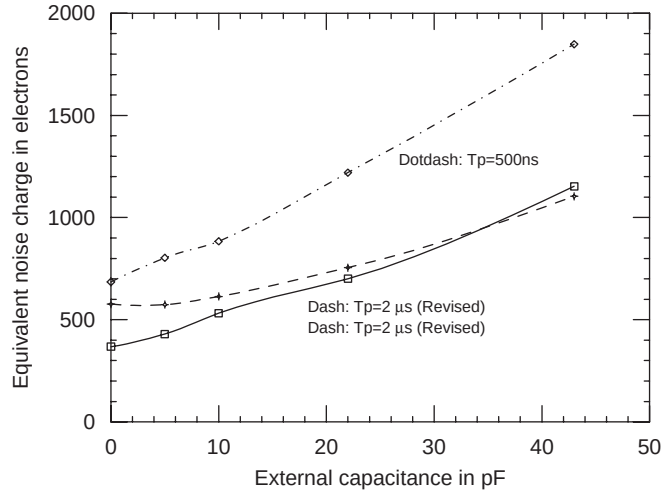

Fig. 12. Equivalent noise charge of CHAIN1 in terms of external capacitance. The drain current of the input FET is 340 μA. The dot-dash line is for the original design with the peaking time of 500 ns; the dash and solid lines are for the revised design with the peaking time of 2 μs and 500 ns.

The noise level for high capacitance region was apparently larger than that predicted by a SPICE simulation. The noise level was slightly affected by the grounding scheme.

In addition to the leakage current of the ESD transistor, an additional noise source was identified for the original design. In the final circuit design, we attached an RC filter at the gate node (VH) of the current source transistor without evaluating the impact on the noise performance. By eliminating the series resistor, 10 kΩ, located at the gate node (VH), we confirmed in the revised design that the overall noise level was drastically reduced, as shown by the two lower lines in Fig. 12. The noise contribution of the 50 Ω resistor series to the input node of the preamplifier is still minor compared to the above mentioned noise source.

4. Summary

Deep sub-micron CMOS processes have been widely employed for high-energy physics, astrophysics, and other uses. To go beyond existing technologies in analog circuit design, we initiated a design using an FD SOI process from Oki Electric Industry Co., Ltd. We submitted a TEG design to identify compatibility with the design practices accumulated for a deep sub-micron CMOS, and the need to incorporate technologies explored in other research fields. The first TEG design together with its revision was evaluated to reveal that the front-end circuit with the FD-SOI was promising for a front-end application. There still remain unexplored area, such as quantitative parameter extraction of the $1/f$ noise, radiation hardness assurance with employment of H-gate transistors, and/or handle-wafer biasing.

Acknowledgments

The SOI chip in this study has been fabricated in the chip fabrication program of the VLSI Design and Education Center(VDEC), the University of Tokyo, in collaboration with Oki Electric Industry Co., Ltd.

References

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