Deep Sub-micron I_{DDQ} Testing: Issues and Solutions

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Abstract

The effectiveness of I_{DDQ} testing in deep sub-micron is threatened by the increased transistor sub-threshold leakage current. In this article, we survey possible solutions and propose a deep sub-micron I_{DDQ} test mode. The methodology provides means for unambiguous measurements of I_{DDQ} components and defect diagnosis. The effectiveness of the test mode is demonstrated with a real life example.

1 Introduction

Static CMOS circuits have very low quiescent current or I_{DDQ}. Most of the manufacturing defects in CMOS ICs, exhibit state dependent elevated I_{DDQ}. Therefore, I_{DDQ} testing is a powerful test method for manufacturing process defects detection. The effectiveness of an I_{DDQ} based test method is incomparable in quality improvement, test complexity and test cost reduction [1].

However, one of the critical requirements of I_{DDQ} testing is the accurate measurement of an extremely small current at the VDD or VSS terminal of the Device Under Test (DUT). Typically, the I_{DDQ} threshold for the pass/fail decision making is set between 1-10 μ A. For an unambiguous decision making, the defect-free I_{DDQ} of the DUT should be at least an order of magnitude lower than the set I_{DDQ} threshold. A rigorous design style need to be followed so that there are no high quiescent current states in the design. Alternatively, I_{DDQ} test vectors must be selected carefully such that high I_{DDQ} states do not invalidate the test. I_{DDQ} testing is a total observability test method. Hence, in general, the satisfaction of controllability condition is sufficient for defect detection.

2 Deep Sub-micron Issues & I_{DDQ} Testing

The defect-free I_{DDQ} has two major components [2]: (i) the reverse biased p-n junction leakage current, and (ii) the transistor sub-threshold leakage (off) current. The reverse biased p-n junction leakage current can be further divided into two segments: state dependent (I_g), and state independent (I_{gw}). The state dependent component *p-n* junction leakage current depends on the reverse biasing of the *p-n* junctions (e.g. transistor source/drain-substrate leakage). The state independent leakage current is due to the reverse biased wells/substrate diode.

The reverse biased p-n junction current may be computed with a reasonable accuracy using formulae described in [3]. Maly et al. [2] utilized these formulae to compute both the components of this current. The state dependent junction leakage current density for junction depth, X_j , of 0.5 micron was 10^{-13} A/u^2. The state independent leakage current density was also calculated to be similar in magnitude. In simple words, the contribution of these components towards defect-free I_{DDQ} current is fairly small and is expected to remain so for future generations of CMOS technology.

2.1 Transistor Sub-threshold Leakage Current

The problem of diagnostics and the pass/fail decision making with I_{DDQ} testing will become increasingly difficult as the feature size and supply voltage are reduced in the deep sub-micron region. These factors will result in increased transistor sub-threshold leakage currents [4,5,6]. The off current of minimum sized devices is expected to increase at least by a factor of 100 as the feature size is reduced from 0.5 micron to 0.1 micron [7,8]. The off current for an enhancement mode transistor is defined as the leakage current when V_{GS}=0. The increase in transistor off current with ULSI complexity will have a significant impact on the future of I_{DDQ} testing.

The simplified MOS theory assumes a zero drain current for $V_{GS} < V_T$. In fact I_{DS} does not drop abruptly but decreases exponentially, similar to the operation of a bipolar transistor. The leakage current is given by minority carriers and diffusion currents in the non-inverted MOS transistor. In the sub-threshold region, the inverse rate of decrease of I_{DS} in Volts per decade, S, is given by [9,10]:

$$S = \left[\frac{d(\log I_{DS})}{dV_{GS}}\right]^{-1} = \left(\frac{k_B T}{q}\right)\ln 10 \bullet \left(1 + \frac{C_D}{C_{gox}}\right) \quad \text{(EQ 1)}$$

Where C_D is the depletion layer capacitance. Source (n+), bulk (p^-), and drain (n^+) terminals of the NMOS transistor form an *npn* bipolar device. The base of this *npn* transistor is capacitively coupled to the gate terminal and as a result only a portion of the gate voltage variation is reflected to the base. The capacitive divider formed by C_D and C_{gox} (Fig. 1) determines how much of the gate voltage swing is seen by the bipolar base [9]. The rest of the equation is a

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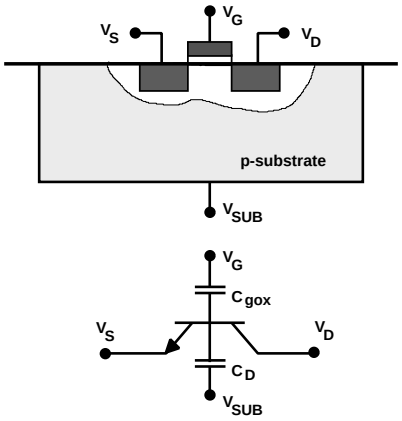


Fig. 1: Cross section and equivalent circuit of an NMOS transistor in sub-threshold region.

different representation of the familiar bipolar current equation. In digital circuits when the transistor is off, V_{gate} and $V_{substrate}$ have the same value, hence the capacitive divider is effectively removed from the EQ. 1.

For a typical CMOS process S is about 80 mV/decade. As the CMOS processes are scaled to the deep sub-micron region, the device reliability and low power constraints enforce a reduction in power supply voltage [7,8] which in turn necessitates lower transistor threshold voltages. For a lower threshold voltage the off current increases. For example, if the threshold voltage of n-channel transistor is reduced from 0.6V to 0.3V, effectively its off current is increased by a factor of $10^{3.75}$ $\{[600-300]/80\}$.

2.2 Solutions for Sub-threshold Leakage

Exponential increase in transistor sub-threshold current with linear decrease in threshold voltage is a cause of grave concern for ULSI devices. An uncontrolled increase in stand-by power defeats the fundamental motivation of scaling, i.e. speed, low power consumption, system reliability, etc. Therefore, there have been many solutions proposed to reduce the stand-by power dissipation [4,5,11-20]. Although these techniques do not change the fundamental problem of sub-threshold leakage, however, they are fairly effective in containing the sub-threshold leakage current to a more acceptable level. These solutions may be summarised as follows:

(a) Technology solution: Silicon On Insulator (SOI) is a promising technology for high speed, high density, low power ICs [8,11,12]. The performance improvement is primarily due the reduced parasitics while a sharper sub-threshold current slope (S<60 mV/decade) makes it attractive for low power applications [8]. For a threshold voltage of 0.3V, SOI offers a reduction of more than an order of magnitude in sub-threshold leakage current compared to bulk CMOS technologies.

Although an order or two reduction in sub-threshold current may not be enough for effective I_{DDQ} testing, SOI along with some design solutions proposed in following subsection could restore the effectiveness of I_{DDQ} testing for deep sub-micron devices.

(b) Design solutions: Application of reverse (back) bias is a popular method to control sub-threshold leakage current in MOS transistors. It was first reported in 1976 to control the threshold voltage [13]. Using two different external voltages the threshold voltage (V_T) of transistors was controlled to a desired value. However, in the same way, the threshold voltage may be increased to reduce the sub-threshold leakage. Since then, many improvisations [14-20] have been made over the basic idea.

Burr et al. [14,15] used transistor threshold voltage close to 0V by eliminating the threshold implant mask. They subsequently used reverse bias to increase the threshold voltage to a desired value. In this manner, they realized an optimum power-delay product for a given circuit.

Sakata et al. [16] proposed sub-threshold current reduction circuits for Multi-Gbit DRAMs. They proposed the hierarchical power line scheme for wordline decoder circuit and sense amplifier driving circuit. The salient feature of the scheme was to utilise decoded address inputs to connect the selected part of the circuit with the VDD. In this way, active as well as stand-by current for a conceptual 16 Gbit DRAMs was reduced. The active current was reduced from 1.2 A to 116 mA. In another paper, the same authors proposed a more generalised scheme to reduce the sub-threshold current for Giga-scale CMOS circuits [17]. The basic idea is to use a switched-source-impedance to reduce the sub-threshold current by 3-4 decades with minimum speed penalty in active mode. The logic transistors were implemented with low V_T s. In order to reduce the sub-threshold leakage common wide transistor(s) with high V_T are introduced between sources of logic transistors and VDD (VSS). The effectiveness of this method was demonstrated with computations over a 16 Gbit DRAM. The sub-threshold current was reduced to 0.3% of the original value. However, the application of this technique resulted in a speed penalty which authors argued can be compensated with increased transistor widths. Somewhat similar ideas were proposed by Takashima et al. [18] to reduce I(leak) to 1 μ A for Sub-1 V operation of 1 G/4 G bit DRAMs.

Mutoh et al. [19] proposed the use of multi-threshold CMOS (MT-CMOS) to reduce power consumption. The technology contained P and N transistors with high as well as low threshold voltage. Logic transistors were implemented with low threshold voltages for high speed operation. The high threshold transistors are introduced between

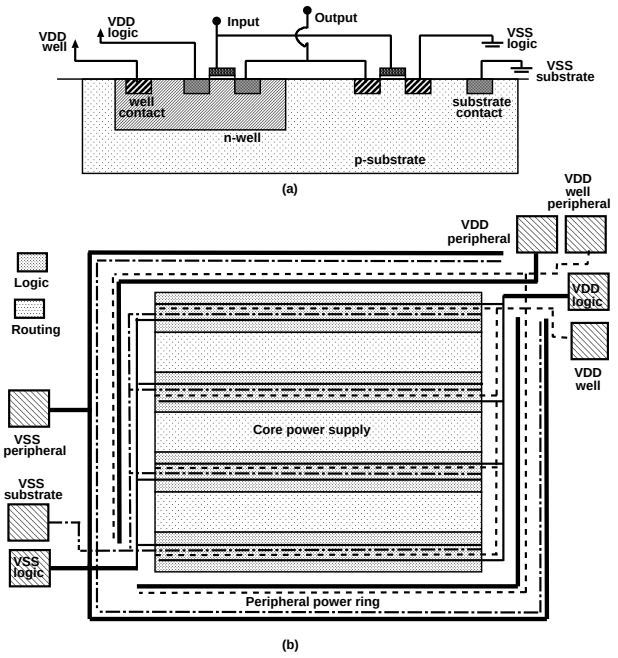


Fig. 2: Separate VDD and VSS supplies for signal and bias paths.

sources and VDD (VSS) such that in the sleep mode power consumption is reduced significantly. However, it should be noted that multi-threshold logic and hierarchical power distribution schemes, etc. do not enhance the effectiveness of I_{DDQ} testing substantially since these techniques cut off a substantial part of the circuit from power supply in the quiescent mode.

Reverse biasing techniques are widely used in DRAMs to reduce the transistor sub-threshold leakage. Almost all of the DRAMs rely on charge pumps for this purpose [20]. Kobayashi and Sakurai [21] proposed a circuit technique to adjust the threshold voltage on the fly. The circuit included a leakage sensor and a self substrate bias circuit to contain the leakage current to a pre-determined value.

3 Deep Sub-micron I_{DDQ} test mode

Most of the design solutions have been optimized for RAMs. RAMs have a very well defined architecture which is cleverly exploited in these solutions to keep the leakage currents down. In the case of digital circuits achieving the same requires a careful analysis of all the operating modes in the circuit. Furthermore, although some of these solutions may be applied on purely digital circuits, the impact on performance is more significant.

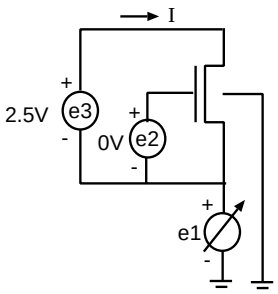
Therefore from the test point of view, it is most natural to create a test mode in which effective deep sub-micron I_{DDQ} test is carried out with its full potential. Depending upon the outcome of the test, subsequently the device is put back into the normal mode to exploit its full parametric functionality. In this way, the impact of the test on VLSI's performance is negligible. This objective is achieved by separating the source and substrate (well) contacts in the test mode [4,5]. This separation allows us to selectively apply substrate bias to reduce sub-threshold leakage currents.The basic idea behind this strategy is illustrated with the help of Fig. 2. In Fig. 2(a) the VDD (and VSS) is split into VDD_{logic} (VSS_{logic}) and VDD_{well} ($VSS_{substrate}$) respectively. Such a segregation allows us to measure different I_{DDQ} components individually and unambiguously. Fig. 2(b) shows the chip level implementation of the concept. The peripheral power supply bus is also split. Owing to the fact that in n-well process, all the NMOS transistors have a common substrate, therefore, substrate connections of peripheral NMOS transistors are connected to $VSS_{substrate}$ only. On the other hand, PMOS transistors are being in n-well have the freedom that their well contact can be connected either to $VDD_{peripheral}$ or to $VDD_{well\text{-}peripheral}$. In the former case, the peripheral VDD is not split, and in the latter case, it is split. In Fig. 2(b) we have illustrated a general case and hence split the peripheral VDD as well.

This work is an extension of our previously reported work. In [4,5] we have outlined a deep sub-micron I_{DDQ} test strategy. In this article, the above mentioned strategy is applied on a simple CMOS shift register circuit to demonstrate its effectiveness and to compute various I_{DDQ} components for a sub-micron CMOS process. The reverse bias in well and substrate is utilised to reduce the sub-threshold current for effective I_{DDQ} testing. Furthermore, we quantify the impact of separate source and substrate power supplies on performance and area.

EQ. 2 illustrates the relationship between substrate bias and transistor threshold shift [10].

$$\Delta V_T = V_T(V_{BS}) - V_T(V_{BS} = 0)$$
$$= K\{\sqrt{2\psi_B + V_{BS}} - \sqrt{2\Psi_B}\} \qquad \textbf{(EQ 2)}$$

Where K is the body effect coefficient, ψ_B is the potential difference between fermi level and intrinsic fermi level for a given process. V_{BS} is the substrate (bulk) to source voltage. For a typical deep sub-micron process the body effect coefficient is 0.59 $V^{1/2}$ and $2\psi_B$ has an approximate value of 0.8 V [19]. For these numbers, an application of 1.2 V reverse bias increases the V_T by 310 mV. In other words, the sub-threshold current is reduced approximately by 10^4.



Sub-bias (mV)	I_D (V_T=0.67) (fA)	I_D (V_T=0.47) (pA)
0	261.53	64.99
100	84.54	22.16
200	32.66	8.10
300	16.10	3.10
400	10.58	1.25

Fig. 3: Simulation of sub-threshold slope for an NMOS transistor.

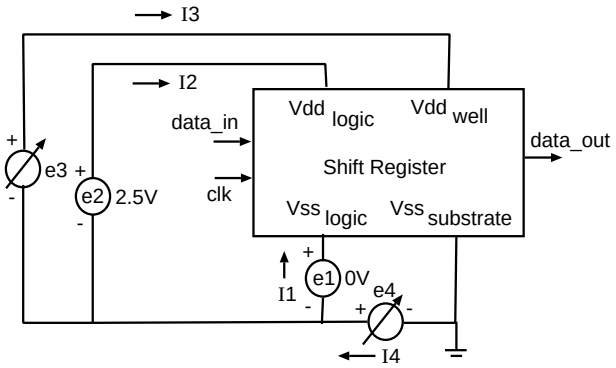


Fig. 4: Circuit simulation of the shift register.

4 Experimental Demonstration

A typical deep sub-micron process has 0.25 micron linewidth with 1.5 V power supply. A typical V_T for such a process ranges from VDD/4 to VDD/6 [6]. However, deep sub-micron VLSI process for mass production are not common yet. Therefore, it becomes difficult to simulate the deep sub-micron phenomena with a circuit simulator (e.g. SPICE) for a realistic process. In particular, to see the appreciable effect of reverse biasing on sub-threshold leakage current, the V_T should be equal to or lower than 0.50 V. For a transistor with higher V_T the off current is already in the range of fA range. Moreover, a basic transistor model does not contain source/substrate and drain substrate diodes. Therefore, care should be taken to select a proper transistor model to simulate various leakage currents. In addition, for a n-well CMOS process, a PMOS transistor model should also include a well/substrate diode. All simulations were carried out with MOS Model 9 transistor model which is capable of modeling transistor sub-threshold behavior [22]. Simulations were carried out on a 0.5 micron CMOS process which has the typical V_T of approximately 0.67 (0.71) V for NMOS (PMOS) transistors. For all simulations the supply voltage was kept at 2.5 V. In order to mimic a more realistic simulation of sub-threshold current for a deep sub-micron process, the transistor model was modified and V_Ts were reduced to 0.47 (0.51) V for NMOS (PMOS) transistor. A more aggressive scaling of V_T was not considered because a drastic change in V_T may cause poor accuracy of the model.

For a typically sized NMOS transistor, the I_D was simulated for different substrate bias conditions. These simulations were conducted with original as well as modified threshold voltages. Fig. 3 illustrates the simulation setup and resultant I_D values. The first column of the table depicts the applied substrate bias, and second, and third columns show I_D under different V_T s. The sub-threshold slope, S, was calculated as 86 mV/decade for original V_T and as 73 mV/decade for modified V_T.

4.1 Simulation of I_{DDQ} Components

A simple CMOS circuit is sufficient to demonstrate the effectiveness of the proposed method. Therefore, a 10-Bit shift register was designed with separate power supplies for this experiment. No particular effort was made to optimize its performance, power consumption, etc. The transistor sizes were chosen to be representative of the technology. The shift register contained approximately 200 transistors.

The shift register was simulated with modified V_T . Fig. 4 illustrates the basic scheme of simulations. Two initial I_{DDQ} simulations were carried out with (i) all inputs low, and (ii) all inputs high, respectively. Voltage sources e2 and e3 both were kept at 2.5V, and voltages sources e1 and e4 had 0V across them. The combined sub-threshold leakage current, I2, was simulated to be 484 pA and 494 pA, respectively for described input conditions. The I3 was simulated to be 2.87 pA.

4.1.1 State Independent Junction Leakage (I_{gw})

Single simulation was needed to measure I_{gw} component. A detailed description of this and other simulation setup is given in [4,5]. However, Fig. 5 illustrates the salient points of the simulations. The figure shows an equivalent circuit of the shift register for these simulations. In this first simulation (Fig. 5(a)) VDD_{logic} was shorted to VSS_{logic} (e1=e2=0 V). VDD_{well} was biased at full VDD potential (2.5 V) and $VSS_{substrate}$ was grounded. Furthermore, no substrate bias was applied to NMOS transistors (e4=0 V) and all inputs were also kept low. Such conditions ensures that sub-threshold leakage current is negligibly small. Now, the current drawn from voltage source e4 will be state independent junction leakage current (I_{gw}). This was measured as 2.62 pA. Similarly, current drawn from voltage source e3 will be equal to the sum of I_{gw} as well as leakage current between n-well contacts and p+ sources (I_{np}). Therefore,

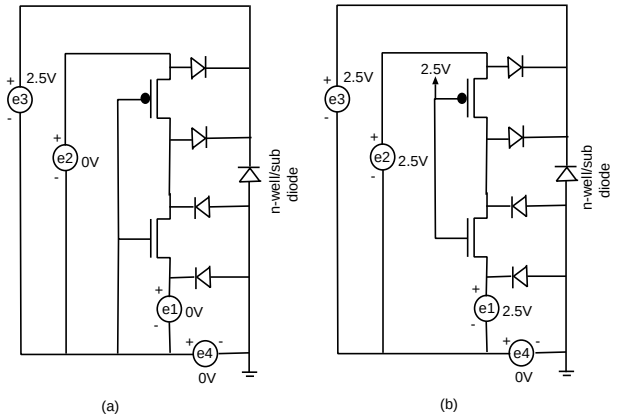


Fig. 5: Simulation of junction leakage current.

$$I_{np} = I(e3) - I(e4) \quad \textbf{(EQ 3)}$$

I_{np} was computed as 0.85 pA.

4.1.2 State Dependent Junction Leakage (I_g)

The second simulation setup is illustrated in Fig. 5(b). Complementary to the first simulation, in the second simulation VDD_{logic} and VSS_{logic} were shorted together and were applied full VDD potential with respect to the ground (i.e. e1=e2=e3=2.5 V). At the same time all the inputs were also kept high. In this case, the current drawn from e3 will be I_{gw} and current drawn from e4 will be sum of I_{gw} and leakage current between substrate contacts and n+ sources (I_{pn}). Therefore the difference of the two will give I_{pn}. I_{gw} was measured as 2.62 pA and I_{pn} was computed as 0.83 pA. The sum of I_{np} and I_{pn} will give the worst case value for state dependent junction leakage current (I_g). From above mentioned two simulations I_g was computed to be 1.7 pA.

As mentioned before, the junction leakage current is reverse biased diode leakage current. Therefore, it depends upon the reverse biased voltage across the diode junction. For 1.5 V the same set of experiments were repeated to compute I_{gw} and I_g. The I_{gw} was found to be 2.22 pA and I_g was computed to be 0.98 pA. Therefore, as voltage is scaled for future technologies, the contribution of junction leakage current to total I_{DDQ} will remain insignificant.

4.2 Sub-threshold Leakage & Defect Detection

Based on the leakage current for the shift register, a million transistor device will have a typical leakage of 2.5 μA. However, for a 0.25 micron process with yet lower VDD and V_T s the leakages are expected to be at least an order or two magnitude higher than computed above. Furthermore, natural process variation of V_T will also contribute an order of two increase in leakage current for good devices.

Well-bias (mV)	Sub-bias (mV)	$I_{leakage}$ (pA)
0	0	484.1
100	100	158.6
200	200	56.0
300	300	21.0
400	400	8.6
500	500	3.8

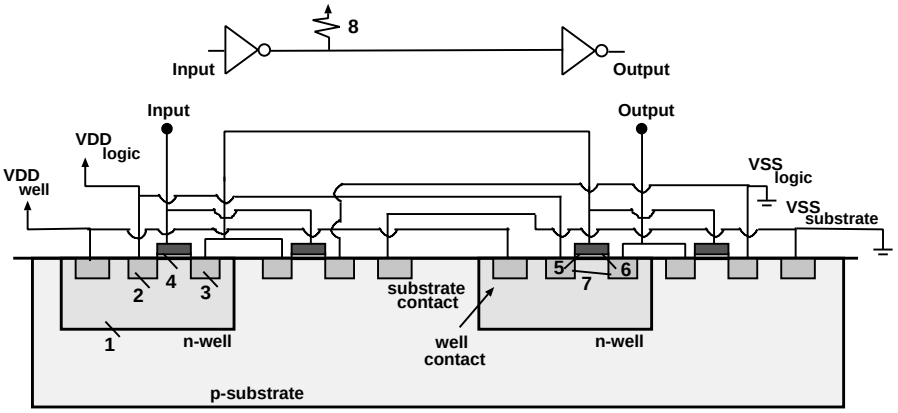
Table 1: Reverse bias and shift register leakage current.

The application of reverse bias on steady state transistor sub-threshold behavior is significant. However, same level of reverse bias has marginal influence on the steady state saturation behavior of a transistor. In other words, saturation current is not changed significantly. At any given instance only a subset of PMOS (NMOS) transistors are in sub-threshold region and the rest of them are in saturation. If reverse bias is applied in well, then the sub-threshold leakage in PMOS off transistors is reduced. However, the overall leakage is determined by the NMOS off transistors. Therefore, application of well bias alone or substrate bias alone is not sufficient to achieve desired results on sub-threshold leakage current reduction. However, if well and substrate reverse bias are applied at the same time, desired reduction in leakage current is achieved.

Let us consider the same shift register once again. Table 1 depicts the application of reverse bias and resultant reduction in the shift register leakage current. As evident from Table 1, the application of 0.5V reverse bias in the well and substrate results in more than two orders of leakage current reduction (S=71 mv/decade) for the shift register which is approximately the same as on a single NMOS transistor with modified V_T. The reverse bias may further be increased if further reduction in the sub-threshold leakage current is desired. It is possible to reduce the sub-threshold leakage by order of four or five.

Process defects may broadly be segregated into opens and shorts in conducting and insulating layers. There are evidences that a class of open defects are also detected by I_{DDQ} testing. Nevertheless, I_{DDQ} is primarily targeted towards shorts. Therefore, for this experimental study, only shorts are considered. Shorts are often collectively called bridging faults which includes leakage faults between two nodes of a transistor [23,24] and bridging faults in the interconnect network. Leakage faults were independently proposed by Nigh et al. [23] and Mao et al. [24]. The leakage fault model is as follows:

- f_{GS} -- the leakage fault between gate and source
- f_{GD} -- the leakage fault between gate and drain



Defect type	Detection Method	Conditions
1 (well/substrate)	High Igw	Reverse bias not needed
2 (source/well)	High $I(VDD_{well})$, $I(VSS_{logic})$, $I(VDD_{logic})$	Reverse bias optional
3 (drain/well)	High $I(VDD_{well})$, $I(VSS_{logic})$, $I(VDD_{logic})$	Reverse bias optional
4 (gate/well)	High $I(VDD_{well})$, $I(VSS_{logic})$	Reverse bias optional
5 (gate/source)	High $I(VDD_{logic})$,$I(VSS_{logic})$	Reverse bias needed
6 (gate/drain)	High $I(VDD_{logic})$,$I(VSS_{logic})$	Reverse bias needed
7 (source/drain)	High $I(VDD_{logic})$,$I(VSS_{logic})$	Reverse bias needed
8 (inter-logic)	High $I(VDD_{logic})$,$I(VSS_{logic})$	Reverse bias needed

Fig. 6: Bridging defects and their I_{DDQ} detection with the proposed methodology.

- f_{SD} -- the leakage fault between source and drain
- f_{BS} -- the leakage fault between bulk and source
- f_{BD} -- the leakage fault between bulk and drain
- f_{BG} -- the leakage fault between bulk and gate

These faults include not only the gate oxide defect causing leakage but the leakages between various diodes required to realize a MOS transistor. Furthermore, Nigh et al. [23] suggested that well to substrate diode defects are not necessary to consider explicitly as leakage or latchup caused by them is easily observable. However, if the VDD is reduced below 1.5V, the latchup is not possible for bulk CMOS technology because triggering and sustenance of the latchup requires more than 1.5V. Therefore, the well to substrate diode defect should also be considered.

Fig. 6 illustrates these defects and conditions for their detection. The figure depicts leakage defects only in PMOS transistors, however, the results are valid for NMOS transistors as well. These defects have been re-arranged according to the reverse biasing conditions. For the first class of defects, reverse bias is not necessary, next class of defects, reverse biasing is not the absolute requirement but may be needed for the diagnostic resolution, and finally, for a class of defects reverse biasing is needed to detect them. These conditions are based upon the fact that defect-free sub-threshold leakage of deep sub-micron VLSIs needs to be suppressed in order to make an unambiguous pass/fail decision with I_{DDQ} testing.

- **First Category:** A leakage defect between well and substrate (Fig. 6, defect 1) comes in this category. This defect is detected by measuring the state independent junction leakage current (I_{gw}) as outlined in previous sub-section. Abnormally high I_{gw} is the indicator of such a defect.

- **Second Category:** In this category are the defects which do not necessarily require reverse biasing. However, reverse bias increases the diagnostic resolution of these defects. These defects are between the well and any of the three terminals of a transistor. The defect 4, f_{BG} , is the example of this class. At the instance when gate is logic low, the defect will give rise to elevated $I(VDD_{well})$ or $I(VSS_{logic})$. The defect detection through former does not require application of reverse bias since its defect-free component is very low. However, defect detection through latter needs application of the reverse bias to suppress defect-free sub-threshold leakage. Furthermore, this defect results in a forward biased diode (assuming gate poly doping is n type) which becomes more forward

biased as well reverse bias is increased. As a result, defective I(VDD_{well}) is increased with well reverse bias. Similarly, f_{BS} and f_{BD} may be detected. It is important to mention here that detection of these defects require setting up of appropriate input conditions such that defective diode junction is excited. Depending upon the input conditions, a defect may be detected by elevated I(VDD_{logic}) or I(VSS_{logic}).

- **Third Category:** This category contains defects that require application of reverse bias to suppress the sub-threshold leakage current for defect detection. Such defects when excited have both of their affected nodes driven by VDD_{logic} and VSS_{logic}. Therefore, this class of defects are detected by elevated current on either of these supply terminals under reverse bias conditions. For example, defect 5 between gate and source under appropriate input stimuli conditions gives rise to elevated I(VDD_{logic}) and I(VSS_{logic}). Now if the reverse bias is applied such that the sub-threshold leakage of the VLSI is suppressed the defect is detected. This class also include bridging defects in the interconnect network (defect 8).

4.3 Implementation Issues

A detailed treatment of these issues is given in [5]. Therefore, we address these issues briefly for the sake of completeness. The implementation of the proposed method requires splitting of VDD and VSS supplies which needs to be routed over the chip. Furthermore, at least two extra pads are needed for extra connections. The total area overhead has been estimated between 3% to 8% of the chip area depending upon various conditions.

Bulk CMOS technology is susceptible for latchup. The latchup sensitivity increases with the proposed method. However, as mentioned before, latchup is not the issue if VDD is less than 1.5 V. Furthermore, layout style is a very effective way to reduce the latchup susceptibility in the bulk CMOS technologies. A latchup immune design style of standard cells is proposed to minimize latchup occurrence [5]. The salient feature of this style is to put VDD and VSS supplies in the middle and, p and n type diffusions on the top and bottom. A similar layout style for CMOS standard cells is proposed for smaller area and efficient routing considerations [25]. Furthermore, such a style reduces the polysilicon width and relaxes the constraint over cell height. Arguably, such a style results in more compact, high performance layout which offsets part of the area and costs associated with routing extra VDD and VSS supplies.

5 Conclusion

Static CMOS circuits have very low I_{DDQ}. Most of the processing related defects exhibit state dependent elevated I_{DDQ}. Therefore, I_{DDQ} testing is a powerful method in detecting such failures. The difference between typical (defect-free) and elevated I_{DDQ} is several orders of magnitude. However, as the technology moves into deep sub-micron, the increased transistor sub-threshold leakage current threatens to wipe out this difference. Furthermore, futuristic devices will contain ever larger number of transistors. These developments will have an impact on future of I_{DDQ} test method since the difference between defect-free and defective I_{DDQ} levels will be small.

There are many ways to reduce the transistor sub-threshold current. Most of them can be characterized as technological solutions or design solutions. These solutions, typically result either in increased area, or reduced performance. In this article, a deep sub-micron I_{DDQ} test strategy is outlined. Following this strategy, an I_{DDQ} test mode is created such that the transistor off currents are suppressed by the application of reverse bias. Such an approach allows us to measure/compute various components of I_{DDQ}. Therefore, a defect causing quiescent current elevation in any of them can be isolated. The advantages of the method include, objective setting of I_{DDQ} thresholds, quicker defect diagnosis and failure analysis. Therefore, resulting in faster feedback to manufacturing process line or designer for corrective measures.

The prerequisite of the test strategy is to split VDD supply into VDD_{logic}, and VDD_{well} , and VSS supply into VSS_{logic} and $VSS_{substrate}$ respectively. However, after the testing, both VDD (VSS) may be bonded together so that the normal operational conditions are restored. Alternatively, reverse bias can be exploited in normal operation, e.g. to reduced quiescent power consumption. The splitting of power buses increase chip area which can be estimated between 3% to 8% depending on various conditions. Different power supplies for sources and well/substrate increase the latchup sensitivity. As the solution for present supply levels, we proposed a cell layout style with power buses routed in between p^+ and n^+ diffusions which significantly reduces the probability of occurrence of latchup. Alternatively, expensive technologies, like SOI, can be utilized for latchup avoidance. Furthermore below 1.5V, latchup will not be an issue in bulk CMOS processes.

The effectiveness of the strategy is demonstrated with a real life circuit. A shift register was designed with split VDD and VSS supplies in 0.5 micron CMOS technology. The transistor threshold voltages were reduced to mimic the sub-threshold leakage of deep sub-micron transistors. It is shown that an application of 0.5V reverse bias in well and substrate reduces the total sub-threshold leakage by more than two orders of magnitude. If the need arises, level of reverse bias may be increased to further reduce the sub-threshold leakage. Furthermore, a defect diagnostic strategy is also outlined.

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