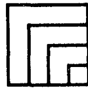

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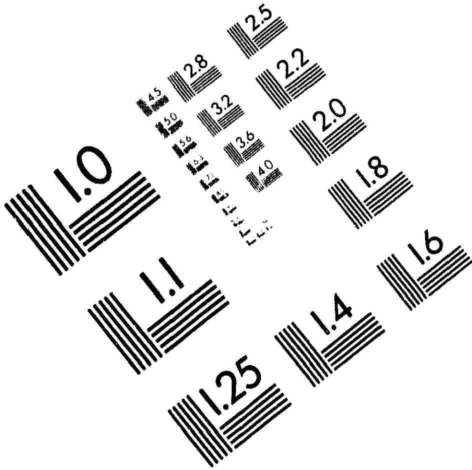
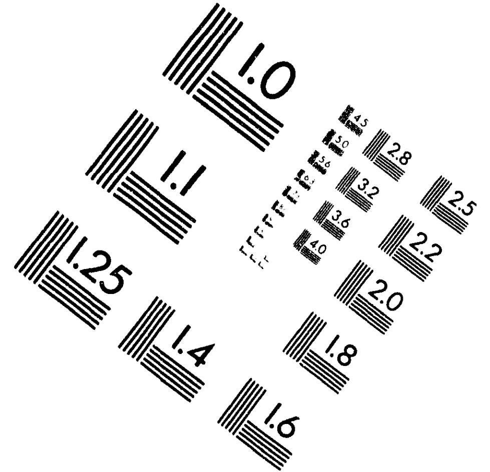

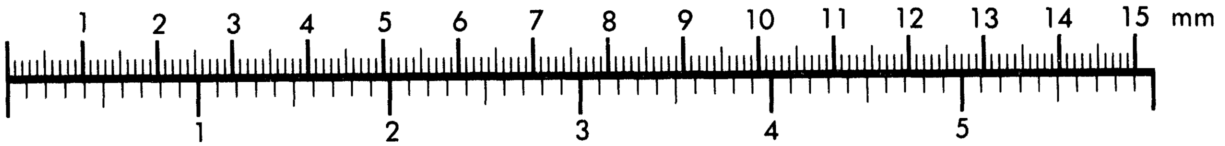

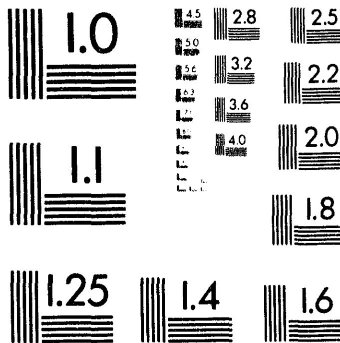

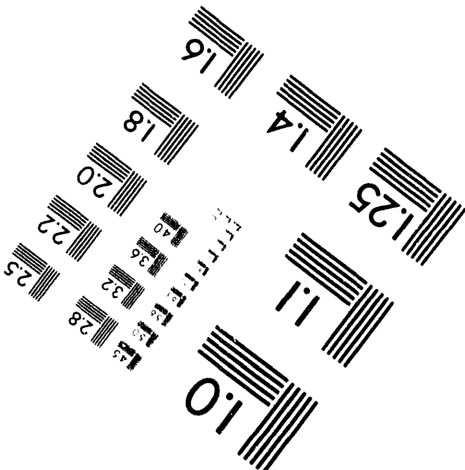
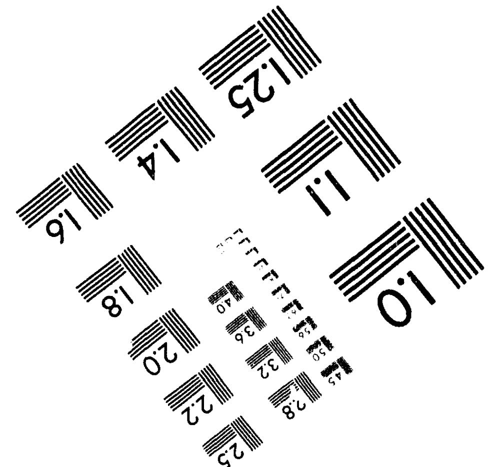

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Defect Classes - An Overdue Paradigm for CMOS IC Testing

Charles F. Hawkins, Jerry M. Soden[†], Alan W. Righter[†], and F. Joel Ferguson[††]

Electrical and Computer Eng. Dept.
University of New Mexico
Albuquerque, New Mexico 87131
(505) 844-7187

[†]Failure Analysis, MCM Applications
Sandia National Labs
Albuquerque, New Mexico 87185
(505) 845-8575, -9582

[††]Computer Engineering Dept.
University of California - Santa Cruz
Santa Cruz, CAlifornia 95064
(408) 459-4172

ABSTRACT: *The IC test industry has struggled for more than 30 years to establish a test approach that would guarantee a low defect level to the customer. We propose a comprehensive strategy for testing CMOS ICs that uses defect classes based on measured defect electrical properties. Defect classes differ from traditional fault models. Our defect class approach requires that the test strategy match the defect electrical properties, while fault models require that IC defects match the fault definition. We use data from Sandia Labs failure analysis and test facilities and from public literature* [1-60]. *We describe test pattern requirements for each defect class and propose a test paradigm.*

I. INTRODUCTION

A 1993 ITC panel titled "Fault Coverage Numbers: What Do They Mean?" drew about 400 people into the intense debate on the use of fault models. Moderator Scott Davidson of AT&T stated that the panel purpose was to encourage people to think about issues rather than come to a conclusion. Presentations by the panel members stirred the audience and there was lively discussion during the question and answer period. Many attendees voiced frustration over the lack of clear direction in the important and expensive choices of test (fault) models. In light of the poor correlation between (fault) coverage and real defect levels, why have we used fault models for test metrics?

Fault models became the vehicle of the 1970-80 era for generating test patterns and evaluating "test coverage" for ICs. Stuck-at-fault (SAF) coverage evolved as the de facto test metric for many companies in the 1980s. The Boolean form of the SAF enabled straightforward (albeit oversimplistic) test pattern generation and fault grading with limited knowledge of the circuit to be tested. Only the logic level netlist was needed for SAF test pattern generation. This property was significant in driving proliferation of the SAF, beginning with bipolar ICs and extending to NMOS and CMOS technologies. High SAF coverage became a goal and a legal requirement in certain customer/supplier relationships. U. S. government military and space agencies required that IC suppliers demonstrate the ability to achieve 99% or higher SAF coverage [61]. Commercial manufacturers and customers often have similar requirements.

Despite extensive use of SAF coverage as a quality metric, data have never been presented proving that 100% SAF testing guarantees zero defects for CMOS ICs. In fact, data from manufacturers show SAF coverage to be a relatively poor test metric for IC, board, and system defect levels [27, 44-48]. These production and application results are consistent with failure analysis studies that show most CMOS IC defects are detected better by either I_{DDQ} or high frequency Boolean tests than by SAF tests [10-23, 25-34]. High SAF coverage is expensive and difficult for many manufacturers to achieve. SAF coverage cannot even be measured for many ICs. The terms "stuck-at fault" and "SAF coverage" have not been defined by any standards organization. SAF coverage calculations often exclude numerous SAF instances, such as those identified as undetectable, abandoned, or redundant. Commercial fault simulation tools from various companies often give very different SAF coverage values, even for simple combinational logic gates.

Historically, fault models reflected our limited knowledge about IC failure and the perceived success of modelling defects with Boolean algebra. However, a fault is a hypothesis that assigns a general behavior to how a circuit fails and usually does not map to a particular defect and its failure mechanism or mode. Detection of IC defects and failure mechanisms, not faults, is the objective of any test process.

This paper addresses these concerns and proposes a test approach, or paradigm, for CMOS ICs based on defect and yield data from Sandia Labs and many authors. The abundance and consistency of these data enable definition of this paradigm. It is based on defect classes, not fault models. I_{DDQ} and different methods of Boolean testing are combined to quantify defect coverage, providing a method for minimizing defect levels by reducing test escapes.

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We first define different test procedures for defect detection. This is followed by a summary description of significant defect classes and their electrical behavior. The paper concludes with a test paradigm for optimal detection of these defects.

II. TEST DEFINITIONS

Most companies adopt individual test approaches since there is not yet general agreement on an optimal (low defect level) test strategy that can be quantified and accepted by both customer and supplier. Most companies also use some, but not all, of the following tests. These tests apply to CMOS ICs (complementary, static designs) and also to ICs with hybrid CMOS circuitry (resistor loads, dynamic logic, etc.), depending upon the particular design.

I_{DDQ} (I_{SSQ}) tests measure the quiescent V_{DD} (V_{SS}) power supply current of the IC [21]. The quiescent state exists when the voltages of all IC nodes have settled to a stable state. Many companies perform some form of I_{DDQ} testing, such as power down tests, with a small set of test patterns (vectors). I_{DDQ} testing does not require propagation of logic values to the primary outputs, resulting in small vector sets with high defect coverage (described in the defect class section). The I_{DDQ} pseudo stuck-at-fault (PSAF) test applies a SAF vector pattern to the input nodes of each logic gate, but only propagates the signal to that gate's output node [42, 47]. The PSAF test vector set has a small vector count compared to a SAF test set. PSAF tests provide I_{DDQ} node coverage for six bridge defects of each transistor in the logic gate and for certain open circuit defects [52, 53].

Boolean tests refer to any test using voltage sensing for verifying logic functionality, including the following types of tests: at-speed functional, delay fault, random pattern, SAF, V_{IL}/V_{IH}, and f_{MAX} testing [62].

A functional test uses a large test sequence designed to functionally verify operation at the design frequency (at-speed). It can also be used at lower frequencies at voltage corners to provide margin information for system operation (for example, input and output levels set at 20% and 80% of V_{DD}). The functional test vector count can become exceedingly large for modern ICs (many millions of vectors). The SAF test provides Boolean controllability and observability. Defects causing SAF effects (nodes stuck at logic 0 or 1) are assumed to do so regardless of clock frequency, temperature, V_{DD}, or any other condition. Delay fault tests use a gate level, two-vector pair to measure circuit propagation delay. The first vector sets the logic output with an initializing vector and the second vector (state change vector) provides the controllability and observability for the targeted path or gate. Tester strobe timing must be carefully set for delay fault tests. These tests can be included as part of the timing tests (rise/fall, prop delay, setup and hold times, etc.). Stuck-open fault testing also requires a two-vector pair to examine each transistor (an initializing vector followed by a state change vector). Correct operation would exist if the targeted fault location changed state. V_{IL}/V_{IH} testing finds the minimum high logic input voltage (for V_{IH}) and maximum low input voltage (for V_{IL}) for all inputs (and input conditions on I/O pins) for correct circuit operation at a fixed frequency. The f_{MAX} test uses a functional test set and repeats this set for increasing clock frequency until the IC fails [62].

Few companies generate tests for fault models such as Boolean logic bridging, stuck-open, and delay. These fault models have been extensively studied but are seldom accepted in practice. Boolean bridging fault models suffer from the assumption of zero ohm defect bridges (bridge resistance is discussed in the next section). Boolean stuck-open models may be computationally too difficult for modern ICs. Delay fault tests targeted for defects causing delay are essential but are presently used only by a small number of companies.

III. DEFECT CLASSES AND SUPPORTING DATA

This section presents data on the electrical behavior of defect classes which then form the basis for an optimal test strategy. Three general categories of defect classes are: (A) bridge, (B) open circuit, and (C) parametric defects causing delay that may not be bridge or open circuit defects. Within these general categories are defect classes denoted as Type-1, Type-2, etc. Bridge defect classes were partially chosen by their natural links to either Boolean or I_{DDQ} testing. Open defect classes were characterized by more distinct electrical properties that can require both testing methods to guarantee detection. The parametric delay defect class has unique and difficult detection properties.

A. Bridge Defects. Bridge defects at transistor node, logic gate I/O, and power bus circuit hierarchies may occur in, or with, a combinational or sequential circuit. Bridge defects include all defects and failure mechanisms that cause unintended electrical connections across two or more circuit nodes. Bridges have nonlinear or linear (ohmic) *I-V* properties with resistance from near zero to >1 MΩ. Nonlinear bridge defects include most types of gate oxide shorts, soft *pn* junctions, transistor punchthrough, and some particulate and physical bridge shorts. Ohmic shorts also occur in IC patterning defects that leave "bridges" of metal (or polysilicon) and in certain forms of gate oxide shorts [10].

Bridge defect detection is more efficient with I_{DDQ} than with Boolean testing and our bridge defect class definitions reflect this. Bridge defect resistance is the dominant factor in bridge detection methods. Correct Boolean functionality exists for signal node bridge defects when the defect exceeds a *critical resistance* [30]. Critical resistance is a function of the contending transistor current drive strengths and therefore varies with circuit design, logic input levels to contending logic gates, and process variation. Critical resistance may lie in a range as low as 10 Ω to about 5 kΩ. Vierhaus *et al.* found that critical resistance decreases as transistor size shrinks [57]. For one bridge defect location, they found that critical resistance dropped from 6 kΩ to 4 kΩ when comparing a 1.5 µm to a 1.0 µm technology. Hao and McCluskey simulated resistive gate-source (GS) and gate-drain (GD) shorts and found critical resistances of about 1 kΩ and 600 Ω [55]. Critical resistance varied with width/length (W/L) ratios and input logic patterns.

Vierhaus *et al.* made a related observation that there is a critical resistance associated with Boolean delay error measurements [57]. Delay error was simulated against a range of defect bridge resistance for small gates. Error signals approached noise levels for bridge defects above about 5 kΩ to 10 kΩ.

Bridge Type-1 Combinational Defect Class. This defect class includes defects that cause the six transistor node bridges (all bridge possibilities between the gate, source, drain, and substrate nodes) [52,53], logic gate I/O signal node to power bus bridges, and power bus-to-power bus bridges. These defects have various physical causes and include ohmic and nonohmic shorts. However, they have similar I_{DDQ} and Boolean responses, share a common test pattern for their detection, and are thus considered as a single defect class. We use SPICE simulations for ease of display to show the Boolean and I_{DDQ} responses.

Transistor node: SPICE simulations were run on the six transistor defect bridges per transistor using 2 µm CMOSN technology for standard inverters, 2-NAND, and 2-NOR gates. The result was Boolean failure when the defect critical resistance was below a value that lay in a range from about 10 Ω to 1 kΩ. Failure was defined with respect to the logic threshold voltage. The I_{DDQ} response for bridge defects was strong up to 5 MΩ (1 µA at 5 V). Fig. 1(a-c) show Boolean and I_{DDQ} behavior for a range of gate to drain bridge resistances for an *n*-channel transistor in a buffered 2-NAND gate circuit. Fig. 1(b) shows a critical resistance of about 1 kΩ and Fig. 1(c) shows the large I_{DDQ} response for the same circuit. Other transistor node bridge defect locations showed similar behavior, but with slightly different critical resistance.

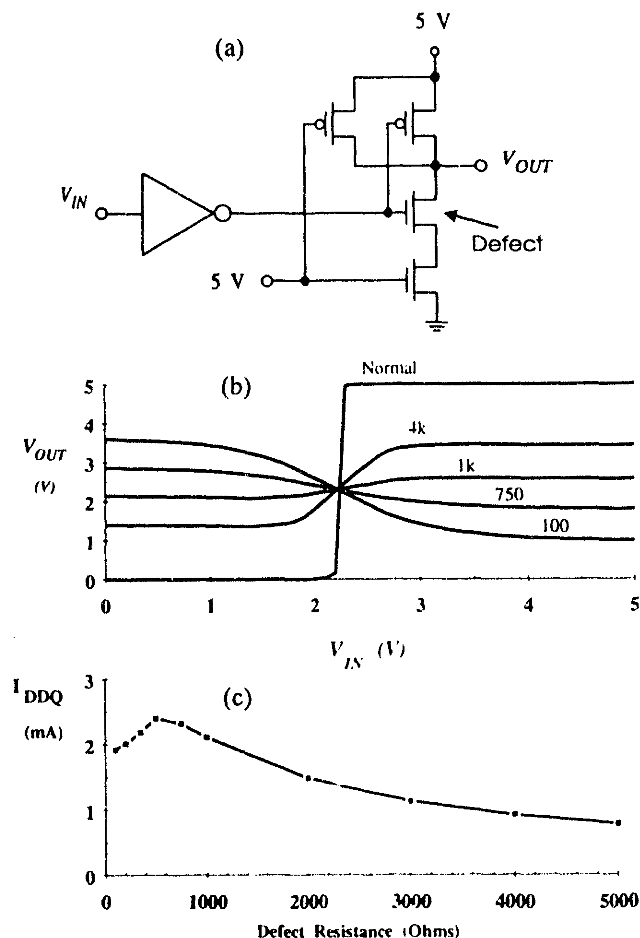

Fig. 1. *n*-channel gate-drain defect resistance (a) in 2-NAND, (b) Boolean response vs. defect resistance, and (c) I_{DDQ} response vs. defect resistance.

Gate oxide shorts have a nonlinear *I-V* behavior for four of the six possible short conditions for *n*- and *p*-channel transistors. Data show that gate shorts often pass a Boolean test but are 100% detectable with I_{DDQ} testing [10,30]. Gate shorts primarily degrade node voltages and elevate I_{DDQ}, rather than causing Boolean failure. Segura *et al.* fabricated test chips having gate oxide shorts and studied the Boolean and I_{DDQ} properties [30]. Their conclusion: ".. logical testing has a limited ability to detect gate oxide short defects even when the defect produces serious I_{DDQ} current deviations. The I_{DDQ} defect detection domain covers the whole area of logic testing." Transistor punchthrough is a drain-to-source short that occurs when the drain depletion region extends across the entire channel length [13]. Punchthrough and leaky *pn* junctions cause nonlinear *I-V* behavior and produce degraded node voltages with increased I_{DDQ}.

Data show that Boolean testing cannot guarantee bridge defect detection when defect resistance exceeds the critical resistance. Vierhaus *et al.* showed that delay fault testing is similarly limited by a critical resistance above which the timing error gets too small for guaranteed detection [57]. Rodriquez *et al.* measured metal-to-metal bridge resistance in a test chip and found clustering near 500 Ω with values to 19 kΩ [29]. Hawkins and Soden reported *n*-channel gate to n^+ diffusion shorts with resistances from 1 kΩ to 4 kΩ. Anderson measured a 570 Ω m1/m1 resistance for an ASIC particulate bridge defect [64]. These reported defect resistances are important because they are well within the nondetection range for Boolean testing.

Signal Node to Power Bus: Bridges can occur from signal nodes to the V_{DD} or V_{SS} power bus. Segura *et al.* studied bridge defects in test chips from a signal node to the V_{DD} bus. They found a critical resistance between an inverter node output and V_{DD} of about 3 kΩ [30]. I_{DDQ} was elevated over a range of defect resistance and transistor W/L ratios to about 50 µA for defects of 100 kΩ.

Power Bus to Power Bus: Power bus bridges (V_{DD} to V_{SS}), such as well to substrate soft breakdowns, are regarded as Boolean insensitive but are easily detected with I_{DDQ} testing for any vector.

In summary, the following bridge defects have been considered: (1) six nodal defects per transistor, (2) two defects between signal nodes and the V_{DD} or V_{SS} power bus, (3) one defect between one power bus and another. These defect classes are insensitive to Boolean tests unless the resistance is low, e.g., below about 1 kΩ. All nine defect classes are 100% detected by I_{DDQ} pseudo SAF test patterns.

Bridge Type-2 Layout Defect Class. These defects occur at a variety of locations and, as opposed to the Type-1 class, they require identification from the layout. These defects include bridges between two or more logic gate signal nodes or between logic gate I/O to transistor nodes. This defect class shows similarities to the Type-1 defect class in having a relatively low critical resistance that affects Boolean functionality. This critical resistance is a function of the relative current strength of the contending transistors and is thus a function of the input logic values of the contending gates. Fig. 2 shows an IC test circuit in which signal voltages and I_{DDQ} levels were measured for test chip circuits with various inputs. Table I gives these values for R_{bridge} = 0 Ω [13]. The last column shows critical resistance values simulated for these logic conditions. Critical resistance was between 150 Ω and 1750 Ω and depended upon logic input values.

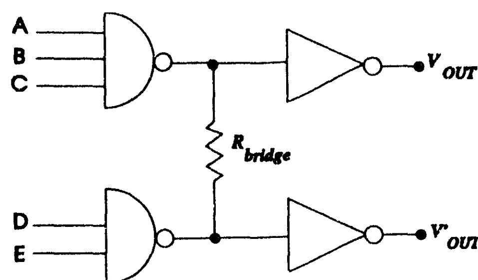

Fig. 2. 3-NAND to 2-NAND bridge defect.

Table I. Logic Gate Bridges.

ABC and *DE* Inputs					For R_{bridge} = 0 Ω			Critical Resist.
A (V)	B (V)	C (V)	D (V)	E (V)	V_{BR} (V)	V_{OUT} (V)	I_{DDQ} (mA)	Functional for R_{bridge} >
0	0	0	5	5	3.95	0.01	2.74	950 Ω
0	0	5	5	5	3.36	0.12	3.07	725 Ω
0	5	5	5	5	2.03	4.02	3.58	150 Ω
5	5	5	0	5	3.38	0.12	2.02	1250 Ω
5	5	5	0	0	4.24	0	1.64	1750 Ω

Bridge defects between certain nodes of a sequential circuit and an external gate can cause unique behavior [31,33,36]. Fig. 3 illustrates that the defect critical resistance determines whether an external logic gate can overdrive and change the memory state without increasing I_{DDQ}. If node s1 contends with the logic value of G2 and R_{bridge} is below a critical value, then G2 may change the state of the latch. I_{DDQ} is elevated only when the defect resistance is

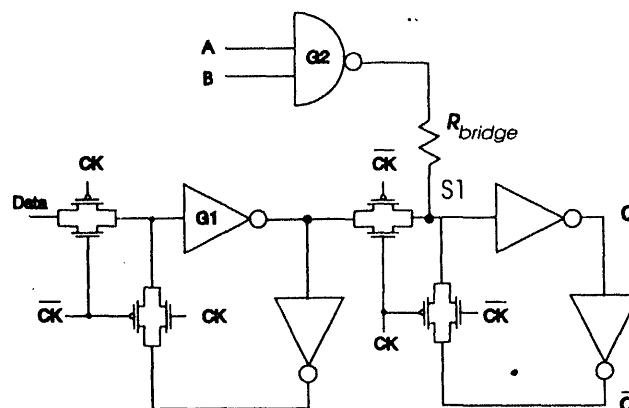

Fig. 3. Latch to logic gate bridge [31,36].

above the critical value. Rodriquez *et al.* found a sequential cell critical resistance of about 2 kΩ for their technology [31]. They also identified 37 total bridges from an inductive fault analysis in a circuit similar to that in Fig. 3. I_{DDQ} testing detected 100% of these defects when the defect resistance was above 2 kΩ and 92% when the defect resistance was less than 2 kΩ. This suggests that tests for bridge defects in sequential elements, such as in scan circuits, should include I_{DDQ} and Boolean vectors.

Most layout dependent bridge defects are easily detected by an I_{DDQ} test whose patterns cover all likely bridges. This defect is insensitive to Boolean tests unless the resistance is low, e.g., below about 1 kΩ. It is also insensitive to Boolean delay testing if the bridge resistance exceeds about 5 kΩ. Type-2 defects require identification of only those nodes having a reasonable likelihood of bridge. Otherwise, for n nodes, the possible number of node to node bridges would be $(n^2 - n)/2$, a very large number. VLSI circuits are too large for possible bridge nodes to be identified manually so software, such as VLASIC [65] or CARAFE [43], must be used. Others have used a capacitance extractor to identify potential bridges in the same interconnection layer [47].

Bridge Type-3 Sequential Defect Class. This defect class includes transistor node bridges of sequential circuits. These bridge defects can be detected by a four pattern I_{DDQ} test performed with sequential elements, such as flip-flops, in both clock phases for both logic states. Each design style of sequential circuitry must be individually analyzed since some designs contain nodes that are not I_{DDQ} testable [66]. Circuit scan chains would typically be tested with the flush and shift tests recommended by Bennetts [67] while measuring both I_{DDQ} and Boolean responses. The flush test initializes the scan chain with logic 1s (0s) and then clocks 0s (1s) through the chain. The shift test uses a 00110011... sequence through the chain to place each FF in all combinations of its present and next states. I_{DDQ} would be measured for both clock states at both logic values. The I_{DDQ} test will normally detect all bridges except a bridge from the latch to an external gate while the Boolean tests observing the scan chain will detect those that I_{DDQ} misses [31,33,35,36].

B. Open Circuit Defect Class. Open circuit defects are unintentional electrical discontinuities. They can cause behavior that may vary greatly and be difficult to predict. These defects include open contacts (missing metal or unopened oxide), metallization opens (patterning, improper etching, electromigration, or stress voiding), or opens in diffusion or polysilicon (mask or fabrication errors). Data are summarized from a range of open circuit defect structures and six open circuit defect classes are defined to account for all open circuit responses. Production and test ICs show that defects from each open defect class occur. Open circuit defect properties depend primarily on defect size, defect location, local electrical structure, and process variables [14,17,19,22-25,28,34,59,68]. The test chip data of Renovell and Cambon [23] and Maly *et al.* [25] illustrate the delay and I_{DDQ} effects of certain open circuit defects. Data are given below for the range of open circuit behavior, followed by classifications of open circuit defects.

Fig. 4(a,b) illustrate the effects of *defect size*. Fig. 4(a) shows a small open defect to a logic gate in which tunneling current (J) occurs across the narrow (< 100 nm) defect cleft [19]. This slows charge transfer thus increasing rise and fall times of the gate input node. ICs with small metallization voids or electromigration type opens are observed to function at clock frequencies into the MHz range. The temperature dependent Boolean response for small interconnect cracks is a signal delay and I_{DDQ} is only elevated if the delayed signal time coincides with the current sample time. I_{DDQ} testing cannot target this defect and the voltage error signal may be in the noise.

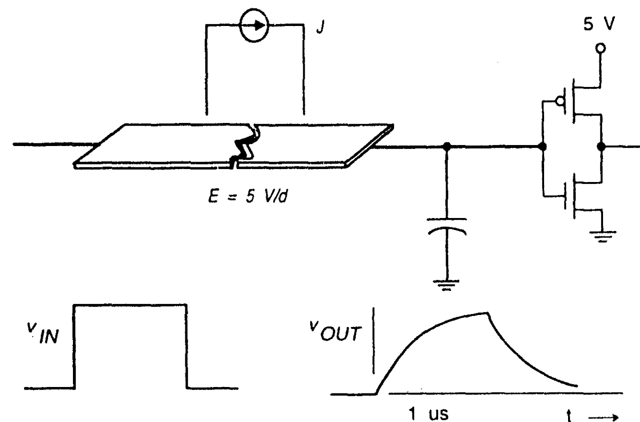

Fig. 4(a) Small open defect to logic gate.

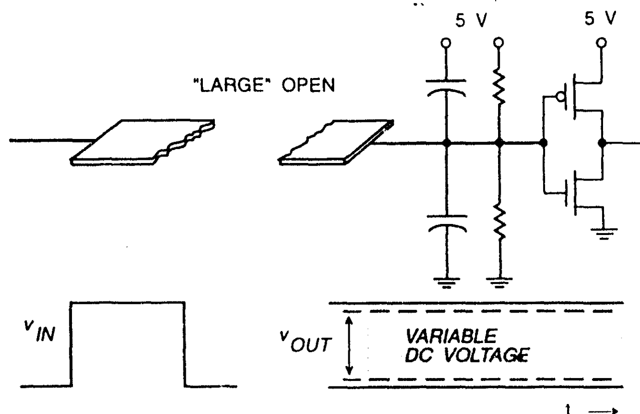

Fig. 4(b). Large open defect to logic gate.

Fig. 4(b) shows a large open defect that decouples the logic gate input node from the signal. The floating gate node acquires a bias voltage that is a function of the *local electrical structures*. Fig. 5 shows the range of behavior with data taken from mask-opened metal interconnections on logic gate test chip structures. Five inverters were fabricated (2 μm MOSIS) with varying lengths of metal interconnect on their open input line. The output voltage and I_{DDQ} measured on these floating gate inverters were superimposed on a normal inverter V_{OUT} and I_{DDQ} transfer curve (Fig. 5). The floating input voltage was estimated from the V_{IN} axis for each measured output voltage. The floating gate node voltage decreased for the longer interconnect lengths reflecting increased capacitance to the grounded substrate.

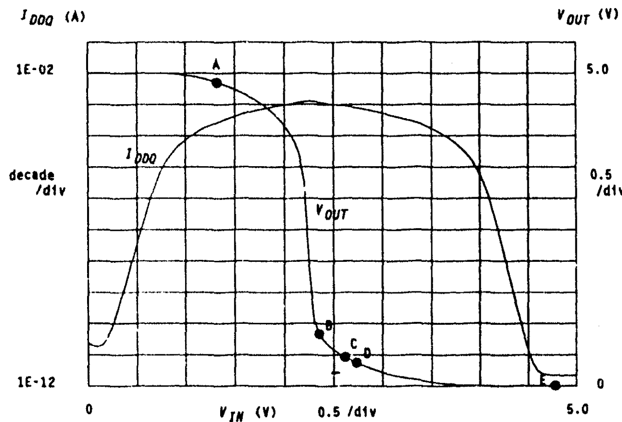

Fig. 5. Open logic gate transfer curves.

Open	Open Location
A	m2 at 2039 um from INV cell
B	m2 at 140 um from INV cell
C	m2 at 15 um from INV cell
D	m2 at entry to INV cell
E	m1 via to poly within cell

Points A-D in Fig. 5 show that both transistor pairs are on with strong I_{DDQ} elevation and weak clamping of the output voltage. I_{DDQ} ranged from 300 μA to 1000 μA for points A-D. Point E had an open circuit defect at the m1/poly contact and the gate voltage, V_{IN}, floated to nearly 5 V. The inverter output clamped to 0 V with no significant I_{DDQ} increase. The *n*-channel device was on and the *p*-channel was off, producing a transistor pair-on/off response. Fig. 5 shows the two expected responses from large open circuit defects occurring at logic gate input nodes. The first response is that both transistor pairs are on, I_{DDQ} is elevated, and weak voltage clamping of the output node occurs (points A-D). The second response is that one transistor of the pair is on, the other is off. I_{DDQ} is not elevated and strong voltage clamping occurs (point E). Johnson discusses an effect of *process-induced* trapped charge in open gate structures that influences the bias voltage of the floating gate [59]. The floating gate voltage is a function of both process-induced positive charge in the thin oxide and V_{DS} capacitive coupling to V_{GS}. It is probable that the points in Fig. 5 are skewed to the right because of these effects.

Fig. 6 shows the effect of *defect location* when the open circuit (node V_{FGI}) is in the gate of a single transistor. The logic gate output voltage V_{OUT} is a function of the signal drive to the complementary transistor and the bias state of the defective transistor. Maly *et al.* and Champac *et al.* analyzed this defect with test chips [25,34]. An open to a single transistor allows strong capacitive coupling between the drain, gate, and source. When V_{OUT} is pulled high, V_T of the open gate transistor is exceeded, causing I_{DDQ} elevation and a degraded high logic voltage. When V_{OUT} drops, then the open gate device remains in conduction until the capacitive coupling drops V_{GS} below threshold. Johnson found V_{GS} values of 0.38 V to 2.3 V for *n*-channel and 0.09 V to 0.24 V for *p*-channel transistors. One source of the variance was attributed to gate area and low leakage current (5 x 10^{-22} A) [59]. For that process, he found that most open gate *n*-channel transistors were normally conducting and the *p*-channels were normally off.

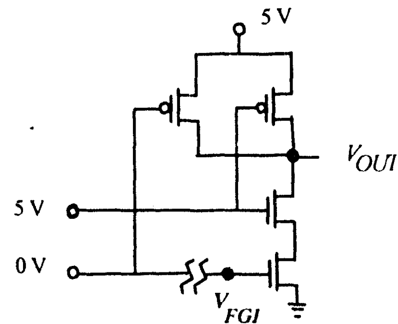

Fig. 6. Open gate defects.

Fig. 7(a) shows a test chip floating gate circuit in which the voltage and I_{DDQ} transfer curves were measured (Fig. 7(b)). The open gate was created by removing the *n*-channel m1/poly contact from the cell layout. When V_{IN} = 0 V, the *p*-channel transistor is fully on while the floating *n*-channel transistor is saturated, producing an I_{DDQ} of 80.7 μA and V_{OUT} = 4.92 V. Normal *n*-channel characteristic curves showed that such bias corresponds to a floating gate potential of $V_{FG} \approx 0.73$ V. The floating *n*-channel transistor is on and contends against the strong *p*-channel transistor drive. When V_{IN} = 5 V, the *p*-channel transistor

is off and the current path from V_{DD} to V_{SS} is effectively open. The weakly driven, open-gate *n*-channel transistor slowly discharges the output node capacitive charge through its drain/source path and cuts off when $V_{GS} < V_T$. Champac *et al.* found a nearly identical result for a test chip inverter with an open *n*-channel transistor gate [34]. A similar open poly/m1 via defect in a *p*-channel transistor elevated I_{DDQ} and weak voltages occurred at both logic high and low states. The output low was V_{OUT} = 0.2 V and I_{DDQ} = 631 μA, giving an estimated V_{FG} = 2.53 V for the floating *p*-channel transistor. The output high was V_{OUT} = 4.5 V with I_{DDQ} = 80 nA.

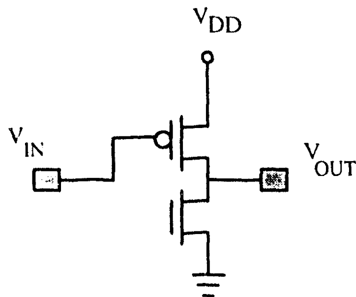

Fig. 7(a). Open *n*-channel transistor gate.

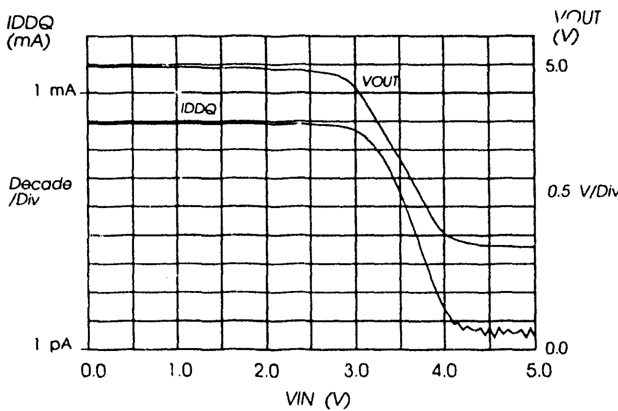

Fig. 7(b). Open *n*-channel transfer curve.

The single transistor open circuit described here has an I_{DDQ} increase in one logic state and is 100% detectable with I_{DDQ} PSAF patterns. The Boolean effect is retention of functionality, but with a weakened output low voltage that causes a delay.

Large open defects in transistor drain or source lines prevent charge transfer at the output node of the logic gate for certain vectors. The transistor acts as if it were permanently off and can cause the CMOS IC memory effect [3,14,69]. A large open at the transistor gate interconnect may also have this effect if the floating node voltage is less than the transistor threshold. This might occur if the open gate circuit was exposed to a structure such as an underpass that was influenced by a *pn* isolation junction.

Sandia failure analysis characterized this defect class on two ICs in which each defect was located in a pulldown transistor of a 2-NOR gate of a ROM decoder [14]. The *n*-channel transistor affected by the defective drain metal line had predictable Boolean memory properties at the 10 MHz tester clock frequency. That is, the 2-NOR gates would hold the logic associated with the previous clock state. If the affected node was undriven and existed in the high impedance state for a period of seconds, then the 2-NOR gate output voltage drifted to a steady state value. The drift time constant was on the order of 2-3 seconds and the final floating node steady state voltage was close to half of the power supply value. Two Boolean failure modes were identified with this defect: (1) a vector sequence dependent failure associated with higher frequency operation of the ICs (> 10 MHz), (2) a failure when a correct logic state for the defective node was allowed to drift over a few seconds to an incorrect logic voltage.

I_{DDQ} showed two time dependent elevations: (1) I_{DDQ} was elevated rapidly (ns response) for certain vectors that either caused row driver contentions, or (2) I_{DDQ} was elevated slowly (ms response) if the high-Z node was allowed to drift to steady state. The logic state voltage changed over an approximate 10 s time for one set of logic conditions and I_{DDQ} elevated as the high-Z node drifted to a voltage allowing load gate *p*- and *n*-channel transistor pairs to conduct.

The open circuit defect properties described above are placed in six defect classes:

Open Type-1 Transistor-On Defect Class. This defect class is 100% detectable using I_{DDQ} testing. An open defect that causes a transistor to be permanently on, or on for one logic state, is detectable with I_{DDQ} PSAF patterns. Boolean testing is difficult because this defect class causes delay attributed to a single transistor. The delay signal may be small and the delay fault test pattern must target individual transistors.

Open Type-2 Transistor Pair-On Defect Class. An open defect that causes a transistor pair to be permanently on is 100% detectable with I_{DDQ} PSAF patterns. It is also detectable with Boolean SAF or delay fault patterns.

Open Type-3 Transistor Pair-On/Off Defect Class. This defect class is detected with a Boolean test set and the test patterns may be either delay fault or SAF. I_{DDQ} is not increased for this defect class.

Open Type-4 Sequential Open Defect Class. Large open circuit defects in sequential circuits cause either degraded voltages with or without Boolean upset or strong clamping to a supply voltage [31,33,35,36]. Degraded voltages are detected by I_{DDQ} tests and nodes clamped to a supply voltage are detected by Boolean tests.

Open Type-5 Transistor-Off Defect Class. Detection of this CMOS IC memory effect is difficult to quantify. A 2-pattern Boolean test that targets each transistor is the only test that guarantees 100% detection but can be numerically intractable due to the need to prevent glitches on other inputs of the gate. This defect can be detected by chance with Boolean and I_{DDQ} tests.

Open Type-6 Delay Defect Class. This defect class includes the delay effect seen in open circuits having small cracks that allow tunneling and subsequent delay error. Detection depends upon the quality of the delay defect test patterns to examine all possible interconnect open situations. I_{DDQ} testing does not target this defect, but by chance may detect some defects in which the signal rise or fall time delay is such that quiescent I_{DDQ} elevation happens to coincide with the measurement strobe. Since the defect influence on test signals may be small, the voltage or current signal can be in the noise and 100% detection guarantee is difficult.

While the response of certain open circuit defects is not always predictable, the possible responses are bounded. Therefore, test strategies for open circuit defects can take account of all six possibilities.

C. Parametric Delay Defect Class. We did not assign a special defect class to all defects causing delay since many opens and bridge defects (defect classes) cause delay. Resistive bridges above a critical resistance (e.g., 1 kΩ) cause delay. "Parametric Delay Defects" defines a class of delay defect that typically is neither in the category of bridges or opens. It is a difficult defect class to detect. Delay defect properties are discussed followed by a defect definition.

Defects cause delay in CMOS ICs in two ways: (1) weakening of logic levels, (2) alteration of parameters in signal transmission paths such as via resistance, transistor thresholds, W/L variations, etc. Weak logic gate voltages have an interesting relation to propagation delay. Fig. 8(a) shows a 3-inverter circuit in which the logic level drive on node *V1* was weakened by adjusting V_{DD1} of the first inverter. Fig. 8(b) shows SPICE simulation results of the increased propagation delay versus weak voltage drive on *V1*. Voltages weakened to 4 V and even 3.5 V do not significantly delay the signal. Only when *V1* approaches the logic gate threshold voltage does appreciable delay

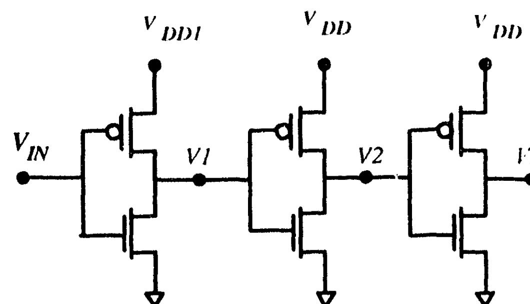

Fig. 8(a). 3-inverter circuit with weak voltage at V1.

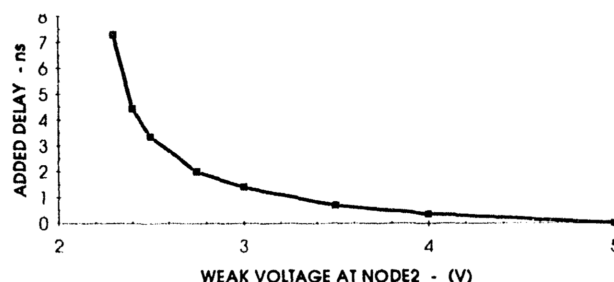

Fig. 8(b). Additional propagation delay time versus weak voltage for 3-inverter.

occur. This property degrades the ability of Boolean tests to detect defects that cause delay, but does make CMOS ICs a functionally robust technology. Others have reported this property [70]. Fig. 8(b) also illustrates I_{DDQ} sensitivity in detecting delay defects that cause weak voltages. I_{DDQ} will detect these defects when the weak voltage drive gets into the subthreshold region or higher (i.e., weaker than about 4.5 V) since both transistor pairs will be in a conduction state.

Vierhaus *et al.* studied the effect of bridge defect resistance on Boolean functionality, delay error, and I_{DDQ} [57]. They found for several combinational logic circuits that delay testing was feasible up to critical defect resistances from about 5 kΩ to 10 kΩ while I_{DDQ} testing was feasible up to resistances of 5 MΩ. Above 5 kΩ to 10 kΩ, the delay signal required finer resolution of the timing error in the range of 10%-20% percentage error. They concluded: "... zero-defect based testing clearly is impossible without I_{DDQ}-based methods, delay fault testing cannot be used as a substitute. This does not affect the necessity for path-based delay fault testing covering distributed fault effects." Lanzoni *et al.* studied bridge defect delay and I_{DDQ} properties using a voltage controlled transistor to vary a bridge resistance on a test chip [58]. They found that the relative increase in the propagation delay due to the

resistance could be small and difficult to detect with Boolean delay testing.

I_{DDQ} leakage to, or from, a signal node weakens node voltages and affects rise and fall times if the leakage path is to a power bus. Fig. 9 illustrates this showing defect leakage from the power supply (V_{DD}) to the output of the 2-NAND. This effect increases signal fall time and decreases rise time at that node. Likewise, a leak from a signal node to ground increases the rise time and decreases the fall time. SPICE simulations show that transition times become significantly degraded when leakage currents exceed approximately 10% of the current strength of the pull down transistors.

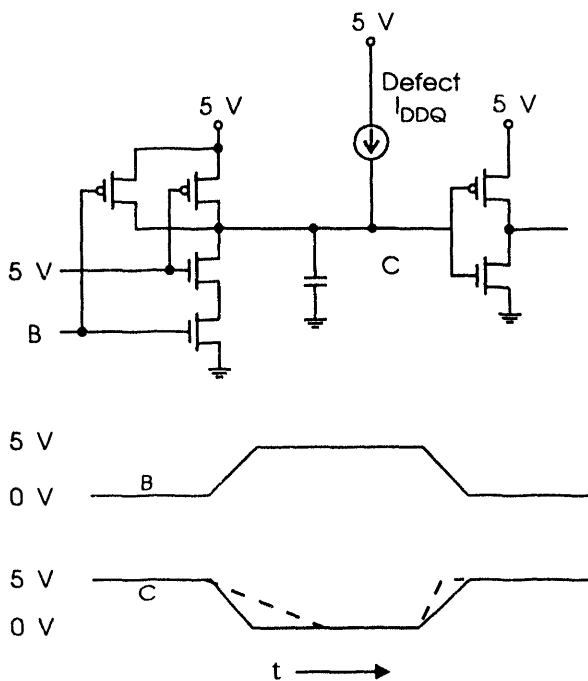

Fig. 9. Timing effects due to increased I_{DDQ} (dotted lines).

Many defects causing delay are I_{DDQ} detectable. However, a class must be defined for defects that cause delay error and don't elevate I_{DDQ}. These include shifts in R_{via}, V_T, W/L, etc. The voltage error signal may be in the tester noise. This defect class is referred to as the Parametric Delay Defect Class and is difficult to detect. It occurs in combinational or sequential circuits. Its nontarget (or accidental) detection by Boolean delay defect test patterns may be low.

An example of detection difficulty is taken from analysis at Sandia Labs of a field failure [17]. A defect existed in the drain contact of an SRAM cell (Fig. 10(a)). This contact had discontinuous metallization on the sidewalls, producing high resistance in the signal path. The

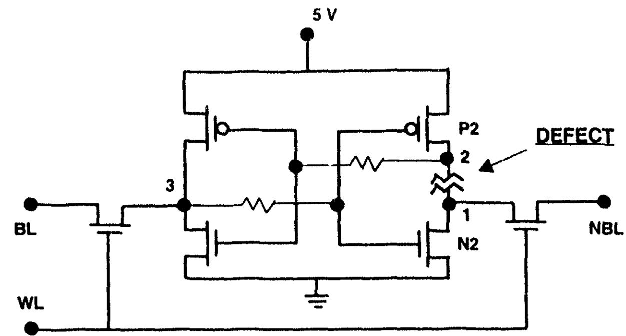

Fig. 10(a). Defect location in SRAM cell.

Fig. 10(b). SEM photo of defective contact.

discontinuity is located between the regions labelled Al in Fig. 10(b). In failure analysis, the defect acted as a parametric failure that caused temperature, power supply, and clock frequency dependent failures. Cold temperature (-55 °C) contraction of the thin metal walls led to a failure mode of a cell stuck at 5 V. Electromigration occurred with repeated testing and the contact completely opened. The only indication of a defect during production testing was an increase in write cycle time delay (about 200 ns) that was within the test limit, but was unusual. No other indication of a defect was found in reexamination of the original test data. Type-1 Delay Defects are difficult to detect since voltage signals often are in the noise and I_{DDQ} is not elevated. Unique test approaches need to be developed for this defect class.

IV. DEFECT CLASS TESTING

Three general defect classes have been described with supporting data. How then do you use this information to construct a test paradigm? Each defect class and its electrical properties allow judgment of the type of test or combinations of tests to use.

Table II summarizes the CMOS IC defect classes. The data justify whether Boolean tests, I_{DDQ} tests, or a combination of tests can achieve 100% detection.

Several defect classes are 100% detectable. I_{DDQ} is the dominant test for bridge defect classes with Boolean patterns used for certain bridge defects linked to sequential circuit nodes. The PSAF I_{DDQ} pattern detects 100% of the Type-1 Bridge and Types-1 and -2 Open defect Classes. Boolean test patterns (SAF or delay) will detect 100% of the Type-3 Open defect class. The Type-2 Bridge Defect Class is 100% detectable using combined I_{DDQ} and Boolean patterns for layout-identified bridges. The Type-3 Bridge defect class is 100% detectable using combined I_{DDQ} and Boolean flush and shift patterns with I_{DDQ} measured for all logic states of I/O and control signals. The Type-4 Open defect class is detectable with these same pattern combinations. These defect classes can be graded for coverage using present pattern generation capabilities.

Table II. CMOS IC Defect Classes.

Defect Class	Description	Test Method	100% Detect
Bridge Type-1	Transistor node, interlogic gate, logic gate to power bus, power bus-to-bus	I_{DDQ} Boolean	Yes No
Bridge Type-2	Layout-identified bridges	I_{DDQ} & Boolean	Yes
Bridge Type-3	Sequential intranodal	I_{DDQ} & Boolean	Yes
Open Type-1	Transistor-on	I_{DDQ} Boolean	Yes No
Open Type-2	Transistor pair-on	I_{DDQ} Boolean	Yes Yes
Open Type-3	Transistor pair-on/off	Boolean I_{DDQ}	Yes No
Open Type-4	Sequential	Boolean & I_{DDQ}	Yes
Open Type-5	Transistor-off (Memory)	I_{DDQ} Boolean	No No
Open Type-6	Delay	I_{DDQ} Boolean	No No
Parametric Delay	R_{su}, V_T, $\Delta(W/L)$	Boolean I_{DDQ}	No No

The test detection overlap of some defect classes allow development of an efficient test paradigm. Table III regroups the defect classes into common test methods. The first I_{DDQ} test uses PSAF patterns supplemented by layout-identified bridge defects to detect four of the defect classes. This test has good nontarget detection of the Open Type-5 defect class. A sequential test pattern including I_{DDQ} and Boolean patterns detects most of the bridge and open defects. The Boolean test using SAF or delay fault patterns detects the Open Type-3 defect class.

The difficult defect classes, Open Type-5 and -6 and Parametric Delay, are listed in Table III as <100% detected for available test methods having nontarget detection capability. Available methods are variations of delay fault [71,72], BIST, f_{MAX}, and functional test methods.

Table III. Test Paradigm.

Test Method	Defect Class	Coverage
1. I_{DDQ} (PSAF and layout bridge patterns)	Bridge Type-1 Bridge Type-2 Open Type-1 Open Type-2 Open Type-5	100% 100% 100% 100% <100%
2. I_{DDQ} & Boolean (Sequential Patterns)	Bridge Type-3 Open Type-4	100% 100%
3. Boolean (SAF or Delay Patterns)	Open Type-3 Open Type-5	100% <100%
4. At-Speed Boolean (Delay Fault, BIST, f_{MAX}, functional)	Parametric Delay Open Type-6 Open Type-5	<100% <100% <100%

<u>Design:</u> All CMOS ICs, and especially VLSI circuit designs, have increased testability when certain design rules are used, such as: (1) design for low background quiescent and transient currents (or have a test mode that supports low current), and (2) scan design. A one million transistor, 100 MHz processor has been designed for I_{DDQ} testing [49]. Low power designs are promising for their test benefits as well as for improved reliability and heat dissipation [73]. High performance ICs can be designed for low quiescent current and a testability penalty is paid when they are not. Data presented here show that most bridge and many open circuit defects require I_{DDQ} testing. Scan design allows efficient test vector generation and delivery for both Boolean and I_{DDQ} patterns, especially for sequential circuits. Without scan, complete sequential circuit controllability and Boolean observability are challenging problems.

Test Coverage: Defect classes allow a more accurate metric for estimating defect detection. Commercial tools exist for measuring seven of the ten defect classes (Type-1,-2,-3 Bridges and Types-1,-2,-3,-4 Opens). The PSAF pattern is efficient for grading all Type-1 bridge defect classes and it simultaneously grades the Type-1 and -2 Open Defects as DS bridges. The layout-identified bridges can be graded by logic simulation of the PSAF patterns with extra patterns added where needed. Bridge and Open defect class coverage of sequential circuits is very high for scan designs (by construction) and requires I_{DDQ}, PSAF, and Boolean SAF pattern analysis for nonscan or partial scan designs. The Type-3 Open Defect class can be graded with either a SAF or a delay fault test set.

The three difficult defect classes to grade are the Open Type-5 (memory), Open Type-6 (delay), and the Parametric Delay Defect Class. Open defects causing memory failures can be Boolean graded with switch level simulation for small ICs, but this has not been feasible for large ICs due to the computational complexity.

Parametric Delay defect grading with a Boolean delay fault simulator is possible in principle, but many defects in this class are not detected by existing voltage sensing, delay test methods. This defect class has either too low an error signal or too high a computational complexity when all possible defect sites are considered. Estimated coverage for this class will remain elusive until more creative test approaches are proven that can examine specific defect sites, such as via integrity. Nontarget tests, such as at-speed Boolean methods, are the only tests available. Other tests, such as the transient power supply current test, i_{DDT}, require further research to describe their capabilities [74,75].

V. CONCLUSIONS AND COMMENTS

Based on the abundance and consistency of the data, we believe that CMOS IC test strategies using these classes will result in reduced cost and lower defect levels. With this paradigm, tests are matched to defect properties, enabling more direct assessment of defect detection. Bridges and most open circuit defects are 100% detectable when I_{DDQ} and Boolean methods are combined. Certain open defects and defects causing parametric delay are difficult to detect and are where modern test research efforts should be directed.

For this test paradigm to be effective at raising the quality and reliability of ICs delivered to customer, several important factors must be considered. The relationship(s) between the predicted defect coverage for the various defect classes and their actual coverage must be understood. The types of defects and failure mechanisms that exist in the ICs directly influence this relationship as well as the cost of the test approach. The types of defects and failure mechanisms in CMOS ICs are dependent on the design, layout, and process technology and therefore can vary not only from vendor to vendor but from wafer lot to wafer lot. For one process, bridge defects may dominate while, for a different process, open circuits may prevail. The nature and stability of the defects must be considered because the behavior of some defects, such as gate oxide shorts, can change with time. This is a factor for the selection of the I_{DDQ} limit because the impact of any particular defect may go beyond simply the magnitude of current it causes. Decisions about targeting the test approach for defect categories (bridge, open, and parametric delay) and classes within these categories are best made with as much knowledge as possible about the entire IC manufacturing process and about customer requirements. The development of the capability to grade defect coverage by defect class is the first step. Improving CMOS IC quality and reliability through improved test methods clearly presents many opportunities for research and technical advances.

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