Defect-Oriented Test Methodology for Complex Mixed-Signal Circuits

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Abstract

Testing of analog blocks in digital circuits is emerging as a critical factor in the succes of mixed-signal ICs. The present specification-oriented testing of these blocks results in high test costs and doesn't ensure detection of all defects, causing potential reliability problems. To solve these problems, in this paper a defect-oriented test methodology for mixed analog-digital circuits is proposed. The strength of the method is demonstrated by an implementation for a complex mixed-signal circuit, a Flash analog-to-digital converter. It is shown that with simple tests 93% of the defects in this circuit can be detected. Moreover, application of DfT guidelines derived from this test methodology may improve the defect coverage to 99%. First impressions lead to the conclusion that the analyzed test obtains a higher defect coverage with lower test costs than functional tests.

1 Introduction

With the increasing integration capabilities of modern CMOS processes, the application of analog components within large digital ICs is becoming increasingly common practice. Testing of analog blocks in digital circuits is emerging as a critical factor in the success of these mixed-signal ICs. The digital parts can be tested using structured testing techniques that are based upon realistic fault models. However, for analog circuits, such fault models are not available and a structured division into functional blocks is difficult to implement because of the performance penalties involved. Therefore, analog testing has been largely functional, resulting in the following problems:

1. Full verification of all specifications makes functional testing costly and time consuming.
2. Limited functional verification does not ensure that all defects are detected.

Therefore, researchers, taking ideas from the digital defect-oriented test approach (*Inductive fault analysis* or IFA [1]), applied a similar method in the analog domain. Meixner [2] and Soma [3] suggested that process defects should be the basis for the generation of analog fault models. Soma verified this hypothesis with studies of various simple analog building blocks [4, 5]. Silicon results on an analog defect-oriented test methodology were presented by Sachdev [6]. He demonstrated that most of the process defects in a Class AB amplifier can be detected by simple DC, Transient and AC measurements. However, some of the parametric faults escaped detection.

A problem is that IFA can only be done for small cells. The circuit-level simulations used to determine the faulty behaviour are not feasible for circuits with a real-world complexity. Harvey [7] tried to tackle this problem by using high-level models for parts of the circuit. In this approach, however, the accuracy of the generated fault models is limited by the high-level models used. In this paper a divide-and-conquer approach is proposed. In analogy with the digital macro test concepts of Beenker [8], a complex circuit is subdivided into smaller blocks, *macro cells*, for analysis/test purposes. Circuit-level simulations are done to generate macro-level fault models, the *fault signatures*. Simulations with higher-level models of the other cells are used to determine detectability of these fault signatures at the edge of the circuit.

To evaluate the proposed defect-oriented test methodology, it is implemented for a realistic and complex mixed-signal circuit, a Flash analog-to-digital converter. The defect detection capability of simple test methods is determined and the effectiveness of some DfT measures is examined. This circuit was chosen because the boundary between analog and digital lies in the ADC. The complexity of the circuit makes the use of macro test concepts necessary. The ADC, as a building block, is in use on several Philips system chips [9]. The paper has been organized as follows. In section 2 an overview of the defect-oriented test methodology is given, which is applied to the ADC in section 3. In the last section some conclusions are drawn.

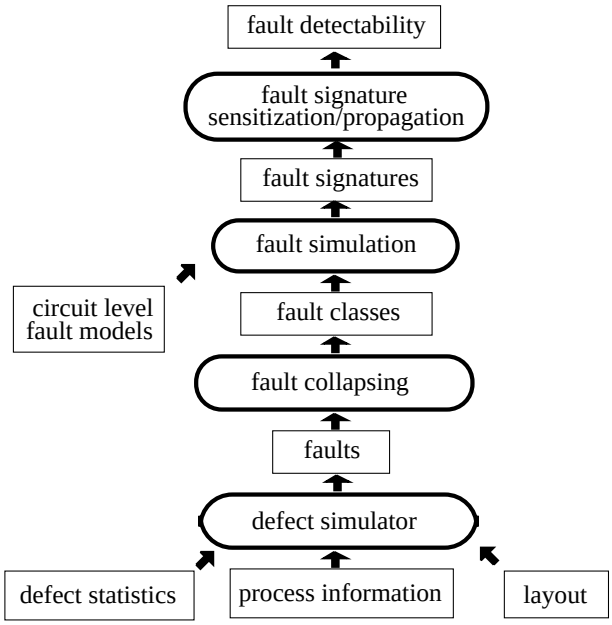

Figure 1: Defect-oriented test path

2 Defect-oriented test methodology

The proposed approach is shown graphipcally in Fig. 1. After division of the circuit into macro cells, the path of this figure has to be completed for each macro. As shown, the input of this flow are the defect statitistics, a description of the process and the layout of the macro cells. The *defect simulator* uses this information to generate circuit level faults specific to the layout and process. This is done by sprinkling defects on the layout in a Monte Carlo manner, determining whether the defects cause faults and, if so, extracting the circuit-level faulty behaviour. The catastrophic defect simulator VLASIC ([10]) is used for this.

In the fault list produced by the defect simulator, a lot of faults are equivalent (for example shorts between the same nodes). The *fault collapser* collapses these faults into classes of circuit-level equivalent faults. The magnitude of a fault class determines the likelihood of this particular type of fault. A circuit-level fault model is made for each fault class. VLASIC only gives information about catastrophic faults, i.e. faults causing a DC change in the connectivity of the circuit. For analog circuits also non-catastrophic faults (e.g. incomplete shorts or size changes of resistors) are important. Therefore non-catastrophic faults are generated from the catastrophic faults.

Then a *fault simulation* of the fault classes is performed: the circuit-level fault model is inserted into the macro cell, and circuit simulations using an analog simulator (e.g. SPICE) are done to determine the impact of the fault at the edge of the macro cell. This impact is modelled in the fault signature, which represents the fault at the macro level. The fault signature should be detailed enough to determine the detectability of faults. For simple test methods often a quite simple model is sufficient (e.g. AC characteristics are not necessary for DC tests) and equivalent signatures can be taken together.

Finally the input stimuli have to be propagated from the input terminals of the circuit to the input terminals of the macro cell, and the resulting fault signatures have to be propagated from the macro cell to the output terminals of the circuit. High-level models of the macro cells can be used in this *fault signature sensitization/propagation* step. A fault is considered detected for a certain set of input stimuli if its fault signature at the edge of the circuit is different from the signature of the fault-free circuit (the *good signature*). However, in the analog domain, the output of a fault-free circuit can vary under the influence of environmental conditions like process, supply voltage and temperature. Thus the good signature is a multi-dimensional space, which has to be compiled for each set of test stimuli, and the faulty circuit has to have a response outside this space to be recognized as faulty.

3 Case study: a Flash ADC

A Flash ADC was selected as a vehicle to examine the effectiveness of the proposed methodology for complex mixed-signal circuits. Flash ADCs are crucial blocks in the Philips multimedia audio/video products. First we look into the Flash structure and implementation. Then we highlight the defect-oriented test path for one of its macro cells, the comparator. After this global results are given. Finally some DfT proposals are made.

3.1 Structure of the Flash ADC

In full-flash converters the analog input signal is converted into a digital code word in one step (in one 'flash' of the input signal). For this, in an n-bit full-flash A/D converter, 2^n reference voltages and comparator stages are used in parallel to convert the analog input signal into a thermometer-like digital code (see Fig. 2). This code is converted into a binary output code by using a digital decoder.

In the case study ADC, the same basic structure can be distinguished. It's an 8-bit CMOS ADC for embedded application intended for video signals. The 256 reference voltages are generated by a dual ladder resistor string [11]. The 256 comparators are each loaded with a flipflop. The biasing and clocking of the converter are not included in the basic structure shown in Fig. 2. These functions are performed by two other macros: a bias generator and a clock generator.

Since a circuit-level simulation of the entire circuit is not possible, it is divided into 5 types of macro cells: 256 comparators, a resistor ladder, a bias generator, a clock genera-

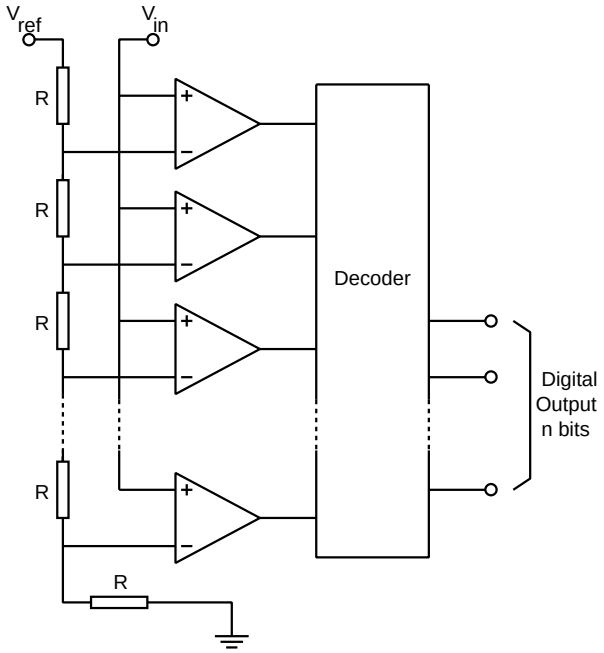

Figure 2: General structure of a Flash ADC

tor and a digital decoder. Owing to the limited space, it is not possible to give the analysis results for all macros. The comparator macro cell is used to highlight the test methodology, since most of the ADC area is covered by these cells and the analog-digital boundary lies within them. Interested readers are referred to [11] for a more comprehensive description of the analysis.

3.2 Defect-oriented test path for the comparator

A complete overview of the test path is given for the comparator macro. First a brief description of the comparator is given. Then the subsequent steps of the test methodology are treated and the final results are given.

Description comparator The comparator macro consists of two parts: a comparator and a flipflop. The comparator compares the input voltage to the reference voltage in three phases: a sampling phase, an amplification phase and a latching phase. It is loaded with a flipflop, which transfers the decision of the comparator, amplified to a logic level, to the output of the flipflop at the beginning of the new sampling phase. The comparator is a fully balanced circuit. Its biasing is class A, with the bias voltages supplied by the bias generator. It needs three clock signals, which are supplied by the clock generator. The flipflop is also completely balanced. Its quiescent current is zero in the amplification and latching phase. However, due to a leakage current, the quiescent current is strongly dependent on transistor parameters in the sampling phase.

Defect simulation and fault collapsing The defect simulator VLASIC was used to sprinkle 25,000 defects on the layout of the comparator. This resulted in 805 catastrophic faults, which could be collapsed into 334 fault classes. To determine a statistically significant magnitude of the fault classes (see [11]), later the defect sprinkling was repeated with 10,000,000 defects[1]. The 334 faultclasses were found to contain 226,596 faults. The relevant information about the faults and fault classes is summarized in Table 1.

fault type	% faults	% fault classes
Short	95.43	81.1
Extra contact	0.18	2.7
Gate oxide pinhole	3.13	3.6
Junction pinhole	1.04	2.7
Thick oxide pinhole	0.18	2.1
Open	0.03	5.1
New device	0.01	2.4
Shorted device	0.002	0.3

Table 1: Catastrophic faults and fault classes for comparator

Clearly, the dominant fault mechanism is the short: more than 95% of the faults were shorts by nature. This is not surprising, since the majority of the spot defects in the fabrication process consist of extra material defects in the metallization steps. Other important fault mechanisms are gate oxide and junction pinholes.

Another observation is the great difference in the percentage of faults and the percentage of fault classes for the differenct fault types. For instance, opens constituted 0.03% of the faults, but 5.1% of the fault classes. The percentage of faults gives the most realistic fault coverage figure and is used in the rest of this paper.

Only 27.8% of the faults in the comparator were found to influence nodes of only this macro cell. The other faults also influenced nodes of other macros (for instance the lines distributing the clock signals to the comparators). To obtain realistic fault signatures, these faults have to be simulated with all affected macro cells at circuit level.

Circuit-level fault models A catastrophic short in the metal layers was modelled as a resistance inserted between the appropriate nodes, with a value determined by the extra material causing the short: 0.2 Ohms for metal, 20 Ohms for polysilicon and 60 Ohms for diffusion. Extra contacts were modelled as a resistance of 2 Ohms. Thick oxide pinholes and junction pinholes were modelled as a resistance of 2 kOhms. Gate oxide pinholes were modelled in three ways: as a resistance of 2 kOhms from the gate to the

[1] This has not initially been done, because the fault collapsing had to be done manually at that time

source, drain and channel of the affected transistor. Of the resulting fault signatures, the worst case (most difficult to detect) signature was choosen. Opens were modelled by splitting the affected node in two parts. New devices were modelled by inserting an extra minimum-size transistor. Finally, shorted devices were modelled as a resistance of 60 Ohms between drain and source of the affected transistor.

Non-catastrophic faults were evolved from the catastrophic shorts and extra contacts. These near-miss types of faults were modelled as a parallel combination of a resistance of 500 Ohms and a capacitance of 1 fF ([12]). The other catastrophic faults were already high-ohmic in nature, and therefore were not used to generate non-catastrophic faults.

Input stimuli and detection mechanisms One of the motives for the case study was to find the fault coverage of simple DC test methods. The comparator, however, is a clocked system, so the 'DC' test stimulus was defined as a series of input voltages which had to be sampled and compared to the reference voltage by the comparator.

Two types of detection mechanisms were considered: voltage detection and current detection of faults. A fault was considered voltage detected, if it caused a *missing code* at the output of the ADC. A missing code means that a certain (digital) output code never occurs, whatever the analog input. To detect all possible missing codes, the analog input voltage corresponding to each digital output number has to be sampled at least once. The missing code test, therefore, consists of applying a triangular waveform at the input of the ADC, taking 1,000 samples and checking if every output number occurs. Since sampling can be done at full speed, this takes 40 μs test time.

For current detection, three types of DC currents were considered: the analog power supply current *IVdd*, the digital quiescent power supply current *IDDQ* (drawn by the clock generator, a digital cell) and the current drawn by or supplied to one of the input terminals (analog input, clock input, reference input, etc., collectively called *Iinput*). A fault was considered current detected if it caused one of these currents to be outside the 3σ-spread due to process variations (e.g. 4.4 mA for IVdd). The currents have to be measured during the sampling, amplification and latching phases of the comparator and for an analog input higher and lower than the reference voltage. Therefore, the current test consists of applying an input voltage higher than the highest reference voltage and lower than the lowest reference voltage and doing three current measurements. Approximately 100 μ is necessary for the transient currents to disappear, so these 6 measurements take 600 μs of test time.

fault signatures	% cat. faults	% non cat. faults
Output Stuck At	63.7	52.4
Offset (> 8mV)	2.5	2.3
Mixed	11.0	3.6
Clock value	4.5	18.3
No deviations	18.3	23.4

Table 2: Voltage fault signatures comparator

Fault simulation results The voltage fault signatures resulting from fault simulation of the catastrophic and non-catastrophic faults in the compator are given in Table 2. Five categories of voltage signatures are distinguished. For the *Output Stuck At*, *Offset* and *Mixed* categories, the output of the comparator displays a corresponding behaviour. For the *Clock value* signatures, the comparator behaves correctly, but due to a fault in the comparator affecting the clock signal distribution lines, one of the clock generator outputs has a deviating value. This kind of fault typically affects the high-frequency behaviour and offset reduction of the comparator, and is not easily detectable by voltage tests. The last category of signatures, *no deviations*, is the same as the fault-free signature. The corresponding faults cannot be detected by voltage tests (for the input stimuli used).

From Table 2 it can be observed that many of the faults cause a stuck-at behavior of the comparator. This is due to the balanced nature of the design and the small biasing currents. A fault (even a non-catastrophic one) can easily tip this balance and keep the comparator stuck at one side. For non-catastrophic faults, the clock value signature becomes more important. This is because the clock signal lines are driven by large buffers in the clock generator. High-ohmic faults in the clock signal lines do not cause the output of these buffers to be stuck-at, but only to change their high and low value slightly.

fault signatures	% cat. faults	& non cat. faults
IVdd	43.8	42.3
IDDQ	24.2	25.6
Iinput	20.5	21.7
No deviations	32.0	32.1

Table 3: Current fault signatures comparator

The current signatures for the comparator are given in Table 3. Four categories of current signatures are distinguished. For faults with the first three signatures, the respective currents deviate more than their 3σ-spread from their nominal value. Faults with the fourth current signature cannot be detected by current measurements. Note that

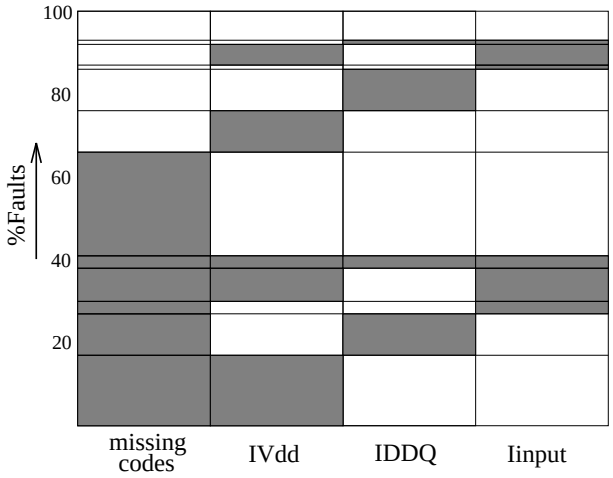

Figure 3: Detectability of catastrophic faults for comparator

the percentages add up to more than 100%, because there is some overlap between the first three signatures. The large amount of faults (24.2% / 25.6%) which can be detected by measuring the quiescent current of the clock generator IDDQ is striking.

Fault signature sensitization/propagation The sensitization of the faults in the comparator is no problem: the analog input of these macro cells is an input terminal of the circuit, and the clocking and biasing signals are the same as in normal functioning of the circuit.

The current signatures need not be propagated , because they are already defined as deviations in currents supplied by an input terminal of the circuit. This is one of the big advantages of using current testing.

The voltage signatures do have to be propagated. However, there is a one-to-one relationship between the categories of voltage signatures given in Table 2 and the simple detection method of *missing codes*: the first two fault signature categories cause missing codes, the others do not.

With these considerations, the fault detection of simple test methods for the comparator can easily be determined. The results are shown in Fig. 3 for catastrophic faults. In this figure, for each fault is determined if it is detected by one of the four detection mechanism. A shaded area means that the faults in this area are detected by the mechanisms mentioned below. For example, the bottom row depicts that 14.5% of the faults is detected by both a missing code measurement and a power-supply current measurement. A similar figure can be made for non-catastrophic faults.

From the figure, some conclusions can be made. A missing code measurement has a high fault detection capability (66.2%). However, current measurements are necessary to obtain the maximum fault detection, since 26.6% of the faults are only current detectable. Note that 10.0% of the faults in the comparator could only be detected by IDDQ measurements of the clock generator. This kind of fault would be difficult to detect by specification-oriented voltage tests. The overlap between different detection mechanisms gives room for the optimization of the test method and fault detection.

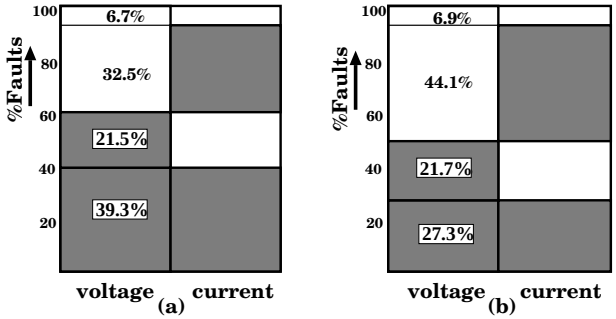

Figure 4: Global detectability of (a) catastrophic and (b) non-catastrophic faults

3.3 Global results

The other macro cells have been analyzed in the way described in section 3.3. A detailed description of this analysis is given in[11]. The high current detectability of faults in some of these cells was striking: in the clock generator 93.8% and in the reference ladder even 99.8% of the faults were current detectable. The results for the separate macro cells can be compiled to obtain global results for the entire circuit. For this purpose, the fault signature probabilities for macro cells have to be scaled into global fault signature probabilities. This scaling is done on the basis that in a real fabrication process, the defect density will be approximately equal for all macro cells.

After scaling and adding all the fault signature probabilities, the global results given in Fig. 4 were obtained. The total fault coverage for catastrophic faults was calculated to be 93.3%. Of the faults 60.8% were detected by voltage measurements. Current measurements were found to be a better test method: 71.8% of the faults were current detectable and 32.5% detectable by current only. However, a combination of both test methods was needed to reach the maximum fault coverage of 93.3%. For the non-catastrophic faults, comparable results were obtained. Current measurements were even more important for the detection of these faults.

3.4 DfT proposals

With the proposed simple test, 93.3% of the catastrophic and 93.1% of the non-catastrophic faults could be detected.

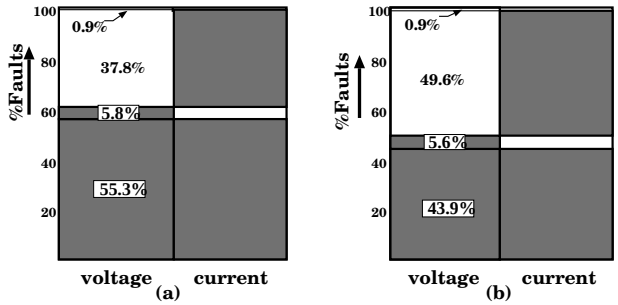

Figure 5: Detectability of (a) catastropic and (b) non-catastrophic faults after DfT measures

This may be satisfacory for a wafer-sort test, but is certainly not enough for an end-of-production test.

The methodology used makes it easy to investigate the reasons for the undetectability of faults. Analysis of the 6.7% (6.9%) of undetectable faults showed that most of them show an elevated IVdd during sampling. A leakage current in the flipflops loading the comparators causes a spread in the power-supply current of 15 mA during sampling, making these current signatures undetectable. A redesign of the flipflop, eliminating the leakage current, would make them detectable.

Another important category of fault signatures is caused by shorts between two bias lines, which carry signals that are only marginally different. A simple solution would be to exchange some bias lines, thereby separating two lines with similar signals by another more deviating signal line.

Application of these Design for Testability measures results in the fault coverages shown in Fig 5. The fault coverage of simple tests is now increased to 99.1%. Another effect is that the amount of faults only detectable by voltage measurements decreases to 5.8% (5.6%). This makes it feasible to use only current tests in the wafer-sort tests.

4 Conclusions

In this paper a defect-oriented test methodology for complex mixed-signal circuits has been proposed. The methodology was used to determine the fault coverage of simple test methods for a Flash ADC. The simple tests were found to be able to detect a high percentage of the occurring faults: 93.3% of the catastrophic and 93.1% of the non-catastrophic faults could be detected. Current measurements were necessary to obtain these high figures. The methodology also proved to give useful DfT feedback. By taking some specific DfT measures, the fault coverage could be increased to 99.1%. The test time needed to obtain this fault coverage is approximately 640 μs, which compares favourably with specification-oriented tests. Moreover, 11.0% of the faults only caused an increased IDDQ in the clock generator. These faults are difficult to detect by specification-oriented voltage tests.

Based on the research done some, general conclusions about mixed-signal DfT can be made. Many faults disturb the boundary between analog and digital, causing an increased quiescent current of the digital part of the IC. To be able to exploit this mechanism to detect faults, the interface between analog and digital should be designed in such a way that in a fault-free circuit the quiescent current is negligible small. Faults influencing lines with almost identical signals are very difficult to detect. Therefore, such lines should not be placed close to each other.

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