Defect Tolerance of QCA Tiles

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Abstract

Quantum dot Cellular Automata (QCA) is one of the promising technologies for nano scale implementation. The operation of QCA systems is based on a new paradigm generally referred to as processing-by-wire (PBW). This paper analyzes the defect tolerance properties of PBW when tiles are employed using molecular QCA cells. Based on a 3×3 *QCA block, with different input/output arrangements, different tiles are analyzed and simulated using a coherence vector engine. The functional characterization and polarization level of these tiles for undeposited cell defects are reported. It is shown that novel features of PBW are possible due to spatial redundancy and QCA tiles are robust and inherently defect tolerant.*

Index words: QCA, defect tolerance, emerging technologies.

1. Introduction

As CMOS faces its fundamental physical limits, much research has been reported to supersede current CMOS by utilizing technologies commonly referred to as *emerging technologies* (such as carbon tubes and tunneling devices). These technologies have the potential to achieve an extremely high density (in the range of 10^{12} devices/cm^2), fast operating speed at Tera Hertz frequencies together with room temperature operation and low power dissipation. Among these emerging technologies and related devices, *Quantum dot Cellular Automata* (QCA) [1] is very promising. QCA necessitates a different methodology for *computation and communication* [2][3]. Logic elements are based on two gate primitives (inverter, or INV, and majority voter, or MV as shown in Figure 1(b)(c)) to implement combinational circuits. Two arrangements referred to as the binary wire and the inverter chain serve as interconnect [4], and are shown in Figure 1 (d)(e). The concept of clocking for QCA has been introduced in [5]; timing consists of four clocking zones.

QCA design involves diverse new paradigms such as

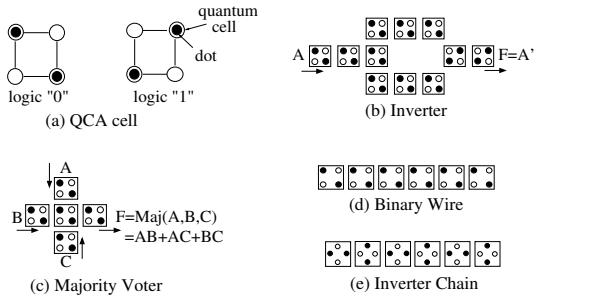

Figure 1. Basic QCA devices

processing-by-wire (PBW) [6]. PBW refers to the ability of QCA by which information manipulation can be accomplished, while transmission and communication of signals take place. PBW capabilities can be observed in the inverter chain as well as in the arrangement of cells in an MV. An implicit PBW feature has also been analyzed in [16] by which testing of QCA devices and their unique logic features have been investigated.

Sequential as well as combinational designs can be realized in QCA [3][15][17]. Currently, micro-sized QCA devices have been fabricated with metal cells which operates at 50mk [7]. Recent developments in QCA manufacturing focus on molecular implementations [8][9], in which higher speed and room-temperature operation are expected. It is expected that homogeneous cell arrangements will be constructed by self-assembly or large scale cell deposition. Modular QCA is well suited to these techniques. However, very little work has been performed on structured QCA design to fully meet the challenges of PBW. The SQUARES methodology (based on a 5×5 grid) has been proposed as an initial effort in modularizing QCA design [10]. This analysis is very limited because it does not consider cell interactions extending over the single grid. A tile-based approach (using a 3×3 grid) has been proposed in our earlier work of [11]. It has been shown that tiles are not only area efficient, but they also offer versatile logic and interconnection functions. However, in previous works in modular QCA [10] [11], logic and interconnect circuits are assumed to be

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defect free. In this paper, the defect tolerance of tiles for the design of QCA circuits is investigated. Three tiles proposed in [11] are analyzed. These tiles can be thought as instances of PBW in a QCA design with spatial redundancy. The logic behavior of the defective tiles are then compared with the defect-free behavior to relate whether the PBW capability of a tile is changed by the defects. The polarization characteristics of the functions for all analyzed tiles are also found by simulation. It is shown that due to their spatial redundancy, the correct functions of the tiles are tolerant to defects. This further validates the premises that tile-based design can be used to efficiently assemble QCA cells.

2. PBW by Tiling

As in the early stages of VLSI, QCA requires building blocks that are versatile to allow flexible manufacturing and assembly of different circuits. An early proposal for modular QCA is the SQUARES methodology [10], which is based on a 5×5 QCA grid. A novel arrangement has been proposed recently [12] for constructing a tile-based serial memory in QCA. Our previous work in [11] has demonstrated that tiles based on the 3×3 grid provides universal and versatile logic functions. It has been shown that both the logic and interconnect parts of QCA circuits can be constructed using tiles [11]. In this paper the defect tolerance of these tiles is investigated; it will be shown that the proposed tiles are not only versatile in logic function generation, but also inherently defect tolerant. A tile is constructed with 9 QCA cells arranged in a 3×3 grid, and is utilized as the basic building block for QCA. Tiles can be arranged to generate the desired logic operations within a Cartesian layout. A tile consists of three 3-cell horizontal (vertical) wires referred to as the upper, center and lower (left, center and lower) wires; additional input and output cells are attached to a tile. This scheme provides the following desirable features for manufacturing: (1) The 3×3 grid provides a better cell utilization than the 5×5 grid of SQUARES [11]; this is due to the separation of logic/interconnect implementations and the reduced size of the building block, i.e. 9 versus 25 cells. (2) Tile-based design allows compatibility with timing/clocking techniques, thus keeping the length of the longest line of QCA cells in a zone (and avoiding kinks).

Defect tolerance is the main focus of this paper. Currently during manufacturing, defects can occur in both the *chemical synthesis* phase (in which the QCA cells are manufactured) and the *deposition* phase (in which the QCA cells are attached to a substrate) [13]. Defects are much more likely to occur in the deposition phase than in the chemical synthesis phase, often resulting in perfectly manufactured but imperfectly placed cells. In this paper, only the undeposited cell defect is considered. This represents the case when the defective cell fails to attach to the substrate. Other possible defects in the deposition phase such as the misplaced cell defect are currently under investigation. For defect tolerance the relationship between a fault-free tile and a tile with undeposited cells is very important because it defines the paradigm of processing-by-wire (PBW) for a tile-based design. It is evident that a tile inherently offers significant defect tolerance as its 9 cells closely interact in a spatial redundancy arrangement.

Processing-by-wire (PBW) is one of the fundamental paradigms of QCA. PBW relates the QCA feature of processing while transferring information, i.e. communication and processing can be *simultaneously* accomplished. PBW is applicable to both combinational and sequential circuits. In this paper, sequential circuits are not considered as analyzed in other manuscripts [12].

For evaluating the effects of PBW in QCA the software simulation tool QCADesigner[1] v1.4.0 (Unix version) is used [14]. QCADesigner v1.4.0 features different simulation engines. Throughout this paper, the coherence vector engine is used due to its accurate and detailed evaluation of QCA. The coherence vector engine is based on the density matrix approach [14] which models the power dissipative effects of QCA. The basic functionality of QCA is based on the Coulombic interaction among neighboring cells; this depends on the distance as well as the angle between the two cells. The radius of effect R defines the Coulombic interactions within an area centered on cell i, i.e. all cells within this area interact with cell i. In all simulations the cell size, is $10nm \times 10nm$ and the cell-to-cell distance is $2.5nm$. The radius of effect R is set to $40nm$.

Hereafter, the following assumptions are made: (1) Only undeposited cell defects are considered as most likely to occur in molecular implementations. (2) The one-dimensional clocking scheme is assumed: all cells in a tile are assumed to be within a timing zone; input and output cells are assumed to be in distinct timing zones. So a total of three timing zones is used in the simulations. (3) The no logic state (referred to as the *undefined state*, denoted by "-") may occur for some defective patterns due to lack of definitive polarization at the output. This happens when the polarization level is very low (less than ± 0.1) for at least some input signals, or only a spike or glitch can be observed at the output.

3. Fan-out Tile

First the so-called *fan-out tile* tile, as shown in Figure 2(a), is analyzed. The fan-out tile has one input (provided by the horizontal cell B) and two outputs (i.e. the horizontal output cell $F1$ and the vertical output cell $F2$). In the defect-free case, both outputs follow the value of the input cell, i.e. $F1$=$F2$=B (wire function), hence the tile behaves as a fan-out point in a CMOS interconnect. The fol-

1 QCADesigner is developed by the ATIPS lab at the University of Calgary in Canada.

Undeposited Cell	$F1$	$F2$	Undeposited Cell	$F1$	$F2$
none	B	B	1	B	B
2	B	B	3	B	B
4	B'	B'	5	B	B
6	B'	B	7	B	B
8	B	B'	9	B	B

Table 1. Single undeposited defect in fan-out tile

lowing observations can be made with respect to the fan-out tile in the presence of undeposited cell defects: (1) Inversion can be expected at the outputs if one of the cells connected to the corresponding output cell (i.e. cell 6 or 8) is undeposited. (2) A straightforward QCA implementation of the fan-out circuit requires only 4 cells (i.e. to deposit cells 4, 5, 6 and 8), so redundancy as basis for defect tolerance is inherently present in the design of this tile.

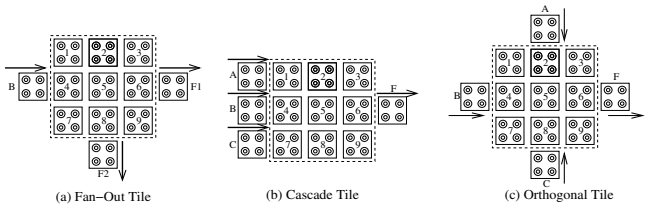

Figure 2. Three Types of Tiles

To evaluate the defect tolerance of the fan-out tile, simulation has been exhaustively performed in the presence of up to 4 undeposited cells (corresponding to a yield level just higher than 50 %). For example, Table 1 shows the results for a single undeposited cell defect. In some cases, at least one erroneous output is observed in the form of the complement of the input variable B, i.e. B'.

The simulation results are summarized in Table 2. In the presence of multiple undeposited cells, in most cases the tile produces either a wire function, or an inverting function (the output is the complement of the input). Even with four undeposited cells due to defects, in almost 90% of the cases the tile can still function either as a wire, or an inverter due to its spatial redundancy, thus providing an excellent level of functionality. The following additional observations can be drawn: (1) The probability of being in an undefined state for an output signal increases with the number of undeposited cells. Moreover, such probability is greater at $F2$ than at $F1$ once the number of defects is more than 2. (2) The probability of having a wire function in the horizontal output $F1$ is greater than for the vertical output $F2$, indicating that signal propagation in the one-dimensional clocking scheme is stronger along the direction of signal flow (perpendicular to the direction of the underlying E field). (3) The probability of having an inverting function in the vertical output $F2$ is greater than for the horizontal output $F1$. This is expected due to the 90 degree orientation of the output cell with respect to the input cell and the possible 45 degree misalignments in the defect-free cells. (4) The polarization plots for two extreme cases are shown in Figures 3(a) (no defect) and 3(b) (all nine cells undeposited). In the defect-free case, both outputs exhibit the wire function with high polarization levels. In the extreme case when all cells in the grid are undeposited, logically $F1$ still produces the wire function, while $F2$ performs the inverting function; however, both outputs have a very low polarization level (below the 0.1 value), thus an undefined state function is generated.

Horizontal Output F1				
# Undeposited Cells	1	2	3	4
# of Defective Patterns	9	36	84	126
Occurrences of Wire Func.	7	20	46	82
Wire Func. Percentage	77.8%	55.6%	54.8%	65.1%
Occurrences of INV Func.	2	16	34	36
INV func. Percentage	22.2%	44.4%	40.1%	28.6%
Occurrences of Undefined	0	0	4	8
Undefined State Percentage	0%	0%	4.76%	6.35%
Vertical Output F2				
# Undeposited cells	1	2	3	4
# of Defective Patterns	9	36	84	126
Occurrences of Wire Func.	7	21	34	43
Wire Func. Percentage	77.8%	58.3%	40.5%	34.1%
Occurrences of INV Func.	2	15	43	70
INV func. percentage	22.2%	41.7%	51.2%	55.6%
Occurrences of Undefined	0	0	7	13
Undefined state Percentage	0%	0%	8.33%	10.32%

Table 2. Functional characterization of fan-out tile with multiple undeposited cell defects

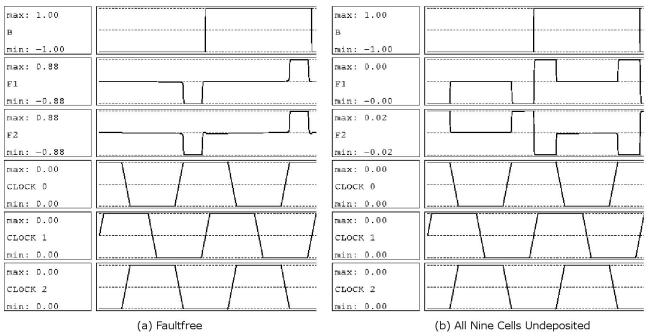

Figure 3. Polarization plot of fan-out tile

These results confirm that PBW takes place in its simplest form, i.e. it performs inversion. Moreover, the fan-out tile has excellent processing capabilities (wire and inverting functions), i.e. 93.6 % of the exhaustive number of combinations for up to 4 undeposited cells.

The average values of the maximum polarization level (magnitude) at the outputs ($F1$ and $F2$) are shown in Figure 4. The diagram shows the average magnitude of the maxi-

Undeposited Cell	F	Undeposited Cell	F
none	Maj(A,B,C)	1	B
2	B	3	B
4	Maj(A,B,C)	5	Maj(A,B,C)
6	Maj(A',B,C')	7	B
8	B	9	B

Table 3. Single undeposited defect in cascade tile

mum output polarization level when undeposited cells are incrementally present. The average magnitude of the maximum polarization level is reported for the wire function, the inverting function, the undefined state function as well as the total. The polarization level of the wire function is higher than the inverting function in all cases, thus confirming that this tile provides excellent defect-tolerant capabilities compared to other functional behaviors due to defects.

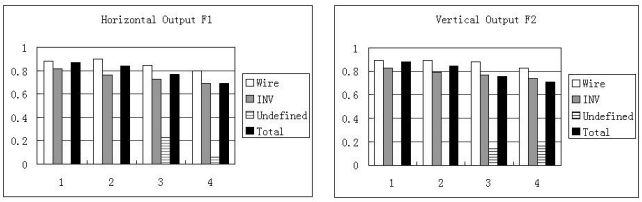

Figure 4. Average magnitude of the maximum polarization level of fan-out tile

4. Cascade Tile

Figure 2(b) shows the so-called *cascade tile*. This tile has three aligned inputs (denoted by A, B and C) at the left-hand side of the tile and a single output (denoted by F) on the right-hand side. In the defect-free case, this tile propagates the Maj(A,B,C) to F. The cascade tile corresponds to the scenario by which tiles are connected serially, thus the cells on the right vertical wire of a tile interact with the cells on the left vertical wire of the next tile (as connected in cascade). Once undeposited cell defects are present, the three input signals may also interact such that different functions can be generated at the output, i.e. the signal relation between the inputs and placement of the cells for PBW may be changed. In particular, the variants of majority function (with complemented input variables) are expected due to possible inversion through the cells of the tile. The variants of the majority function are referred to as MV-like functions (the cardinality of the MV-like function set can be at most 7).

A similar evaluation as for the fan-out tile has been pursued. The results are shown in Table 3 for the exhaustive

# of Undeposited Cells	1	2	3	4
# of Defective Patterns	9	36	84	126
Occurrences of Wire Func.	6	27	41	54
Wire Func. Percentage	66.7%	75%	48.8%	42.8%
Occurrences of INV Func.	0	6	26	48
INV Func. Percentage	0%	16.7%	30.9%	38.1%
Occurrences of MV Func.	2	1	5	3
MV Func. Percentage	22.2%	2.78%	5.95%	2.38%
Occurrences of MV-like Func.	1	0	8	11
MV-like Func. Percentage	11.1%	0%	9.52%	8.73%
Occurrences of Undefined	0	2	4	10
Undefined State Percentage	0%	5.56%	4.76%	7.49%

Table 4. Functional characterization of cascade tile with multiple undeposited cell defects

simulation under the single undeposited cell scenario; the tile operates as in the defect free scenario for 22.2% of the cases of a single undeposited cell. Table 4 shows the summarized results in the presence of undeposited cells. In most cases, the tile behaves either as a wire (albeit the output is now equal to one of the inputs), or an inverter (output is the complement of one of the inputs). In many cases, this tile can also function as an MV or MV-like circuit.

The following conclusions can be drawn from the functional characterization of the cascade tile: (1) The MV-like function with B' appears in the presence of at least 3 undeposited cell defects. (2) For all simulated cases, there is no MV-like function with all three complemented variables. In the presence of a single undeposited cell, the probability of generating the MV function is not substantial (i.e. 22%), yielding the conclusion that for defect-tolerance the cascade tile can be used rather efficiently provided A=B=C. In this last case a defect-tolerant signal flow can be attained at 88%. The case of equal inputs (i.e. A=B=C) corresponds to a defect-tolerant QCA wire by which the undeposited defects occurring at any single cell located in the upper and lower horizontal wires does not affect the condition F=B.

MV-like functions provide a significant degree of freedom in designing QCA circuits. A detailed characterization of MV-like functions can be found in [11]. For example, an MV-like function with two complemented variables can implement a two-input NAND or NOR gate (thus saving on the number of QCA cells as compared with a traditional design that utilizes an MV and an inverter). The average magnitude of the maximum polarization level of the output of the cascade tile is shown in Figure 5 for the different functions and the total. In this case, the inverting function has the lowest polarization level (except the undefined state function of course).

As the cascade tile corresponds to the case in which tiles are serially connected, these results demonstrate that PBW can occur not only in a single tile, but also between tiles. This features must be controlled properly [11] because QCA cells are usually attached to a substrate and aligned

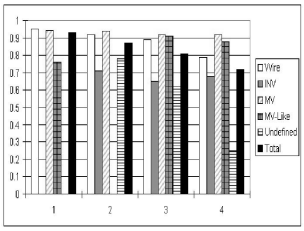

Figure 5. Average magnitude of the maximum polarization level for cascade tile

Undeposited Cell	F	Undeposited Cell	F
none	Maj(A,B,C)	1	Maj(A,B,C)
2	Maj(A',B,C)	3	Maj(A,B,C)
4	Maj(A,B,C)	5	Maj(A,B,C)
6	Maj(A',B,C')	7	Maj(A,B,C)
8	Maj(A,B,C')	9	Maj(A,B,C)

Table 5. Single undeposited defect in orthogonal tile

through parallel tracks. The inherent spatial redundancy at the inputs of the tiles can be used as a processing capability for PBW when multiple defects are present. The most obvious example is the cascade tile and its capability of providing a defect-tolerant signal propagation among tiles.

5. The Orthogonal tile

Figure 2(c) shows the so-called *orthogonal tile*. Three input cells (A, B, C) are connected to the tile at distinct sides, while an output cell (F) is provided at the remaining side. In the defect-free case, the output of this tile is Maj(A,B,C). Thus, this is the basic logic block in the tile-based design of QCA and its defect-tolerant properties are very important to assess.

The simulation results are shown in Table 5 for the one undeposited cell scenario, while Table 6 shows the statistics for the exhaustive simulation in the presence of up to 4 undeposited cells.

The following observations can be made from the simulations: (1) In almost all cases, an orthogonal tile with undeposited cells (as defects) behaves in the following two ways: wire/inverting functions or MV/MV-like functions. (2) Undeposited cell defects occurring on corner cells (cells 1, 3, 7 and 9) does not change the logic function of the tile, thus confirming the non-defect tolerant design of a majority voter. (3) In the simulations using the coherence vector engine, whenever cell 6 is undeposited, the polarization level experiences a drop. In all simulated occurrences with cell 6 present, the magnitude of the maximum polarization is above ± 0.9. However, when cell 6 is undeposited, then the magnitude of the maximum polarization level drops below

# of undeposited cells	1	2	3	4
# of Defective Patterns	9	36	84	126
Occurrences of Wire Func.	0	4	22	32
Wire Func. Percentage	0%	11.1%	26.1%	25.3%
Occurrences on INV Func.	0	4	23	51
INV Func. Percentage	0%	11.1%	27.3%	40.48%
Occurrences of MV Func.	6	13	14	8
MV Func. Percentage	66.7%	36.1%	16.6%	6.34%
Occurrences of MV-like Func.	3	11	14	11
MV-like Func. Percentage	33.3%	30.5%	16.6%	8.73%
Occurrences of Undefined	0	4	11	24
Undefined State Percentage	0%	11.1%	13.1%	19.1%

Table 6. Functional characterization of orthogonal tile with multiple undeposited cell defects

± 0.77. When other additional cells are undeposited (besides cell 6), in many cases the polarization level for some input patterns is so low that no definite logic function can be observed at the output.

The simulation results show that even with multiple undeposited cells, the tile still performs the same 4 logic functions as in the cascade tile. The results are summarized in Table 6. Note that by definition the MV-like function set does not include the defect-free MV function.

The average magnitude of the maximum polarization level of the output when a number of cells are undeposited are shown in Figure 6. As for previous tiles, in some cases the output exhibits no definite polarization level. However, in some of these cases the polarization level is quite high. This is due to the fact that for some cases, only some of the input patterns cause no or very low polarization, while other input patterns give definite outputs with high polarization levels. Also, when increasing the number of undeposited cells as defects, the decrease in polarization level is not significant.

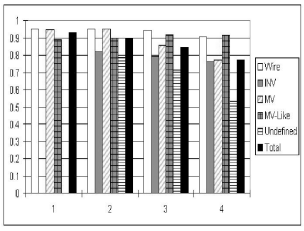

Figure 6. Average magnitude of the maximum polarization level of orthogonal tile

6. Discussion and Analysis of Results

For the polarization level in the presence of defects, the simulation results show: (1) In all tiles, the total average magnitude of the maximum polarization level decreases by

increasing the number of undeposited cells. While there is little difference between the cascade and fan-out tiles, the orthogonal tile presents a higher level of total polarization. This is caused by the placement of the three inputs and the dominant majority nature of PBW in this tile. (2) In all considered tiles, the probability of no polarization increases when increasing the number of undeposited cells. This is expected because no polarization will be encountered due to the large inter-cell spacing.

As for functional characterization, the tiles show the following behavior: (1) Both the cascade and fan-out tiles show a non-linear dependency between the number of undeposited cells and defect tolerance. By increasing the number of undeposited cells, the probability of having the wire function at the output $F1$ of the fan-out tile and the single output of the cascade tile does not monotonically decrease. This is possibly caused by the non-symmetric placement of the input/output signals in both these tiles. For example, the fan-out tile has no input or output cell directly connected to the cells along the upper horizontal wire of this tile. Therefore, polarization is transferred from the single input cell to the two output cells, thus cells on this wire are only used for moving information. (2) The presence of new logic functions (such as the inverting function in the fan-out tile, or the MV-like functions in the cascade and orthogonal tiles) shows that defect tolerance can be utilized in accomplishing PBW even under a large number of defective cells and low yield levels. The undefined state occurs in the presence of at least 2 (for the fan-out tile) and/or 3 (for the cascade and orthogonal tiles) undeposited cells.

7. Conclusion

In this paper, the defect tolerance of QCA tiles has been analyzed. The simulation results have shown that PBW by tiling in the presence of undeposited cell defects is still very versatile and robust. The capability of generating the defect-free function is preserved with very high probability for at most one defective cell per tile. Even in the presence of multiple undeposited cells, tiles can still be used in most cases to perform useful logic functions. Throughout the exhaustive simulation (up to 4 defective cells per tile), the following logic functions consistently appear at the output(s), i.e. (1) the wire function, (2) the inverting function, (3) the majority function, (4) majority-like functions (i.e. majority function with one or two complemented variables). This suggests that tile-based design is not restrictive as using an a-priori device-based configurations in the assembly of QCA circuits. This modularity is reinforced by the flexibility in generating the same set of functions using different tiles with various arrangements for the input/output cells.

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