Defect Tolerant N^2-Transistor Structure for Reliable Nanoelectronic Designs

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Abstract

Nanodevices based circuit design will be based on the acceptance that a high percentage of devices in the design will be defective. In this work, we investigate a defect tolerant technique that adds redundancy at the transistor level and provides built-in immunity to permanent defects (stuck-open, stuck-short and bridges). The proposed technique is based on replacing each transistor by N^2-transistor structure ($N \geq 2$) that guarantees defect tolerance of all N-1 defects as validated by theoretical analysis and simulation. As demonstrated by extensive simulation results using ISCAS 85 and 89 benchmark circuits, the investigated technique achieves significantly higher defect tolerance than recently reported nanoelectronics defect-tolerant techniques (even with up to 4 to 5 times more transistor defect probability) and at reduced area overhead. For example, the quadded-transistor structure technique requires nearly half the area of the quadded logic technique.

1. Introduction

With CMOS technology reaching the scaling limits, the need for alternative technologies became necessary. Nanotechnology-based fabrication is expected to offer the extra density and potential performance to take electronic circuits the next step. It is estimated that molecular electronics can achieve very high densities (10^{12} devices per cm^2) and operate at very high frequencies (of the order of THz) [1]. Several successful nano-scale electronic devices have been demonstrated by researchers, some of the most promising being carbon nanotubes (CNT) [2], silicon nano-wires (NW) [3, 4], and quantum dot cells [5]. It is expected, however, that nanodevices will suffer from significantly increased permanent failure rates mainly due to the fundamental limitations of the fabrication processes that limit the yield of such devices [5]. At these nanometer scales, the small cross section areas of wires make them fragile, increasing the likelihood that they will break during assembly. Moreover, the contact area between nanowires, and between nanowires and devices, depends on a few atomic-scale bonds resulting in some connections being poor and effectively unusable [6, 7]. Hewlett-Packard has fabricated 8x8

crossbar switches using molecular switches at the crosspoints [7]. They observed that only 85% of the switches were programmable while the other 15% were defective. Therefore, the necessity to cope with intrinsic defects at the circuit level must be recognized as a key aspect of nanodevices-based designs. To implement such robustness and defect tolerance, circuit design techniques capable of absorbing a large number of defects and still be able to perform their functions need to be investigated.

In the context of reliable nanoelectronics, two main approaches have been proposed: defect tolerance and defect avoidance [8]. Defect tolerance techniques are based on adding redundancy in the design to tolerate defects or faults. However, defect avoidance techniques are based on identifying the defects and avoiding them possibly through the use of reconfigurable blocks. Recently, traditional fault tolerance techniques such as triple-modular redundancy, triple interwoven redundant logic, and quadded logic have been investigated [9] with the aim to improve the defect tolerance of nanoelectronics design. It has been demonstrated that such techniques are capable of making nanoelectronic circuits more robust to defects.

Triple-modular redundancy (TMR) is based on triplicating each module of a given size followed by an arbitration unit deciding the correct value based on majority. Figure 1 (b) shows the application of TMR technique on the module given in Figure 1 (a). The module is replicated three times and the outputs of the three modules are fed to a majority gate. This way all errors occurring in only one of the replicated modules will be tolerated. The reliability of such designs is limited by that of the final arbitration unit, making the approach difficult in the context of highly integrated nanosystems [8]. A TMR circuit can be further triplicated. The obtained circuit thus has nine copies of the original module and two layers of majority gates. This process can be repeated if necessary, resulting in a technique called cascaded triple modular redundancy (CTMR) or recursive triple modular redundancy (RTMR). It is shown in [10] that using CTMR in a nanochip with large nanoscale devices would require an extremely low device error rate. It is also shown in [11] that recursive voting leads to a double exponential decrease in a circuit's failure probability. However, a single error in the last majority gate can cause an incorrect result, hampering the technique's effectiveness.

Quadded logic [9] requires four times the circuit size. A quadded circuit implementation based on NAND gates replaces each NAND gate with a group of four NAND gates, each of which has twice as many inputs as the one it replaces. The four outputs of each group are divided into two sets of outputs, each providing inputs to two gates in a succeeding stage. In order to guarantee single error tolerance, it must be ensured that the interconnect set pattern at the output of a stage differ from the interconnect set patterns of any of its inputs. The interconnect set pattern determines the set of gates to which an interconnect is connected. Figure 1 (c) shows the application of quadded logic technique on the module given in Figure 1 (a).

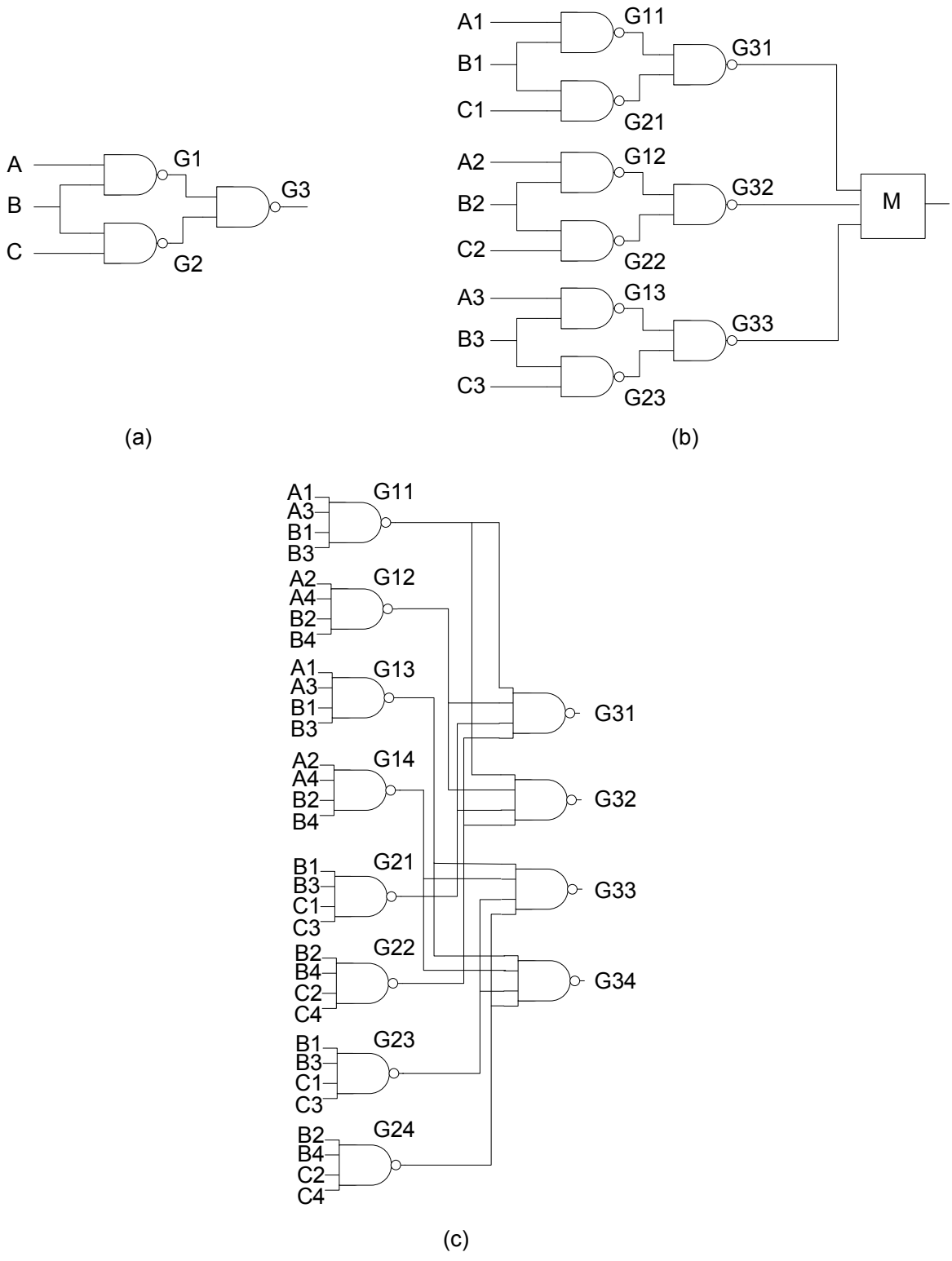

Figure 1 (a) Original circuit, (b) TMR circuit, (c) Quadded logic circuit.

For example, the set pattern for input A with respect to gate G1 is {(1, 3), (2, 4)} which indicates that inputs A1 and A3 are connected to gates G11 and G13, while inputs A2 and A4 are connected to gates G12 and G14. The interconnect set pattern for gate G1 is {(1, 2), (3, 4)}, which is different from the set pattern of any of its inputs. Note that the equation of G31 is equal to A1A3B1B3 + A2A4B2B4 + B1B3C1C3 + B2B4C2C4. This guarantees the tolerance of any single error at any of the interconnects of the inputs A, B, and C. The same applies for the remaining gates. While quadded logic guarantees tolerance of most single errors, errors occurring at the outputs of the last two stages of logic may not be corrected [9].

The previous approaches of defect-tolerance for reliable nanoelectronics have focused on adding redundancy at the functional or unit level such as TMR [10, 11], or gate level such as quadded logic [9]. In this paper, we propose adding redundancy at the transistor level and show that it provides higher defect tolerance than unit and gate levels and at reduced area overhead.

Adding redundancy at the transistor level itself to improve reliability is not new. Indeed, in [12, 13] transistors were employed to improve the reliability of relay networks. In this work, we investigate the effectiveness of transistor-level approach when applied to ISCAS benchmark circuits, since in [12, 13] bipolar transistors were employed with very simple circuits. We investigate circuit defect tolerance based on N^2-transistor structure with respect to stuck-open, stuck-short and bridging defects. Furthermore, a comparison is made with recent approaches proposed for defect tolerance in nanoelectronics.

This paper is organized as follows. The proposed defect tolerant technique is described in Section 2. Experimental results analyzing the defect tolerance of stuck-open, stuck-short and bridging defects are given in Section 3. Section 4 concludes the paper.

2. Proposed Defect Tolerant Technique

IBM has recently demonstrated experimentally that carbon nanotubes can exhibit electrical characteristics that are similar to that of the state-of-the-art Si-based MOSFETs [14]. In this work, we investigate defect tolerance based on adding redundancy at the transistor-level for electronic circuits. Our work is focused on transistor stuck-open, stuck-short and bridges between gates of transistors. A transistor is considered defective if its expected behavior changes regardless of the type of defect causing it. In order to tolerate single defective transistors, each transistor, A, is replaced by a quadded-transistor structure implementing either the logic function (A+A)(A+A) or the logic function (AA)+(AA), as shown in Figure 2. In both of the quadded-transistor structures shown in Figure 2 (b) & (c), any single transistor defect (stuck-open, stuck-short, AND/OR-bridge) will not change the logic behavior, and hence the defect is tolerated. It should be observed

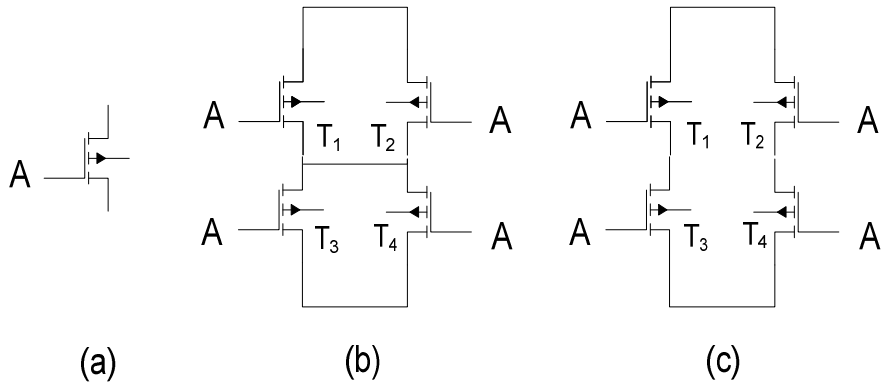

Figure 2 (a) Transistor in original gate implementation, (b) First quadded-transistor structure, (c) Seconed quadded-transistor structure.

that for NMOS transistors, OR-bridge and stuck-short defects produce the same behavior while AND-bridge and stuck-open defects have the same behavior. Similarly, for PMOS transistors, OR-bridge and stuck-open defects produce the same behavior while AND-bridge and stuck-short defects have the same behavior.

Double stuck-open (or their corresponding bridge) defects are tolerated as long as they do not occur in any two parallel transistors (T_1&T_2 or T_3&T_4 for the structure in Figure 2(b), and T1&T2, T_1&T_4, T_3&T_2 or T_3&T_4 for the structure in Figure 2(c)). Double stuck-short (or their corresponding bridge) defects are tolerated as long as they do not occur in any two series transistors (T_1&T_3, T_1&T_4, T_2&T_3 or T_2&T_4 for the structure in Figure 2(b), and T_1&T_3 or T_2&T_4 for the structure in Figure 2(c)). In addition, any triple defect that does not include two parallel stuck-open defects or two series stuck-short defects or their corresponding bridging defects is tolerated. Thus, one can easily see that using either of the quadded-transistor structures, the defect tolerance of gate implementation could be significantly improved.

It should be observed that the quadded-transistor structures have the same effective resistance as the original transistor. However, in the presence of a single defect, the worst case effective resistance of the first quadded-transistor structure (Figure 2(b)) is 1.5R while that of the second quadded-transistor structure (Figure 2(c)) is 2R, where R is the effective resistance of a transistor. This occurs in the case of single stuck-open (or corresponding bridge) defects. For tolerable multiple defects, the worst case effective resistance of both structures is 2R. To reduce the impact on delay in presence of defects, the first quadded-transistor structure (Figure 2(b)) is adopted in this work.

2.1 Analysis of Circuit Failure Probability and Defect Tolerance

In this subsection, we analyze the circuit failure probability and defect tolerance of N^2-transistor structure. We first determine the probability of circuit failure given a transistor defect probability using quadded-transistor structures. A transistor is considered defective if it does not function properly due to manufacturing defects.

Theorem I: Given a transistor defect probability, *P*, the probability of quadded-transistor structure failure is $P_q = \frac{3}{2}P^2 - \frac{1}{2}P^3$.

Theorem I is proved in Appendix.

Theorem II: Given a transistor-defect probability, *P*, and a circuit with *N* quadded-transistor structures, the probability of circuit failure and circuit defect tolerance are:

$$P_f = \sum_{i=1}^{N} (-1)^{i-1} \binom{N}{i} (P_q)^i$$

$$DT = 1 - P_f = 1 - \sum_{i=1}^{N} (-1)^{i+1} \binom{N}{i} (P_q)^i .$$

Theorem II is based on the inclusion-exclusion principle [15]. The probability of circuit failure may also be computed based on the binomial distribution as $P_f = \sum_{i=1}^{N} \binom{N}{i} (P_q^i)(1-P_q)^{N-i}$, which produces equivalent results.

It should be observed that while the result above represents the exact circuit failure probability for stuck-open and stuck-short defects, it represents an upper bound for bridging defects. This is due to the fact that not all bridging defects that result in a faulty quadded-transistor structure result in a faulty gate behavior. For example, AND-bridging defects between gates of transistors within the same NAND gate do not change the gate behavior regardless of their multiplicity. Similarly, OR-bridging defects between gates of transistors within the same NOR gate do not change the gate behavior regardless of their multiplicity.

The quadded-transistor structure, given in Figure 2(b), can be generalized to an N^2-transistor structure, where $N \geq 2$. An N^2-transistor structure is composed of N blocks connected in series with each block composed of N parallel transistors, as shown in Figure 3. An N^2-transistor structure guarantees defect tolerance of all

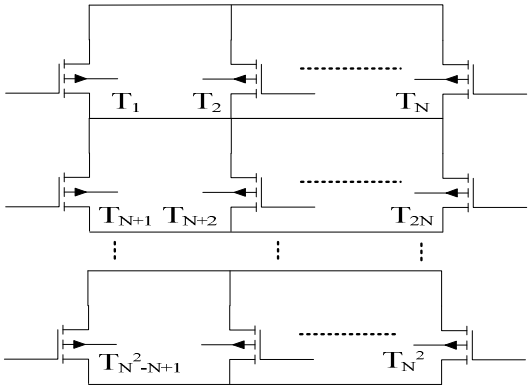

Figure 3 Defect-tolerant N^2-transistor structure.

defects of multiplicity less than or equal to (N-1) in the structure. Hence, a large number of multiple defects can be tolerated in a circuit implemented based on these structures.

Next, we determine the probability of circuit failure for a nona-transistor structure, where N=3.

Theorem III: Given a transistor defect probability, P, the probability of a nona-transistor structure failure is $P_n = \frac{30}{8}P^3 - \frac{81}{16}P^4 + \frac{27}{8}P^5 - \frac{21}{16}P^6 + \frac{31}{128}P^7 - \frac{19}{128}P^8 + \frac{5}{32}P^9$.

Theorem III is proved in Appendix.

Similarly, given a transistor-defect probability, P, and a circuit with N nona-transistor structures, the probability of circuit failure and circuit defect tolerance are computed based on Theoem II replacing P_q with P_n.

Based on the analysis of the quadded- and nona-transistor structures, it can be deduced that the probability of failure for an N^2-transistor structure will be $O(P^N)$. The N^2-transistor structure, for N>2, may be applied selectively for critical gates due to its increased overhead.

An interesting advantage of the N^2-transistor structure is that it fits well in existing design and test methodologies. In synthesis, a library of gates implemented based on the N^2-transistor structure will be used in the technology mapping process. The same testing methodology will be used assuming testing is done at the gate level based on the single stuck-at fault model. So, the same test set derived for the original gate-level structure can be used without any change.

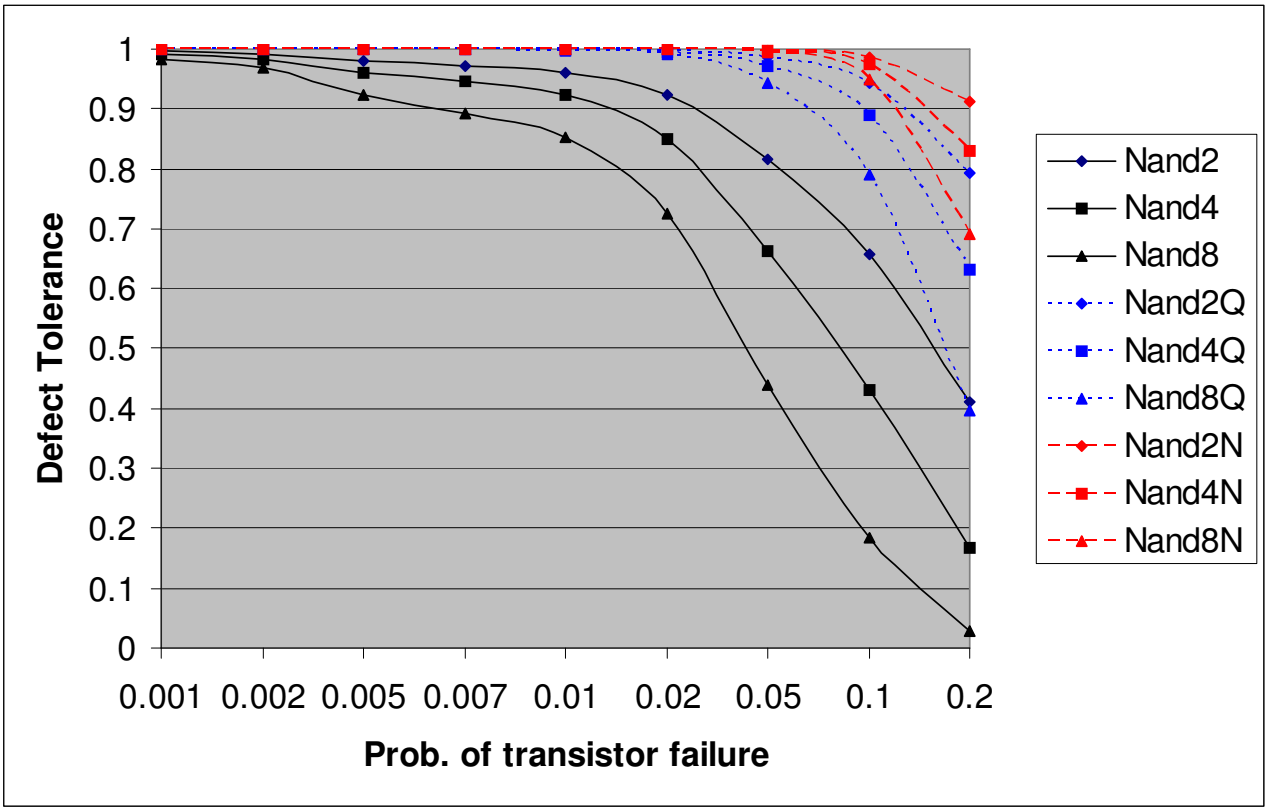

Figure 4 Gate defect tolerance comparison between quadded-transistor structure (Q), nona-transistor structure (N) and complementary CMOS.

Figure 4 compares the defect tolerance of several NAND gates of various inputs, including 2, 4 and 8, implemented using the quadded-transistor structure, the nona-transistor structure and conventional complementary (pull-up, pull-down) CMOS implementation for stuck-open and stuck-short defects. As can be seen, the defect tolerance of gates implemented using the quadded-transistor and nona-transistor structures is significantly higher than that of conventional gate implementation. For example, for an 8-input NAND gate, with a probability of transistor failure = 10%, the gate defect tolerance for the nona-transistor structure-based design is 95%, the gate defect tolerance for the quadded-transistor structure-based design is 79%, while the gate defect tolerance for the conventional CMOS implementation is 19%. Furthermore, as the number of inputs increases, the probability of gate failure increases and defect tolerance decreases, as expected.

2.2 Impact on Area, Delay and Power

The gate capacitance that the quadded-transistor structure induces on the gate connected to the input A is four times the original gate capacitance. This has an impact on both delay and power dissipation. However, as shown in [16], a gate with higher load capacitance has better noise rejection curves and hence is more resistant to soft errors resulting in noise glitches.

Table 1. Area, delay and power values of basic 0.5µ cells designed using quadded-transistor structure (Fig. 3b) and complementary (pull-up, pull-down) CMOS.

Characteristics		INV		NAND2		NOR2	
		CMOS	QT	CMOS	QT	CMOS	QT
Delay (ps)	Fall	270.8	763.0	416.6	1143	285.7	902.5
	Rise	566.6	1775	606.9	2217	1124	3986
	T_{PHL}	169.6	469.0	239.1	604.9	180.7	557.6
	T_{PLH}	300.3	973.3	324.9	1182	548.2	1965
Dyn. Power (mW)	Avg.	0.120	0.340	0.175	0.533	0.180	0.542
	Max.	1.469	2.602	1.709	2.602	1.691	2.606
	RMS	0.355	0.665	0.431	0.815	0.432	0.810
Area (um^2)		89	208	128	402	126	397

To determine the area, delay and power impact of the quadded-transistor structure, we have designed, using Magic, two libraries based on the 0.5u CMOS Alcatel process. The libraries are composed of three basic cells, Inverter (INV), 2-input Nand gate (NAND2), and 2-input Nor gate (NOR2) based on the quadded-transistor structure and the conventional CMOS implementation. Then, we obtained delay and power characteristics using SPICE simulations based on the extracted netlists. Delay characteristics were calculated after supplying proper load and drive conditions. For all the cells the drive was composed of two inverters in series and the load was composed of two inverters in parallel. The inverters were chosen from the same library. Dynamic power was measured using the .measure command in SPICE for the same period of time in both libraries. Table 1 summarizes delay, power and area characteristics of the two libraries. The delay and power consumption of cells designed based on the quadded-transistor structure are in the worst case 3.65 times more than the conventional cells and the cell area is about 3 times more.

While the quadded-transistor structure increases the area, this increase is less than other gate-level defect tolerance techniques as will be shown in the experimental results. As with all defect tolerance techniques, the increase in area, delay and power is traded off by more circuit defect tolerance. This is justified given that it is predicted that nanotechnology will provide much higher integration densities, speed and power advantages.

3. Experimental Results

To demonstrate the effectiveness of the N^2-transistor structure technique, we have performed experiments on a number of the largest ISCAS85 and ISCAS89 benchmark circuits (replacing flip-flops by inputs and outputs). Two types of permanent defects are analyzed separately: transistor stuck-open and stuck-short defects, and AND/OR bridging defects.

For evaluating circuit failure probability and defect tolerance, we adopt the simulation-based model used in [9]. We compare circuit defect tolerance based on the quadded-transistor and nona-transistor structures with the compared approaches in [9] including Triple Interwoven Redundancy (TIR) and Quadded logic. We use a complete test set *T* that detects all detectable single stuck-at faults in a circuit. We have used test sets generated by Mintest ATPG tool [17]. To compute the circuit failure probability, F_m, resulting from injecting *m* defective transistors, we use the following procedure:

1. Set the number of iterations to be performed, *I*, to 1000 and the number of failed simulations, *K*, to 0.
2. Simulate the fault-free circuit by applying the test set *T*.
3. Randomly inject *m* transistor defects.
4. Simulate the faulty circuit by applying the test set *T*.
5. If the outputs of the fault-free and faulty circuits are different, increment *K* by 1.
6. Decrement *I* by 1 and if *I* is not 0 goto step 3.
7. Failure Rate $F_m = K/1000$.

Assuming that every transistor has the same defect probability, *P*, and that defects are randomly and independently distributed, the probability of having a number of *m* defective transistors in a circuit with *N* transistors follows the binomial distribution [9] as shown below:

$$P(m) = \binom{N}{m} P^m \times (1-P)^{N-m}$$

Assuming the number of transistor defects, *m*, as a random variable and using the circuit failure probability F_m as a failure distribution in *m*, the probability of circuit failure, *F*, and circuit defect tolerance, *DT*, are computed as follows [9]:

$$F = \sum_{m=0}^{N} F_m \times P(m)$$

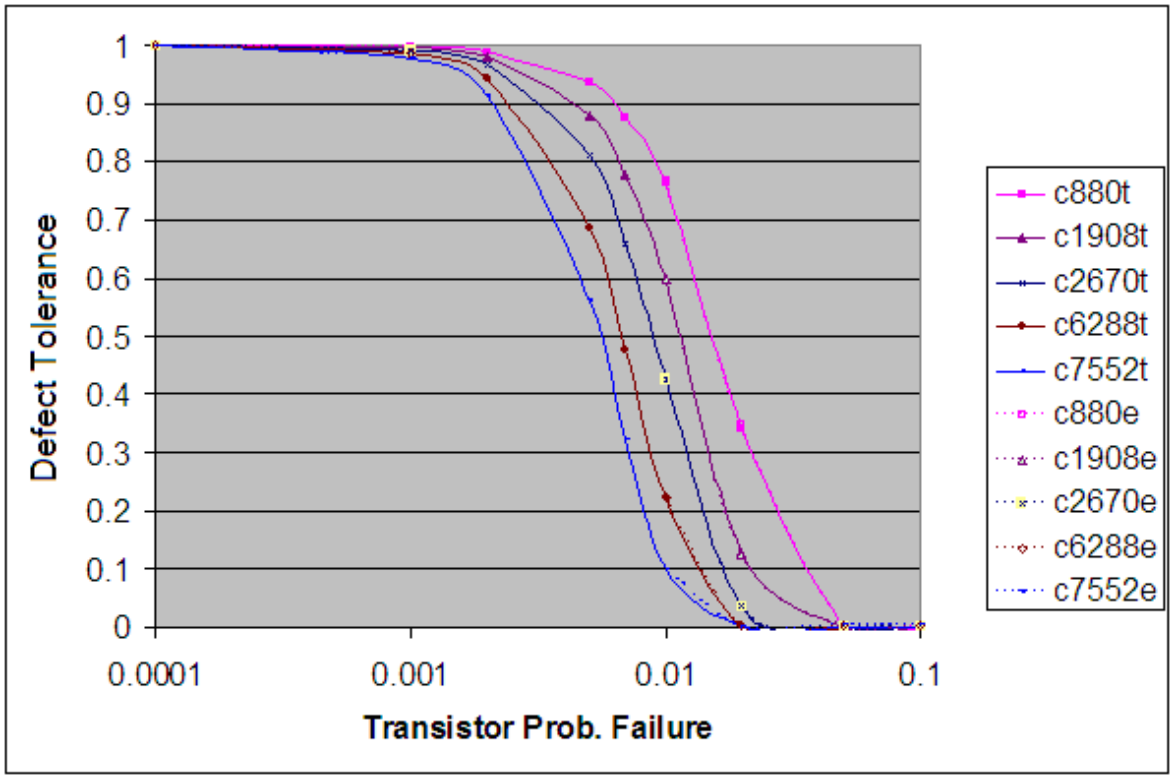

Figure 5 Defect tolerance obtained both theoretically (t) and experimentally (e) based on quadded-transistor structure and stuck-open and stuck-short defects.

$$DT = 1 - F = 1 - \sum_{m=0}^{N} F_m \times P(m)$$

3.1 Stuck-Open & Stuck-Short Defect Analysis

Figure 5 shows the reliability of some of the ISCAS85 benchmark circuits obtained both theoretically and experimentally based on the above simulation procedure and formulas for stuck-open and stuck short defects. As can be seen, there is almost identical match, clearly validating the derived theoretical results.

In Figure 6, we compare the probability of circuit failure for a given percentage of stuck-open and stuck-short defects between the quadded-transistor structure (QT), nona-transistor structure (NT), quadded logic (QL) [9] and TIR logic [9]. It should be observed that TIR is a generalization of TMR logic. The comparison is made based on an 8-stage cascaded half adder circuit used in [9]. TIR logic is implemented by adding a majority gate for each sum and carry-out signal at each stage. Majority gate is also implemented as a single gate. As can be seen, adding transistor-level defect tolerance generates circuits with significantly less

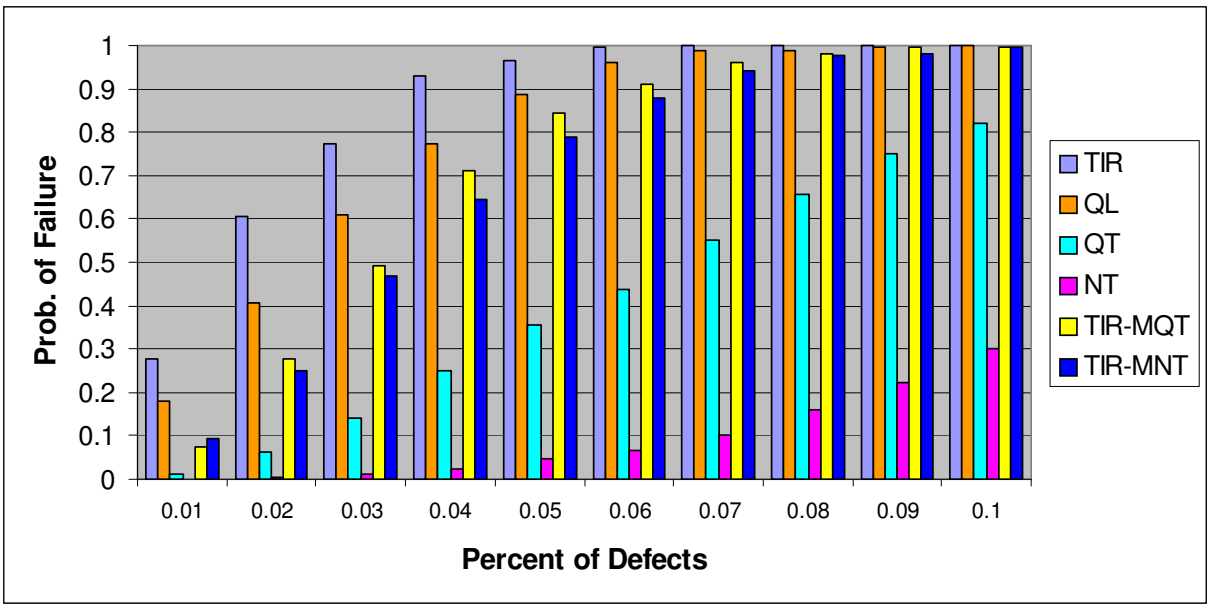

Figure 6 Comparison of circuit failure probability for an 8-stage cascaded half-adder circuit for stuck-open and stuck short defects.

probability of circuit failure than those that add defect tolerance at gate level (QL) and unit level (TMR). This is in addition to smaller area overhead in terms of smaller number of transistors used in the case of quadded-transistor structure. The number of transistors in the quadded-transistor structure implementation is 512, while it is 608 for TIR logic, 1024 for quadded logic and 1152 for the nona-transistor structure.

The probability of circuit failure for TIR and TMR logic can be improved by enhancing the reliability of majority gates. We have implemented the majority gates in the 8-stage cascaded half adder TIR logic circuit based on the quadded-transistor structure (TIR-MQT) and the nona-transistor structure (TIR-MNT). As shown in Figure 6, the defect tolerance of the implemented circuit has improved compared to TIR circuit at the expense of increased number of transistors (1280 for TIR-MQT and 2400 for TIR-MNT). However, the defect tolerance of the individual modules needs also more enhancements to improve the overall defect tolerance of the circuit. This shows an interesting potential application of the N^2-transistor structure in improving the defect tolerance of voter-based redundancy techniques.

For TMR to be effective, a careful balance between the module size and the number of majority gates used needs to be made. For this reason, we focus comparison of the defect tolerance of ISCAS benchmark circuits between the quadded-transistor and nona-transistor structures and quadded logic.

Table 2. Comparison of circuit failure probability between quadded-transistor structure and quadded logic approaches for stuck-open and stuck-short defects.

Circuit	Quadded-Transistor Structure					Quadded Logic				
	#Trans	0.25%	0.5%	0.75%	1%	#Trans	0.25%	0.5%	0.75%	1%
c880	7208	0.015	0.060	0.135	0.237	13616	0.452	0.783	0.905	0.978
c1355	9232	0.023	0.082	0.176	0.287	18304	0.531	0.846	0.975	0.995
c1908	13784	0.030	0.115	0.248	0.400	24112	0.673	0.94	0.984	≈1
c2670	22672	0.047	0.188	0.375	0.569	36064	0.958	0.999	≈1	≈1
c3540	30016	0.067	0.238	0.457	0.674	46976	0.59	0.901	0.996	0.999
c5315	45048	0.095	0.341	0.614	0.816	74112	0.991	≈1	≈1	≈1
c6288	40448	0.085	0.307	0.576	0.787	77312	0.685	0.962	0.999	≈1
c7552	61600	0.136	0.441	0.732	0.909	96816	0.985	≈1	≈1	≈1
s5378	35608	0.081	0.282	0.521	0.737	59760	≈1	≈1	≈1	≈1
s9234	74856	0.166	0.510	0.791	0.939	103488	0.999	≈1	≈1	≈1
s13207	103544	0.212	0.625	0.888	0.980	150448	≈1	≈1	≈1	≈1
s15850	128016	0.257	0.697	0.936	0.992	171664	≈1	≈1	≈1	≈1

A comprehensive comparison of the probability of circuit failure between the quadded-transistor structure and the quadded logic is given in Table 2 for several percentages of injected stuck-open and stuck-short defects. For all the circuits, the quadded-transistor technique achieves significantly lower circuit failure probability than the quadded logic technique for the same and for twice the percentage of injected defects. For 10 out of 12 circuits, it achieves lower failure probability with four times the percentage of injected defects. In Table 3, we report the defect tolerance results obtained based on the simulation procedure outlined above for the quadded-transistor structure and quadded logic approaches for several transistor defect probabilities based on stuck-open and stuck-short defects. The effectiveness of the quadded-transistor structure technique is clearly demonstrated by the results as it achieves higher circuit defect tolerance with 4 to 5 times more transistor defect probability. This is in addition to the observation that the quadded-transistor structure technique requires nearly half the area of the quadded logic technique as indicated by the number of transistors.

In Table 4, we report the circuit defect tolerance for the nona-transistor structure technique for several transistor defect probabilities based on stuck-open and stuck-short defects. The nona-transistor structure technique achieves higher circuit defect tolerance than the quadded logic technique with 20 times more transistor defect probability. It also achieves higher circuit defect tolerance than the quadded-transistor structure technique with 4 to 5 times more transistor defect probability.

Table 3. Comparison of circuit defect tolerance between quadded-transistor structure and quadded logic approaches for stuck-open and stuck-short defects.

Circuit	Quadded-Transistor Structure						Quadded Logic					
	#Trans	0.01%	0.1%	0.2%	0.5%	1%	#Trans	0.01%	0.1%	0.2%	0.5%	1%
c880	7208	0.999	0.997	0.989	0.934	0.767	13616	0.979	0.822	0.651	0.283	0.042
c1355	9232	0.999	0.996	0.986	0.917	0.713	18304	0.975	0.765	0.575	0.187	0.008
c1908	13784	0.999	0.994	0.979	0.879	0.596	24112	0.975	0.755	0.558	0.261	0.001
c2670	22672	0.999	0.991	0.967	0.809	0.427	36064	0.904	0.350	0.112	0.001	0.000
c3540	30016	0.999	0.989	0.956	0.755	0.327	46976	0.981	0.805	0.614	0.237	0.000
c5315	45048	0.999	0.984	0.935	0.656	0.185	74112	0.853	0.227	0.034	0.001	0.000
c6288	40448	0.999	0.986	0.941	0.685	0.222	77312	0.971	0.718	0.465	0.024	0.000
c7552	61600	0.999	0.978	0.912	0.562	0.101	96816	0.874	0.292	0.077	0.000	0.000
s5378	35608	0.999	0.985	0.948	0.717	0.263	59760	0.811	0.134	0.015	0.001	0.000
s9234	74856	0.999	0.972	0.894	0.496	0.061	103488	0.821	0.140	0.001	0.000	0.000
s13207	103544	0.999	0.961	0.856	0.379	0.023	150448	0.518	0.008	0.000	0.000	0.000
s15850	128016	0.999	0.953	0.825	0.302	0.008	171664	0.576	0.009	0.000	0.000	0.000

3.2 Bridging Defect Analysis

In order to analyze the defect tolerance of the quadded-transistor structure and the quadded logic techniques to bridging defects, the same simulation-based model was used. The experiments were performed on the same set of ISCAS circuits. The bridging defects were injected randomly between the gates of the defected transistor and one of its neighbors, located within a window of local transistors in the netlist (±8 transistors). Both *AND* and *OR* bridging defects were injected equally. It should be observed that for injecting m defective transistors due to bridges, only $m/2$ bridges need to be injected.

Table 5 shows the results obtained for several percentages of injected bridging defects for the quadded-transistor and the quadded logic techniques. As can be seen, the quadded-transistor structure technique exhibits a much lower failure probability than quadded-logic technique. The quadded-transistor structure technique achieves failure rates lower than quadded-logic for the same and twice the percentage of injected bridging faults. For 0.25% of injected defects, it achieves failure rates nine times less than quadded-logic and three times less for 0.5% of injected defects in most of the circuits. It should be observed that for the same percentage of defective transistors, the failure rate for bridging defects is less than that of stuck-open and stuck-short defects. This is due to the fact that not all bridging defects will result in a faulty gate behavior.

Table 4. Circuit defect tolerance for the nona-transistor structure approach for stuck-open and stuck-short defects.

Circuit	#Trans.	0.01%	0.1%	0.2%	0.5%	1%	2%	5%
c880	16218	≈1	0.999	0.999	0.999	0.993	0.948	0.453
c1355	20772	≈1	0.999	0.999	0.998	0.991	0.934	0.363
c1908	31014	≈1	0.999	0.999	0.998	0.987	0.904	0.22
c2670	51012	≈1	0.999	0.999	0.997	0.979	0.847	0.083
c3540	67536	≈1	0.999	0.999	0.996	0.972	0.803	0.037
c5315	101358	≈1	0.999	0.999	0.994	0.959	0.719	0.007
c6288	91008	≈1	0.999	0.999	0.995	0.963	0.744	0.011
c7552	138600	≈1	0.999	0.999	0.992	0.944	0.637	0.0011
s5378	80118	≈1	0.999	0.999	0.995	0.967	0.771	0.02
s9234	168426	≈1	0.999	0.999	0.991	0.933	0.578	0.00027
s13207	232974	≈1	0.999	0.999	0.988	0.908	0.469	0.00001
s15850	288036	≈1	0.999	0.999	0.985	0.888	0.392	0

In order to minimize the required CPU intensive simulations and since the defect tolerance of circuits in the presence of stuck-open and stuck short defects is a lower bound on that in the presence of bridge defects, the defect tolerance of the nona-transistor structure with respect to bridging defects is not performed.

4. Conclusion

In this work, we have investigated a defect tolerant technique based on adding redundancy at the transistor level. The proposed technique provides defect tolerance against a large number of permanent defects including stuck-open, stuck-short and bridging defects. Experimental results have demonstrated that the proposed technique provides significantly less circuit failure probability and higher defect tolerance than recently investigated techniques based on gate level (quadded logic) and unit level (Triple modular redundancy). This improvement is achieved at less area overhead; for example 50% less transistors than quadded logic in the case of using the quadded-transistor structure. The results have been investigated theoretically and by simulation using large ISCAS 85 and 89 benchmark circuits.

Whilst the paper focused on tolerance of transistor defects, the proposed technique is capable of tolerating defects in interconnect, which is seen by many researchers as a source of unreliability in nanodevices. This can be achieved by using four parallel interconnect lines to connect the driving gate to the four transistors in a quadded-transistor structure. This attractive feature adds to the credibility of the proposed approach for reliable nanoelectronics.

Table 5. Comparison of circuit failure probability between quadded-transistor structure and quadded logic approaches for bridging defects.

Circuit	Quadded-Transistor Structure					Quadded Logic				
	#Trans	0.25%	0.5%	0.75%	1%	#Trans	0.25%	0.5%	0.75%	1%
c880	7208	0.011	0.046	0.084	0.134	13616	0.168	0.279	0.437	0.539
c1355	9232	0.008	0.047	0.095	0.158	18304	0.195	0.339	0.498	0.571
c1908	13784	0.018	0.091	0.201	0.272	24112	0.384	0.690	0.827	0.916
c2670	22672	0.034	0.110	0.229	0.381	36064	0.768	0.945	0.988	≈1
c3540	30016	0.043	0.171	0.325	0.496	46976	0.303	0.532	0.683	0.803
c5315	45048	0.058	0.208	0.419	0.631	74112	0.648	0.866	0.953	0.984
c6288	40448	0.041	0.138	0.292	0.452	77312	0.163	0.324	0.480	0.588
c7552	61600	0.088	0.294	0.512	0.699	96816	0.574	0.837	0.935	0.973
s5378	35608	0.060	0.179	0.392	0.671	59760	0.672	0.793	0.924	0.940
s9234	74856	0.079	0.324	0.572	0.802	103488	0.733	0.929	0.982	0.995
s13207	103544	0.119	0.386	0.661	0.853	150448	0.998	≈1	≈1	≈1
s15850	128016	0.110	0.357	0.649	0.846	171664	0.987	≈1	≈1	≈1

Appendix

Theorem I & Theorem III are proved with respect to stuck-open and stuck-short defects as bridge defects have equivalent behaviors to them as explained earlier.

Proof of Theorem I:

If there are only two defective transistors in a quadded-transistor structure, then we have four possible pairs of stuck-open and stuck short defects. In all cases, only one of those pair of defects produces an error. Thus, the probability of failure in this case is $\frac{1}{4}*\binom{4}{2}P^2(1-P)^2=\frac{3}{2}P^2(1-P)^2$

If we assume that three transistors are defective, then we have eight possible combinations of stuck-open and stuck short defects. In all cases, five out of those combinations produce an error. Thus, the probability of failure in this case is

$$\frac{5}{8}*\binom{4}{3}P^3(1-P)\ =\frac{5}{2}P^3(1-P)$$

If four transistors are assumed defective, then in this case there will always be an error and the probability of failure is $1*\binom{4}{4}P^4=P^4$

Thus, the probability of quadded-transistor structure failure is

$$P_q = \frac{3}{2}P^2(1-P)^2 + \frac{5}{2}P^3(1-P) + P^4$$

$$= \frac{3}{2}P^2 - 3P^3 + \frac{3}{2}P^4 + \frac{5}{2}P^3 - \frac{5}{2}P^4 + P^4$$

$$= \frac{3}{2}P^2 - \frac{1}{2}P^3 .$$

Proof of Theorem III:

If there are only two defective transistors in a nona-transistor structure, the defect will always be tolerated. If there are three defective transistors in a nona-transistor structure, then we have eight possible combinations of stuck-open and stuck short defects. In all cases, only one of those combinations of defects produces an error for 3 unique parallel (stuck-open) and 27 unique series (stuck-short) defective transistor structures. Thus, the probability of failure in this case is

$$(3 * \frac{1}{8} + 27 * \frac{1}{8}) P^3 (1-P)^6 .$$

If we assume that four transistors are defective, then we have sixteen possible combinations of stuck-open and stuck short defects. Among those, only two combinations produce an error for 18 unique parallel transistor structures. Moreover, only three combinations produce an error for 81 unique series transistor structures. Thus, the probability of failure in this case is

$$(18 * \frac{2}{16} + 81 * \frac{3}{16}) P^4 (1-P)^5$$

If we assume that five transistors are defective, then we have thirty two possible combinations of stuck-open and stuck short defects. Among those, only four combinations produce an error for 18 unique parallel transistor structures. Moreover, only eleven combinations produce an error for 27 series transistor structures which are overlapping with parallel transistor structures. Also, nine combinations produce an error for 81 series transistor structures which are non-overlapping with parallel transistor structures. Thus, the probability of failure in this case is

$$(18 * \frac{4}{32} + 27 * \frac{11}{32} + 81 * \frac{9}{32}) P^5 (1-P)^4$$

If we assume that six transistors are defective, then we have sixty-four possible combinations of stuck-open and stuck short defects. Among those, only fifteen combinations produce an error for 3 unique parallel transistor structures. Moreover, only twenty-nine combinations produce an error for 54 series transistor structures which are overlapping with parallel transistor structures. Also, twenty-seven combinations produce an error for 27 series transistor structures which are non-overlapping with parallel transistor structures. Thus, the probability of failure in this case is

$$(3 * \frac{15}{64} + 54 * \frac{29}{64} + 27 * \frac{27}{64}) P^6 (1 - P)^3$$

If we assume that seven transistors are defective, then we have one hundred and twenty eight possible combinations of stuck-open and stuck short defects. Among those, there are no unique parallel transistor structures. Moreover, only seventy-four combinations produce an error for 1 series transistor structure which is overlapping with parallel transistor structures. Also, seventy-nine combinations produce an error for the other 35 series transistor structures which are overlapping with parallel transistor structures. There are no series transistor structures which are non-overlapping with parallel transistor structures. Thus, the probability of failure in this case is

$$(1 * \frac{74}{128} + 35 * \frac{79}{128}) P^7 (1 - P)^2$$

If we assume that eight transistors are defective, then we have two hundred and fifty six possible combinations of stuck-open and stuck short defects. Among those, there are no unique parallel transistor structures. Moreover, only one hundred and fifty eight of those combinations produce an error for 1 series transistor structure which is overlapping with parallel transistor structures. Also, two hundred and seven combinations produce an error for the other 8 series transistor structures which are overlapping with parallel transistor structures. There are no series transistor structures which are non-overlapping with parallel transistor structures. Thus, the probability of failure in this case is

$$(1 * \frac{158}{256} + 8 * \frac{207}{256}) P^8 (1 - P)$$

If nine transistors are assumed defective, then in this case there will always be an error and the probability of failure is $1 * \binom{9}{9} P^9 = P^9$

Thus, the probability of nona-transistor structure failure is

$$P_n = (3 * \frac{1}{8} + 27 * \frac{1}{8}) P^3 (1 - P)^6 + (18 * \frac{2}{16} + 81 * \frac{3}{16}) P^4 (1 - P)^5 +$$

$$(18 * \frac{4}{32} + 27 * \frac{11}{32} + 81 * \frac{9}{32}) P^5 (1 - P)^4 +$$

$$(3 * \frac{15}{64} + 54 * \frac{29}{64} + 27 * \frac{27}{64}) P^6 (1 - P)^3 + (1 * \frac{74}{128} + 35 * \frac{79}{128}) P^7 (1 - P)^2 +$$

$$(1 * \frac{158}{256} + 8 * \frac{207}{256}) P^8 (1 - P) + P^9$$

$$P_n = \frac{30}{8} P^3 - \frac{81}{16} P^4 + \frac{27}{8} P^5 - \frac{21}{16} P^6 + \frac{31}{128} P^7 - \frac{19}{128} P^8 + \frac{5}{32} P^9$$

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