Degradation Mechanisms of GaN HEMTs With p-Type Gate Under Forward Gate Bias Overstress

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***Abstract*— This paper investigates the degradation of GaN-based HEMTs with p-type gate submitted to positive gate bias stress. Based on combined electrical and optical testing, we demonstrate the existence of different degradation processes, depending on the applied stress voltage $V_{Gstress}$: 1) for $V_{Gstress} < 7$ V, no significant degradation is observed, thus demonstrating a good stability of the analyzed technology; 2) for $7 V < V_{Gstress} < 11.5$ V, a negative shift in threshold voltage (V_{th}) is observed, well correlated with a decrease in the gate leakage current and of the luminescence signal associated with hole injection. The negative V_{th} shift is ascribed to the trapping of holes in the AlGaN and/or p-GaN/AlGaN interface; and 3) for $V_{Gstress} \geq 12$ V, threshold voltage recovers its initial value. This is ascribed to a net-negative charge, generated either by the trapping of electrons injected from the 2-D electron gas to the AlGaN or to the de-trapping of the holes injected in 2). The results described within this paper provide relevant information for understanding the degradation dynamics of normally off GaN transistors submitted to extremely high gate voltage levels far beyond maximum use.**

***Index Terms*— Gallium nitride, HEMT, leakage currents, stability, threshold voltage.**

I. Introduction

LATERAL enhancement-mode transistors are promising for power applications, thanks to the low on-resistance (lower than 50 mΩ on 30-A/650-V devices [1]), the low on-resistance × gate charge product ($R_{on} * Q_g$ smaller than 290 mΩnC for 30-A/650-V device, see [1] and references therein), and the high breakdown voltage (>650–1000 V [1], [2]). The preferred approach for E-mode operation consists in placing a p-type GaN or AlGaN layer on the top of the AlGaN/GaN heterostructure. This leads to the depletion of the channel at null gate bias, and to positive threshold voltages in the range of 1–1.5 V [1]. For such technology, the issue of dynamic-R_{on} has been solved through a careful optimization of the epitaxial stack and of the back end: transistors with negligible dynamic R_{on} up to 850 V have already been demonstrated [3].

The reliability of transistors with p-type gate is still under investigation. There are two different approaches for fabricating contacts on p-type GaN: one approach is to use a Schottky junction [4], for instance by using TiN as a gate metal. This approach guarantees a substantial reduction of gate leakage, since the metal/p-GaN junction is reversely biased when the transistor is operated at high gate bias. However, devices with a Schottky junction on p-GaN may suffer from limited reliability, due to the time-dependent breakdown of the metal/p-GaN-AlGaN stack. Tallarico *et al.* [4] and Rossetto *et al.* [5] suggested that the high field reached at the metal/p-GaN junction may contribute to device degradation. A second approach for fabricating devices with a p-GaN gate is to use an ohmic contact on p-GaN [7]. In this case, the gate leakage may be slightly higher, but the absence of a depleted region (having a high peak field) at the metal/p-GaN interface can significantly improve reliability. A number of papers (see for instance [4], [5], [8]) on the stability of transistors with a Schottky-gate metal have been published; on the other hand, no extensive study on the stability of transistors having a ohmic contact on p-GaN has been published to date in the literature.

The aim of this paper is to contribute to the understanding of the reliability of GaN-based transistors with p-GaN gate. For the first time, we present an extensive analysis of the degradation of transistors having an ohmic contact on p-GaN, based on combined electrical characterization and electroluminescence (EL) analysis.

We demonstrate the following relevant results.

1) When the devices are submitted to positive gate-step stress, no significant change in device characteristics (V_{th}, R_{on}, and gate leakage) is observed up to VGS = 7 V, indicating a good stability of the analyzed technology (in real-life applications, the gate is driven

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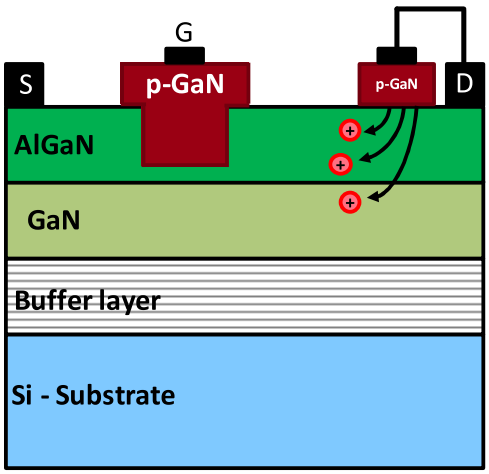

Fig. 1. Schematic of one of the analyzed devices.

with typical average currents of 10 mA for a 70-mΩ device, which corresponds to a gate voltage of 3.5 V, maximum gate peak currents of 2 A correspond to voltage spikes of 5.5 V).

2) For gate voltages between 7 and 11.5 V, a negative shift of threshold voltage is observed. This effect is correlated with a decrease in the gate leakage current and of the hole-related luminescence signal, and is ascribed to the trapping of holes in the AlGaN or at the p-GaN/AlGaN interface.
3) For higher voltages, the threshold voltage shifts positively, due either to the trapping of electrons in the AlGaN layer or to the de-trapping of the holes trapped in phase 2).

A capacitance–voltage analysis was carried out, indicating an enhanced trapping for stress voltages higher than 7 V. Finally, we demonstrated that the observed degradation process is partly recoverable through stress-recovery experiments.

II. Experimental Details

The structure of tested device is similar to that of a conventional GIT [7] with in addition the p-GaN region formed the next to the drain connected to the drain terminal (see Fig. 1). Hole injection from the drain helps reducing dynamic R_{on} which—in these devices—is almost 0 at 600 V, 150 °C (not shown here for brevity). The operating principle of the GIT is presented in [3]; the tested device shows e-mode operation thanks to the upward shift of the band diagram and significant increase in the drain current due to the conductivity modulation. The devices have a gate width $W_G = 200\ \mu$m, a gate–source distance $L_{GS} = 2\ \mu$m, gate–drain distance $L_{GD} = 12\ \mu$m, and gate length of 0.8 μm. The devices were submitted to dc characterization and step-stress experiments by means of a semiconductor parameter analyzer. EL measurements carried out during the execution of the step-stress experiments, by using a cooled-CCD camera mounted on an optical microscope.

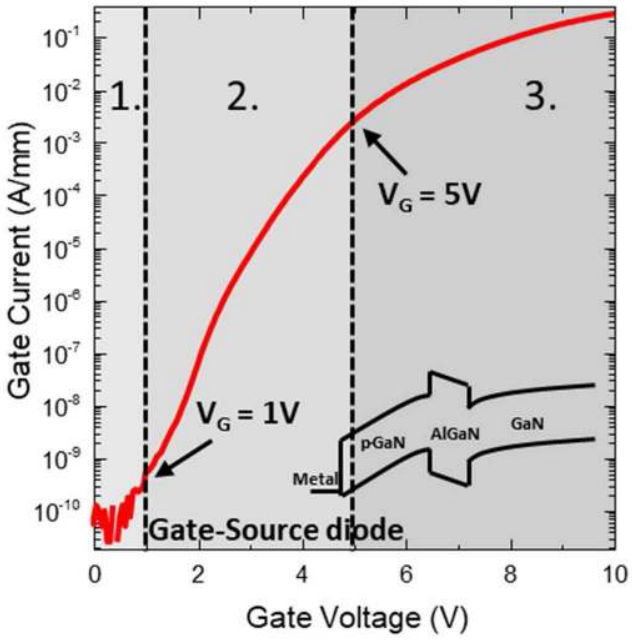

Fig. 2. *I–V* of the gate–source diode on one of the analyzed devices. Inset: schematic band diagram of the analyzed structures.

III. Results

A. I–V Curves of the Gate Diode

Fig. 2 reports the current–voltage (I–V) curve of the gate–source diode of one of the analyzed devices. The curve can be divided in three main regions: for V < 1 V (region 1), the 2-D electron gas (2-DEG) is not formed, and the AlGaN layer blocks the flow of current from the p-GaN layer toward the 2-DEG. For voltages in the range between 1 and 5 V (region 2), a significant conduction takes place, thanks to the joint contribution of holes injected from p-GaN toward the channel, and electrons flowing from the 2-DEG toward the gate. For higher voltages (region 3), the contribution of series resistance becomes dominant, and the slope of the I–V curves decreases. It is worth noticing that during real-life operation; the devices never reach region 3, since here the gate current, e.g., for a 70-mΩ device already exceeds 2 A. However, the study of the degradation mechanisms taking place in this voltage range can be of interest for device optimization.

B. Results of Step-Stress Experiments: Three Regimes are Observed

Fig. 3 shows the gate leakage current measured during the execution of a step-stress experiment. The gate voltage was increased by 0.5 V every 120 s; the staircase represents the stress voltage, while the colored lines represent the gate leakage measured at each stage of the stress experiment. As can be noticed, with increasing stress voltages, three different regimes can be identified. For stress voltages lower than 7 V, gate leakage current increases with increasing stress voltage. During each stage of the step-stress experiment, leakage is stable (for lower voltages), or slightly increasing (for higher voltages). In the same voltage range, the EL

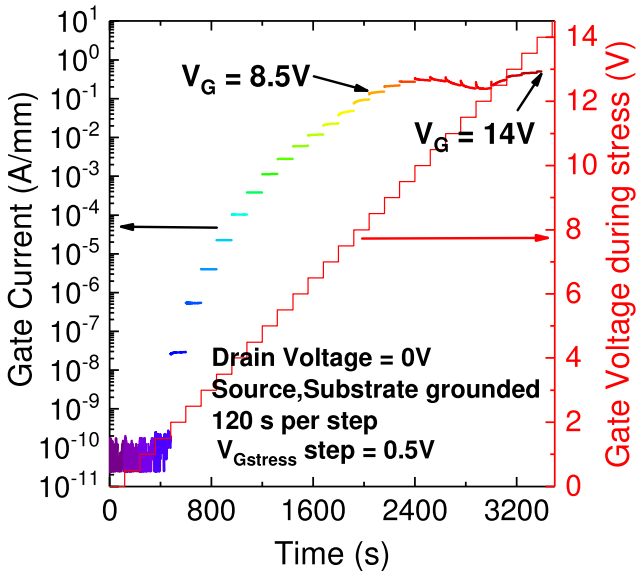

Fig. 3. Step-stress performed by increasing the gate voltage of 0.5 V step from 0 V up to failure, with $V_D = V_S = 0$ V. The device fails when the gate current reaches the value of 0.5 A/mm after 14 V of gate bias of stress.

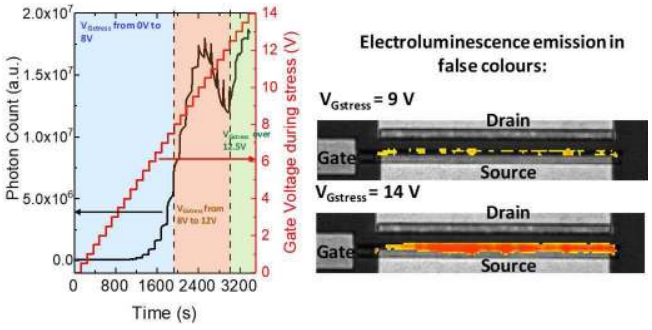

Fig. 4. EL emission in false colors taken at different steps of stress (9 and 14 V). The device starts to emit from the active region at 7 V. At the step of stress at 9 V, the light is clearly visible. The image at 14 V shows the EL taken before the failure. The light observed out of the active region is probably the results of light rays bounding off reflective surfaces.

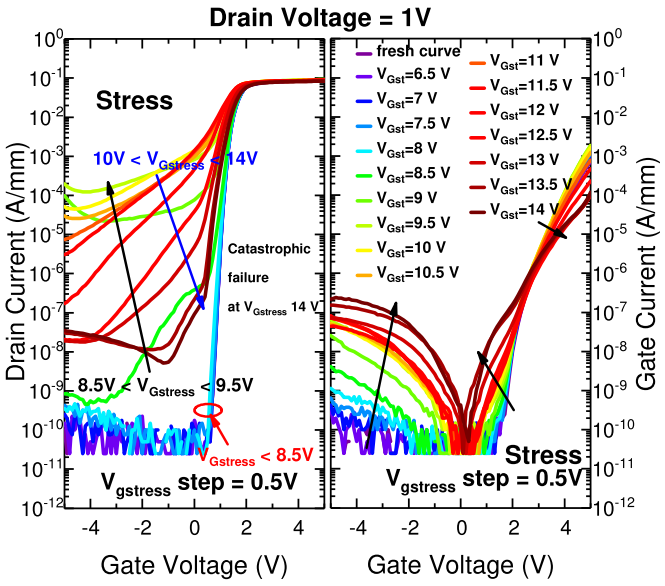

Fig. 5. I_DV_G curves (left) and I_GV_G curves (right) at $V_D = 1$ V monitored at each step of stress. The I_DV_G characteristic is not affected by the stress up to 8 V; at 8.5 V, we observe an increase of drain current up to 1 mA/mm. At 9.5 V of $V_{Gstress}$, the drain current decreases. The I_GV_G plot shows a strong increase in the gate current after $V_{Gstress} = 8.5$ V then continues to increase up to failure at 14 V.

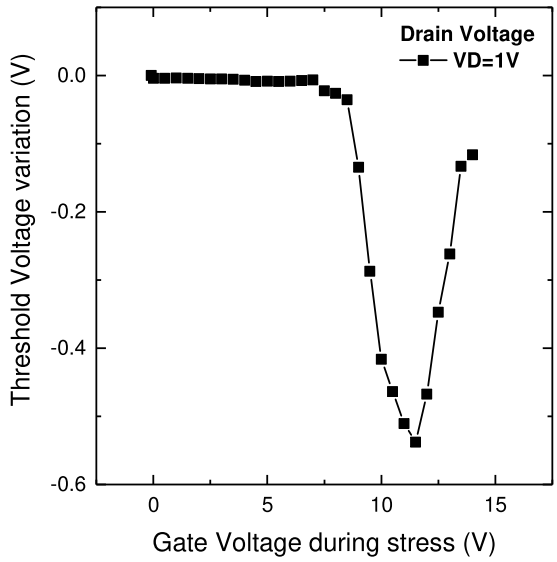

Fig. 6. Threshold voltage variation calculated by linear interpolation on the linear part of I_DV_G curves at $V_D = 1$ V for different values of gate voltage during stress.

signal emitted by the forward-biased gate also increases nearly exponentially (Fig. 4). Since EL signal originates from the recombination of holes injected from p-GaN and electrons injected from the 2-DEG toward the p-GaN [9], these results indicate that for 0 V $< V_{Gstress} <$ 7 V, an increasing carrier injection takes place (holes injected from the metal contact and electrons injected from 2-DEG to p-GaN through thermionic emission [see Fig. 7(a)]). In the same stress voltage range, no change in the I_D–V_{GS} curves and I_G–V_{GS} curves of the devices is observed [in Fig. 5 (left) and (right) are reported the I_D–V_{GS} and I_G–V_{GS} from 6.5 V of gate stress], and the threshold voltage (minimum gate-to-source voltage needed to create the conductive channel) is stable over time (Fig. 6), indicating a good stability of the analyzed technology. The value of the threshold voltage is calculated evaluating the intercept with x-axis (V_G) of the linear interpolation of the linear region of the I_DV_G at $V_D = 1$ V. For voltages in the range 7 V $< V_{Gstress} <$ 12 V, both leakage current (Fig. 3) and EL (Figs. 4–6) show a nonmonotonic behavior: first, gate leakage continues to increase (7 V $< V_{Gstress} <$ 10 V, Fig. 3), then a decrease is detected (10 V $< V_{Gstress} <$ 12 V). We suggest that the increase in gate leakage is due to increase in hole injection. This hypothesis is supported by two facts: first, the EL signal associated with the electron-hole recombination increases for 7 V $< V_{Gstress} <$ 11.5 V, consistently with the observed increase in gate leakage in the same voltage range. Second, a strong negative shift in threshold voltage is observed for 7 V $< V_{Gstress} <$ 11.5 V (Fig. 6), indicating the trapping of positive charge (injected holes) under the gate

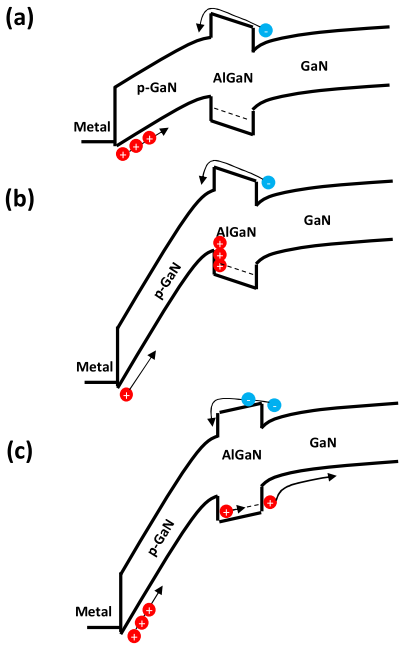

Fig. 7. Schematic representation of the three different stress regimes investigated within this paper. Notice that the picture is not exhaustive regarding the exact bending of the layers. (a) $V_{Gstress} < 7$ V leakage increases with voltage, absence of V_{th} shift indicates no trapping in the AlGaN. (b) 8 V $< V_{Gstress} <$ 11.5 V, negative V_{th} shift indicates hole trapping in the AlGaN; as a consequence, hole leakage decreases (repulsive effect of trapped holes). (c) $V_{Gstress} > 12$ V, positive trapped charge lowers field in AlGaN; hole detrapping is favored (V_{th} shows full recovery), and leakage current increases again).

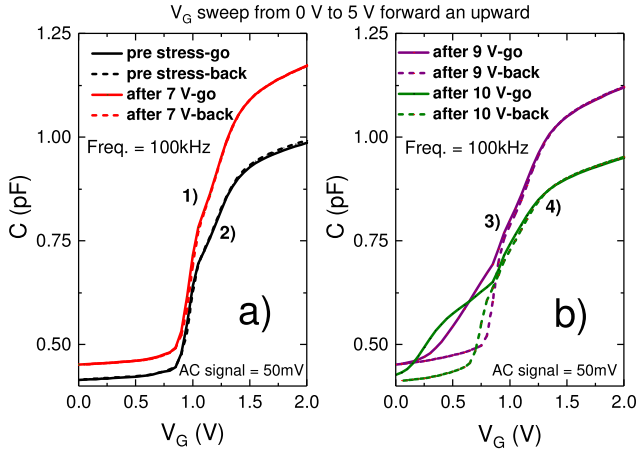

Fig. 8. Curves of capacitance–voltage plotted go and back, carried out after different steps of stress. (a) Preliminary capacitance–voltage plot (1) with the plot of the same measurement performed after 7 V of gate step of stress (2) are reported. (b) *C–V* plots after 9 (3) and 10 V (4) of gate stress are reported. After 7 V of gate voltage of stress the curves go and back start to show a hysteresis.

(possibly at the p-GaN/AlGaN interface or in the AlGaN layer [see Fig. 7(b)]). It is worth noticing that—in the same stress voltage range—also a significant increase in the subthreshold current [Fig. 5 (left)] and in the gate current [Fig. 5 (right)] is observed from the I_D–V_{GS} curves taken after each stage of the step-stress test. The trapping of positive charge under the gate may lead to a temporary "normally on" behavior of the devices that results in a conductive channel even at negative gate bias. The normally on behavior can also originate from the creation of a parasitic channel of defects created after stress at the AlGaN/GaN interface.

Also this effect is explained by the trapping of holes under the gate, which results in higher 2-DEG conductivity. For higher voltages ($V_{Gstress} > 12$ V), the gate leakage and the EL signal measured over stress time slowly increase again (see Figs. 3 and 4). At the same time, the I_D–V_{GS} curves [Fig. 5 (left)] and the threshold voltage (Fig. 6) show a substantial recovery, and become very similar to those measured before stress. This result indicates that the trapped positive charge responsible for the V_{th} shift is almost completely removed when the gate-stack is stressed at high positive bias. As described by the schematic in Fig. 7(c), we propose that when the devices are stressed with $V_{Gstress} > 12$ V, the high amount of holes trapped at the p-GaN/AlGaN interface may lower the electric field in the AlGaN layer, which counteracts both injection of electrons from the 2-DEG to the AlGaN, and the de-trapping of holes. As a consequence, leakage current can slowly increase again, and threshold voltage shows an almost complete recovery, thanks to the de-trapping of holes from the p-GaN/AlGaN interface [10]. It is worth noticing that also defect generation/electron trapping in the AlGaN [11], [12], at the AlGaN/GaN interface [13], or in the buffer may lead to the observed behavior.

C. Capacitance–Voltage Characterization Confirms the Trapping of Positive Charge

In Section III-B, we have suggested that when the stress voltage is in the range between 9 and 11.5 V, a significant threshold voltage shift takes place due to the trapping of charges under the gate. To provide an experimental evidence for this hypothesis, we have carried out capacitance–voltage characterization of the devices after stress at increasing voltage levels. A summary of this analysis is reported in Figs. 8 and 9. Fig. 8(a) reports the *C–V* curves measured before stress (1); a forward sweep and a consecutive backward sweep were measured to verify the presence of hysteresis, which is indicative of charge-trapping phenomena. The forward sweep is indicated by the solid line, while the backward sweep is indicated through a dashed line; the speed of the voltage ramp used for the *C–V* measurement is 50 mV/s. Before stress, no significant hysteresis was observed in the *C–V* curves, indicating the absence of charge trapping phenomena. The same absence of hysteresis was observed also after stress at 7 V (2); this is consistent with the data reported in Fig. 6 that indicate the absence of charge trapping (and threshold voltage shift) for stress voltages lower than 7 V. Remarkably, the *C–V* curves measured after stress at 9 (3) and 10 V (4) showed a different behavior: in the upward sweep, the *C–V* curve shows an early turn ON, which is consistent with the negative V_{th} shift described in Fig. 6. During the backward sweep, a hysteresis is noticed, consisting in a rightward shift of threshold voltage. This hysteresis can be ascribed to the change in the occupancy of the traps filled during stress and/or

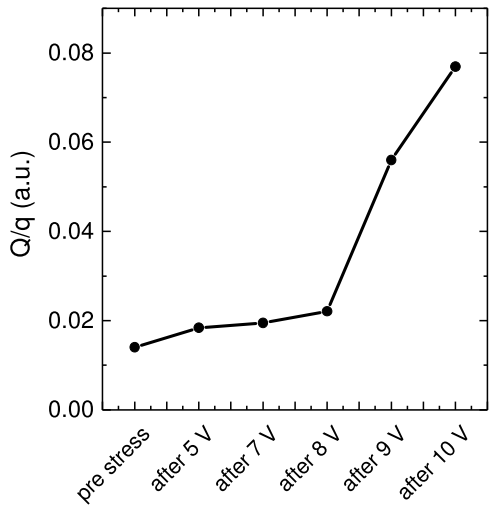

Fig. 9. Values of charge calculated from the hysteresis observed from the curves go and back of capacitance voltage after several steps of stress.

during the CV sweep (e.g., hole traps filled during stress, and emptied during the CV sweep). De-trapping can be favored by the long measurement times, and/or by the injection of electrons from the 2-DEG to the p-GaN/AlGaN. Also trapping in defects generated after stress in the buffer and/or at the AlGaN/GaN interface (as proposed in [11]) may explain the observed behavior of the C–V curves [14]. Fig. 9 quantifies the hysteresis observed in C–V measurements carried out after stress at increasing voltage levels, by showing the integral of the difference between the forward and backward C–V sweep. As can be noticed, no hysteresis is observed up to $V_{\text{Gstress}} = 8$ V; for higher voltages, a significant hysteresis is observed, indicating the storage of charge in the structure after stress. This is well correlated with the V_{th} variation shown in Fig. 6.

D. Is This a Recoverable Degradation Process?

After describing the degradation process, we carried out a set of tests, to evaluate if the observed mechanisms are recoverable or permanent. As shown in Figs. 5 and 6, the strongest degradation is observed for stress voltages between 9 and 10 V. We, therefore, step-stressed devices up to $V_{\text{Gstress}} = 9.5$ V, and then evaluated the recovery under zero bias [see Fig. 10 (left)]. The results indicate that the degradation mechanism described within this paper is slowly recoverable. Both threshold voltage and subthreshold current move back toward the values of the untreated devices if a sufficiently long time elapses under zero bias. This result indicates that the degradation process described above (accumulation of positive charge under the gate-stack) is mostly related to the trapping of mobile charges, rather than to the generation of positively charged fixed defects. Still, degradation is not fully recoverable, and some permanent effect is supposed to contribute as well. Only the I_{G}–V_{GS} plot does not show any recovery in the gate current [Fig. 10 (right)], demonstrating that the mechanism responsible of the gate current increase (electron injection) is not yet fully exhausted after 14 days.

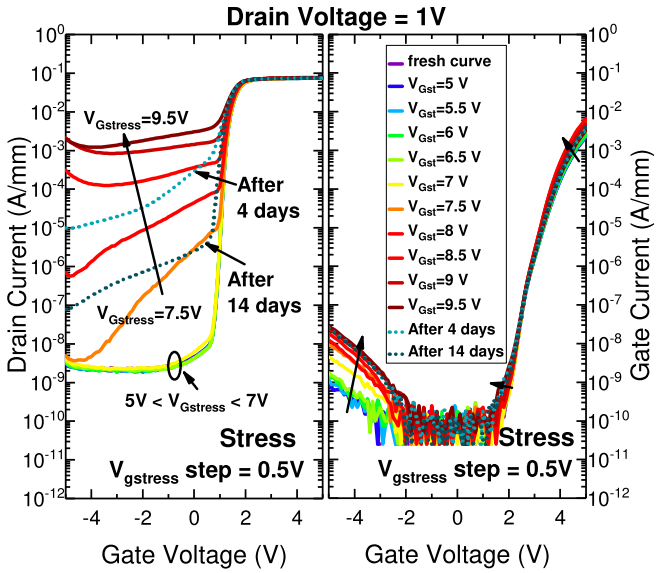

Fig. 10. I_{D} V_{G} characteristic (left) and I_{G} V_{G} characteristic (right) with V_{G} from −5 to 5 V performed during the step stress. The measurement was carried out by applying a step stress of gate of 120 s with $V_{\text{D}} = V_{\text{S}} = 0$ V, by increasing the gate bias (from 5 V) of 0.5 V for each step and by stopping the stress before failure (at 9.5 V). In order to evaluate the recovery, we tested the device after 4 days and after 14 days: we observe a recovery only in the I_{D} V_{G} characteristic.

IV. Conclusion

In this paper, we have studied the forward bias gate degradation of GaN-based HEMTs with p-type gate. The devices were submitted to dc characterization and step-stress experiments by monitoring the EL. We demonstrate the existence of different degradation processes, depending on the applied stress voltage V_{Gstress}.

1) For $V_{\text{Gstress}} < 7$ V, no significant degradation is observed, indicating a good stability of the analyzed technology (which is operating at typical gate voltages of 3.5 V with voltage spikes effectively self-clamped by the gate diode to below 5.5 V).
2) Gate voltages between 7 and 11.5 V induce a negative shift of threshold voltage, correlated with a decrease in the gate leakage current and EL. This phenomenon can be ascribed to the trapping of holes in the AlGaN or at the p-GaN/AlGAN interface.
3) For $V_{\text{Gstress}} \geq 12$ V, threshold voltage recovers its initial value due to the de-trapping of the holes previously trapped.

Such a mechanism was confirmed by means of go–back C–V measurements: up to 7 V of gate voltage the absence of hysteresis (no charge trapping) was noticed. Once the holes are trapped in the AlGaN or at the p-GaN/AlGAN interface for higher V_{Gstress}, a significant hysteresis is observed in the C–V plot. Finally, we demonstrated that the observed degradation process is not permanent, but it shows a slow recovery.

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