

Demonstration of 2kV SiC Deep-Implanted Super-Junction PiN Diodes

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Abstract. We report successful demonstration of 2kV, SiC super-junction (SJ) PiN diodes formed by deep implantation of Al and N. In our devices, alternating 12 μ m deep n-type and p-type SJ pillars fabricated on a 10 μ m pitch and result in a SJ diode with a measured blocking voltage 500V higher than comparable non-SJ diodes. Four activation anneals ranging from 1700 °C to 2000 °C were compared for effectiveness in eliminating post-implant lattice damage, and the optimum anneal condition was identified.

Introduction

Wide bandgap Silicon Carbide (SiC) power switches and diodes offer the promise of lower conduction and switching losses leading to efficient power conversion. However, for Medium Voltage (MV) class (>3.3 kV) applications, the advantage of SiC technology is diminished compared to the incumbent Si IGBT technology. MV SiC unipolar devices suffer from high conduction losses at elevated temperatures [1]–[3], and SiC bipolar devices such as IGBTs require a prohibitive 3V junction drop during conduction [4], [5]. SiC super-junctions (SJ) can break the unipolar limit and offer an improved trade-off between specific on-resistance and blocking voltage for MV-class applications. To date, multi-epitaxial growth [6] and trench-refill [7] approaches have been demonstrated for 1.2kV and 6.5kV SiC SJ devices. For typical dopant implant energies of several hundred keV, the multi-epitaxial solution for SiC SJs is limited to switches rated to block <2kV. Above this rating, the number of epitaxial regrowth steps becomes too large. The trench-refill approach is also challenging, since the refill process tends to produce crystallographic damage, and it is difficult to refill the trenches with the required dopant uniformity. Recently, SiC charge-balanced (CB) diodes and MOSFETs were reported as an alternative solution to SJ devices with a simpler fabrication process [8], [9]. However, the stacked nature of CB devices and the charge carrier redistribution required during switching, results in a device with switching delays that increase with each additional layer, becoming prohibitive when scaling SiC CB devices beyond 4.5kV.

For scaling beyond 4.5kV, a new class of SJ devices is being developed that relies on Megavolt-level implantation to form deep p-type and n-type pillars. This multi-epitaxial SJ approach can be implemented in high voltage SiC devices with a smaller number of regrowth steps. However, high-energy implantation of dopants in SiC may introduce lattice damage that will significantly limit the performance of such devices. Therefore, to evaluate the feasibility of high-energy implantation, single layer 2kV SiC SJ PiN diodes were fabricated and characterized as a first building block of deep-implanted SJ technology. We employed several activation anneal splits and studied the leakage of PiN diodes to evaluate the presence of lattice damage following high-energy implantation and anneal. We also extracted the Al activation rate of the implanted p-pillars for each anneal split.

Experimental

SiC SJ-PiN diodes were fabricated on 100-mm SiC wafers. A 12 μ m thick n-type epitaxial layer doped to 1×10^{15} cm⁻³ was grown on the starting N⁺ substrates, and n-type and p-type pillars were formed in the epitaxial layer by multi-energy implantations of Al and N through a patterned, thick, high-density hard mask. The mask was designed to provide enough stopping power to mask implantation energies up to 50MeV. Implantation was accomplished using a 15MV Van de Graaff accelerator based tool [10]. To validate the effectiveness of our process in both masking the high

energy implants and aligning the n-type and p-type pillars, a preliminary SiC test wafer was processed and characterized by SEM imaging. In order to improve SEM contrast, implant doses for the test wafer were targeted to achieve dopings of $4 \times 10^{16} \text{cm}^{-3}$ in both the Al and N pillars (four times the device design target of $1 \times 10^{16} \text{cm}^{-3}$). Fig.1 shows a SEM cross section of the fabricated structure. Clearly the masking and alignment process was successful and a $10 \mu\text{m}$ pitch SJ structure with $12 \mu\text{m}$ deep Al and N doped pillars formed by high-energy implantation is feasible. For subsequent device wafers, following high energy implantation of the $1 \times 10^{16} \text{cm}^{-3}$ doped SJ pillars, P+ anode and edge termination regions of the diodes were formed using additional low energy Al implantations. Then, the front sides of the wafers were protected with graphitized photoresist in preparation for the dopant activation anneal. To evaluate the effect of temperature in annealing out high-energy implantation lattice damage, four splits were chosen for the anneal (Table1). SJ diode wafers were annealed at temperatures ranging from $1700 \text{ }^\circ\text{C}$ to $2000 \text{ }^\circ\text{C}$ in an Ar ambient.

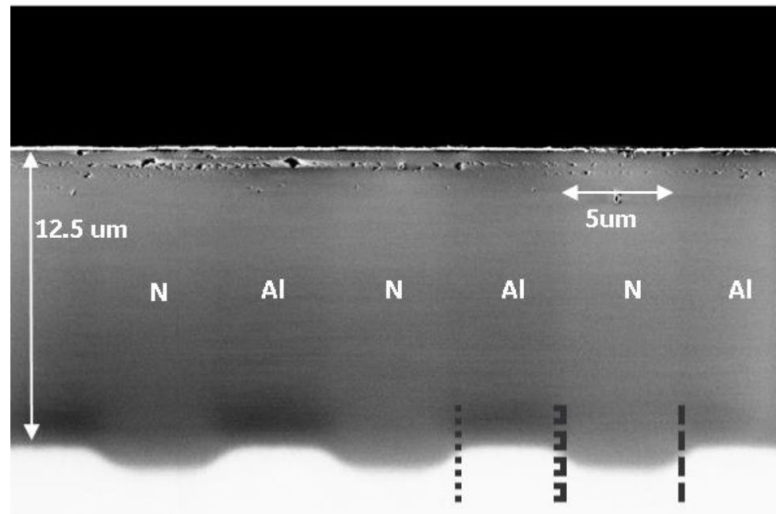


Fig. 1: SEM characteristics of implanted P/N pillars formed on a SiC test wafer.

Table 1: Activation anneal splits for SiC SJ PiN diodes

Split	Activation Anneal Temperature ($^\circ\text{C}$)	Duration (hours)
1	$1700 \text{ }^\circ\text{C}$	30 min
2	$1800 \text{ }^\circ\text{C}$	120 min
3	$1900 \text{ }^\circ\text{C}$	60 min
4	$2000 \text{ }^\circ\text{C}$	40 min

The graphite layer was removed following the high temperature activation anneal and the SiC surface roughness was measured using an optical profilometer in special test areas distributed across the wafers. Fig. 2(right) shows the average surface roughness for each of the implanted regions. Surface roughness seems to be relatively independent of implantation type, but varies with activation temperature, with a maximum roughness for the highest activation anneal at $2000 \text{ }^\circ\text{C}$. The graphite layer appears to be capable of protecting the front surface during high temperature anneal. However, the wafer back surface was not protected and was significantly altered following activation. As shown in Fig. 2(left), the topography of the SiC back surface shows a marked difference between split 1 and the higher temperature splits. This suggests fundamentally different surface kinetics at temperatures above $1700 \text{ }^\circ\text{C}$.

Forward IV characteristics of 0.6mm^2 SJ PiN diodes and extracted differential specific resistances at $25 \text{ }^\circ\text{C}$ are plotted in Fig. 3(right). From this plot, higher activation anneal temperatures increase specific on-resistance from $2.5 \text{m}\Omega \cdot \text{cm}^2$ for activation anneal split 1 to $4.3 \text{m}\Omega \cdot \text{cm}^2$ and $5 \text{m}\Omega \cdot \text{cm}^2$ for activation anneal splits 3 and 4 respectively. We believe altered surface topography for anneal

temperatures above 1700 °C has adversely affected the cathode contact resistance, and protecting the wafer backside with graphite during activation can avoid this cathode contact damage.

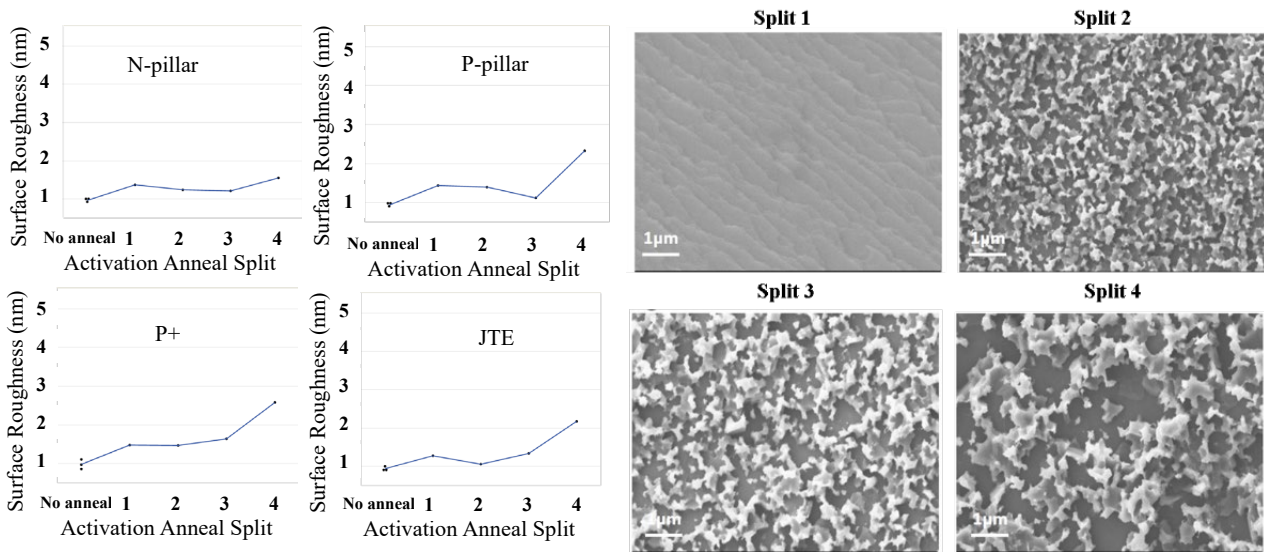


Fig. 2 Left: SiC front-side surface roughness over different implanted regions versus activation anneal splits. Right: SEM images of wafer backsides following high temperature activation anneal.

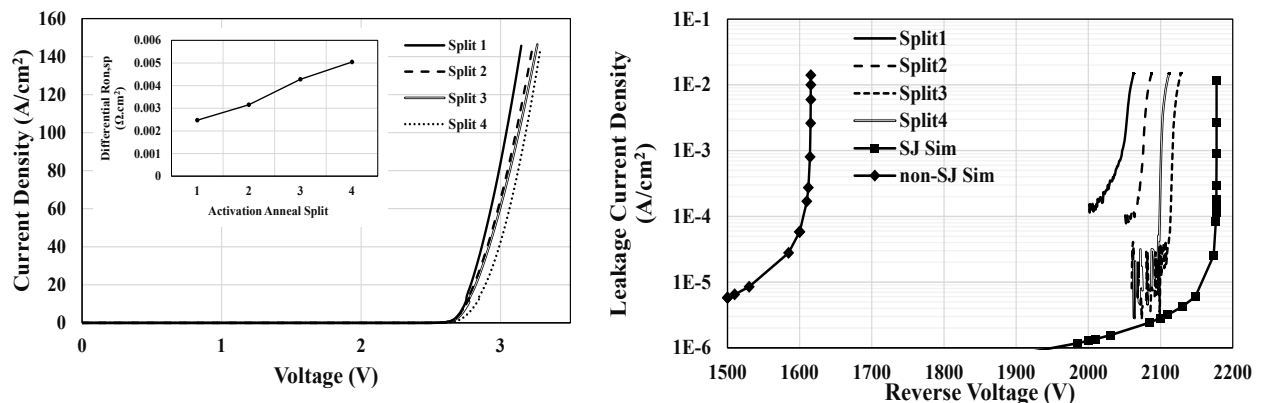


Fig. 3 Left: Forward IV characteristics of SiC SJ PiN diodes and extracted differential Ronp (inset) for different activation anneal splits. Right: Reverse IV characteristics of SiC SJ-PiN diodes for different activation anneal splits.

Reverse IV characteristics of SJ PiN diodes and simulated blocking plots for ideal SJ diodes and non-SJ diodes with similar initial drift layer doping profiles ($12\mu\text{m}$ thick and doped to $1 \times 10^{16}\text{cm}^{-3}$) are plotted in Fig. 3(left). From this plot, diodes with activation anneal splits 3 and 4 (1900 °C and 2000 °C) result in breakdown voltages of $>2100\text{V}$. This blocking level is 500V higher than the simulated breakdown voltage of SiC non-SJ diodes and is similar to the simulated plot for an ideal SiC SJ PiN diode. Therefore, we conclude that our implanted n-type and p-type SJ pillars achieve active doping levels close to charge-balance, providing higher blocking voltage for SiC PiN diodes that cannot be achieved with non-SJ structures. However, activation anneal splits 1 and 2 (1700 °C and 1800 °C) suffer from high leakage current prior to the breakdown and suggests that to fully anneal lattice damage generated during high-energy implantation an activation anneal at >1900 °C is required.

The activation rate of the implanted Al p-pillars was extracted from capacitance-voltage (CV) structures fabricated in test areas of the device wafers. In Fig. 4, a capacitance-voltage plot and extracted profile of electrically active Al over a $2\mu\text{m}$ depth of the p-pillar implanted region is plotted for the activation anneal splits. No significant difference is observed in capacitance values and

extracted active Al concentrations between different anneal temperatures. Extracted Al concentration for p-pillar implants for all activation splits was close to the implant target of $1 \times 10^{16} \text{ cm}^{-3}$. This suggests that unlike high dose Al implantation in SiC, activation anneal at $>1700 \text{ }^\circ\text{C}$ can fully activate low dose Al implantations in SiC. This is in agreement with Al activation models previously reported [11].

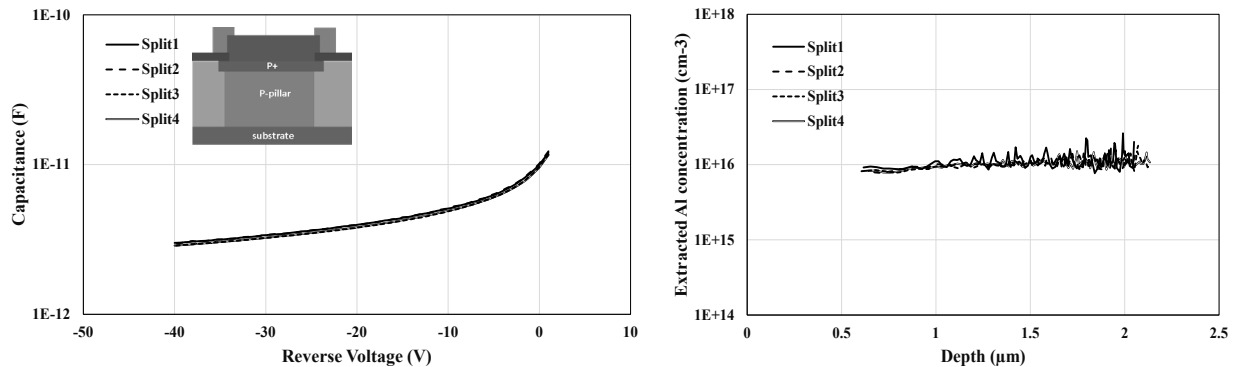


Fig. 4 C-V characteristics (left) and extracted active Al doping (right) in p-pillar implanted PiN diodes for different activation anneal splits.

Conclusion

2kV SiC SJ PiN diodes were fabricated using high-energy implantation of Al and N. SJ diodes showed measured blocking voltage 500V higher than comparable non-SJ diodes. Four different activation anneal splits were employed to remove lattice damage following high-energy implantation. The data shows that SiC SJ PiN diodes annealed at $1800 \text{ }^\circ\text{C}$ and below, suffer from high blocking leakage and anneals at $>1900 \text{ }^\circ\text{C}$ are required for maximum damage recovery. However, activation anneal temperatures as low as $1700 \text{ }^\circ\text{C}$ can fully activate low dose implanted Al in SiC.

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