Dependence of Injection Velocity and Capacitance of Si Nanowires on Diameter, Orientation, and Gate Bias: An Atomistic Tight-Binding Study

Neophytos Neophytou, Hans Kosina,
and Siegfried Selberherr
Institute for Microelectronics, TU Wien
Gußhausstraße 27-29/E360, A-1040
Wien, Austria
e-mail: {neophytou|kosina|selberherr}@iue.tuwien.ac.at

Gerhard Klimeck
Network for Computational Nanotechnology,
Purdue University, West Lafayette, IN 47906, USA
gekco@purdue.edu

***Abstract*— We present a simulation study of Si nanowire (NW) transistor devices for logic applications using an atomistic tight-binding (TB) model for the electronic structure calculation, self consistently coupled to a two-dimensional Poisson solver for the solution of the electrostatics. A semiclassical ballistic model is used for the transport calculation. The average carrier velocity and the capacitance of cylindrical NMOS and PMOS NWs with diameters from 3nm to 12nm, in the [100], [110] and [111] transport orientations are calculated at different gate bias. The capacitance of all wires is only a function of the wires' diameter, and in all cases is degraded from the oxide capacitance by ~20%. The carrier velocities increase with increasing gate biases. The carrier velocity of PMOS NWs in the [110] and [111] orientations is a strong function of the wires' diameter, whereas that of [100] and [111] NMOS and [100] PMOS devices has only a weak dependence on the diameter.**

Keywords - nanowire; injection velocity; PMOS; NMOS; capacitance; bandstructure; MOSFETs; tight binding; atomistic;

I. INTRODUCTION

As CMOS device scaling apparently saturates, alternative structures and devices are investigated in order to continue the performance trend of the past years. Gate-all-around nanowire (NW) FET devices are among the potential candidates for future device applications [1-4]. Such devices can provide enhanced electrostatic control, as well as the possibility of utilizing a variety of orientations and cross sectional shapes for device optimization. NW devices of diameters down to 3nm and channel lengths of 15nm have already been demonstrated [3]. We investigate ballistic transport features in NW devices using the $sp^3d^5s^*$-spin-orbit-coupled atomistic tight-binding model (TB) [5] with a semi-classical ballistic transport model [6]. We address atomistically the dependence of NW capacitance and injection velocity on diameter and orientation for NWs of sizes from 3nm up to 12nm in diameter. Cylindrical NWs in various transport orientations ([100], [110], [111]), both for NMOS and PMOS devices are examined. It is found that the total gate capacitance in all wire cases is degraded from the oxide capacitance (C_{OX}) value by ~20%, independent of NMOS, PMOS orientation and diameter. In general, the average carrier velocity increases as the device is pushed further into inversion, because states in the bandstructure with higher velocities are occupied. The carrier velocities of PMOS NWs in [110] and [111], and NMOS NWs in [110] transport orientations also have a strong dependence on the NWs' diameter with the velocity been higher for smaller diameters. Only a slight velocity dependence on diameter is observed for PMOS NWs in [100] and NMOS NWs in [100] and [111] orientations. These observations can be understood from features of the Si bandstructure.

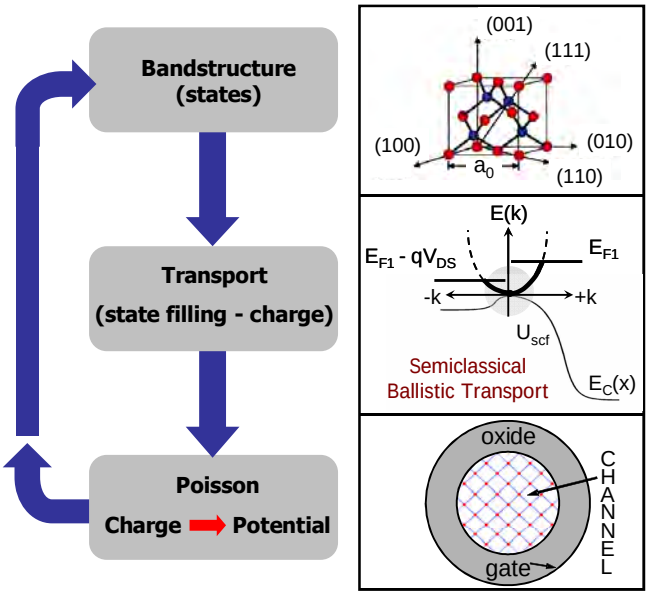

Figure 1. (a) The computational model. The atomistic $sp^3d^5s^*$-SO TB model is used for the electronic structure. A semiclassical ballistic model is used to calculate transport characteristics and fill the bandstructure states. A two-dimensional Poisson is solved in the cross section of the NW for the electrostatic potential. The process is repeated until self consistency is achieved.

II. APPROACH

The NWs' bandstructure is calculated using a 20 orbital atomistic tight-binding spin-orbit-coupled model ($sp^3d^5s^*$-SO)

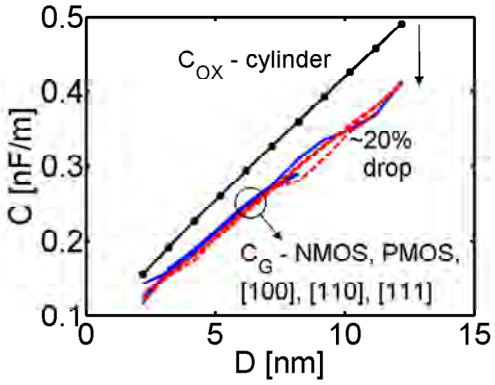

Figure 2. The capacitance of the NWs vs. diameter for NMOS, and PMOS in [100], [110], and [111] orientations. The oxide capacitance is shown in black.

[7] self-consistently coupled to the two-dimensional Poisson equation for the electrostatic potential. A semi-classical ballistic transport model [6] is used to fill the bandstructure states according to the Fermi levels of the source and drain, and compute the transport characteristics (Fig. 1). The model is then coupled to a two-dimensional Poisson solver for the electrostatic potential in the cross section of the NW. The potential is then used to recalculate the bandstructure until self consistency is achieved. The model and procedure is described in detail in [7], and Ref. [8] elaborates on its validity for NWs. In Fig. 1 we present the simulation flow for reference. The NWs considered are cylindrical, gate-all-around, with 3.5nm gate oxide thickness and diameters varying from 3nm to 12nm. These dimensions are the same as in recent experimental devices [3]. DIBL and subthreshold swing are included through a source/drain capacitive (C_S, C_D) model. The capacitances were calibrated to match the DIBL and the subthreshold swing of the D=8nm diameter devices in [3].

III. RESULTS

The variations of the capacitance and carrier injection velocities are examined as the dimension and the orientation of the NWs change. Although the charge distribution in the cross section of different NWs can be quite different [7, 9], showing a preferential distribution on the high quantization mass surfaces, it is found that the capacitance is very similar for wires of the same diameter, independent of band type (NMOS or PMOS) and orientation. Figure 2 shows the capacitance of NMOS (dash-red) and PMOS (solid-blue) NWs, in [100], [110] and [111] orientations as a function of the wires' diameter. The gate capacitance (C_G) of all devices is degraded from the oxide capacitance (the capacitance of a cylinder) by ~20% due to the low quantum capacitance (C_Q) of the channel (low density of states (*DOS*)). C_G is of very similar magnitude for all NWs, and all lines in Fig. 2 lie almost on top of each other. The reason is that C_G consists of two parts, the oxide capacitance (C_{OX}) and the semiconductor capacitance (C_{SC}). Out of these, only C_{SC} differs slightly between wires, and, therefore, these differences do not show up in C_G even in cases of thinner oxides, in which the importance of C_{SC} is more prominent [7, 9]. This implies that the inversion charge is very similar in all these devices, independently of any differences in their *DOS*. The carrier

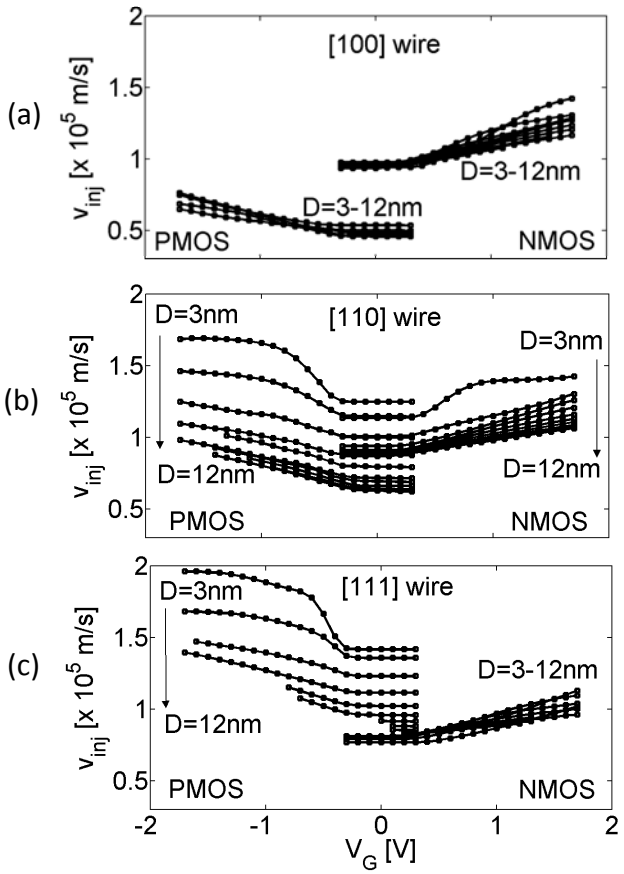

Figure 3. The injection velocity of the carriers in the NWs. Results for NWs of diameters D = 3nm to 12nm, PMOS and NMOS, and various gate biases are shown. For negative gate biases the results present the PMOS NWs. For the positive gate biases, the NMOS results are shown. The arrows indicate the direction of diameter increase in the cases for which a uni-directional trend is observed. (a) [100] oriented wires. [b] [110] oriented wires. (c) [111] oriented wires. The PMOS [110] and [111] NWs exhibit the largest carrier velocity variation.

velocity is therefore the parameter that determines the NWs' relative performance.

Unlike the capacitance, the average carrier velocities (or injection velocity in this case, v_{inj}) of the wires depend strongly on band type, orientation, and bias. Figures 3a, 3b, and 3c show the carrier velocities for NMOS and PMOS NWs of D=3nm to 12nm for [100], [110], and [111] orientations, respectively. In the case of NMOS NWs, the velocities vary by ~50% (in each orientation case) as the diameter and bias vary. Since the v_{inj} values are also very similar, the relevant differences in performances of NMOS NWs are not large (with the [110] and [100] performing better than the [111] NWs due to higher velocities). Small v_{inj} variations are also observed in PMOS [100] wires. On the other hand, the velocity of PMOS [110] and [111] NWs has a strong dependence on diameter variations. Higher velocities are observed for smaller wire diameters. This behavior can be understood from bandstructure quantization features and the strong anisotropic behavior of the heavy holes, which provides bands with large curvature at strong quantization [8]. Similar strong variation in the velocities has been observed for rectangular NWs too [10]. In

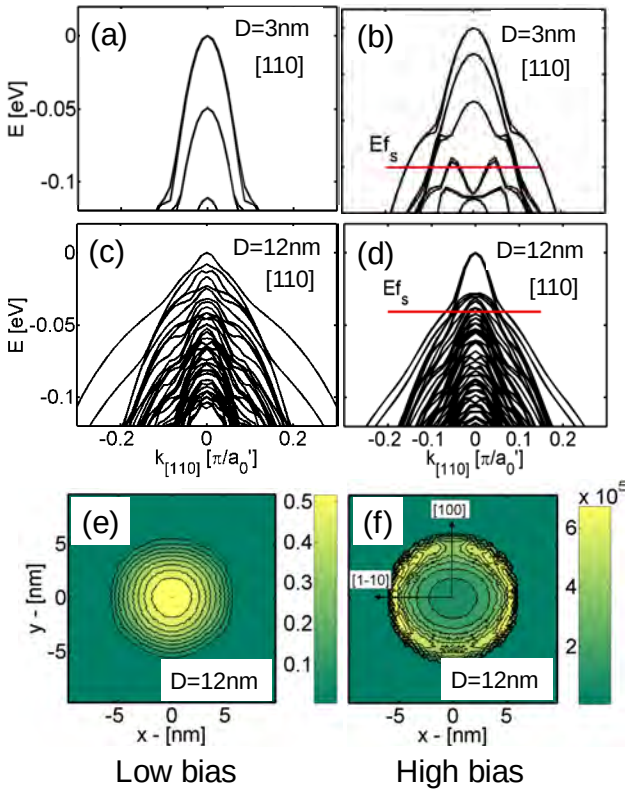

Figure 4. Features of [110] PMOS NWs under low gate biases (V_G=0.1V) – left column, and under high inversion (V_G=-1.7V) – right column. (a) The bandstructure of the D=3nm wire under low gate bias. (b) The bandstructure of the D=3nm under high (negative) gate bias. (c) The bandstructure of the D=12nm NW under low gate bias. (d) The bandstructure of the D=12nm NW under high (negative) gate bias. (e) The charge distribution in the cross section of the D=12nm NW under low gate bias, and (f) under high (negative) gate bias.

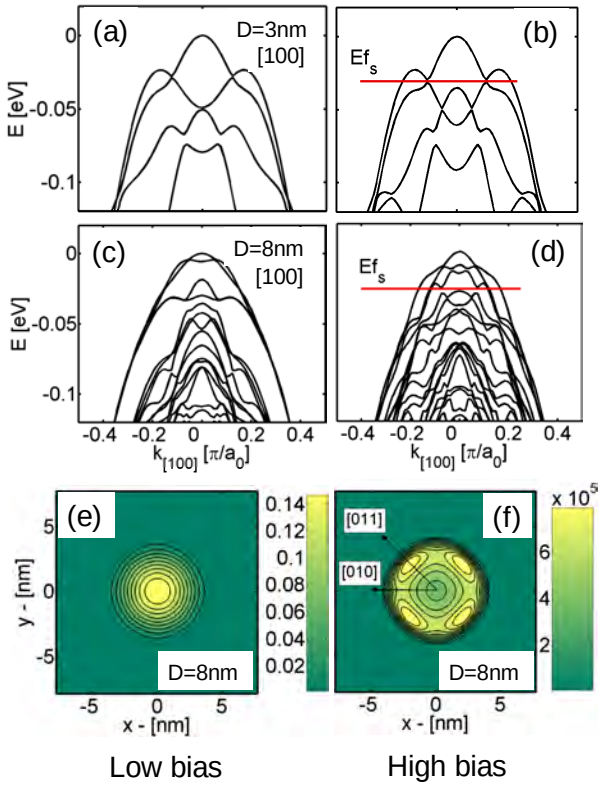

Figure 5. Features of [100] PMOS NWs under low gate biases (V_G=0.1V) – left column, and under high inversion (V_G=-1.2V) – right column. (a) The bandstructure of the D=3nm wire under low gate bias. (b) The bandstructure of the D=3nm under high (negative) gate bias. (c) The bandstructure of the D=8nm NW under low gate bias. (d) The bandstructure of the D=8nm NW under high (negative) gate bias. (e) The charge distribution in the cross section of the D=8nm NW under low gate bias, and (f) under high (negative) gate bias.

that case, because of the large velocity variation, design geometries which exhibit an ON-current performance that is either immune to design size variations, or very sensitive to variations can be identified, providing guidance to design optimization. The velocity being higher for stronger quantization has two implications: (i) [110] and [111] narrow PMOS NWs will outperform [100] PMOS wires. (ii) The counter-acting effect of velocity reduction and capacitance increase as the diameter increases, can make these wires more tolerant to on-current variations caused by diameter variations. It is to note, however, that these v_{inj} results hold for unstrained PMOS Si. In case of strained channels, where the bandstructure and anisotropy can change, the variation pattern presented here will also change.

IV. Discussion

In order to understand the large velocity variations observed in the case of the [110] and [111] PMOS NW devices as a function of diameter and gate bias, Fig. 4 shows the bandstructures of the narrow diameter D=3nm (a,b) and the larger diameter D=12nm (c,d) NWs under low and high (negative) V_G. The bandstructures are all shifted to 0eV to have the same energy reference and to be able to easily compare their shapes. The electronic structure of the D=3nm wire shown in Fig. 4a consists of large curvature bands, providing low effective masses and high carrier velocities. At higher inversion conditions (gate negative gate biases) (Fig. 4b), the Fermi level (E_{Fs} – red horizontal line) moves far into the valence band, where higher velocity states are occupied, and the carrier velocity increases. The bandstructure of the device with the larger D=12nm diameter (Fig. 4c), has a bandstructure which consists of much heavier subbands compared to Fig. 3a. This explains why the velocities decrease as the diameter of the [110] PMOS NW increases. As the device is driven into inversion, the carrier velocities in all wires increase because i) the Fermi level occupies higher velocity states and ii) the bandstructure of the D=12nm wire undergoes large changes, with the highest subbands acquiring lighter masses, which increase the carrier velocities (Fig. 4d). This change can be explained from the charge profiles in Fig. 4e and Fig. 4f. Under low biases (Fig. 4e), the charge resides in the volume of the NW. Under high inversion (Fig. 4f), however, an inversion layer forms around the circumference of the wire, preferentially along the [110] direction (left/right) which has a larger quantization mass. This confines the charge in a small region, similar to structural confinement, providing

light mass subbands as in the case of the D=3nm NWs. The charge associated from the heavier transport mass subbands at the position of the Fermi level, resides in lower, more negative energies and is less confined toward the surfaces.

In the case of the [100] PMOS NWs, the carrier velocities have only a small dependence on the NWs' diameter. Figure 5 shows the same features as Fig. 4, but now for the [100] PMOS NW. The bandstructure of the D=3nm NW under low and high (negative) gate biases (Fig. 5a, Fig. 5b respectively), consists of oscillating curvature features. In these bandstructures the carrier velocity can even become zero at some energies due to the zero slope of the bands. The overall carrier velocities are therefore slowed down compared to the [110] and [111] PMOS NWs, and the performance is degraded [8]. A small velocity increase is still observed under high inversion conditions (large negative gate biases) as higher velocity states are populated. At larger diameters (Fig. 5c, Fig. 5d), the same oscillatory features are observed, which again keep the velocity low. No significant variation with diameter is therefore observed. The charge distribution in the cross section of the wires is shown in Fig. 5e, Fig. 5f. At low biases (V_G=0.1V) the charge is distributed in the entire volume of the NW. At high inversion it is pushed along the circumference of the wire. Due to the higher quantization mass along the [110] equivalent directions, the charge preferentially accumulates in the four [110] sides of the cylindrical NW (Fig. 5f).

For NMOS NWs only a light dependence of the velocity on the diameter is observed (right side branches in Fig. 3). The bands of NMOS NWs form out of parabolic bands from the conduction band of silicon, projected onto the one-dimensional Brillouin zone. The [100] and [110] wires have bands with masses $m^*=0.19m_0$, whereas [111] NWs have heavier masses of $m^*=0.43m_0$ originating from the projection of the tilted ellipsoids onto the one-dimensional Brillouin zone [7]. The [111] wires therefore, have lower carrier velocities, whereas the [100] and [110] wires, have higher carrier velocities. Still there are some slight variations in the carrier velocity as a function of the diameter due to the slight effect of non-parabolicity in the [100] and [111] NWs, which tends to increase the mass and reduce the carrier velocity as the quantization increases [7]. On the other hand, in the [110] NW case, the anisotropy in the conduction band causes the transverse mass $m_t=0.19m_0$ to *decrease* with quantization [7]. This has two implications: i) it decreases the transport mass of the Γ valleys and, ii) it decreases the quantization mass of the heavier off-Γ valleys which are now shifted higher in energy and do not participate strongly in transport. Overall, the carrier velocity is slightly increased. An increase in the velocities at high gate biases is still observed due to the population of parts of the bandstructure with larger slopes.

V. Conclusion

An atomistic tight-binding approach and a semi-classical ballistic model is used to calculate the ballistic transport properties (v_{inj} and capacitance) of cylindrical nanowire devices self-consistently with the electrostatic potential. NMOS and PMOS NWs of diameters from D=3nm to 12nm in [100], [110], and [111] orientations are considered. The carrier velocities are examined as a function of diameter and gate bias. Although the capacitance of the devices is a function of only the NWs' diameter, the carrier velocities are strong functions of orientation, band type, bias, and diameter. PMOS [110] and [111] NWs indicate the largest velocity sensitivity with stronger quantization resulting in higher velocities. This can be understood from features of the electronic structure of the nanowires. In particular, the electronic structure of narrow PMOS NWs in [110] and [111] orientations consists of lighter mass subbands than that of NWs with larger diameters. The electronic structure of these wires can be a strong function of the inversion bias conditions. Electrostatic quantization can have a similar effect as structural quantization, reshaping the band curvature and affecting the carrier velocities.

Acknowledgment

This work has been partially supported by funds from the Austrian Science Fund, FWF, contract I79-N16. Computational resources of the Network for Computational Nanotechnology (NCN) are acknowledged. The simulations in this work can be duplicated with Bandstructure Lab on nanoHUB.org [11].

References

[1] ITRS Public Home Page. http://www.itrs.net/reports.html

[2] N. Singh et. al., "Ultra-narrow silicon nanowire gate-all-around CMOS devices: Impact of diameter, channel-orientation and low temperature on device performance," *In. Elec. Dev. Meeting*, 2006.

[3] K. H. Cho, *et* al., "Experimental evidence of ballistic transport in cylindrical gate-all-around twin silicon nanowire metal-oxide-semiconductor field-effect transistors," *Appl. Phys. Lett.*, 92, 052102, 2008.

[4] M. Kobayashi and T. Hiramoto, "Experimental study on quantum confinement effects in silicon nanowire metal-oxide-semiconductor field-effect transistors and single-electron transistors," *J. Appl. Phys.*, 103, 053709, 2008.

[5] T. B. Boykin, G. Klimeck, and F. Oyafuso, "Valence band effective-mass expressions in the $sp^3d^5s^*$ empirical tight-binding model applied to a Si and Ge parametrization," *Phys. Rev. B*, vol. 69, pp. 115201-115210, 2004.

[6] A. Rahman, J. Guo, S. Datta, and M. Lundstrom, "Theory of ballistic nanotransistors," *IEEE Trans. Elect. Dev.*, vol. 50, no. 9, pp. 1853-1864, 2003.

[7] N. Neophytou, A. Paul, M. Lundstrom, and G. Klimeck, "Bandstructure effects in silicon nanowire electron transport," *IEEE Trans. Elect. Dev.*, vol. 55, no. 6, pp. 1286-1297, 2008.

[8] A. Paul, S. Mehrotra, G. Klimeck and M. Luisier, "On the validity of the top of the barrier quantum tranport model for ballistic nanowire MOSFETs, " *Proc. In. Workshop on Comp. Electronics (IWCE)*, pp. 177-180, Beijing China, Mai, 2009.

[9] N. Neophytou, A. Paul, and G. Klimeck, "Bandstructure effects in silicon nanowire hole transport," *IEEE Trans. Nanotechnol.*, vol. 7, no. 6, pp. 710-719, 2008.

[10] N. Neophytou and G. Klimeck, "Design space for low sensitivity to size variations in [110] PMOS nanowire devices: The implications of anisotropy in the quantization mass," *Nano Lett.*,vol. 9, no. 2, pp. 623-630, 2009.

[11] Bandstructure Lab on nanoHUB.org (http://www.nanohub.org/tools/bandstrlab)