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Derivation, Design and Simulation of the Single-Ended Primary-Inductor Converter (SEPIC)

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Abstract

The purpose of the paper is to guide engineering students and ease their transition from the most basic DC-DC converter topologies to more advanced types. The buck, boost and buck-boost converters are the usual suspects in textbooks and engineering classes to introduce students to the basics of power electronics and switch mode power supplies. There is a gap of how detailed such second order DC-DC converters are described and the more advanced fourth order such as the Ćuk, Zeta and Single-Ended Primary-Inductor Converter (SEPIC). This paper gives a detailed derivation of the equations governing the SEPIC. An example of sizing of components is presented for a range of input voltages and power levels. Finally the design is verified by a circuit simulation using LTSpice.

1 Introduction

Engineering students are introduced to the topics of power electronics and switch mode power supplies through the derivation of the simple second order DC-DC converter topologies such as the buck, boost and buck-boost. The operation of such converters is described in detail and the governing equations are derived step by step in various text books and freely available online sources. However, there is a steep learning curve in open access knowledge when it comes to expanding this knowledge further to fourth order DC-DC converter types such as the Ćuk, Zeta and Single-Ended Primary-Inductor Converter (SEPIC) topologies. The SEPIC is used as the primary case of study for this paper. Often in literature the SEPIC is briefly described and final equations for design are presented with little information of how the equations were originally derived [1–6]. While these references give useful design tips and considerations for choice of components, they do not give a fundamental understanding of the operation of the converter. Popular power electronics textbooks by Muhammed E. Rashid [7], Robert W. Erickson & Dragan Maksimović [8] and Ned Mohan *et al.* [9] introduce fourth order DC-DC converters, but the SEPIC is left out. Once the fundamentals are

understood there are many resources such as describing the topology with coupled inductors [10, 11], its controllability [12–14] and circuit modifications to improve certain performance characteristics [15–17]

The aim of this paper is to narrow the knowledge gap for engineering students between simple second order DC-DC converters and the advanced research papers of fourth order topologies. This is done by providing a detailed derivation of the governing equations for the SEPIC, as described in Section 3 and verifying the design from Section 4 through a circuit simulation in LTSpice in Section 5. This allows engineering student easier access to study and become familiar with the SEPIC topology.

2 Brief discussion of converter topologies

The Ćuk, Zeta and SEPIC topologies include an extra inductor and capacitor compared with the buck, boost and buck-boost topologies and thus they have four passive components to size, hence their name: fourth order converters. The following section briefly describes the thoughts behind the reasoning of choosing a fourth order DC-DC converter topologies over simpler second order.

One of the features is that the Ćuk, Zeta and SEPIC are all capable of both stepping up and down the voltage, when compared to the simple buck and boost topologies. This is often required in applications with variable input voltages such as photovoltaics, batteries or fuel cells. Additionally, as the boost converter topology is only able to step up the voltage, it poses a threat in case of faults on the load, as it is not possible to decrease the output voltage below the input. Thus a large current will flow through the converter, even when the duty cycle is zero. A drawback of the buck and buck-boost converters is that they do not have an inductor on the input, and thus the input source experiences a larger amount of switching harmonics, which is often undesirable. These issues are solved by the use of a fourth order DC-DC converter, such as the Ćuk or SEPIC. These two topologies are DC-DC converters with an input inductor and they are capable of both stepping the voltage up and down. The Zeta converter does not have an input inductor. For quick comparison between the SEPIC and Ćuk, it is worth mentioning that the Ćuk converter has an inverting output voltage, but also has an inductor on the output, meaning that the output capacitor is not as heavily pulsed by currents as for the SEPIC. The following section continues with the derivation of the governing equations of the SEPIC.

3 Derivation and analysis of SEPIC

Initially a general analysis regarding the SEPIC topology is conducted. From this analysis equations to determine the actual component values are obtained. In the following section instantaneous values of currents and voltages are denoted by lower case letters, i and v respectively. Capital letters are used to denote average current and voltage values as I and V.

The circuit diagram of the SEPIC is shown in Fig. 1. Initially its conver-

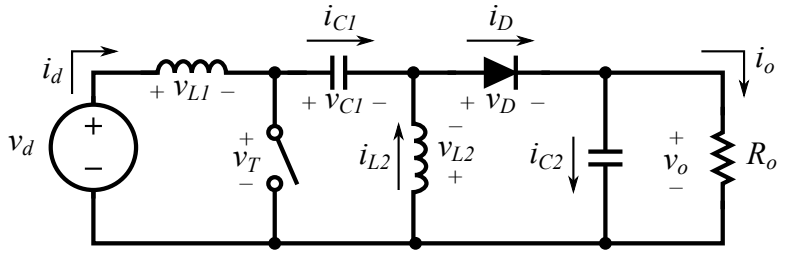

Fig. 1: Circuit diagram of the SEPIC.

sion ratio is determined by using the volt-second balance of the inductors. The volt-second balance states that for the converter operating in steady state the average voltage during a switching cycle of the inductor must be zero. For L_1, when the switch, T, is on the voltage is $v_{L1} = V_d$, while it is $v_{L1} = V_d - V_o - V_{C1}$ when the switch is off, as shown in Fig. 2. Thus when

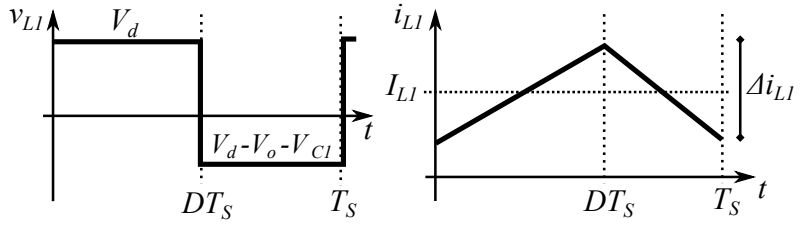

Fig. 2: Voltage and current waveforms of the inductor L_1.

taking the average voltage and equalling it to zero it is obtained that

$$\frac{1}{T_s}\int_0^{T_s} v_{L1}dt = \frac{1}{T_s}\left(\int_0^{DT_s} v_{L1}dt + \int_{DT_s}^{T_s} v_{L1}dt\right) = 0$$
$$\frac{1}{T_s}\left(V_d DT_s + (V_d - V_o - V_{C1})(1-D)T_s\right) = 0$$
$$V_d D + V_d - V_d D - Vo + V_o D - V_{C1} + V_{C1} D = 0$$
$$V_d = (V_o + V_{C1})(1-D)$$
$$V_o + V_{C1} = \frac{V_d}{1-D} \tag{1}$$

Current and voltage waveforms for the inductor, L_2, are shown in Fig. 3. Similarly, by volt-second balance of L_2 it is obtained.

$$\frac{1}{T_s}\int_0^{T_s} v_{L2}dt = \frac{1}{T_s}\left(\int_0^{DT_s} v_{L2}dt + \int_{DT_s}^{T_s} v_{L2}dt\right) = 0$$
$$V_{C1} D - V_o(1-D) = 0$$
$$V_{C1} D - V_o + V_o D = 0$$
$$V_o + V_{C1} = \frac{V_o}{D} \tag{2}$$

By combining (1) and (2) the transfer ratio is obtained as

$$\frac{V_o}{D} = \frac{V_d}{1-D}$$
$$\frac{V_o}{V_d} = \frac{D}{1-D} \tag{3}$$

The average voltage of the two capacitors, V_{C1} and V_{C2}, can now be

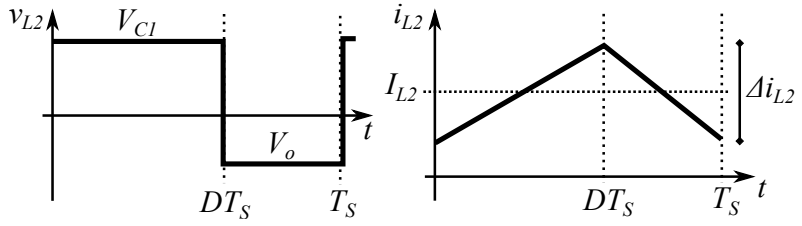

Fig. 3: Voltage and current waveforms of the inductor L_2.

determined. This is done by combining (1) and (3)

$$\begin{aligned} V_{C1} &= \frac{V_d}{1-D} - V_o \\ V_{C1} &= \frac{V_d}{1-D} - \frac{DV_d}{1-D} \\ V_{C1} &= \frac{(1-D)V_d}{(1-D)} = V_d \end{aligned} \tag{4}$$

The average voltage of C_2 is obtained directly from Fig. 1, by assuming that the capacitor is sufficiently large to maintain a constant output voltage, it is seen that

$$V_{C2} = V_o \tag{5}$$

Next is to find the average and ripple currents of the two inductors. For this the power balance between input and output is utilized

$$V_d I_d = V_o I_o \tag{6}$$

From Fig. 1 it is noticed that $I_{L1} = I_d$, thus by combining (6) and (3) it is obtained that

$$I_{L1} = I_d = \frac{V_o I_o}{V_d} = \frac{D}{1-D} I_o \tag{7}$$

To find I_{L2} it is utilized that the average current in the capacitors are known to be zero during steady state operation. Thus from Fig. 1 it is seen that the average output current must be supplied through the diode. The diode only conducts during the time interval from $t = DT_s$ to $t = T_s$, as shown in Fig. 4, and thus it is found that.

$$I_o = I_D = \frac{1}{T_s} \int_{DT_s}^{T_s} i_D dt = \frac{1}{T_s} \left(I_{L1} + I_{L2} \right) (1-D) T_s \tag{8}$$

By inserting (7) to (8) it is obtained that

$$\begin{aligned} I_o &= \frac{D}{1-D} I_o (1-D) + I_{L2}(1-D) \\ (1-D) I_o &= I_{L2}(1-D) \\ I_{L2} &= I_o \end{aligned} \tag{9}$$

The current ripple, Δi_L, is determined by looking at the applied voltage during the on or off state, by utilizing that $v_L = L\frac{di}{dt}$. Assuming constant voltage and thereby linear increasing current it is obtained $v_L = L\frac{\Delta i}{\Delta t}$. During

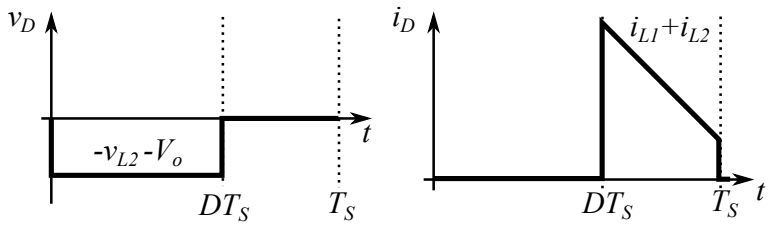

Fig. 4: Voltage and current waveforms of the diode.

the switch on-time the applied voltage to L_1 is $v_{L1} = V_d$. Thus for the inductor, L_1 its current ripple is determined by

$$\Delta i_{L1} = \frac{V_d D T_s}{L_1} \tag{10}$$

By inserting (3) to (10) it is found

$$\Delta i_{L1} = \frac{(1-D)V_o T_s}{L_1} \tag{11}$$

Similarly for L_2 the applied voltage during the off state is $v_{L2} = V_o$, and thus

$$\Delta i_{L2} = \frac{(1-D)V_o T_s}{L_2} \tag{12}$$

For the converter to always operate in continuous conduction mode (CCM) it must be ensured that the current in the two inductors never reaches zero before the end of the switching period. The converter operates on the border between CCM and discontinuous conduction mode (DCM) when the current, i_{L1}, of Fig. 2, reaches zero just at the end of the switching period. At that point it is geometrically seen that the average current I_{L1} is equal to $\frac{\Delta i_{L1}}{2}$, because of the triangular waveform. Thus to ensure CCM one constraint must be for inductor L_1 to fulfil that

$$2I_{L1} \geq \Delta i_{L1} \tag{13}$$

From Fig. 1 it was found $I_{L1} = I_d$, and by inserting (11) to (13) yields

$$L_1 \geq \frac{(1-D)V_o}{2I_d f_s} \tag{14}$$

By substituting (7) for I_d it is found that

$$L_1 \geq \frac{(1-D)^2}{D}\frac{R_o}{2f_s} \tag{15}$$

A similar constraint of CCM operation is made for for L_2, and thus it is obtained that

$$\begin{aligned} 2I_{L2} &\geq \Delta i_{L2} \\ L_2 &\geq \frac{(1-D)V_o}{2I_o f_s} \\ L_2 &\geq (1-D)\frac{R_o}{2f_s} \end{aligned} \tag{16}$$

Sizing the inductors L_1 and L_2 to fulfil (15) and (16) for all operating conditions ensures the converter to operate in CCM.

A requirement is that the voltage ripple ΔV, of the capacitors C_1 and C_2 must not be excessive. To determine the size of the capacitors, C_1 and C_2, it is used that the capacitance is given as $C = \frac{dQ}{dV}$. Rewriting it as the rate of change $\Delta V = \frac{\Delta Q}{C}$. Stating that the change in voltage is proportional to the change in charge over its capacitance. The change in charge is determined by $\Delta Q = \int i(t)dt$. For C_1, by neglecting the current ripple, it is charged by $I_{L2} = I_o$ during the switch on time, as shown in Fig. 5.

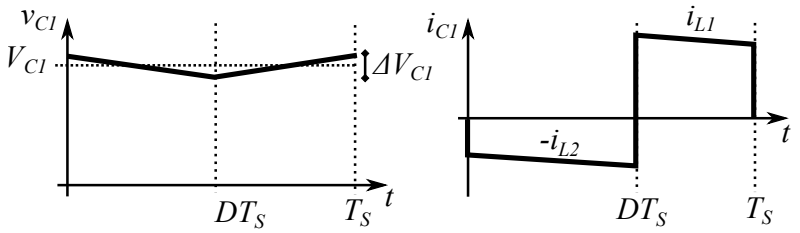

Fig. 5: Voltage and current waveforms of the capacitor, C_1.

Thus it is obtained that

$$\Delta V_1 = \frac{\int_0^{DT_s} I_o dt}{C_1} \tag{17}$$

which equals

$$\Delta V_1 = \frac{I_o D T_s}{C_1} \tag{18}$$

This equation is rearranged to give the value of the capacitance, C_1. However, (18) states how large the voltage ripple is for a given value of C_1. To ensure that the actual voltage ripple is lower than the limit, the equality sign is replaced by an inequality.

$$C_1 \geq \frac{I_o D}{f_s \Delta V_1} \tag{19}$$

Likewise for C_2 which must supply the output current, I_o, to the load during the switch on time, as shown in Fig. 6. It is similarly given that

$$\Delta V_2 = \frac{\int_0^{DT_s} I_o dt}{C_2} \tag{20}$$

which is rearranged to

$$\Delta V_2 = \frac{I_o D T_s}{C_2} \tag{21}$$

$$C_2 \geq \frac{I_o D}{f_s \Delta V_2} \tag{22}$$

Thus from the derivation of the SEPIC, the sizes of inductors, L_1, L_2 and capacitors C_1, C_2 can now be determined. Likewise, expressions of current averages and ripples are obtained.

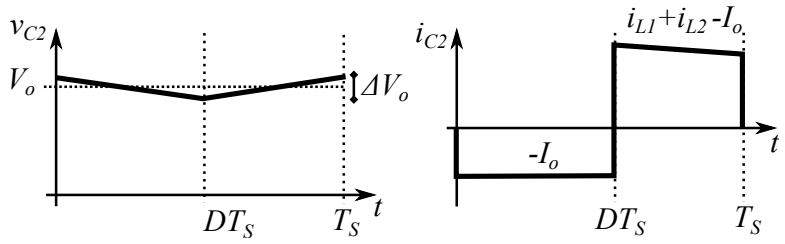

Fig. 6: Voltage and current waveforms of the capacitor, C_2.

4 Calculation of components size

The converter is to be designed to fulfil a given set of requirements by using the derived equations. The converter will be designed and evaluated for its maximum and minimum values, to ensure that it will work under worst case steady state operating conditions. For variables the maximum value and minimum value is denoted $\widehat{X}$ and $\check{X}$, respectively, where X is an arbitrary variable.

The converter must be able to convert a variable input voltage, V_d, of 40 to 60 V into a constant output voltage, V_o, of 100 V with less than 1 % output voltage ripple, ΔV_o, under the worst case, steady state operating conditions. The designed converter should operate in CCM for all expected operating conditions, where the output power, P_o, may vary between 10 and 20 W. Additionally, it is specified that the allowed voltage ripple for the

internal capacitor C_1 is 1 % of its DC-value. Thus for C_1 the voltage ripple must be less than $\Delta V_1 = 0.01 \cdot \widetilde{V_d} = 0.01 \cdot 40V = 0.4V$. The calculations are done for a case where the switching frequency is $f_s = 50$ kHz.

The duty cycle is calculated by rearranging (3) as shown

$$\begin{aligned} \frac{V_o}{V_d} &= \frac{D}{1-D} \\ D &= \frac{V_o}{V_o + V_d} \end{aligned} \tag{23}$$

Because the input voltage, V_d, may vary, the duty will be in the following range

$$\breve{D} = \frac{100\text{V}}{100\text{V} + 60\text{V}} = 0.625 \qquad \widehat{D} = \frac{100\text{V}}{100\text{V} + 40\text{V}} = 0.714 \tag{24}$$

The maximum and minimum current and load resistances are evaluated, as these quantities are used for further calculations.

$$I_o = \frac{P_o}{V_o} \qquad \breve{I_o} = \frac{10\text{W}}{100\text{V}} = 0.1\text{A} \qquad \widehat{I_o} = \frac{20\text{W}}{100\text{V}} = 0.2\text{A} \tag{25}$$

And likewise for the resistance

$$R_o = \frac{V_o}{I_o} \qquad \widetilde{R_o} = \frac{100\text{V}}{0.2\text{A}} = 500\Omega \qquad \widehat{R_o} = \frac{100\text{V}}{0.1\text{A}} = 1000\Omega \tag{26}$$

The size of inductor L_1 is determined by using (15). The worst case condition to ensure CCM occurs when the duty cycle is minimum (during high input voltage, consequently low input current) and the load resistance is high (corresponding to low output current).

$$L_1 \geq \frac{(1-\breve{D})^2}{\breve{D}} \frac{\widehat{R_o}}{2f_s} = \frac{(1-0.625)^2}{0.625} \frac{1000\Omega}{2 \cdot 50000\text{Hz}} = 2.25\text{mH} \tag{27}$$

Similarly is done for L_2 where (15) is used

$$L_2 \geq (1-\breve{D}) \frac{\widehat{R_o}}{2f_s} = (1-0.625) \frac{1000\Omega}{2 \cdot 50000\text{Hz}} = 3.75\text{mH} \tag{28}$$

Now (19) is used to determine the size of capacitor C_1. For this component the worst case conditions occur when the capacitor must maintain its voltage while being subjected to the maximum current I_o for the longest time interval DT_s. Thus the capacitor size is given by

$$C_1 \geq \frac{\widehat{I_o}\widehat{D}}{f_s \Delta V_1} = \frac{0.2\text{A} \cdot 0.7143}{50000\text{Hz} \cdot 0.4\text{V}} = 7.14\mu\text{F} \tag{29}$$

Similarly for C_2 where (22) is used

$$C_2 \geq \frac{\widehat{I}_o \widehat{D}}{f_s \Delta V_2} = \frac{0.2\text{A} \cdot 0.7143}{50000\text{Hz} \cdot 1\text{V}} = 2.86\mu\text{F} \tag{30}$$

5 LTSpice simulation of 50kHz design

In the following section a simulation of the designed SEPIC in LTSpice is presented. The LTSpice circuit diagram is shown in Fig. 7. In addition to

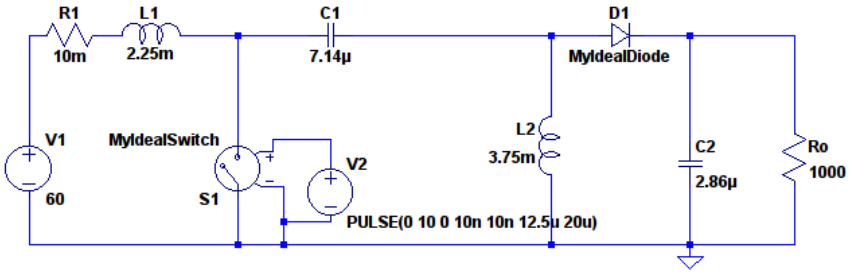

Fig. 7: Screenshot of the LTSpice diagram of the SEPIC.

the circuit diagram, `SPICE Directives` are used to specify models to be used for the diode and the switch, and to specify how the circuit is solved. The `SPICE Directives` used for the diagram in Fig. 7 are

```
1  .model MyIdealSwitch SW(Ron=.01 Roff=1Meg Vt=.001)
2  .model MyIdealDiode D(Ron=.01 Roff=1Meg Vfwd=.001)
3  .tran 3
```

The circuit elements do not turn on instantaneously and cannot have either zero or infinite resistance. Models for both the switch and the diode are specified with finite values in Line 1 and 2. The switch is given finite on and off resistances, but are set very low and high, respectively, to nearly simulate ideal behaviour. Similarly is done for the diode. The trip voltage of the switch is set to 1 mV to ensure it turns on as soon as a non-zero signal is fed to the gate. In Line 3 it is specified that the circuit is solved with non-linear transient analysis. Only the stop time of 3 seconds is specified. This results in the solver using its default settings for all other parameters. This includes a variable step size, which speeds up the simulation process. Otherwise a low time step has to be used to accurately simulate the fast switch turn on/off transients, however this would slow the subsequent solving of the relatively longer on- or off-periods.

When comparing Fig. 7 to Fig. 1 an input resistance, R_1, has been added to the former. When the circuit simulation is initially started a large in-rush currents occur in the circuit. This causes oscillation of the undamped series resonant circuit of L_1, C_1 and L_2. The resistance R_1 is added for the oscillations to eventually diminish.

The duty cycle of the circuit is set by changing the on-time period of the pulse voltage source used as input to the switch gate. The total switching period is set to $T_s = 20\mu$s. The period on-time is set depending on the desired duty cycle. Thus for $D = 0.625$ the $T_{on} = 0.625 \cdot 20\mu\text{s} = 12.5\mu$s and similarly for $D = 0.714$ the on-time period is $T_{on} = 0.714 \cdot 20\mu\text{s} = 14.28\mu$s. The pulse voltage source has transient turn on/off times of 10 ns. It was noted that if these values are set to zero the solver chooses an arbitrary numerical value which is significantly larger than 10 ns. This caused the actual duty cycle to be different than intended.

5.1 Verification by simulation

In the following section the design is verified by simulation of the converter in LTSpice. Initially the size of the inductors, L_1 and L_2, is verified. The inductors were designed to just operate on the limit between CCM and DCM under worst-case, steady-state operating conditions. In this case the worst case condition is when the input current and output current are minimum. This occurs when the input voltage is 60 V and output current, I_o, 0.1 A. To ensure this in the simulation model the input voltage is set to 60 V, the switch on period is set to 12.5 μs and output resistance, R_o equal to 1000 Ω. This produces the inductor current waveforms as shown in Fig. 8.

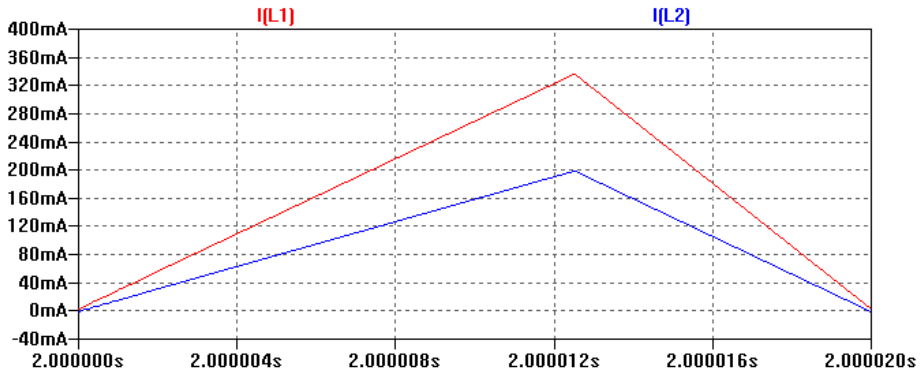

Fig. 8: Inductor current waveforms are on the boundary between CCM and DCM, when $V_d = 60$ V and $R_o = 1000$ Ω.

As seen in Fig. 8 both current waveforms reach zero at the end of the switching period, and thus under the worst-case steady state operating conditions they operate just on the boundary between CCM and DCM as intended. In Section 4 it was found that the worst case operating conditions for C_1 and C_2, is when they have to supply the largest current for the longest amount of time, which is equivalent to low input voltage, $V_d = 40$ V, high duty cycle, $D = 0.714$ and high output power, $R_o = 500\ \Omega$. The specification for both of them is to allow a maximum voltage ripple of 1 % of their DC value. This is 1 V for C_1 while it is 0.4 V for C_2. The voltage of the capacitor during one switching cycle is shown in Fig. 9.

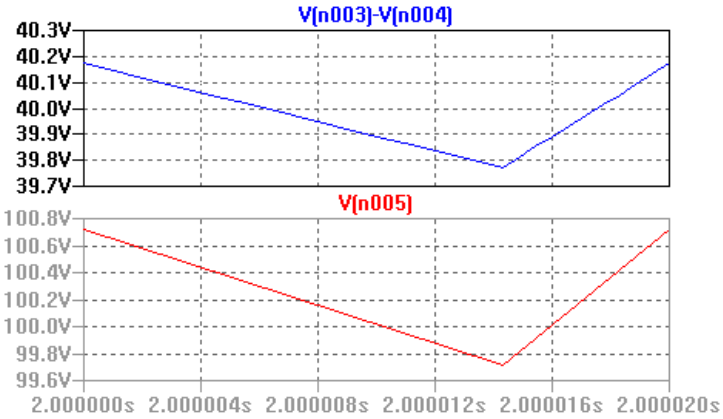

Fig. 9: Capacitor voltages of C_1 (top) and C_2 (bottom) during one switch cycling of their worst case operating conditions.

From Fig. 9 it is verified that the capacitor voltages of C_1 and C_2 are within their specification limit of 1 V and 0.4 V, respectively. However, it is also noted that they both have a small DC-shift. The average DC-voltage of C_1 is found by *"Ctrl + Left click"* on the trace title in LTSpice. This calculates the average value to be 39.973 V. Likewise for C_2 the average voltage is 100.22 V. These are errors of -0.07 % and 0.22 % for C_1 and C_2, respectively. These errors are relatively small and expected to be due to numerical round off errors in the calculations and simulation model specifications. The lower voltage of C_1 is likely to be caused by the voltage drop of the added input resistance, R_1.

For the purpose of doing loss calculations of the switch and diode it is possible to read the average and the root mean square (RMS) current directly from LTSpice. Once again this is done by *"Ctrl + Left click"* trace titles of Fig. 10 to make dialog windows show up in LTSpice, from which both

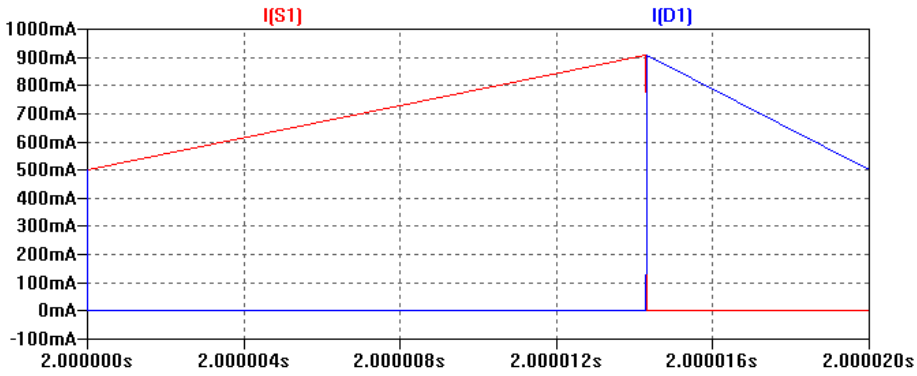

Fig. 10: Current through the switch and the diode.

average and RMS-values are calculated as shown in Fig. 11. This concludes the description of the simulation.

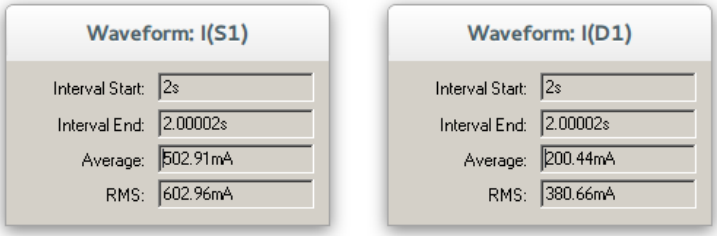

Fig. 11: Calculated RMS values by LTSpice of the switch (left) and diode (right).

6 Conclusion

The literature often lacks a detailed description of the governing equations for the fourth order DC-DC converter topologies such as SEPIC, Ćuk and Zeta. This may create a knowledge gap for engineering students when studying the simple second-order topologies buck, boost and buck-boost converters and the advanced research and design papers available for the fourth order topologies. A detailed analytical derivation of the governing equations of the SEPIC is presented in Section 3. The inductor sizes, L_1 and L_2 are derived from a requirement of CCM operation under steady state operating conditions. Design equations for the sizing of capacitors C_1 and C_2 are based

on an allowable voltage ripple.

Passive component sizes are evaluated for a given set of operating conditions in Section 4. In Section 5 the converter design is simulated in LTSpice. The LTSpice circuit diagram of the SEPIC is provided and the required near-ideal semiconductor models are defined. An additional input resistance is added on the input to reduce resonance oscillations caused by initial in-rush currents when the circuit simulation is started. Without the resistance the oscillations remain due to an undamped series resonant circuit consisting of C_1, L_1 and L_2. The analytical results evaluated in Section 4 are verified by the LTSpice simulation. All calculated quantities show good compliance with the simulation.

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