

Design and Analysis of a Full-Bridge LLC-Based PEV Charger Optimized for Wide Battery Voltage Range

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Abstract—In this paper, a two-stage onboard battery charger is analyzed for plug-in electric vehicles (PEVs). An interleaved boost topology is employed in the first stage for power factor correction (PFC) and to reduce total harmonic distortion (THD). In the second stage, a full-bridge LLC-based multiresonant converter is adopted for galvanic isolation and dc/dc conversion. Design considerations are discussed, focusing on reducing the charger volume and optimizing the conversion efficiency over the wide battery-pack voltage range. A detailed design procedure is provided for a 1-kW prototype, charging the battery with an output voltage range of 320–420 V from 110-V 60-Hz single-phase grid. Experimental results show that the first-stage PFC converter achieves THD of less than 4% and a power factor higher than 0.99, and the second-stage LLC converter operates with 95.4% peak efficiency and good overall efficiency over wide output voltage ranges.

Index Terms—Full-bridge LLC, interleaved boost converter, onboard charger, plug-in electric vehicle (PEV).

I. INTRODUCTION

HIGH power density, high conversion efficiency, high power factor, and low total harmonic distortion (THD) are the desired features expected from onboard plug-in electric vehicle (PEV) battery chargers [1]–[4]. Fig. 1 shows the general power electronic architecture of a typical onboard PEV battery charger. The system consists of a front-end ac/dc converter used for rectification at a unity power factor and a second-stage dc/dc converter responsible for battery current regulation and providing galvanic isolation [5], [6]. A comprehensive topological survey of the currently available PEV charging solutions has been presented in [4].

A boost converter is a common front-end PFC interface due to its simple structure, good THD reduction performance, and unity power factor operation capability [7], [8]. However, the

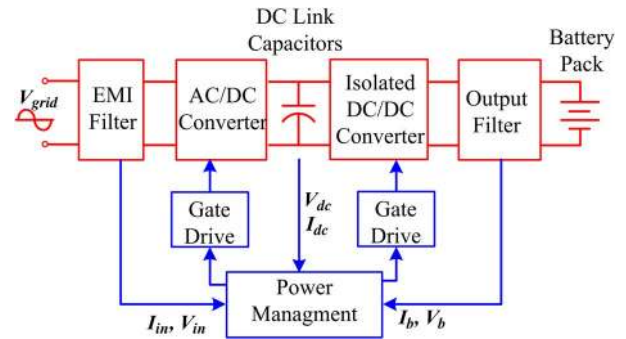


Fig. 1. General system architecture of a battery charger.

volume of the converter tends to increase with the increase in charging power. Moreover, high RMS current in the dc-link capacitors would generate high power loss and significantly reduce the capacitor's lifetime, leading to capacitor failures. In addition, the required inductance value to reduce the ripples in the input current for better THD performance would considerably increase as the charging power increases [9]. This results in a large-volume inductor core and wire size. Compared with a single-phase boost PFC converter, the interleaved boost topology has the benefits of reduced overall volume and improved power density [10]–[12].

In the dc/dc isolation stage, resonant converters are preferable at high-voltage and high-power PEV battery charging applications. In particular, multiresonance-based LLC topology has several advantages over other resonant topologies, such as 1) good voltage regulation performance at light load condition, 2) the ability to operate with zero-voltage switching (ZVS) over wide load ranges, 3) no diode reverse recovery losses through soft commutation, 4) low voltage stress on the output diodes, and 5) having only a capacitor as the output filter compared with the conventional LC filters [13], [14]. Despite these advantages, operating the circuit at the maximum efficiency considering the conduction and switching losses over the full output voltage ranges remains a challenging issue as the battery voltage varies in a wide range depending on the different states of charge (SOCs) [15]–[17].

In this paper, an onboard PEV charger topology consisting of an interleaved boost PFC rectifier followed by an LLC multiresonant dc/dc converter is proposed. Both the interleaved boost PFC and full-bridge LLC stages are extendable to higher

Manuscript received August 6, 2013; revised October 8, 2013; accepted October 26, 2013. Date of publication November 5, 2013; date of current version May 8, 2014. This work was supported in part by the Maryland Industrial Partnerships Program. The review of this paper was coordinated by Dr. C. C. Mi.

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Digital Object Identifier 10.1109/TVT.2013.2288772

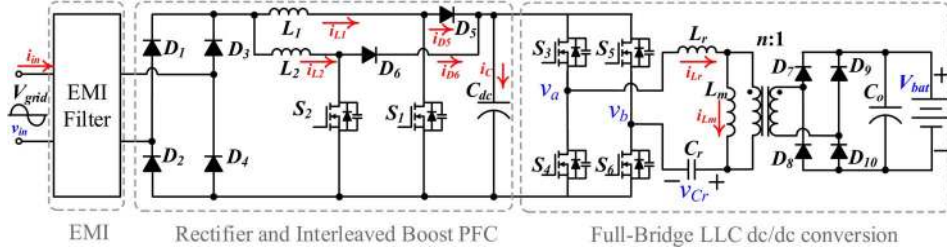


Fig. 2. Schematic of the proposed isolated onboard charger.

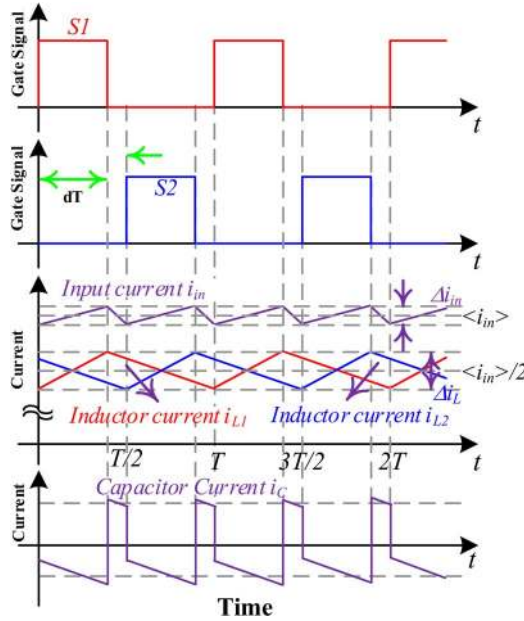


Fig. 3. Waveforms of the two-leg interleaved boost converter ($d < 0.5$).

power levels with high power density and conversion efficiency. The proposed charger design is optimized for a wide voltage range (320–420 V) in a lithium-ion battery pack. Moreover, the optimum design of LLC magnetic components, to achieve the maximum overall efficiency, is addressed in detail. In addition, circumstantial loss analysis is addressed to evaluate the LLC converter's overall performance.

II. PROPOSED CHARGER BASED ON INTERLEAVED BOOST FOLLOWED BY LLC CONVERTER

The schematic of the proposed isolated charger with interleaved boost front-end rectifier followed by an LLC dc/dc converter is shown in Fig. 2.

A. Interleaved Boost PFC Converter

The interleaved converter is a multileg converter, with each leg operating $2\pi/n$ out of phase, where n denotes the number of phases. In this structure, a two-leg interleaved boost converter, whose interleaving legs are operated with π phase difference, is utilized. Fig. 3 shows the waveforms of a two-leg interleaved boost converter. As shown in Fig. 3, the control of the interleaved converter is based on shifting the phase of S_1 with respect to S_2 such that the ripples cancel out each other either completely or to some extent, depending on the

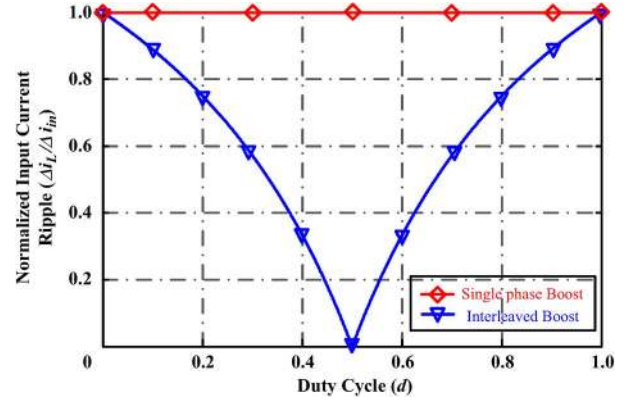


Fig. 4. Effective input current ripple cancellation in the two-leg interleaved converter.

duty-cycle ratio. The following shows how the normalized input current ripple $K(d)$ varies as a function of duty cycle d :

$$K(d) = \frac{\Delta i_{in}}{\Delta i_L} = \begin{cases} \frac{1-2d}{1-d}, & d \leq 0.5 \\ \frac{2d-1}{1-d}, & d > 0.5 \end{cases} \quad (1)$$

As demonstrated in Fig. 4, in comparison with single-stage boost topology, the current ripple of the interleaved boost converter is improved over the full duty-cycle range. In particular, at 50% duty cycle, a ripple-free current can be maintained.

Another advantage of an interleaved topology is that the input current is evenly shared between the interleaved inductors. For the two-leg interleaved topology, the energy stored in the inductor is defined as

$$E = \frac{1}{2}L \left(\frac{i_{in,rms}}{2} \right)^2 + \frac{1}{2}L \left(\frac{i_{in,rms}}{2} \right)^2 = \frac{1}{4}Li_{in,rms}^2. \quad (2)$$

According to (2), the energy stored in the inductor is half in comparison with single-stage boost topology. This reduction could effectively reduce the inductor volume for the same performance criteria as of the conventional boost converter. In [18], a 500-W two-leg interleaved boost converter with an output of 385 V has been analyzed, and a volume reduction of 32% is reported.

In the proposed interleaved structure, the output capacitor current can be expressed as

$$i_C = i_{D5} + i_{D6} - i_o. \quad (3)$$

The normalized capacitor RMS current ($i_{C,rms}/i_{in}$) is a function of duty cycle and can be expressed as

$$i_{C,rms}/i_{in} = \begin{cases} \sqrt{-d^2 + 0.5d}, & d \leq 0.5 \\ \sqrt{-d^2 + 1.5d - 0.5}, & d > 0.5 \end{cases} \quad (4)$$

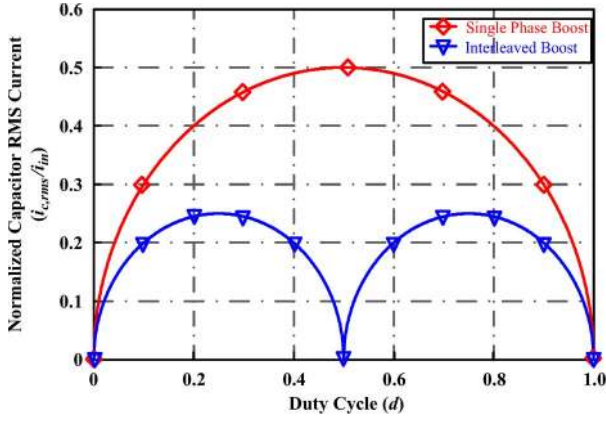


Fig. 5. Effective output capacitor RMS current reduction in the two-leg interleaved converter.

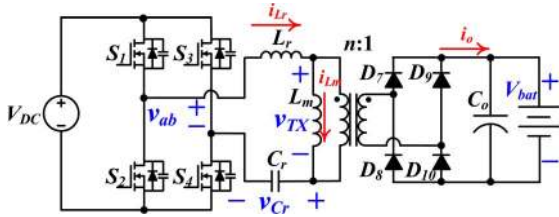


Fig. 6. Schematic of a full-bridge LLC resonant converter.

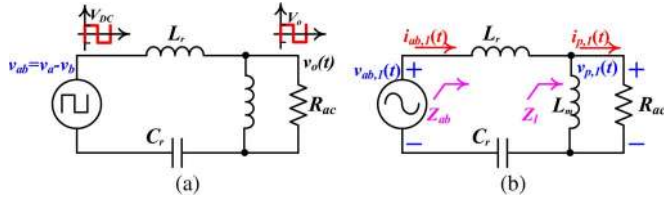


Fig. 7. (a) Simplified LLC full-bridge converter circuit. (b) Circuit model under FHA.

Fig. 5 shows the normalized capacitor RMS current in a single-stage boost converter and a two-leg interleaved boost converter. The peak capacitor RMS current is half in the interleaved structure. The improvement in the capacitor RMS current reduces the power loss dissipation on the equivalent series resistance (ESR) of the capacitor along with the electrical and thermal stresses on the capacitor, thereby improving the converter reliability.

B. Full-Bridge LLC Resonant Converter

As shown in Fig. 6, the full-bridge LLC resonant converter consists of four parts: 1) a dc voltage source and a complementary switching network, which operate as a square-wave generator; 2) a resonant tank; 3) a transformer with $n:1$ turns ratio; 4) a full-bridge rectifier; and 5) a filter capacitor.

The battery pack, which is the load of the LLC resonant converter, can be treated equivalent to a resistive load, whose resistance equals to the battery voltage divided by the charging current. This resistive load in the secondary side of the transformer can be expressed as an effective resistor in the primary side [see Fig. 7(a)]. The LLC resonant network functions similar to a filter, which filters out the higher odd harmonics of the input square wave. To simplify the analysis, using first har-

monic approximation (FHA), the LLC converter is modeled as shown in Fig. 7(b), where $v_{ab,1}(t)$, $i_{ab,1}(t)$, $v_{p,1}(t)$, and $i_{p,1}(t)$ denote the first harmonic components of input voltage $v_{ab}(t)$, input current $i_{ab}(t)$, voltage of the primary side of transformer $v_p(t)$, and the current of the primary side of transformer $i_p(t)$, respectively.

The resistance of the equivalent ac resistor can be derived as

$$R_{ac} = \frac{8n^2}{\pi^2} R_L = \frac{8n^2}{\pi^2} \frac{V_{bat}}{I_{bat}}. \quad (5)$$

According to the ac equivalent model shown in Fig. 7(b), the normalized voltage gain, transconductance, and the conductance of the circuit can be derived as

$$G_n = \frac{v_{p,1,rms}}{v_{ab,1,rms}} = \left| \frac{Z_l}{Z_{in}} \right| \quad (6)$$

$$g_n = \frac{i_{p,1,rms}}{v_{ab,1,rms}} = \left| \frac{Z_l}{Z_{in}} \right| \frac{1}{R_{ac}} \quad (7)$$

$$C_n = \frac{i_{ab,1,rms}}{v_{ab,1,rms}} = \left| \frac{1}{Z_{ab}} \right| \quad (8)$$

where Z_{ab} and Z_l are the input impedance and load impedance of the ac equivalent model. Assuming that the FHA is sufficiently accurate, the battery voltage, charging current, and input RMS current can be expressed as

$$V_{bat} \approx \frac{v_{p,1,rms}}{v_{in,1,rms}} \frac{V_{dc}}{n} = \left| \frac{Z_l}{Z_{in}} \right| \frac{V_{dc}}{n} \quad (9)$$

$$I_{bat} = \frac{V_{bat}}{R_L} \approx \left| \frac{Z_l}{Z_{in}} \right| \frac{8n}{R_{ac}\pi^2} \quad (10)$$

$$i_{ab,rms} = \left| \frac{v_{ab,rms}}{Z_{ab}} \right| = \left| \frac{V_{dc}}{Z_{ab}} \right|. \quad (11)$$

The input impedance of the ac equivalent model Z_{ab} can be either capacitive or inductive. Operating in the inductive region facilitates the ZVS feature of power MOSFETs. Consequently, only the inductive region is considered since MOSFETs are utilized as the primary switch.

As the switching frequency increases, the size of energy storage components reduces and the energy density of the converter effectively improves. Therefore, MOSFETs operating at high switching frequency in the inductive region are considered in the following analyses.

Two resonance frequencies f_p and f_s are defined in

$$f_p = \frac{1}{2\pi\sqrt{L_r C_r}} \quad (12)$$

$$f_s = \frac{1}{2\pi\sqrt{(L_r + L_m) C_r}}. \quad (13)$$

To illustrate different load conditions, quality factor Q is introduced. Q is defined to be the ratio between characteristic impedance ($\sqrt{L_r/C_r}$) and the load resistance

$$Q = \frac{\sqrt{L_r/C_r}}{R_{ac}}. \quad (14)$$

Large Q corresponds to small load resistance and heavy load condition. On the contrary, small Q corresponds to large load resistance and light load condition.

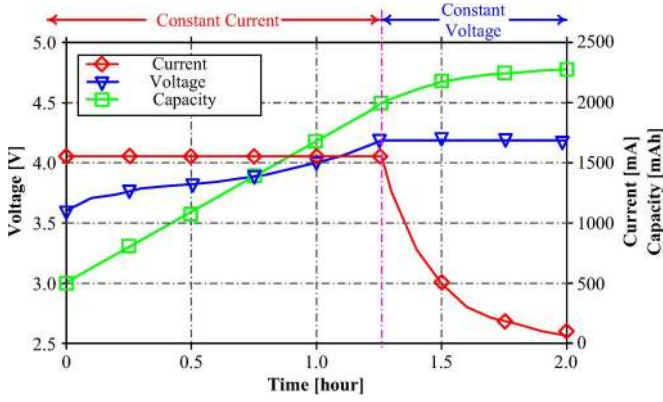


Fig. 8. Charging characteristics of a Li-ion battery cell [21].

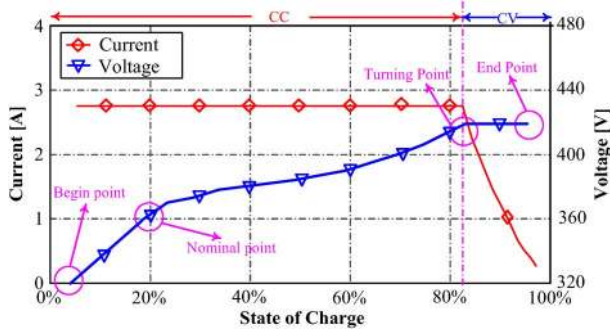


Fig. 9. Charging profile of the Li-ion battery pack.

TABLE I

KEY POINTS IN THE CHARGING PROFILE OF THE PEV BATTERY PACK

Parameter	Begin Point	Nominal point	Turning point	End point
V_{bat}	320V	360V	420V	420V
I_{bat}	2.38A	2.38A	2.38A	0.24A
P	762 W	857 W	1000 W	100 W
R_{Tl}	134.5Ω	151.3Ω	176.5Ω	1750 Ω

III. DESIGNING A 1-kW PLUG-IN ELECTRIC VEHICLE CHARGER PROTOTYPE

Here, the design considerations for an interleaved boost and LLC-Based PEV charger rated at 1 kW is presented. It is aimed to charge a Li-ion battery with nominal voltage of 360 V from depleted (320 V) to fully charged (420 V) conditions. The charging process is divided into constant current (CC) and constant voltage charging (CV) stages [19], [20].

A. Charging Profile of the Li-Ion Battery

Fig. 8 provides the charging characteristics of a single Li-ion battery cell. The nominal voltage of the battery is 3.6 V. Based on the charging data of a single battery cell, the charging profile of the Li-ion battery pack can be obtained, as plotted in Fig. 9.

According to Fig. 9, there are four key points in the charging process. The beginning point and the end point correspond to the beginning and end of the charging process, respectively. At the nominal point, the battery voltage is equal to the nominal voltage of the battery pack. The turning point marks the transition from CC to CV charging mode. Parameters of those four key points are summarized in Table I. The quality factor at each point can be calculated using (5) and (14).

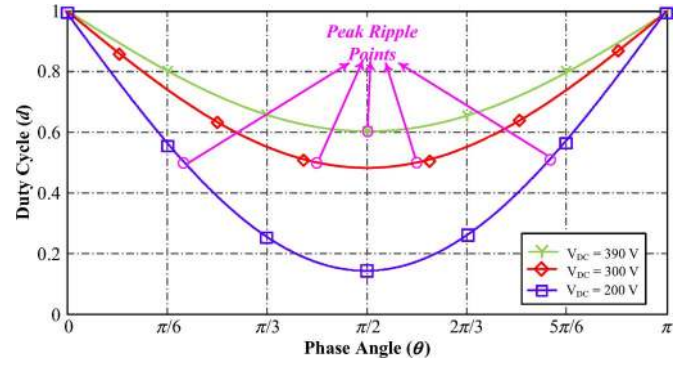


Fig. 10. Duty cycles corresponding to dc-link voltages of 390, 300, and 200 V.

The following section outlines charger design to ensure meeting battery charging requirements on these four critical operating points.

B. Interleaved Boost PFC Converter Design

In the PFC boost converter, the instantaneous duty cycle d varies with the input voltage as

$$d(\theta) = 1 - \frac{|V_{in}|}{V_{dc}} = 1 - \frac{155.5|\sin \theta|}{V_{dc}} \quad (15)$$

where 155.5 V is the peak input voltage, and θ is the phase angle between the input voltage and current. The inductor current ripple can be expressed as

$$\Delta I_L = \frac{|V_{in}|}{L} d(\theta) T_s = \frac{155.5 T_s}{L} \left(|\sin \theta| - \frac{155.5}{V_{dc}} (\sin \theta)^2 \right). \quad (16)$$

Assume that $x = |\sin \theta|$, then $0 \leq x \leq 1$. The derivative of ΔI_L is calculated as

$$\frac{\delta \Delta I_L}{\delta x} = \frac{155.5 T_s}{L} \left(1 - \frac{311}{V_{dc}} x \right). \quad (17)$$

According to (17), if $V_{dc} \leq 311$ V, the peak ripple happens when $x = V_{dc}/311$. Substituting x into (15), d is calculated as 0.5. If $V_{dc} > 311$ V, the peak ripple happens when $x = 1$, and $\theta = \pi/2$. Based on the previous analysis in Section II-A, the duty cycle close to 50% provides the best inductor current ripple cancellation, as well as RMS capacitor current cancellation.

Conventionally, the dc-link voltage of the grid-connected front-end ac/dc converter V_{dc} has the typical value to be 390 V [21]. However, in this paper, V_{dc} is designed to be 300 V. This is because $V_{dc} = 300$ V has overall duty cycles closer to 0.5 and better ripple cancellation effect, which could be clearly observed in Fig. 10.

The circuit is designed to operate at the switching frequency of 200 kHz, taking the tradeoff between the sizes of the inductors and dc-link filter capacitor and switching losses into account. The inductor ripple current at the peak of line ($\theta = \pi/2$) is designed to be 30% of the inductor current, i.e.,

$$\Delta I_{L \max} = \sqrt{2} I_{L \text{rms}} \times 0.3 = \sqrt{2} \frac{P_{\max}}{2 V_{in, \text{rms}}} \times 0.3. \quad (18)$$

According to (16) and (18), inductances could be calculated as

$$L_1 = L_2 = \frac{T_s V_{in,rms} \times \sqrt{2}}{\Delta I_{L,max}} d \left(\theta = \frac{\pi}{2} \right). \quad (19)$$

The ripple voltage at the dc-link capacitor is set to be 5% of the dc-link voltage, which is 15 V. Based on this ripple voltage, the dc-link capacitance could be calculated as follows:

$$C_{dc} = \frac{2P_{max}}{2\pi V_{dc} V_{ripple} 2f_{line}}. \quad (20)$$

C. Full-Bridge Series LLC Converter Design

In this paper, design and optimization of the LLC converter are both facilitated by FHA analysis and the Simulink simulation. As aforementioned in Section II, f_p and f_s are the two resonance frequencies of the LLC resonant tank. When the switching frequency f is higher than f_p , the resonant tank becomes inductive. When the f is lower than f_s , the resonant tank becomes capacitive. In between f_s and f_p , inductive or capacitive operation region is determined by the load. On the other hand, as the switching frequency is varied closer to f_p , the impedance of the resonant tank becomes smaller. This can reduce the circulating energy in the resonant tank, which results in the reduction in the conduction losses of the LLC converter. Therefore, the LLC converter is desired to operate in the inductive region and close to f_p for minimizing switching and conduction losses and maximizing efficiency.

For design considerations, f_p is preset by the optimum operating frequency of the MOSFETs, considering the tradeoff between high frequency operation and switching power loss. Thus, the product of L_r and C_r can be determined as the initial design step. Short-circuit performance ($Q = \infty$) and peak voltage gain at maximum output power ($Q = Q_{turn}$) are two important considerations in designing L_r and C_r . When the short circuit happens, the power management module shifts the switching frequency to a higher value ($2 \sim 3f_p$) to increase the impedance of the resonant tank; hence, the short-circuit current could be effectively reduced and limited to a predetermined value. If L_r is large, the resonant-tank impedance becomes large as well, whereas the short-circuit current becomes smaller. However, for constant f_p , a larger L_r would result in a smaller C_r , which increases the voltage stress of the resonant capacitor and the quality factor. The increase in quality factor reduces the peak voltage gain. This might cause potential failure to fulfill the voltage gain specification at heavy load condition. The values of L_r and C_r are determined based on this tradeoff.

The design of L_m is based on the tradeoff between conduction losses and switching losses. Smaller L_m corresponds to a smaller operation frequency range, which provides lower conduction losses. However, if L_m decreases, the switch turning off current increases, which in turn would result in higher switching losses. The value of L_m is determined from this tradeoff.

Based on those two design tradeoffs, the dc/dc stage parameters can be designed. Fig. 11 summarized the flowchart to achieve the optimal design.

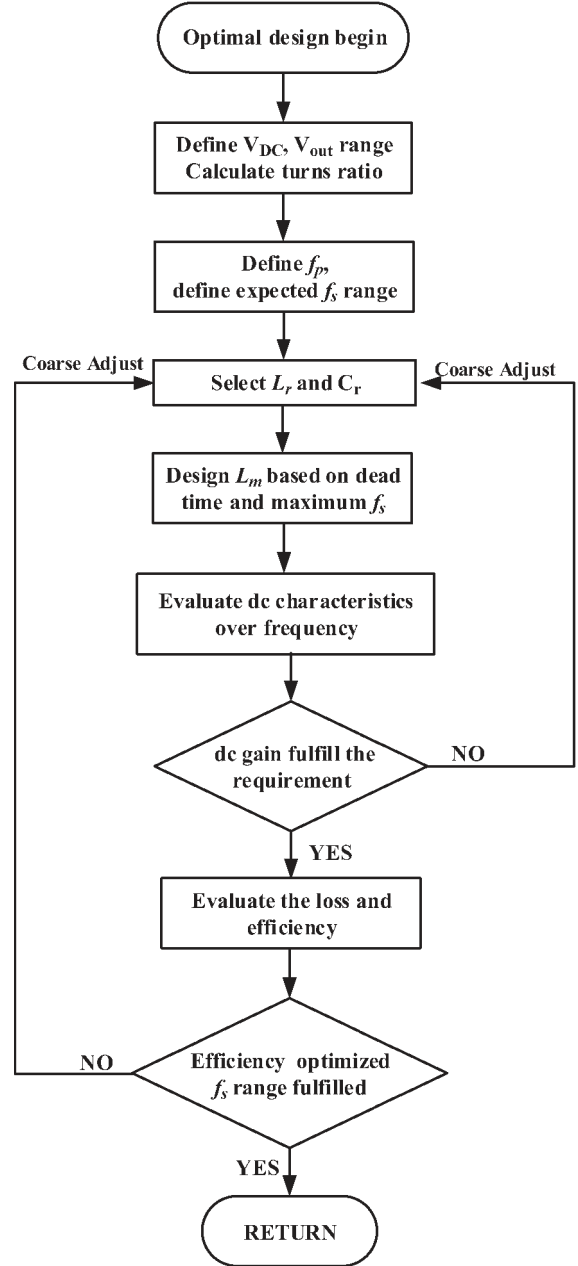


Fig. 11. Flowchart of the resonant network design.

1) *Selection of the Turns Ratio of the Transformer:* The transformer turns ratio is determined by the ratio between dc-link voltage and the nominal voltage of the battery pack, i.e.,

$$n = \frac{V_{dc}}{V_{nom} + 2V_d} \quad (21)$$

where V_d is the voltage drop across the secondary-side diode.

According to (21), at nominal voltage, the LLC converter would operate at the primary switching frequency since the time interval when the battery-pack voltage is below nominal voltage only takes a small part of the charging process. The time period when the LLC converter is operating in ZVS region 2 ($f \geq f_p$) can be minimized. Thus, the reverse recovery problem of secondary diodes can be relieved. Moreover, in CV charging mode, the operating region would be close to the primary resonant frequency, which brings the benefit of reduced circulating losses.

2) *Selection of L_r and C_r* : The primary resonance frequency was determined as $f_p = 200$ kHz. According to (12), the product of L_r and C_r can be found as

$$\sqrt{L_r C_r} = 1/(2\pi f_p). \quad (22)$$

As aforementioned, there is a tradeoff between the peak voltage gain at heavy load and the short-circuit current. In this case, the peak voltage gain at the turning point is the heaviest load condition in CV charging mode. The voltage gain must be larger than $420/360 = 1.17$. The short-circuit current should be smaller than the maximum current of the charger (2.38 A). Based on this tradeoff and following the flowchart shown in Fig. 11, multiply iterations have been done before finalizing the value of Q_{turn} to be 0.94. With this quality factor, both the requirements on the switching frequency range and short-circuit current can be fulfilled. Thus, the ratio between L_r and C_r can be determined by

$$\sqrt{L_r/C_r} = Q_{\text{turn}} \times \frac{8n^2}{\pi^2} \times 176.5 \Omega. \quad (23)$$

From (22) and (23), L_r and C_r are calculated as $63.4 \mu\text{H}$ and 10 nF , respectively.

3) *Selection of the Magnetizing Inductance L_m* : To ensure ZVS operation, the upper limit of L_m can be derived as

$$L_m \leq \frac{t_{\text{dead}}}{16C_{\text{oss}}f_{\text{max}}} \quad (24)$$

where C_{oss} is the equivalent output capacitance of the power MOSFET, t_{dead} is the deadband, and f_{max} is the maximum switching frequency. On one hand, L_m must be large enough to reduce the circulating current in L_m and the turning off current. On the other hand, L_m must be small enough to ensure a narrow switching frequency region, which corresponds to small input impedance and small circulating current.

Based on this tradeoff and following the flowchart shown in Fig. 11, multiple iterations have been done before finalizing the value of L_m to be $160 \mu\text{H}$.

4) *Evaluation of DC Frequency Characteristics*: After determining the critical parameters, the dc frequency response of the designed LLC converter must be evaluated to ensure that it fulfills the design specifications and exhibits overall good performance. If the design does not fulfill the requirement, we must go back to the initial step and adjust the design procedures until the optimal design is achieved.

Based on (9)–(11), voltage and current curves versus a wide frequency range for 1-kW charger are plotted in Fig. 12. These parameters correspond to the beginning-point, nominal-point, turning-point, end-point, and short-circuit conditions.

According to Fig. 12(a), in CV charging mode, the output voltage is constrained at 420 V, which is the fully charged battery-pack voltage. From the turning point to the end point, the switching frequency increases from 159.1 to 171.2 kHz. As shown in Fig. 12(b), in CC charging mode, the charging current is limited to 2.38 A. From the beginning point to the turning point, the switching frequency decreases from 225.3 to 159.1 kHz. Under short-circuit condition, the switching frequency needs to be boosted to higher than 330 kHz so that the

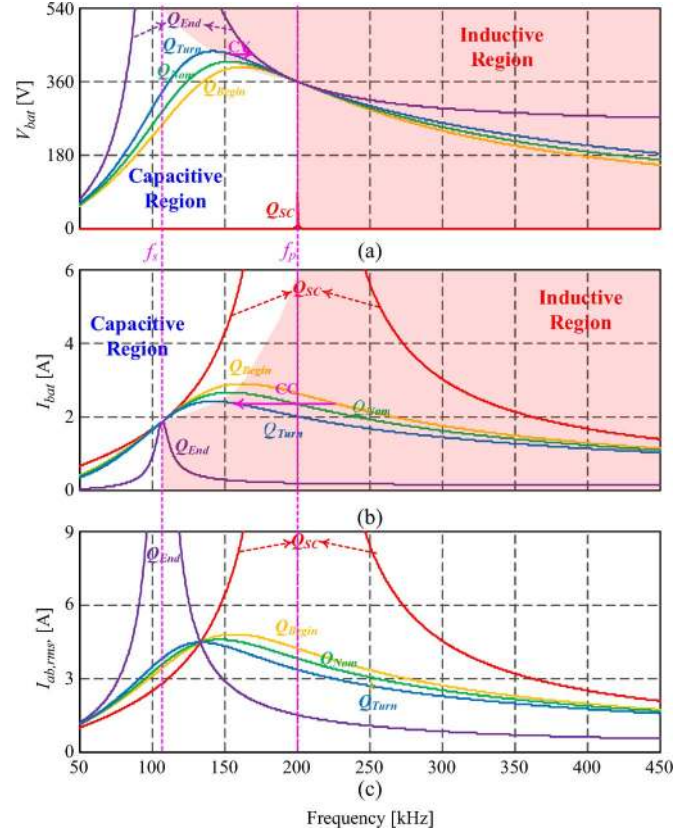


Fig. 12. DC characteristics of the designed 1-kW LLC converter. (a) Output voltage. (b) Charging current. (c) Input current.

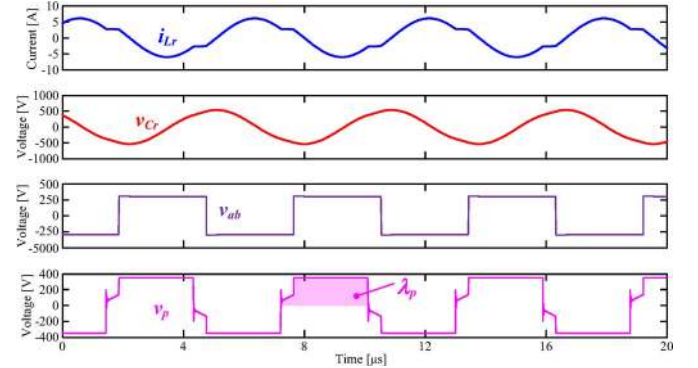


Fig. 13. Simulated LLC results at the turning point ($V_{\text{bat}} = 420$ V, and $I_{\text{bat}} = 2.38$ A).

short-circuit current could be constrained to be lower than the nominal current.

IV. OPTIMIZATION OF THE LLC MAGNETIC COMPONENTS

Due to the rigid requirements on the values of L_m and L_r , both the transformer and the resonant inductor need to be customized.

To obtain the voltage and current ratings of the magnetic components, waveforms at peak power point (1 kW), which corresponds to the turning point of the charging process, are simulated, and resultant waveforms of resonant inductor current i_{L_r} , resonant capacitor voltage v_{C_r} , input voltage to the resonant tank v_{ab} , and voltage at the primary side of transformer v_p are plotted in Fig. 13.

A. Optimization of Transformer

As shown in Fig. 13, due to the alternating current in the transformer primary side, flux in the magnetic core crosses both the first and third quadrants of the B – H loop. Peak ac flux density ΔB is determined by the volt-second on the primary side of the transformer λ_p as

$$\Delta B = \frac{\lambda_p}{2n_p A_e} \quad (25)$$

where A_e is the effective cross-sectional area of the core; n_p is the number of primary turns.

Core loss P_{fe} is associated with ΔB as

$$P_{fe} = P_{cv} V_e = K_{fe} (\Delta B)^\beta V_e \quad (26)$$

where P_{cv} is the core-loss volume density; K_{fe} is a constant of proportionality, which depends on the switching frequency; and β is a constant, depending on the material. For ferrite power material, the typical value of β is 2.7.

Copper loss P_{cu} can be calculated as

$$P_{cu} = R_{cu} I_{tot}^2 = \frac{\rho n \text{MLT}}{A_w} I_{tot}^2 \quad (27)$$

where ρ is the wire resistivity, MLT is mean length per turn, A_w is the cross-sectional area of the wire, and I_{tot} is the total RMS winding current, which is referred to the primary side, i.e.,

$$I_{tot} = I_{p,rms} + n I_{s,rms}. \quad (28)$$

According to (24)–(26), the total loss P_{tot} can be derived as a function of ΔB :

$$P_{tot} = P_{fe} + P_{cu} = K_{fe} (\Delta B)^\beta V_e + \frac{\rho \text{MLT}}{A_w} \frac{\lambda_p}{2 \Delta B A_e} I_{tot}^2. \quad (29)$$

According to (29), the derivative of P_{tot} over ΔB_L could be calculated as

$$\frac{dP_{tot}}{d\Delta B_L} = K_{fe} V_e (\Delta B)^{\beta-1} - \frac{\rho \text{MLT}}{A_w} \frac{\lambda_p}{2 (\Delta B)^2 A_e} I_{rms}^2. \quad (30)$$

By equalizing the derivative to be zero, the optimal value of ΔB , which corresponds to the minimum total loss, can be obtained. The design of the resonant inductor is based on this optimization. Design procedures are provided in the following.

1) *Select Core Material*: In this application, ferrite cores, which have high saturation flux B_s and low losses at high frequencies, are preferable. PC40 ferrite core, with B_s of 0.51 T at room temperature, is chosen for both transformer and inductor.

2) *Determine Core Size*: According to (25), a big core corresponds to big A_e and provides sufficient margin to regulate both ΔB and core loss to a low value. Moreover, the core window must be large enough to fill the wire winding with a specific gauge. However, a big core has the penalty of big core weight, and there will be little margin to tune the air gap length. Based on this consideration, ETD44 core is selected. Critical parameters of ETD44 core are detailed in Table II.

TABLE II
CRITICAL PARAMETERS OF MAGNETIC COMPONENTS

Parameter	Symbol	Transformer	Resonant Inductor
Core type	N/A	ETD44	ETD39
Core material	N/A	PC47	PC47
Saturation flux (25°C)	B_s	0.51 Tesla	0.51 Tesla
Vacuum permeability	μ_o	$4\pi \times 10^{-7}$	$4\pi \times 10^{-7}$
Inductance	L	160 μH	61.3 μH
Magnetic path length	l_m	10.3 cm	9.21 cm
Effective cross-section area	A_e	1.75 cm ²	1.25 cm ²
Bobbin winding area	A_w	2.13 cm ²	1.74 cm ²
Mean Length Path	MLT	7.62 cm	6.86 cm
Effective Core Volume	V_e	18 cm ³	11.5 cm ³
Primary turns	n_p	20 turns	28 turns
Secondary turns	n_s	24 turns	N/A
Maximum flux	ΔB_{max}	0.15 Tesla	0.12 Tesla
Air gap length	l_g	0.55 mm	1.6 mm
Litz wire gauge	AWG	14	14

3) *Select the Number of Turns*: Based on (30) and Table II, optimal ΔB is calculated to be 0.15 T. The volt-second on the primary side of the transformer at 1 kW operation, which corresponds to the shaded area in Fig. 13, is calculated as

$$\lambda_p = \int v_p dt = 1.03 \times 10^{-3} \text{Vs}. \quad (31)$$

According to (25), the number of primary turns could be obtained:

$$n_p = \frac{\lambda_p}{2 \Delta B A_e} = \frac{1.03 \times 10^{-3}}{2 \times 0.15 \times 1.75 \times 10^{-4}} = 19.62 \approx 20. \quad (32)$$

The secondary turns are found by

$$n_s = \frac{n_p}{n} \approx 24. \quad (33)$$

4) *Air-Gap Length*: The length of air gap l_g can be calculated according to the desired inductance [22]

$$l_g = \frac{\mu_o n^2 A_e}{L} = \frac{4\pi \times 10^{-7} \times 20^2 \times 1.75 \times 10^{-4}}{160 \times 10^{-6}} = 0.55 \text{ mm}. \quad (34)$$

5) *Check for Saturation*: ΔB equals to the maximum flux density. Since ΔB (0.14 T) is designed to be much smaller than B_{sat} (0.51 T), saturation could be efficiently avoided in this design.

6) *Evaluating the Wire Size*: The upper limit cross-sectional areas of primary and secondary wires A_{wp} and A_{ws} , respectively, can be evaluated based on (34) as follows:

$$A_{wp} n_p + A_{ws} n_s \leq K_u A_w \quad (35)$$

where A_w is the bobbin winding area. K_u is the fill factor of the core window and is assumed to be 0.5 in this design.

In high switching frequency operation, the Litz wire must be used to reduce the skin effect and proximity effect losses. To have the wire radius smaller than twice the skin depth, AWG 44 wire must be used. In this design, the wire-gauge AWG 15 Litz cable, which is made of 810 strands of AWG 44 wires, is used to wind both primary and secondary turns [23].

B. Optimization of Inductor

Practically, the leakage inductance on the primary side of the transformer must be excluded from the theoretical resonant inductance. In this design, the leakage inductance of the transformer is measured to be $2.1 \mu\text{H}$. Thus, the inductance of the discrete inductor is calibrated as

$$L = L_{L_r} - L_{\text{Leak}}. \quad (36)$$

The design of inductor follows the same procedures as that of the transformer. Obtained design parameters of the inductor and the transformer are summarized in Table II.

V. LOSS ANALYSIS OF THE FULL-BRIDGE LLC CONVERTER

A. Conduction Losses

The apparent power S from the dc link could be found from the following:

$$S = V_{\text{dc}} I_{\text{in, rms}}. \quad (37)$$

The real power P delivered to the battery pack is

$$P = V_{\text{bat}} I_{\text{bat}}. \quad (38)$$

The reactive power Q_r , which corresponds to the circulating power in the resonant tank, can be calculated as

$$Q_r = \sqrt{S^2 - P^2} = \sqrt{(V_{\text{dc}} I_{\text{in, rms}})^2 - (V_{\text{bat}} I_{\text{bat}})^2}. \quad (39)$$

According to (39) and the data extracted from Fig. 13, the reactive power corresponding to any specific point of the charging process can be calculated. The reactive power is the figure of merit to evaluate the conduction losses in the circuit since conduction losses are proportional to the reactive power as it circulates in the circuit.

For this specific design, the reactive power levels at the beginning point, the nominal point, the turning point, and the end point are 726, 693, 602, and 570 VA, respectively. The reactive power provides an intuitive insight to the level of conduction losses. Accurate conduction losses could be approximated based on RMS current, ESRs of circuit components, and the diode forward voltage drop.

B. Switching Losses

Since the converter operates in the inductive region, both the turning on of MOSFETs and turning off of freewheeling diodes are ZVS and lossless. In addition, losses associated with the turn-on process of power diodes are negligible. Moreover, diodes for rectification in the secondary side are turned on and off at zero current, and hence do not impose any additional switching losses. Consequently, turning-off losses of MOSFETs dominate the switching losses of LLC converter. The associated switching losses of each single MOSFET can be approximated based on

$$P_{\text{switch}} = \frac{(I_{\text{off}} t_{\text{fall}})^2}{6C_{\text{HB}}} \quad (40)$$

where I_{off} is the turning-off current, t_{fall} is the fall time, and C_{HB} is the equivalent capacitance in the half-bridge.

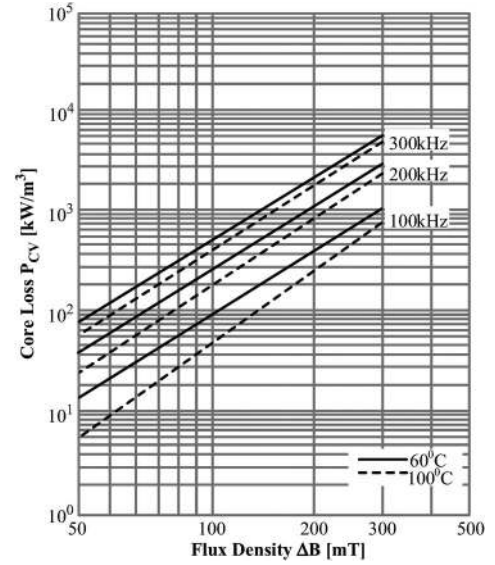


Fig. 14. Typical core-loss chart for PC47 ferrite [25].



Fig. 15. One-kilowatt interleaved boost PFC converter prototype.

C. Core Losses

Core-loss volume density P_{CV} is the function of both the switching frequency and the peak ac flux density (ΔB). The curves of P_{CV} for PC47 ferrite are plotted in Fig. 14. Using (24), ΔB can be calculated. Likewise, the switching frequencies at different operation points can be obtained from the dc characteristics of the LLC converter. Consequently, core losses can be calculated as

$$P_{\text{core}} = P_{\text{CV}}(f, \Delta B) \times V_e \quad (41)$$

where V_e is the effective core volume.

VI. EXPERIMENT RESULTS

A 1-kW prototype was built as a proof-of-concept to verify theoretical analyses (see Figs. 15 and 16). Key parameters and power devices of the prototype are listed in Table III. Photos of the interleaved boost converter and the full-bridge LLC converter are provided in Figs. 16 and 17, respectively. In Fig. 17, the two magnetic components are the resonant inductor and the transformer, respectively.

The waveforms achieved in the first-stage interleaved boost converter are presented in Figs. 17 and 18. As shown in Fig. 17, the input current is in phase with the input voltage. The converter demonstrates a power factor higher than 0.99. The

TABLE III
DESIGN OF AN INTERLEAVED FULL-BRIDGE LLC ONBOARD CHARGER

Symbol	Quantity or Device	Parameter
C_{DC}	DC link capacitor	$3 \times 330 \mu\text{F}$
V_{in}	Input voltage	110 V/60 Hz
V_{DC}	DC link voltage	300 Vdc
f_{pfc}	Switching frequency for PFC stage	100 kHz
IC1	PFC controller	UCC28070
V_b	Battery voltage range	320 V to 420 V
P_{max}	Rated maximum power	1 kW
f_p	Primary resonant frequency	200 kHz
f_s	Secondary resonant frequency	105.1 kHz
N	Transformer turn ratio	5:6
L_m	Magnetizing inductor	160 μH
L_r	Resonant inductor	62.51 μH
C_r	Resonant capacitor	10 nF
C_f	Output filter capacitor	$3 \times 3.3 \mu\text{F}$
IC2	Resonant controller	UCC25600
$D_1 \sim D_4$	Diode Rectifier	NTE5322
$S_1 \sim S_2$	Boost MOSFETs	FCA16N60N
$D_5 \sim D_6$	Boost Diodes	IDB06S60C
$S_3 \sim S_6$	LLC MOSFETs	STB23NM60ND
$D_7 \sim D_{10}$	Secondary Diode Rectifier	DSEP29-06A

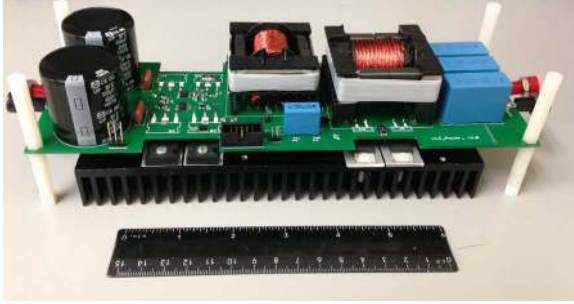


Fig. 16. One-kilowatt full-bridge LLC converter prototype.

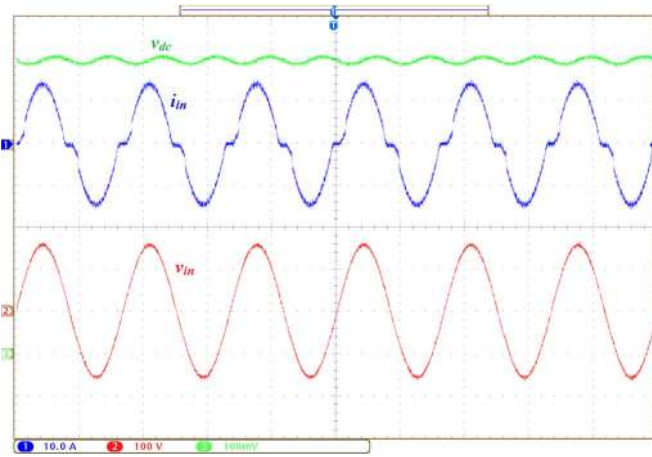


Fig. 17. Interleaved boost PFC converter operating at 1 kW. From top to bottom: v_{dc} (50 V/div), i_{in} (10 A/div), v_{in} (100 V/div), and time (10 ms/div).

dc-link voltage is regulated at 300 V with a ripple voltage of 14.5 V. According to Fig. 18, in comparison with the current ripples in i_{L_1} and i_{L_2} , the current ripple in i_{in} is significantly reduced. This well demonstrated the optimal ripple cancellation effect with a dc-link voltage of 300 V. The current spikes

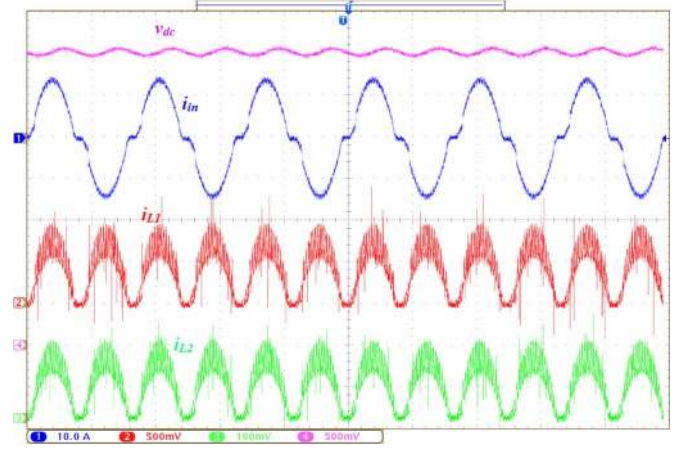


Fig. 18. Interleaved boost PFC converter operating at 1 kW. From top to bottom: v_{dc} (50 V/div), i_{in} (10 A/div), i_{L_1} (5 A/div), i_{L_2} (5 A/div), and time (10 ms/div).

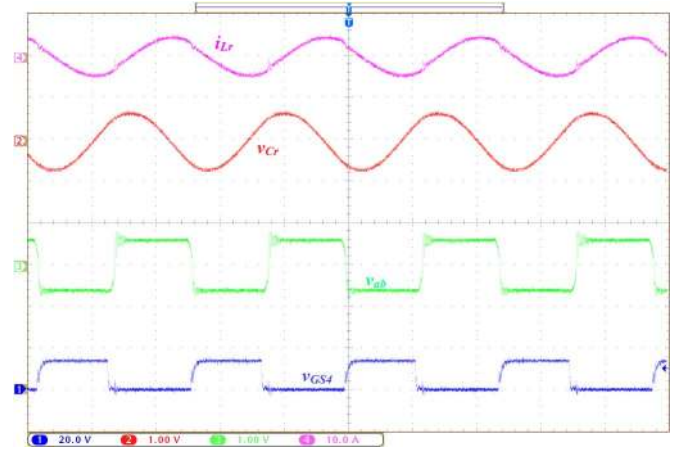


Fig. 19. LLC converter operating at the beginning point ($V_{bat} = 320$ V, and $I_{bat} = 2.38$ A). From top to bottom: i_{L_r} (10 A/div), v_{C_r} (500 V/div), v_{ab} (500 V/div), v_{GS4} (20 V/div), and time (2 μs /div).

are caused by the inaccuracy of the current probe Tektronix A622. At 1-kW operation, THD and conversion efficiency are measured as 3.61% and 96.3%, respectively.

The experiment results of the second-stage LLC converter are presented in Figs. 18–22. The waveforms of resonant inductor current i_{L_r} , resonant capacitor voltage v_{C_r} , output voltage of full-bridge inverter v_{ab} , and gate drive signal of S_4 v_{GS4} , are recorded. High-voltage differential probes, with attenuation rate of 1/500, are used to track and capture the waveforms of v_{C_r} and v_{ab} . As shown in the figures, the full-bridge LLC converter always operates in the inductive region, where i_{L_r} lags v_{ab} . The turning-on process of MOSFETs and the turning-off process of freewheeling diodes are both lossless.

Fig. 19 demonstrates the operation at the beginning point, where the switching frequency is regulated at 208.3 kHz. Fig. 20 shows the operation waveforms at the nominal point. At this point, switching frequency is regulated at 192.5 kHz. Likewise, Fig. 21 shows the operation at the turning point. The peak power of 1 kW is achieved at this point, where the switching frequency is regulated at 172.3 kHz. The operation waveforms representing the end point are plotted in Fig. 22. The corresponding switching frequency is 185.1 kHz.

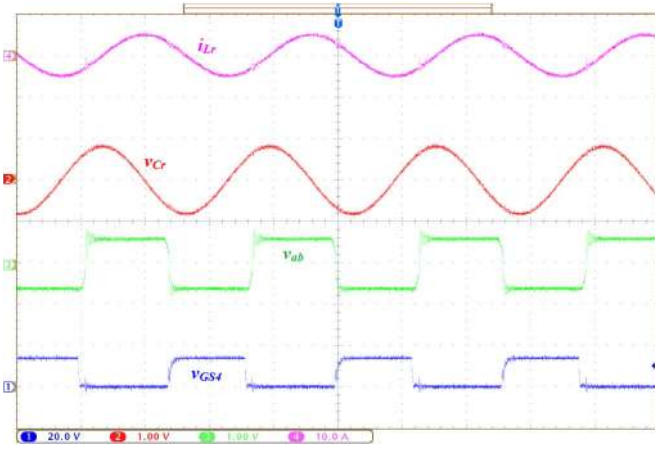


Fig. 20. LLC converter operating at nominal point ($V_{\text{bat}} = 360$ V, and $I_{\text{bat}} = 2.38$ A). From top to bottom: i_{L_r} (10 A/div), v_{C_r} (500 V/div), v_{ab} (500 V/div), v_{GS4} (20 V/div), and time (2 μs /div).

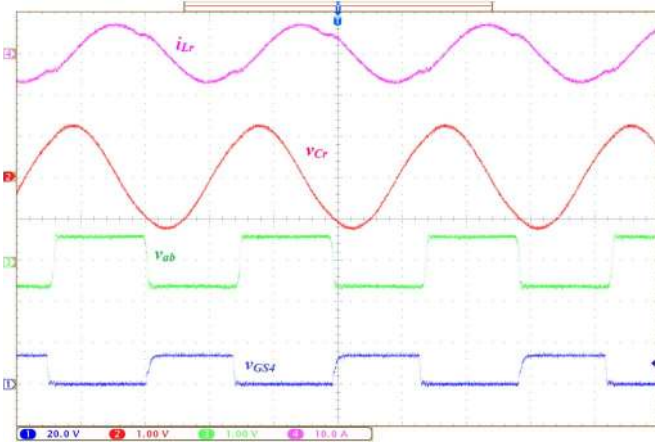


Fig. 21. LLC converter operating at turning point ($V_{\text{bat}} = 420$ V, and $I_{\text{bat}} = 2.38$ A). From top to bottom: i_{L_r} (10 A/div), v_{C_r} (500 V/div), v_{ab} (500 V/div), v_{GS4} (20 V/div), and time (2 μs /div).

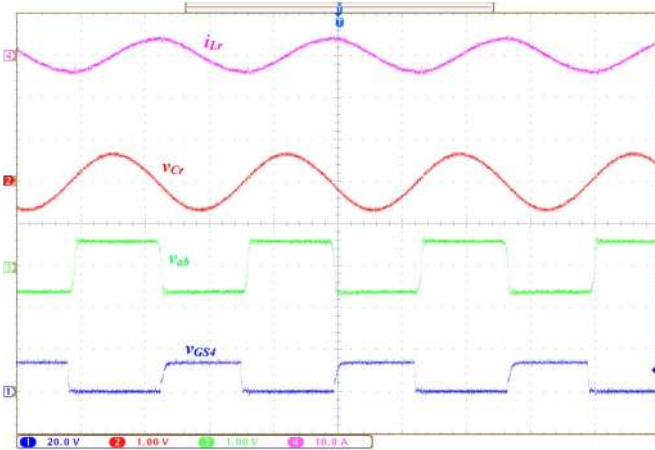


Fig. 22. LLC converter operating at end point ($V_{\text{bat}} = 420$ V, and $I_{\text{bat}} = 0.24$ A). From top to bottom: i_{L_r} (10 A/div), v_{C_r} (500 V/div), v_{ab} (500 V/div), v_{GS4} (20 V/div), time (2 μs /div).

A multiresonance phenomenon is clearly shown in Fig. 21. At the moment that S_2 and S_4 are turned off, i_{L_r} starts to commutate from S_2 and S_4 to D_{S1} and D_{S3} . This forces v_{ab}

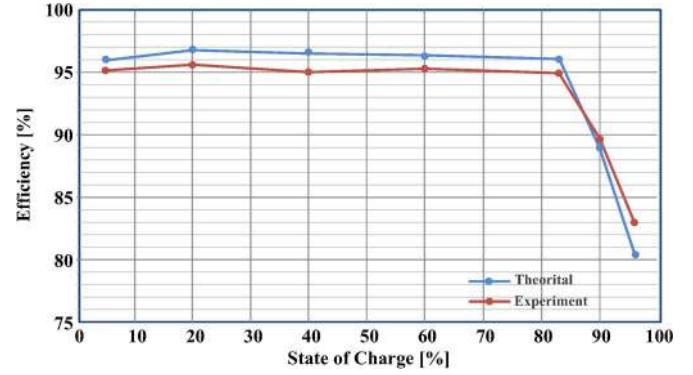


Fig. 23. Efficiency of the designed LLC converter versus SOC of the battery pack.

to abruptly change from -300 to 300 V. From then on, L_r resonates with C_r . Since secondary diodes D_7 and D_{10} are on, V_{bat} is applied to the secondary side of the transformer. This makes the current in the magnetizing inductor i_{L_m} to increase linearly. When i_{L_m} reaches i_{L_r} , L_m begins to participate in the resonance with L_r and C_r .

The efficiency of the LLC stage versus SOC of the battery pack is shown in Fig. 23. As shown in Fig. 23, the LLC stage maintains good efficiency performance from the beginning point to the turning point, where the output voltage varies from 320 to 420 V. There is an obvious efficiency drop from the turning point to the end point. This is because, in CV charging mode, I_{bat} decreases fast. Hence, the charging power quickly decreases with the increase in the SOC. However, the circulating power in the resonant tank remains high, which incurs high conduction loss. On the other hand, ΔB of magnetic core does not tend to decrease significantly, which poses relatively high core losses.

VII. CONCLUSION

In this paper, an onboard PEV battery charger has been proposed, analyzed, designed, and developed. Interleaved boost topology is used in the first stage for PFC and THD reduction, as well as reduction of the volume of the magnetic components. In the second stage, a full-bridge LLC resonant converter is employed to achieve high conversion efficiency over the full voltage range of the battery pack.

The suitability and advantages of the proposed converter are discussed, and design guidelines are provided through theoretical analyses for both stages. As a case study, design considerations for a 1-kW charger prototype, which converts 110-V 60-Hz ac to the battery voltage range of 320–420 V, are provided, considering the characteristics of the converter.

Finally, the experiment results are presented for validation. The first-stage interleaved boost converter demonstrates unity power factor operation at the rated power and achieves THD less than 4%. In the second-stage LLC converter, the switching losses, conduction losses, and core losses are optimized to achieve good overall efficiency performance over a wide output voltage range. The future research will be focused on expanding the power of the charger to a higher level.

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