

Design and Analysis of a High-Efficiency High-Voltage Class-D Power Output Stage

Haifeng Ma, Ronan van der Zee and Bram Nauta

IC Design group, CTIT Institute, University of Twente, Enschede, The Netherlands

Abstract — The analysis and design of a highly-efficient 80V class-D power stage design in a 0.14 μ m SOI-based BCD process is described. It features immunity to the on-chip supply bounce, realized by internally regulated floating supplies, variable driving strength for the gate driver, and an efficient 2-step level shifter design. Fast switching transition and low switching loss are achieved with 94% peak efficiency for the complete class-D power stage in the realized chip.

Keywords — Class-D amplifier, output stage, supply bouncing, CMOS, BCDMOS, high-voltage, gate driver, high efficiency, level shifter, on-chip regulator, hard switching, soft switching.

I. INTRODUCTION

Piezoelectric actuators are increasingly adopted in a wide range of applications like smart materials for vibration and noise control, precision actuators, etc.[1]. In these applications, the signal frequency is in the range of several tens to hundreds of Hz and the piezoelectric actuator can electrically be treated as a capacitive load. The higher efficiency offered by class-D power amplifiers compared to class-AB makes them ideal for driving such loads, where typically several tens of Watt reactive power are being processed and the compactness requirement mandates the usage of small or even no heat sinks.

Class-D amplifiers for these applications bear similarities to the integrated high-voltage high-power class-D output stages for audio discussed in [2]-[9]. One significant design problem of such switching power stages is the on-chip supply bouncing [2],[9]. The output current switching between the high-side and low-side power switches (Fig. 1) causes a large di/dt , leading to on-chip supply bounce caused by parasitic inductances. For high-voltage DMOS output devices, the maximum allowed gate-source voltage (V_{gs}) is the same as for normal MOS devices in the same process node and is much lower than their maximum drain-source voltage (V_{ds}). The integration of complex signal processing functions and features on the same chip as the power blocks necessitates the power stage design in deep-submicron process nodes. However, the supply bouncing magnitude of several volts, while not yet a problem in [2]-[9], makes the design in these smaller process nodes prone to performance degradation or even malfunction.

In [6], parallel-connected power switches with weighted size are configured to perform staged turn-on/off for preventing inductive flyback to the supply rails. This way supply bounce can be reduced, with some tradeoff on efficiency because the turn-on of the HS and LS power switches have to be overlapped. Active clamp circuits [11] can also be used as an effective way to reduce the voltage stress across the power switches and prevent damage to circuits. Yet the clamping can only mitigate power supply overshoot, while undershoot associated with the supply bounce is not clamped. In this paper we describe a gate driver topology that overcomes the supply bouncing issue and enables a high-voltage, high-power class-D power stage design in a deep-submicron process node [12]. This is achieved by using gate drivers with on-chip regulated floating supplies, with the low-voltage driver and control circuits fully shielded from all the supply bounce. Moreover, simultaneous supply bounce minimization and efficient switching transitions are realized by adopting an in-cycle variable gate-driving strength.

Adding to [12], the gate driver sizing for limiting on-chip supply bounce and the associated power efficiency, reliability and chip area issues are discussed in detail, both for the cases with and without the presented gate driver topology. In section II we show a detailed analysis of the gate driver sizing considering the on-chip supply bounce and its associated power efficiency degradation issues. The proposed floating gate driver and in-cycle variable gate-driving strength techniques for realizing efficient switching transitions are described in section III. In Section IV the requirement overview and circuit topology of the level shifter circuit for the class-D power stage are analyzed. Section V discusses the measurement results and in section VI the conclusions are drawn.

II. GATE DRIVER SIZING ISSUES

A typical class-D power stage for high-voltage high-power applications consists of two identical NDMOS devices as High Side (HS) and Low Side (LS) switches as shown in Fig. 1 [2]-[7]. Since for DMOS power transistors the maximum V_{gs} is typically much lower than the maximum V_{ds} , the LS gate driver is supplied by a separate low-voltage supply and externally decoupled. For the HS gate driver, an external bootstrapping capacitor can be used as the supply. Here we use the three-line earth symbol for the power ground V_{SSP} , which is the off-chip reference ground. Later in the paper the single-line ground symbol will be adopted to represent the on-chip grounds as to distinguish them from the off-chip reference ground. The circuit parameters of this power stage used for the simulations in this paper are summarized in TABLE I. The switching frequency f_{sw} is chosen at 500kHz as a typical value of class-D f_{sw} in general [2]-[9]. For

piezoelectric-actuator applications, a lower f_{sw} can also be used if the signal bandwidth is lower. The output DC current I_{out} is the average inductor current I_L within one switching cycle. It is set at 1A with the output V_{pwm} duty cycle being 0.5. This represents the scenario of the instant when the output stage is discharging the capacitive piezoelectric load from mid-supply. Nevertheless, the analysis itself is general and also holds for other output current and duty cycle combinations, as well as when the output stage is processing a dynamic output signal.

A. Power Transistor Dissipation

The dominating power dissipation in the power MOSFETs of a high-voltage Class-D output stage consists of three types of losses [10]: 1) P_{cond} : conduction loss caused by the power MOSFETs' r_{on} . 2) P_{cap} : capacitive loss caused by charging and discharging parasitic capacitances on V_{pwm} , and 3) P_{sw} : switching losses caused by V-I overlap in the switches during switching transitions. Among the three dissipation sources, P_{cond} is inversely proportional to the power transistor size S while P_{cap} is proportional to the power transistor size S . As for P_{sw} , in the optimal case (very fast switching) its dominant contribution is the intrinsic reverse-recovery current [4] and this is also proportional to the power transistor size S . The total dissipation can then be optimized by choosing the correct transistor size to balance the three power dissipation sources [10]. Under the circuit operating conditions in TABLE I, an optimized DMOS power transistor size is derived as $56000\mu m/0.75\mu m$, with TABLE II listing each dissipation source and their respective contributing ratio. This optimization is considered in the ideal case, i.e. with no power supply parasitic inductances included.

Because our first attempt here is to examine what the dissipation sources should be and how they contribute to the total dissipation in the optimal case, the driver stage (Fig. 2) for driving the two power switches should also be designed to behave as close to ideal drivers as possible in this optimization. This has two implications 1) the drivers should turn on the power switches very fast such that the main contribution to V-I overlap is caused by the reverse-recovery current. Since we do not consider power supply parasitic inductances in this phase, the driver pull-up transistor can be increased as much as necessary to reach this minimum P_{sw} . The minimized P_{sw} is then proportional to the reverse-recovery charge in the body diode and thus proportional to the power transistor size S . 2) The driver should turn off the power switches very fast and then be able to completely keep the power switches off when required. Similarly since power supply parasitic inductances are not considered yet, the driver pull-down transistor is sized to be much larger than the pull-up transistor as to avoid cross conduction [7].

However, although switching can be arbitrarily fast in this optimization procedure, in reality it will cause large di/dt , and consequently supply bounce which affects the circuit operation. In the following subsection we will show how the gate drivers influence the supply bounce (di/dt) for different switching scenarios and how efficiency deteriorates if supply bounce has to be limited by proper gate driver sizing.

B. Supply Bounce Analysis and Gate Driver Sizing

The switching behavior of a class-D output stage can be categorized into two types of switching transitions: soft switching, where I_L (dis)charges the parasitic output capacitance of the switch transistors and hard switching, where the transistors (dis)charge these parasitics [11]. Depending on the relative amplitude of the inductor ripple current and the load current, I_L can either be bidirectional with both switching transitions being soft switching or unidirectional, where one transition is soft switching and the other is hard switching. The power stage circuit diagram in Fig. 2 is used to illustrate the two switching transitions. The load current I_L is flowing into the power stage and keeps flowing in this direction during the full switching cycle. Fig. 3(a) shows the simulation waveforms in one complete switching cycle, consisting of soft and hard switching transitions while Fig. 3(b) and Fig. 3(c) shows the two edges in detail.

In Fig. 3(b) for the soft switching transition edge, the V_{pwm} low-to-high transition starts when M_{LS} is turning off, and I_L provides the current to charge V_{pwm} to V_{DDP} without resorting to the active devices. From the driver sizing point of view, when we look at the current flowing in M_{LS} (I_{MLS}), first, I_{MLS} is decreased such that I_L can provide for the current necessary to charge the M_{LS} parasitic capacitances and to discharge the M_{HS} parasitic capacitances. Then there comes a period where V_{pwm} is slewing and I_{MLS} keeps nearly constant. When the slewing is over, I_{MLS} is further decreased to be conducted by the HS body diode within the dead time. During both times when I_{MLS} is decreasing, the di/dt is proportional to how fast M_{LS} is being turned off, and thus is proportional to the gate driver pull-down (PD) transistor $M_{n,LS}$ size S_n .

For the hard switching transition as shown in Fig. 3(c), first M_{HS} is turned off, and the current flows through the M_{HS} back-gate diode. V_{pwm} remains high until M_{LS} has been turned on and has taken over all the load current as well as the current for discharging the V_{pwm} node. The rate at which I_{MLS} is increasing during this time is proportional to the driver pull-up (PU) transistor $M_{p,LS}$ size S_p . After that, V_{pwm} starts slewing with a rate determined by $C_{dg,LS}$ and the on resistance of $M_{p,LS}$ (with size S_p). This slewing will also cause the M_{HS} gate-source voltage to rise through $C_{dg,HS}$ and the on resistance of $M_{n,HS}$ (with size S_n), so the driver PD transistor $M_{n,HS}$ should be sized with a much lower on resistance than PU transistor $M_{p,LS}$ to avoid cross conduction.

Because the HS and LS drivers and power switches are identical, the driver size versus di/dt analysis made above also holds for the case that the V_{pwm} high-to-low transition is soft switching while the V_{pwm} low-to-high is hard switching. The difference is that, since the HS gate driver supply is referred to V_{pwm} , the di/dt of the current flowing in M_{HS} and the subsequent supply bounce on V_{DDP} will not influence the HS gate driver supply. This will only be the case for class-D output stage topologies employing complementary output power transistors [8].

In conclusion, regarding the relationship between the gate driver sizing and the switching dynamics, 1) S_n is limited by the permissible di/dt in soft switching 2) S_p is limited by the permissible di/dt in hard switching, and 3) $S_p/S_n \ll 1$ to prevent cross conduction during hard switching. From 1)-3) we further conclude that S_n in soft switching is the major concern when it comes to supply bounce.

For relating the analyzed di/dt to the on-chip supply bounce, the class-D power stage with parasitic inductances of power supply and decoupling capacitor included is shown in Fig. 4. The parasitic inductances consist of bond wires, lead fingers, and PCB traces between the on-chip power supply pads and the decoupling capacitors of the external power supplies, which can easily add up to tens of nano-Henrys [2]. With a modeled parasitic inductance L_{par} of 10nH, Fig. 5 illustrates the influence of the bounce on the power stage switching transitions with 3.3V gate driver supply. Even though in this simulation 500pF on-chip V_{DD} decoupling was added between $V_{DD,int}$ and $V_{SSP,int}$, and furthermore extremely slow switching was adapted to ensure that oscillatory switching transitions [12] are overcome, 60% variation on the gate driver supply is evident with the modeled L_{par} of 10nH. The main concerns here include the robustness considerations for the low-voltage circuit blocks as well as the suboptimal switching loss P_{sw} performance. To gain insight into how efficiency gets deteriorated, the gate driver sizing procedure with constrained on-chip supply bounce is derived as follows,

- (1) Determine the driver pull-down transistor size S_n , based on the tolerable maximum gate driver supply bounce limited by soft switching transition.

Fig. 6 shows the simulation result of different driver pull-down transistor size and the corresponding on-chip supply bouncing, for different on-chip V_{DD} decoupling capacitor values. We see that the on-chip V_{DD} bounce increases with the driver pull-down transistor size. Also, adding more on-chip decoupling capacitor will help to decrease the bounce, but with limits. As also shown in Fig. 6, for a $S_n/S_o = 40$ to limit the bounce, adding on-chip decoupling capacitor from 200pF to 500pF will not

decrease the on-chip bounce anymore, primarily because the $L_{\text{par}} \cdot C_{\text{decap-on-chip}}$ bandwidth limits the effectiveness of bounce suppression. Determine the driver pull-up transistor size S_p , limited with respect to the pull-down transistor S_n for avoiding cross conduction of the two output power DMOS switches.

- (2) Determine the driver pull-up transistor size S_p , limited with respect to the pull-down transistor S_n for avoiding cross conduction of the two output power DMOS switches.

Considering the already limited S_n for suppressing the on-chip supply bounce, S_p is further limited by the requirement to avoid cross conduction. This means that hard switching transitions have to be either extremely slow or cause cross conduction, with both cases causing suboptimal switching loss. Fig. 7(a) shows the S_p sizing when S_n/S_o has been chosen at 40. The efficiency degradation caused by this limitation is evident in Fig. 7(b).

An increase of S_p/S_o from 8 to 20 results in faster switching, which lowers P_{sw} . However, a larger S_p also results in cross conduction, adding to P_{sw} , so P_{sw} is not reduced to the optimal value compared to the other losses $P_{\text{cond}} + P_{\text{cap}}$ (optimum ratio should be 0.72 as in TABLE II).

Since the main factor that determines the power supply bouncing during switching transitions is the driver-size-related di/dt , the analysis made above is not limited by the power transistor size chosen in TABLE II. If a different power transistor size is chosen, the driver size will have to be scaled accordingly to meet the same requirement on di/dt as well as on avoiding cross conduction. Consequently the design trade-offs for limiting the di/dt in soft switching and aiming for fast transitions in hard switching are the same. Regarding the effect of process and temperature variation on the on-chip supply bounce magnitude, the analysis of the relationship between the driver transistor size and the bounce magnitude also holds. A decrease in temperature or a fast process corner has the same effect as an increase in transistor size, which will cause more bounce. Additionally, in designs where a larger L_{par} than the modelled 10nH exists through longer decoupling loops, e.g. larger packages than required or decoupling capacitors placed far away from the supply pins, the supply bounce magnitude will also increase.

III. FLOATING GATE DRIVER TOPOLOGY

A. Supply-Regulated Floating Gate Driver

To overcome the on-chip driver supply bouncing issue without sacrificing efficiency during switching transitions, we propose a gate driver topology with on-chip regulated floating supply. As shown in Fig. 8(a), two on-chip voltage regulators are used to provide stable on-chip supply voltages to the gate driver circuits. The two regulators track the two reference nodes $V_{SSP,int}$ and V_{pwm} respectively, so the on-chip bouncing will not be seen by the driver circuits. The unregulated input supply voltage for the regulators are chosen based on the estimated maximum bouncing magnitude plus the minimum operation voltage of the regulator circuits (12V unregulated V_{DD} is used here). The detailed gate driver circuit is shown in Fig. 8(b). The pull-up current has been divided into two parts. The main I_{pu} is supplied by the unregulated V_{DD} while an auxiliary I_{pu} is used to turn the output power transistor fully on. By this configuration the regulators are not required to supply the hundreds of milliamps for I_{pu} and their design can be simplified. For the pull-down current path, an in-cycle variable gate driving strength is implemented and will be explained next.

B. In-Cycle Variable Gate-Driving Strength

As explained in the previous section, the main reason for excessive switching loss during hard switching is because the driver PU transistor has to be much weaker than the PD transistor, other than limited by on-chip bounce considerations. To circumvent this limitation of the driver PU strength, we propose to use an in-cycle variable gate-driving strength. As shown in Fig. 9(a), when the driver input and output status have both been detected as already off, the combined strength of M_{n1} and M_{n2} will be used to keep the power transistor off when the other driver is turning on based on the S_p/S_n driver ratio requirement. However, when the driver is in the process of turning its output off and hasn't yet reached the level determined by the Schmitt trigger, only the weaker M_{n1} will provide the pull-down current to turn off the output power transistor slowly in order to keep di/dt low (Fig. 9(b)). This way we have the design freedom to both choose the correct S_p/S_n ratio to avoid cross conduction, and limit the on-chip supply bounce. Simulation waveforms for comparing the effectiveness with and without the adaptive driver turn-off strength are shown in Fig. 10, with the modeled L_{par} of 10nH in the simulation. Fig. 10(a) shows that the same effect for keeping the power transistor off is obtained while Fig. 10(b) illustrates that the supply bouncing is significantly reduced when a weaker PD strength can be applied for turning the power transistor off. Fig. 10(a) and Fig. 10(b) are enlarged simulation waveforms within one switching period.

C. Sizing of the Floating Gate Drivers

Compared with the sizing of the gate driver with externally decoupled low-voltage gate driver supply, the sizing of the floating gate driver combined with the variable gate-driving strength can now have the following advantages:

- (1) The gate driver PD transistor can be sized larger, since the floating gate drivers can sustain a much higher on-chip supply bouncing amplitude and the floating regulated driver supplies will not be directly influenced.

As can be seen in Fig. 11, although the off-chip decoupled 12V supply still has large variations during switching, the on-chip floating supply varies only 10% with the adopted floating regulator circuit discussed in subsection D. This variation is mainly due to the load regulation of the regulator for providing the PU current. Also, this clean gate driver supply is achieved without using area-consuming on-chip decoupling capacitors in the hundred pF range.

- (2) The PU transistor can be sized larger to improve efficiency without getting limited by the maximum S_p/S_n ratio. Cross condition is avoided by the additional keep-off strength.

In Fig. 12(a) we see the effect of added keep-off strength to the PU transistor sizing. With the same $S_n/S_o=40$ as used in Section II for limited bounce, 4x added keep-off strength can ensure that ΔV_{gs} is far below V_{th} when choosing S_p/S_o up to 20. Fig. 12(b) shows that efficient hard switching transitions can be realized since now larger PU transistor size can be adopted. With S_p/S_o set to 20, the $P_{sw}/(P_{con}+P_{cap})$ ratio is now 0.73, close to the minimized $P_{sw}/(P_{con}+P_{cap})$ ratio of 0.72 in TABLE II.

D. On-chip Floating Voltage Regulator

The on-chip floating regulator circuit for both HS and LS is shown in Fig. 13. For fast response and low output voltage ripple, the output $V_{DDF}/V_{DDF,boot}$ has been excluded from the feedback loop [13]. The drawback on precision is not critical here since the regulator supplies mainly digital blocks. The output devices of the regulator are also DMOS devices to sustain the higher 12V unregulated V_{DD} as well as the bouncing superimposed on it.

On-chip decoupling capacitor C_G is important for power supply ripple rejection. It is vital to minimize its parasitic capacitance $C_{par,sub}$ to the substrate as any disturbance from the $V_{SSP, int}/V_{pwm}$ node will be coupled to V_B by a ratio $C_{par,sub}/(C_G+C_{par,sub})$. As an example, the output voltage V_{PWM} slews 80V in a few nanoseconds;

even with 1% parasitic capacitance 0.8V will be coupled to the 3.3V output, which is an unacceptable 25% variation. Consequently it is rather important that these decoupling capacitors are fully shielded from the substrate as shown in Fig. 13. Here for the metal fringe capacitor the whole first metal plate is connected to the $V_{SSP,int}/V_{pwm}$ node such that V_B is fully shielded. The output decoupling capacitor C_{out} has a value of 20pF, which is much more area efficient than the decoupling capacitor of an unregulated gate-driver supply (Fig. 6).

Efficient switching transitions as shown in Fig. 14 are achieved by this gate driver topology. The on-chip floating regulators provide a reliable 3.3V supply to the gate driver circuit during both soft- and hard-switching transients. Also, thanks to the in-cycle variable gate-driving strength, the high-to-low hard switching here is performed fast, simultaneously avoiding cross conduction and excessive bounce on the off-chip decoupled 12V supply (Fig. 10).

IV. POWER-EFFICIENT 2-STEP LEVEL SHIFTER

Another important circuit block for the class-D power stage is the level shifter circuit [14]-[17]. It is used for communication between signals referred to the digital ground V_{SSD} and those referred to the power ground $V_{SSP,int}$ or the floating HS V_{pwm} , as shown in Fig. 15. With a 3.3V supply for both the low-voltage control blocks and the gate drivers, the on-chip supply bouncing magnitude higher than the 3.3V supply itself presents a challenge for reliable level shifting. As shown in Fig. 15, the $>3.3V$ bounce causes the voltage potential between V_{DDF} and V_{SSD} to be very uncertain. This makes conventional level shifting by building a direct interface circuit using V_{DDF} and V_{SSD} as power and ground [2], [14], [15] not feasible. For reliable level shifting, a two-step approach has been adopted here, where the voltage level is first referred to the higher 12V $V_{DD,int}$ and then to $V_{SSP,int}$.

In addition, compared to level shifters used for transferring to voltage levels referred to fixed supply rails [8], [16], [17], level shifting to the slewing V_{pwm} is associated with disturbance that could corrupt the transferred signal. We consider the SR latch referred to the V_{pwm} voltage domain as shown in Fig. 16. The supply rail referred to V_{pwm} has the same high slew rate as V_{pwm} (up to 10kV/ μ s in this design). If there exist parasitic capacitances e.g. to the substrate at the input of the latch, and the stage preceding the latch has a resistive load, this directly translates to a common-mode disturbance for the latch and a possible logic output error can occur.

To cope with the $>3.3V$ supply bounce, the two-step level shifting approach is shown in the circuit schematic in Fig. 17, where the voltage level is first referred to the higher 12V $V_{DD,int}$ and then to $V_{SSP,int}$. As

shown in Fig. 17, the already available 12V $V_{DD,int}$ referred to V_{SSD} is not influenced too much by the bounce and thus establishing a reliable interface circuit across $V_{DD,int}$ and V_{SSD} as the 1st level shifting step. Subsequently the 2nd level shifting transfers the signal to the one referred to $V_{SSP,int}$, tolerating the supply voltage variation between $V_{DD,int}$ and $V_{SSP,int}$.

For the HS level shifter circuit, the power dissipation could be significant because the current for transferring the signal has to flow between the maximum 92V $V_{boot,int}$ and ground. Two approaches have been implemented in the level shifter circuit of Fig. 17 to minimize its power dissipation and make it power efficient for HS usage. Firstly, pulsed set and reset input are applied such that only pulsed current are bridging most of the 92V [15]. Additionally, we introduce an active load (transistors M1-M4) with partial positive feedback characterized by a lower impedance for common-mode disturbances like $V_{DD,int}$ or V_{pwm} , and a higher impedance for the differential-mode signal pulses. The diode-connected M1 and M4 are configured with slightly larger W/L ratio compared with the cross-coupled M2 and M3. From a large-signal perspective, approximately 2x larger (M1+M2) and (M3+M4) are used for conducting the common-mode disturbance current $I_{cm,disturb}$ while only M1 or M4 are used for conducting the signal current $I_{dm,sig}$. This way, compared to using a simple active load [14], significantly lower current pulses can be applied in the first level shifting while maintaining its common-mode noise immunity. Concluding, with the introduction of a two-step level shifting, pulsed set/reset signaling as well as an active load with partial positive feedback, the level shifter circuit shown in Fig. 17 can deal with the design challenges for both HS and LS and thus identical circuits are used for both HS and LS level shifting.

V. MEASUREMENT RESULTS

The 80V power output stage has been fabricated in NXP A-BCD9, a 0.14 μ m SOI-based BCD process and the chip photograph is shown in Fig. 18. For the layout of the power stage, two bondpads are used for each of the V_{DDP} , V_{SSP} and V_{pwm} pins to ensure enough current handling capability. The top-metal layer connected to these power supply bondpads is triangular (as is evident in the chip photograph in Fig. 18) to realize a uniform current density, resulting in minimal metal resistance in the power transistors.

Packaged chips are used for all the measurements that follow, with external heat sinks attached to the package for thermal stability considerations. Off-chip decoupling capacitors are required for the decoupling of the following critical voltage domains: high-voltage power supply V_{DDP}/V_{SSP} , LS gate driver supply V_{DD}/V_{SSP} , HS gate driver bootstrapped supply V_{boot}/V_{pwm} . Minimum current loops [2] should be ensured in the PCB

design for these decoupling loops as to minimize L_{par} . Two power supplies are required: the 12V gate-driver supply as well as the 80V high-voltage power supply.

For measuring efficiency, first a current-source load instead of the capacitive piezoelectric load is used to make the power stage delivering active output power. When the output voltage is fixed, the output power is varied by sweeping the output current value of the current-source load, and the output power is dissipated in this load. For a fixed output voltage of 40V (duty cycle of 0.5) and a switching frequency of 230kHz as well as 530kHz, the efficiency measurement results are shown in Fig. 19. The measured peak efficiency for 230kHz switching frequency is 94%. For power efficiency measurements when driving capacitive piezoelectric load, a series-connected $23\mu F + 1.6\Omega$ is used to model the piezo-actuator [1] and this load is mostly capacitive at the input signal frequency f_{sig} of several tens to hundreds of Hz. Efficiency is defined here as

$$Eff = P_{out,app} / (P_{out,app} + P_d),$$

where $P_{out,app}$ is the apparent output power $V_{out,rms} * I_{out,rms}$ (VA) processed by the amplifier and P_d is the total amplifier dissipation. Even though there will be no real power delivered to the load for the purely capacitive load case, this expression for power efficiency (Eff) can still be used to characterize the power stage efficiency, since it is based on how much will be dissipated (P_d) when processing a certain amount of power ($P_{out,app}$). Fig. 20 shows the measurement results with a 500Hz signal applied on the load and maximum $P_{out,rms}$ of 45VA. The peak efficiency is 92% and 89% for switching frequency of 230kHz and 530kHz respectively. The current supplied by both the 12V and 80V supply are taken into account for all of these power efficiency measurements.

For measuring linearity, the power stage is operated within a hysteretic-based feedback loop [18]-[20]. For a 1st-order hysteretic-based loop [20] with the switching frequency set at 230kHz for $D=0.5$, Fig. 21 shows the THD+N performance when driving a series-connected $2.2\mu F + 3\Omega$ load. A THD+N of 0.03% is achieved for $f_{sig}=1kHz$, which is comparable to [20]. Compared with the case of $f_{sig}=1kHz$, THD+N level will increase for the $f_{sig}=2kHz$ case. This is mainly because the output power is higher due to the capacitive load, and the loop gain of the feedback loop for suppressing the harmonics of the 2kHz signal is lower than the loop gain in the 1kHz case.

Compared to other power stage designs, this design offers the best possibilities for integration with other mixed-signal functions and especially digital circuitry thanks to the smaller process node being used, $0.14\mu m$ versus $0.25\text{--}3\mu m$ in [2]-[9]. This is permitted by the supply bounce immunity features, enabling its operation

with a 3.3V V_{gs} other than 5-12V V_{gs} in [2]-[8] and 18V $V_{gs}=V_{ds}$ in [9]. The >90% peak efficiency compares favorably with [2]-[9]. This is also ensured by the supply-bouncing immunity, as well as by the in-cycle variable gate drive strength.

VI. CONCLUSIONS

Fast switching transitions are crucial for minimizing class-D switching losses. In this paper the gate driver sizing issues considering the on-chip supply bounce are discussed in detail. It is shown that for traditional gate driver circuits both the pull-up and pull-down strength have to be limited to avoid excessive supply bounce and this in turn limits the realization of power-efficient fast switching transitions. The introduction of regulated floating supplies, variable driving strength for the gate driver and a 2-step level shifter ensure fast switching transitions not disturbed by on-chip supply bounce. A high-voltage, high-power class-D power stage with 3.3V V_{gs} is realized and measures with over 94% peak efficiency.

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Figure Captions:

Fig. 1. Topology of a typical class-D power stage

Fig. 2. Circuit diagram with combined gate driver and output power switches for analyzing class-D power stage switching dynamics

Fig. 3. Simulation waveforms with both V_{pwm} soft switching and hard switching transitions. (a) One complete switching cycle (b) Soft switching transition (c) Hard switching transition

Fig. 4. Class-D power stage with power supply parasitic inductance included

Fig. 5. Simulation waveforms illustrating the influence of supply bouncing, V_{pwm} high-to-low transition has to be extremely slow and results in high switching loss.

Fig. 6. Simulation result of different driver pull-down transistor size and the corresponding on-chip supply bouncing, under different on-chip decoupling capacitor values, S_n value is normalized to a S_o of $3.2\mu m/0.32\mu m$.

Fig. 7. Driver pull-up transistor sizing with S_n/S_o chosen at 40. S_n and S_p values are normalized to an S_o of $3.2\mu m/0.32\mu m$. (a) S_p limited for avoiding cross conduction (b) Suboptimal switching loss performance

Fig. 8. Proposed power stage topology (a) supply bouncing influence on the functionality of the gate driver is eliminated by the on-chip regulated gate-driver supply (b) Detailed gate driver structure.

Fig. 9. Gate driver with adaptive turn-off strength (a) Stronger pull-down transistors for keeping the power transistor off (b) Weaker pull-down transistors for turning the power transistor off

Fig. 10. Simulation waveforms for the on-chip supply bouncing with and without the adaptive turn-off strength within one switching cycle (a) When one power transistor turns on, the other power transistor can be kept off (b) On-chip supply bouncing can be significantly reduced.

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Fig. 17. Level shifter circuit and illustration of the on-chip supply/ground waveforms which necessitates a 2-step approach for the level shifting

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TABLE II. List of each dissipation source with an optimized power transistor size S of 56000 μ m/0.75 μ m

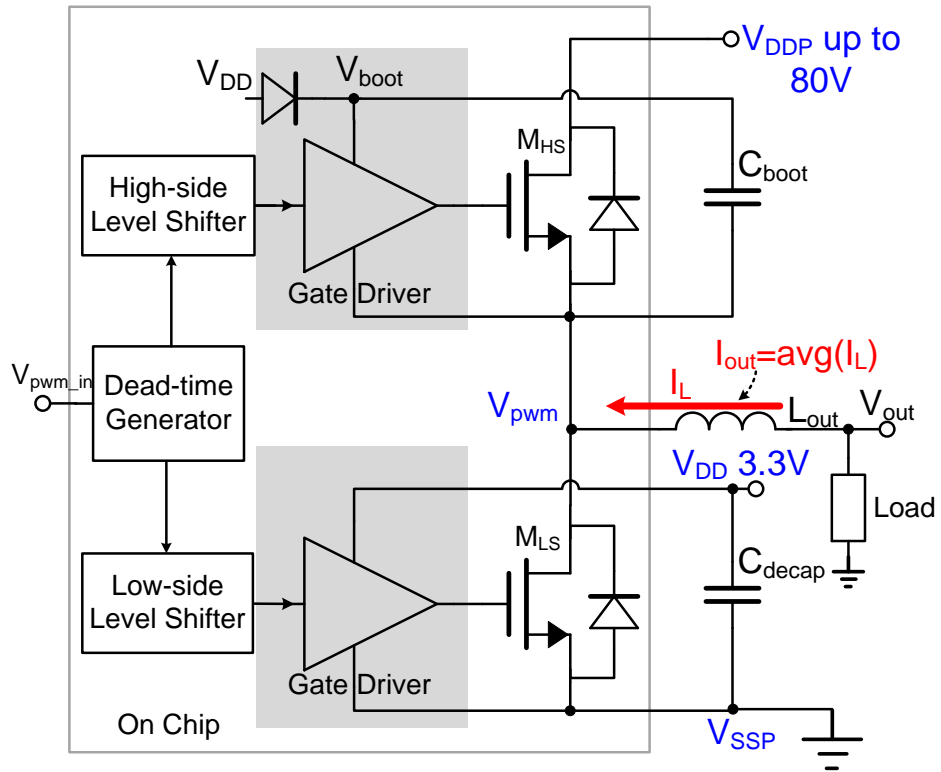


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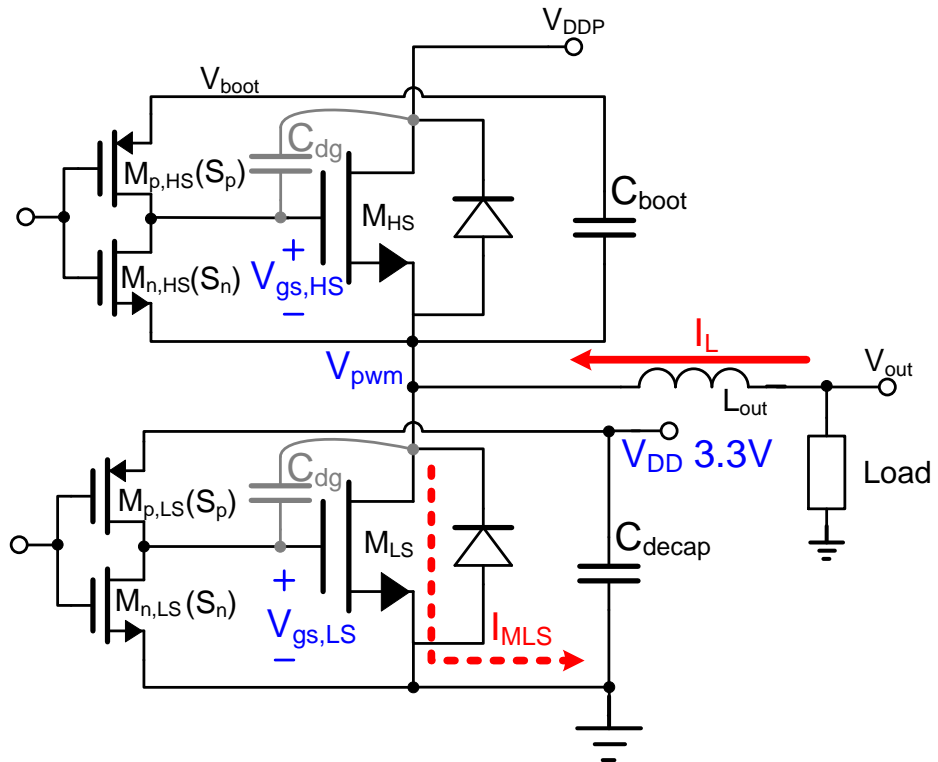


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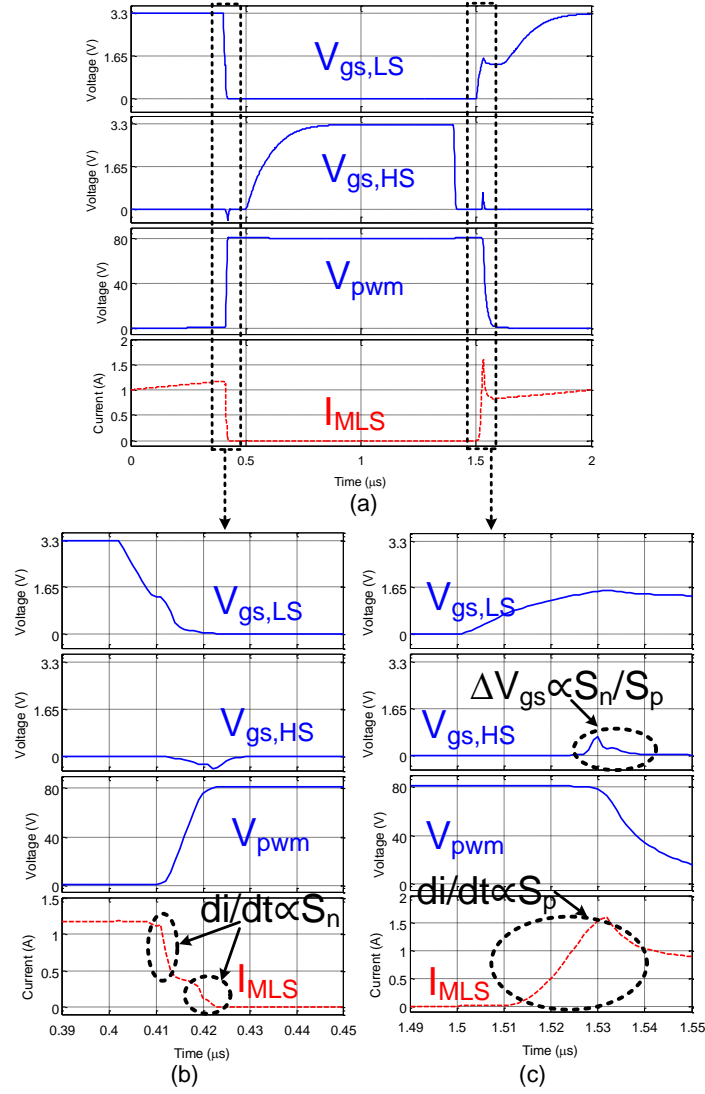


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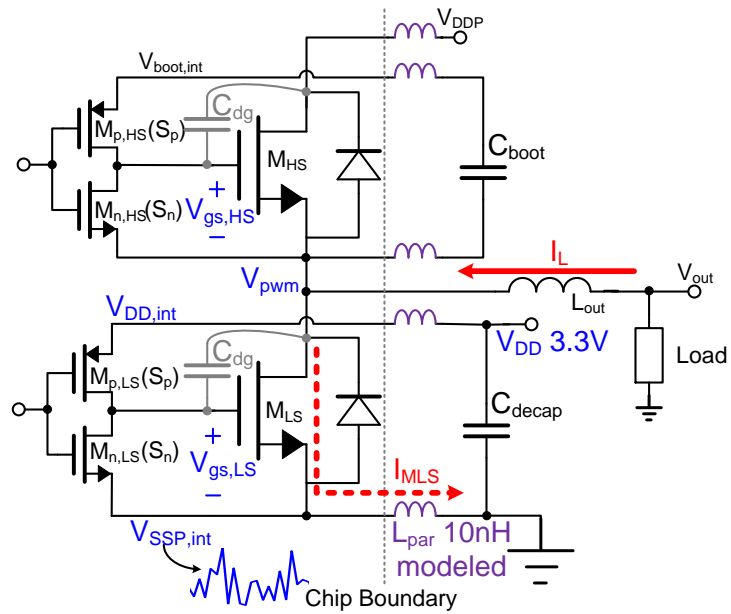


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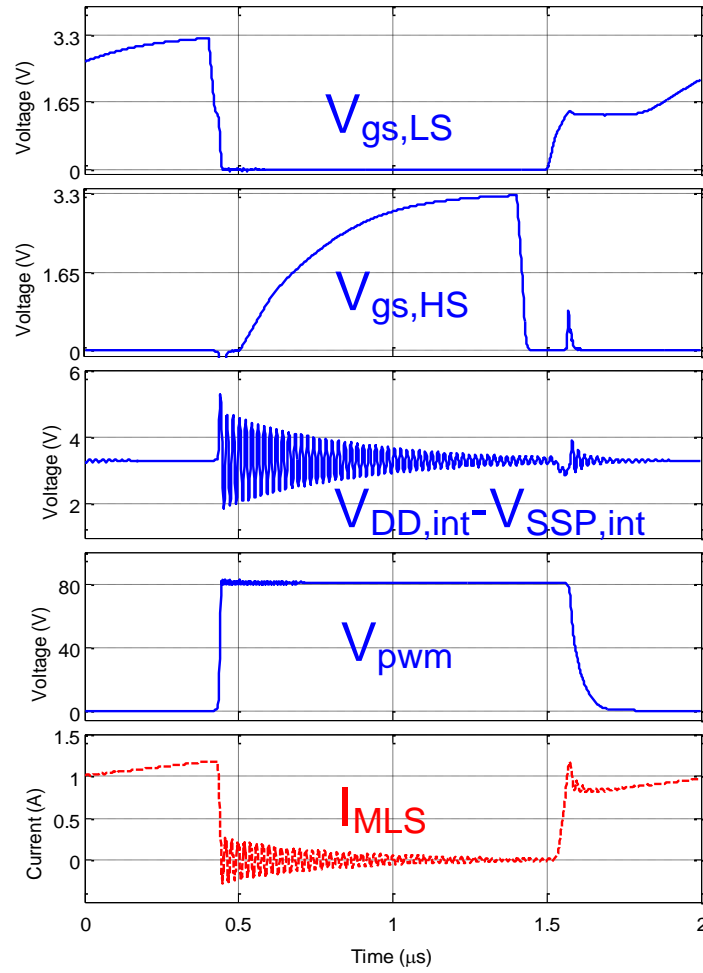


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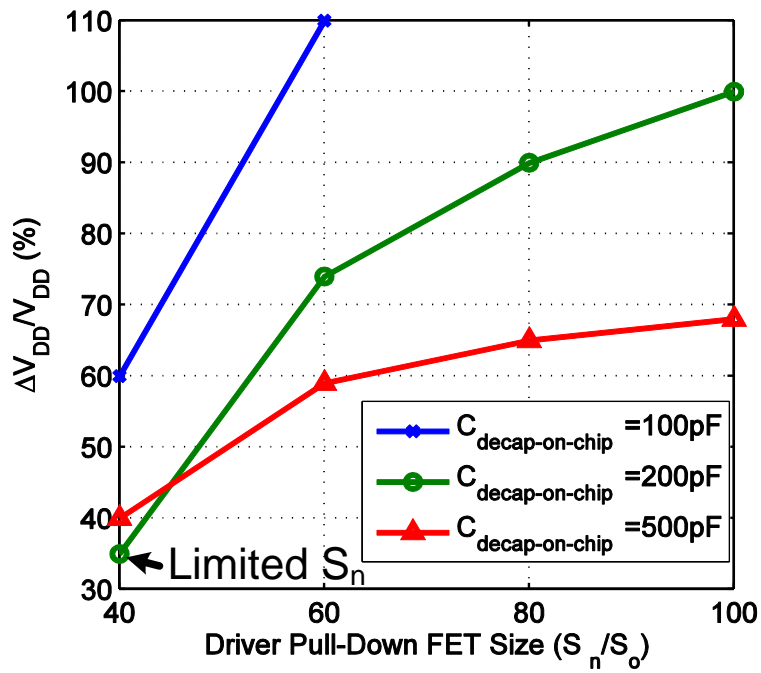
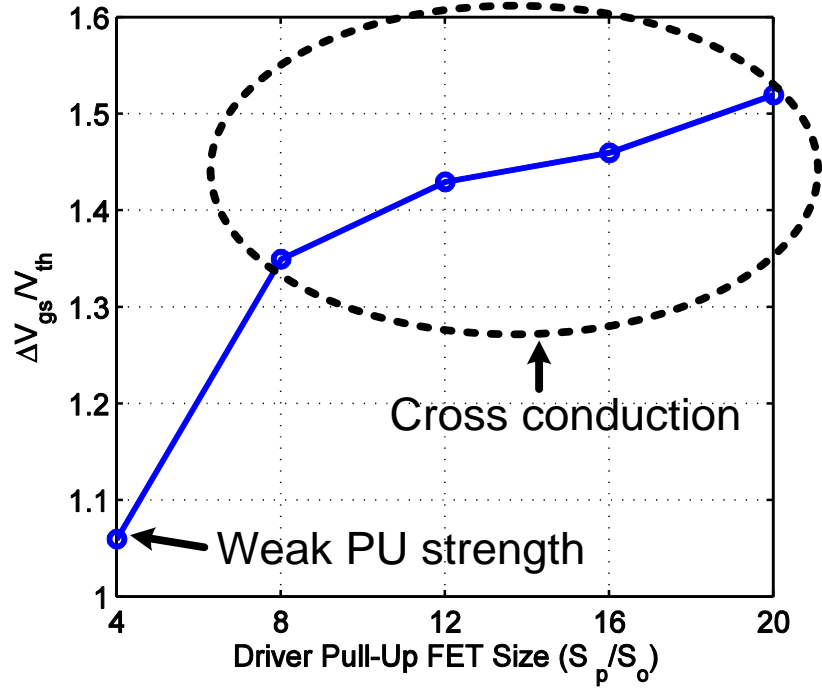
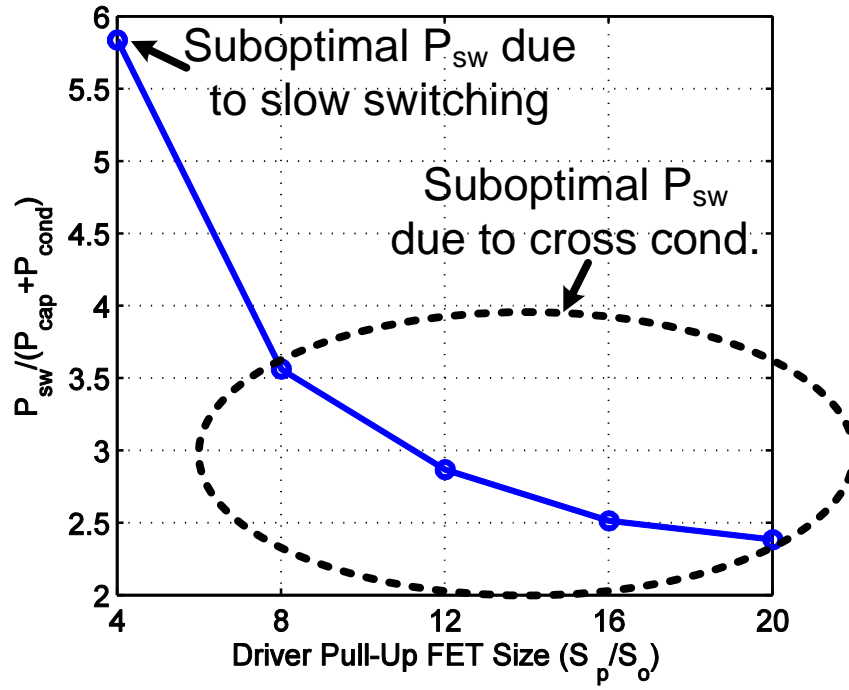


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(a)



(b)

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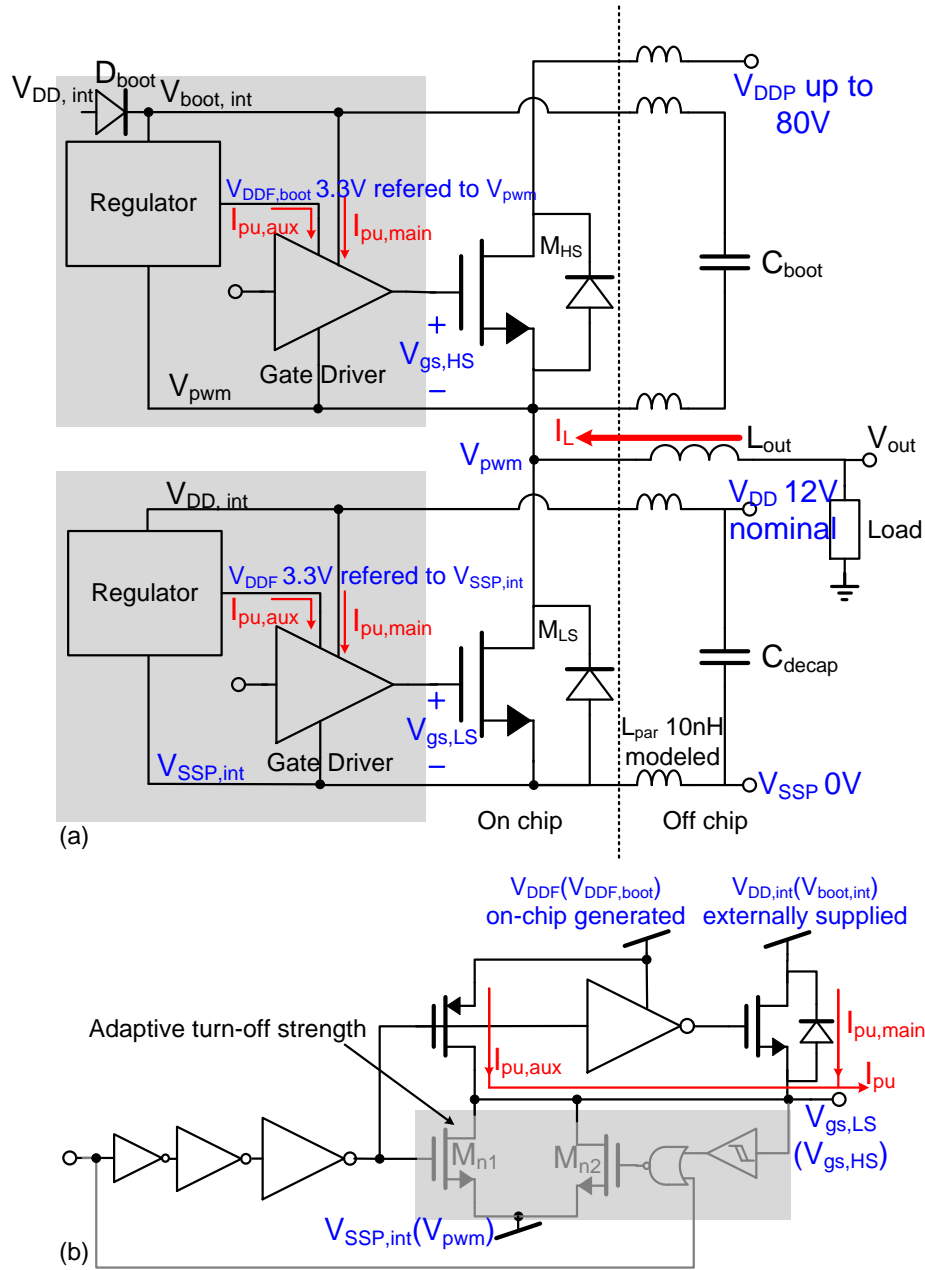


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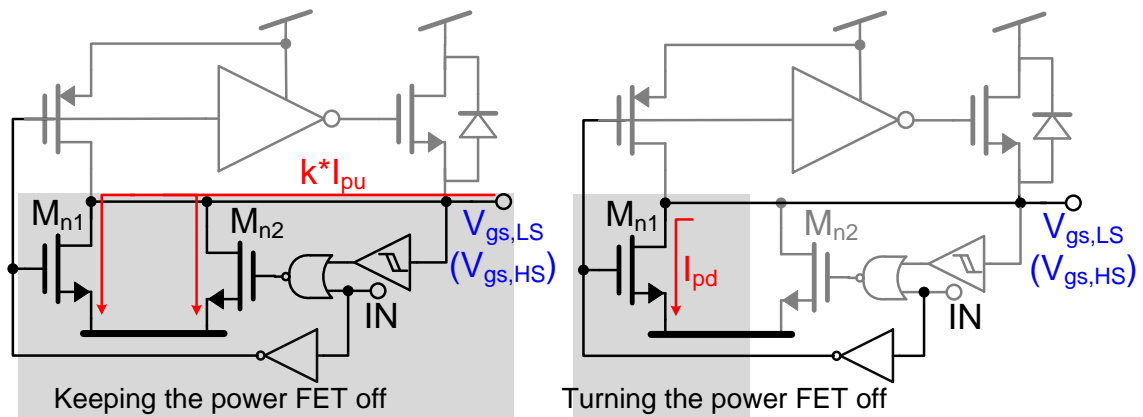


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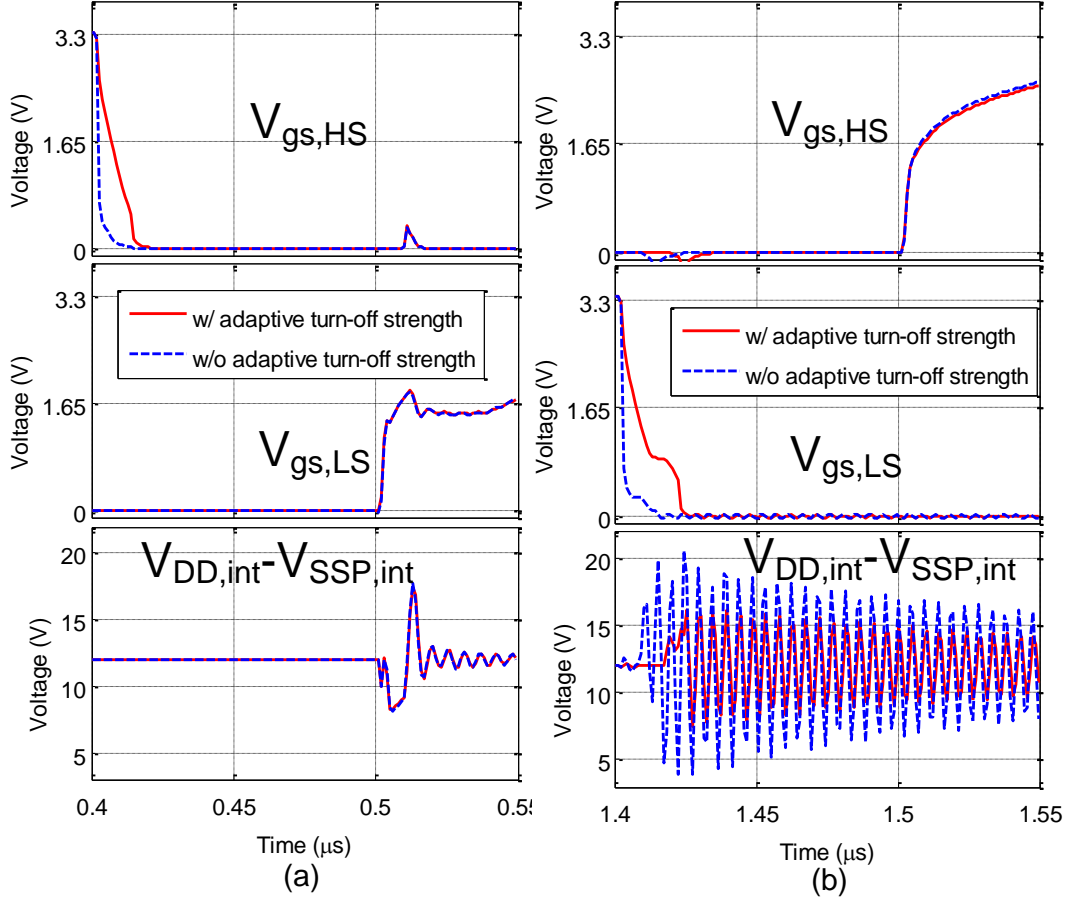


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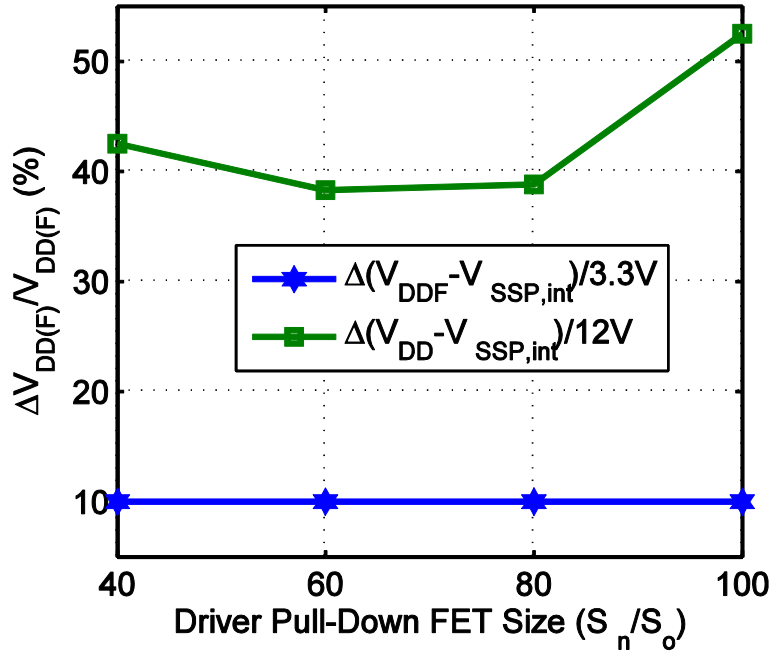
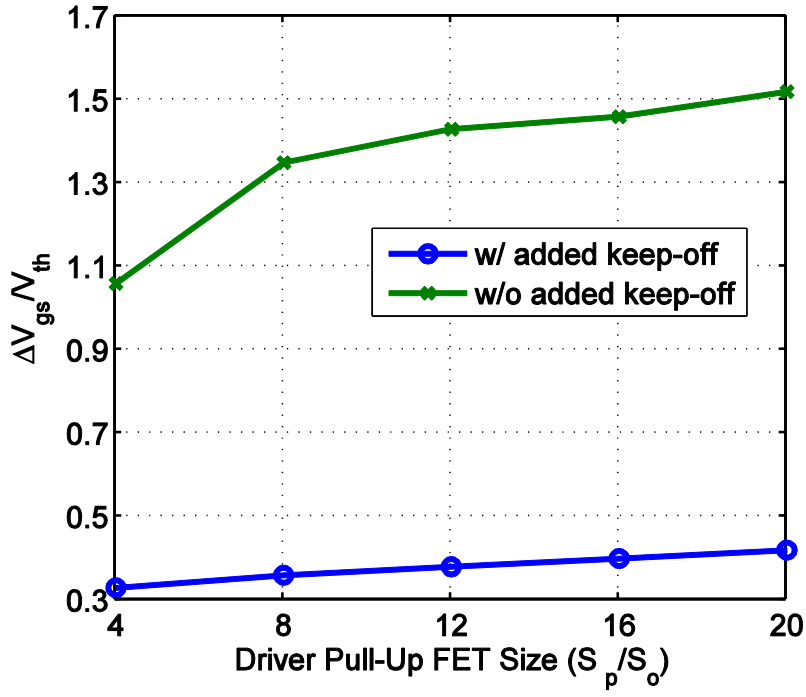
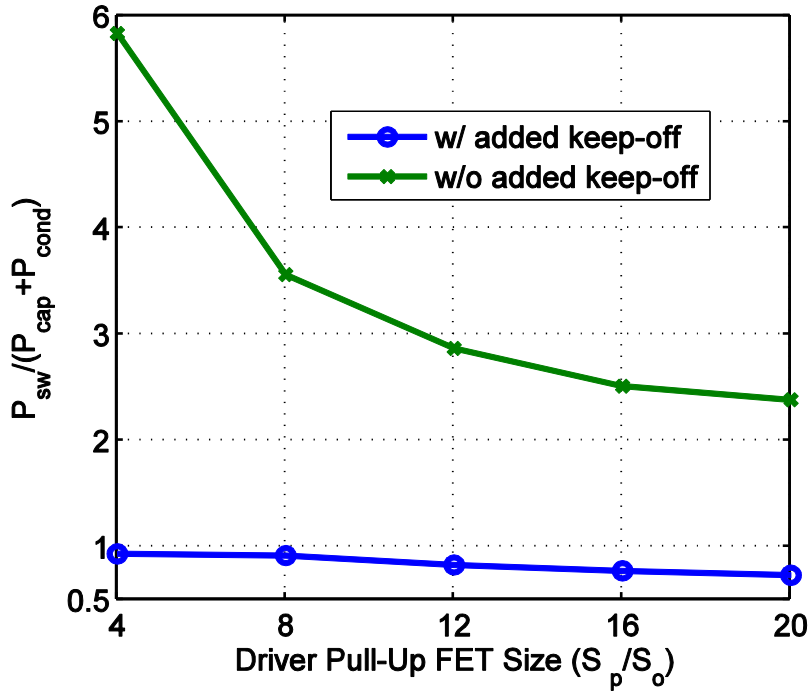


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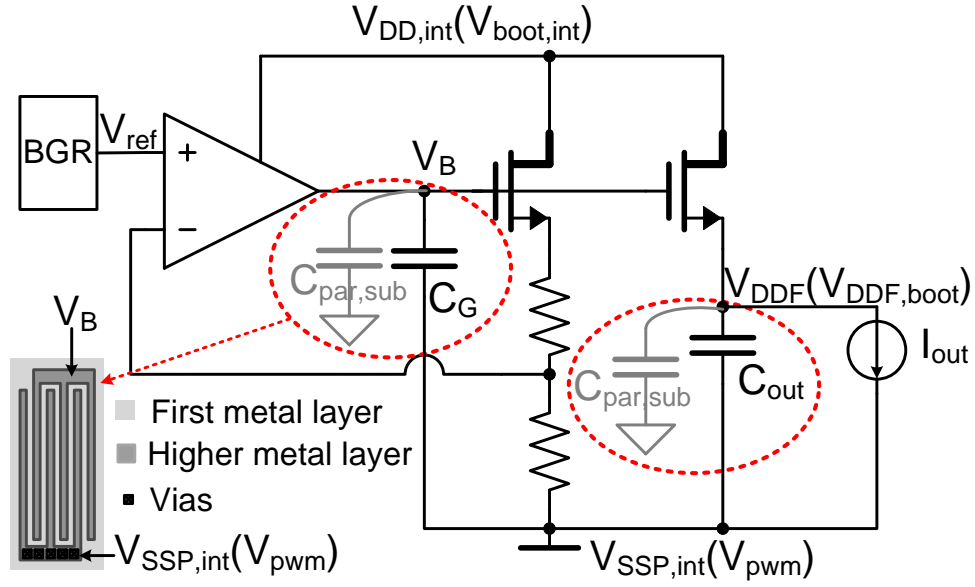


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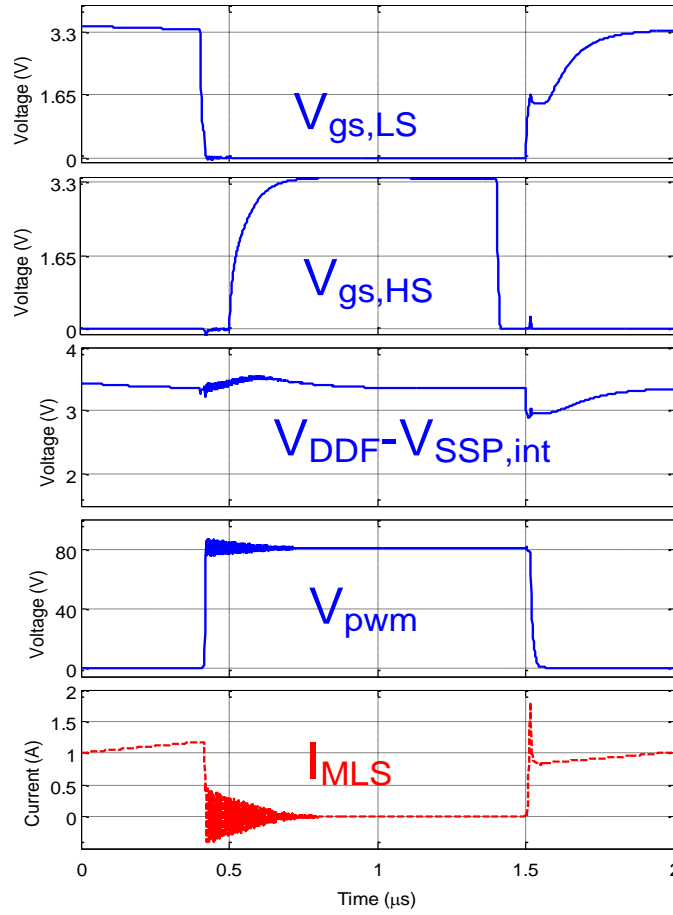


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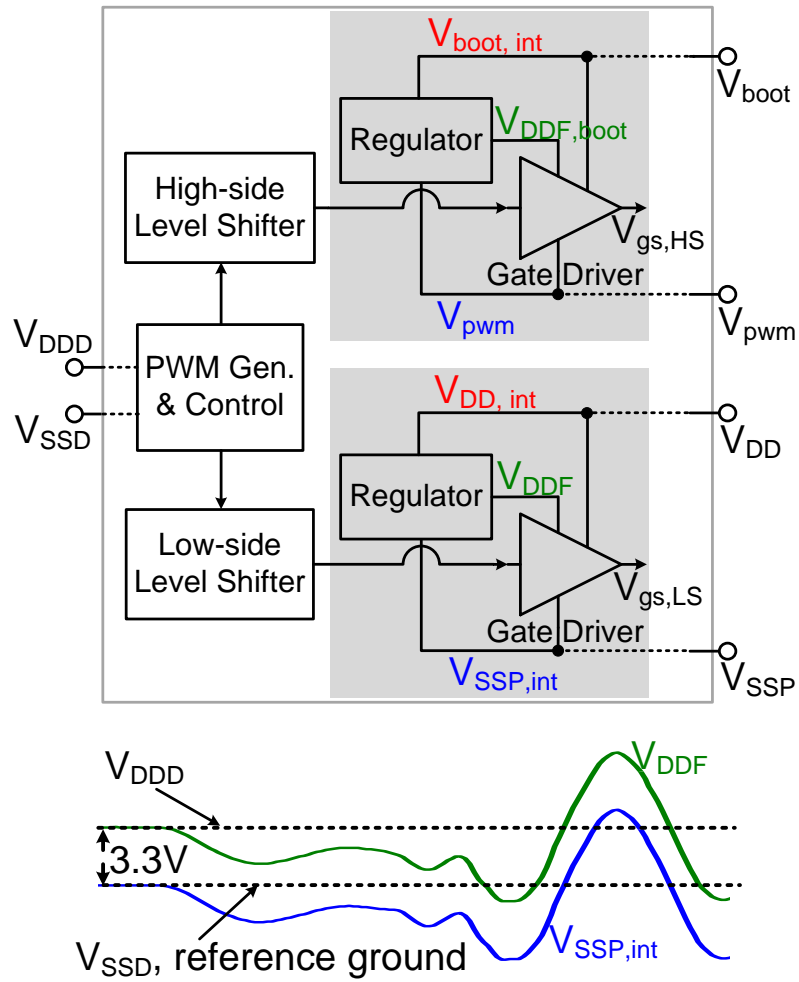


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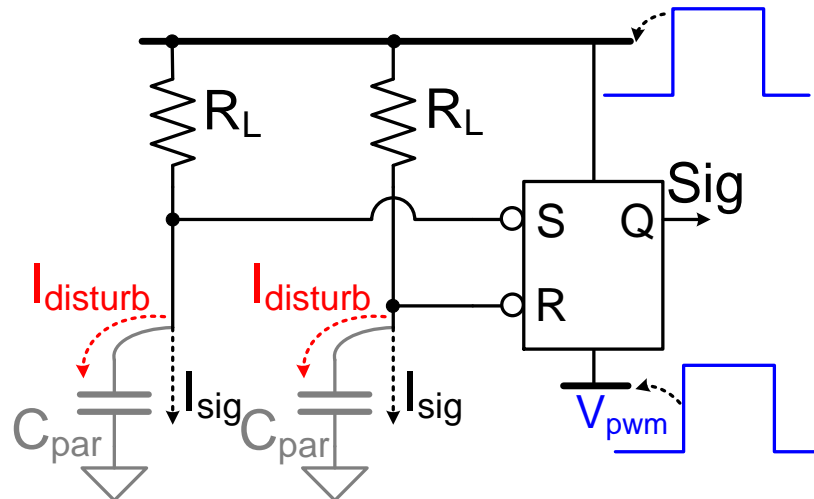


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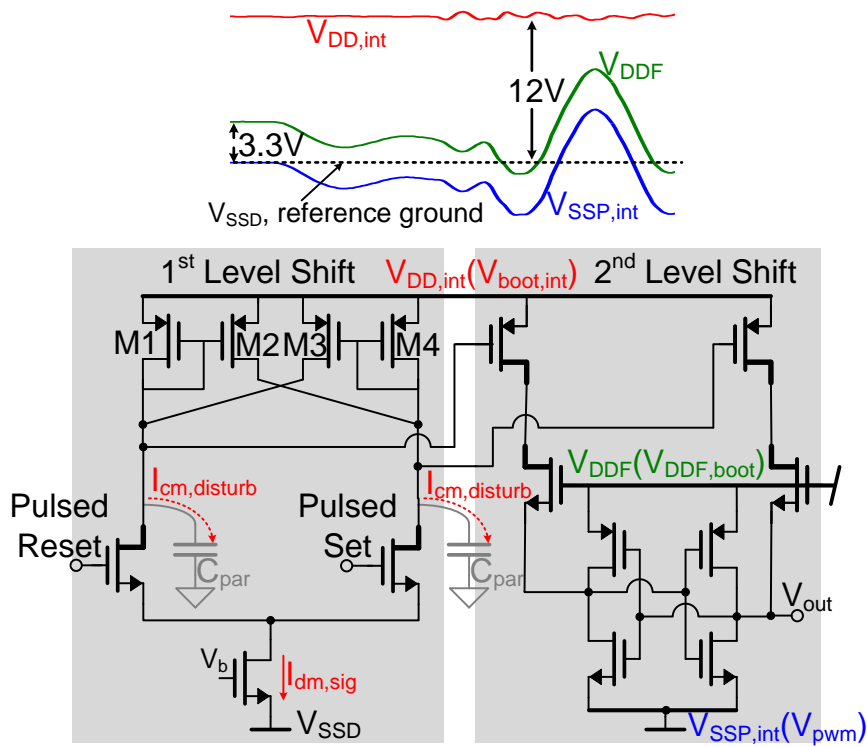


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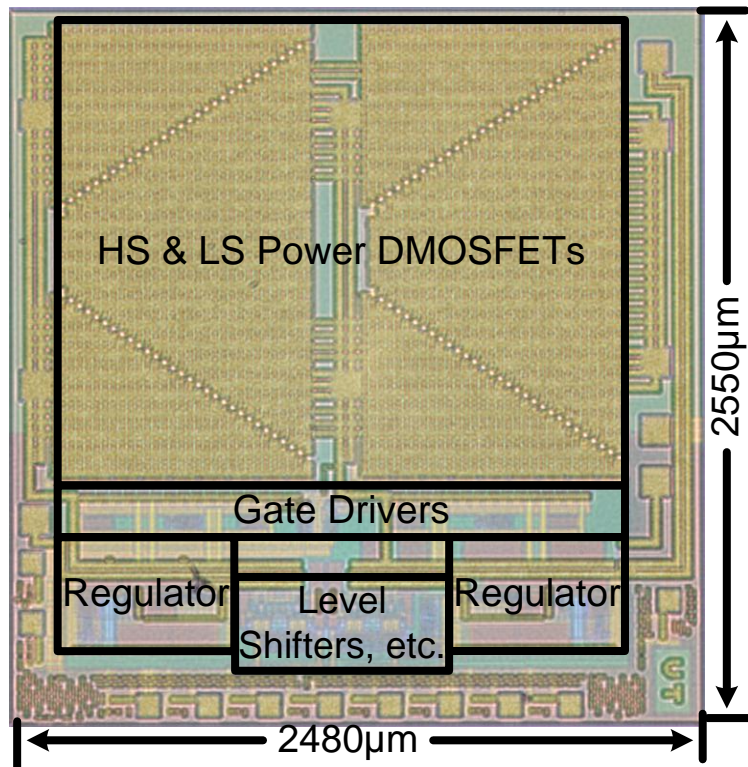


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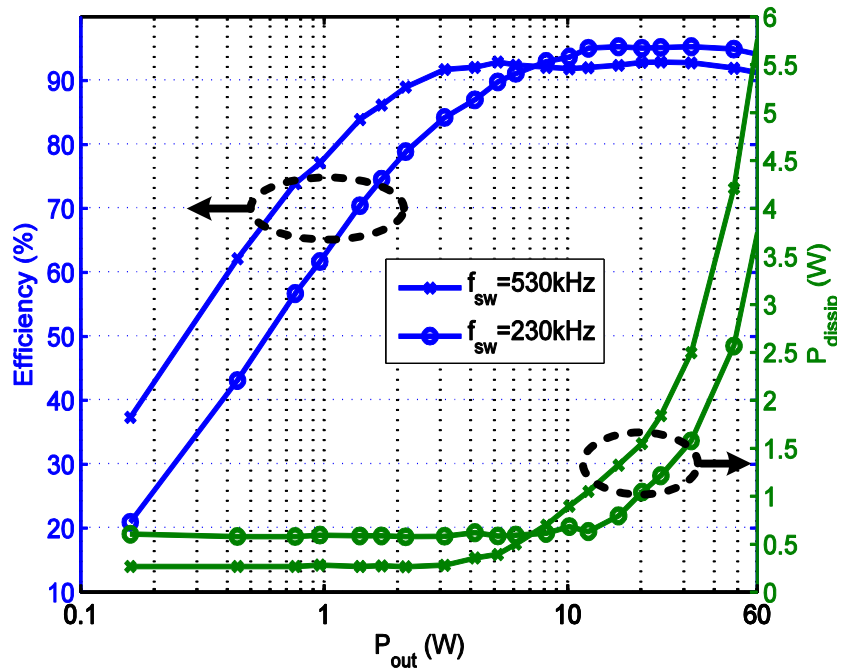


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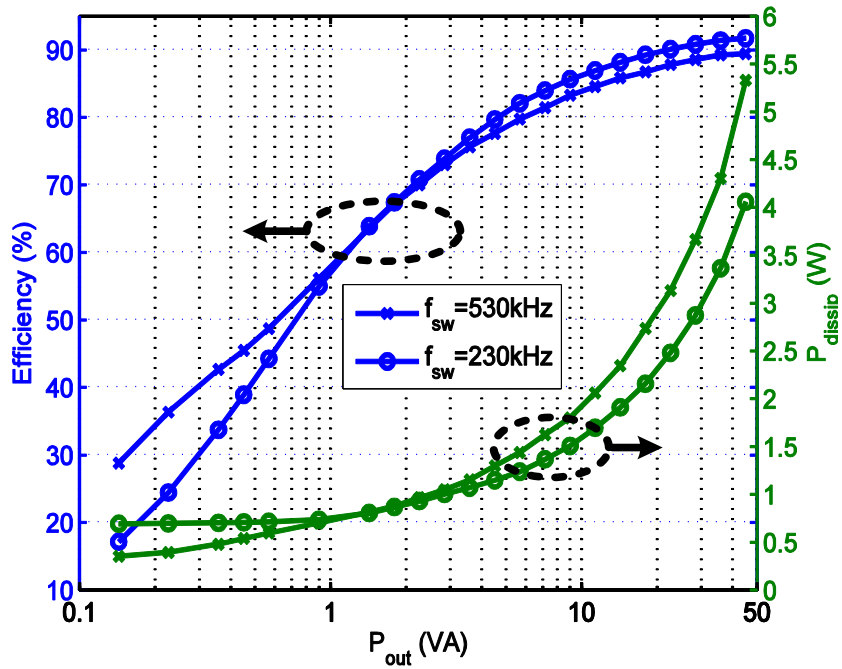


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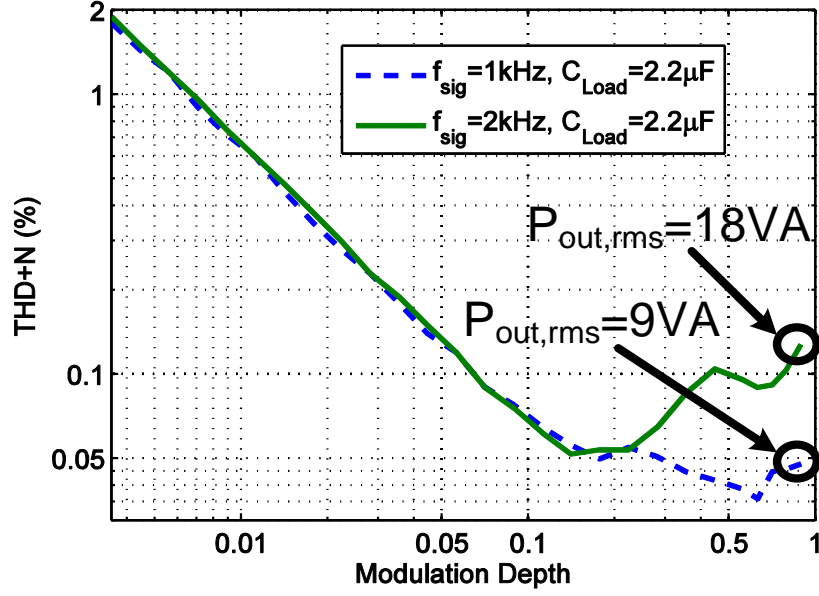


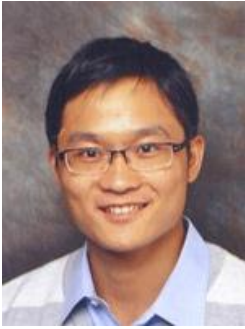
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TABLE I. SUMMARY OF THE PARAMETERS USED IN THE POWER STAGE SIMULATION

| Parameters | Value |
|------------------------------|--------|
| Power Stage Supply V_{DDP} | 80V |
| DMOSFET's Maximum V_{gs} | 3.3V |
| Output Inductance L_{out} | 100μH |
| Switching Frequency f_{sw} | 500kHz |
| Output DC Current I_{out} | 1A |
| V_{pwm} Duty Cycle | 0.5 |
| Dead Time t_d | 100ns |

TABLE II. LIST OF EACH DISSIPATION SOURCE WITH AN OPTIMIZED POWER TRANSISTOR SIZE S OF 56000μm/0.75μm

| Dissipation Source | Power Loss Type | Power Loss | Ratio |
|-----------------------------|-----------------|------------|-------|
| Total Output DMOSFETs' Loss | Balanced | 1.2W | 100% |
| P_{cond} | $\propto 1/S$ | 570mW | 48% |
| P_{cap} | $\propto S$ | 120mW | 10% |
| P_{sw} | $\propto S$ | 510mW | 42% |



Haifeng Ma (S'13) received the B.S. degree in Physics from Nanjing University, Nanjing, China, in 2007, and the M.S. degree (with Honor) in Microelectronics from Fudan University, Shanghai, China, in 2010. The same year, he joined the IC Design group at the University of Twente, Enschede, The Netherlands, as a Ph.D. student.

His research interest is in analog IC design, with current focus on switching power amplifiers.



Ronan van der Zee (M'07) received the M.Sc. degree (cum laude) in electrical engineering from the University of Twente, Enschede, the Netherlands in 1994. In 1999, he received the Ph.D. degree from the same university on the subject of high-efficiency audio amplifiers. In 1999, he joined Philips Semiconductors, where he worked on class AB and class D power amplifiers. In 2003, he joined the IC Design group at the University of Twente. His current research interests include linear and switching power amplifiers, RF frontends and wireless sensor networks.



Bram Nauta (F'08) was born in Hengelo, The Netherlands. In 1987 he received the M.Sc degree (cum laude) in electrical engineering from the University of Twente, Enschede, The Netherlands. In 1991 he received the Ph.D. degree from the same university on the subject of analog CMOS filters for very high frequencies. In 1991 he joined the Mixed-Signal Circuits and Systems Department of Philips Research, Eindhoven the Netherlands. In 1998 he returned to the University of Twente, as full professor heading the IC Design group. His current research interest is high-speed analog CMOS circuits.

He served as Associate Editor of IEEE Transactions on Circuits and Systems II (1997-1999). He was Guest Editor, Associate Editor (2001-2006) and later the Editor-in-Chief (2007-2010) of IEEE Journal of Solid-State Circuits. He was member of the technical program committee of the International Solid State Circuits Conference (ISSCC) where he served in several roles including the European Chair and the 2013 Program Chair. He also served in the Technical Program Committee of the Symposium on VLSI circuits (2009-2013) and is in the steering committee and programme committee of the European Solid State Circuit Conference (ESSCIRC). He is co-recipient of the ISSCC 2002 and 2009 "Van Vessel Outstanding Paper Award". He served as distinguished lecturer of the IEEE, is member of IEEE-SSCS AdCom and is IEEE fellow.