Design and analysis of a high-performance CNFET-based Full Adder

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This paper presents a high-speed and high-performance CNFET-based Full Adder cell for low-voltage applications. The proposed Full Adder cell is composed of two separate modules with identical hardware configurations which generate the Sum and C_{out} signals in a parallel manner. The great advantage of the proposed structure is its very short critical path which is composed of only two CNT pass-transistors. This design also takes advantage of the unique properties of MOSFET-like CNFETs such as the feasibility of adjusting the threshold voltage of a CNFET by adjusting the diameter of its nanotubes to correct the voltage levels as well as to achieve a high performance. Comprehensive experiments are performed in various situations to evaluate the performance of the proposed design. Simulations are carried out using Synopsys HSPICE with 32nm-CMOS and 32nm-CNFET technologies. The simulation results demonstrate the superiority of the proposed design in terms of speed, power consumption, power delay product (PDP) and less susceptibility to process variations, compared to other classical and modern CMOS and CNFET-based Full Adder cells.

Keywords: Carbon Nanotube Field Effect Transistor (CNFET), Full Adder Cell, Exclusive-OR (XOR), Majority Function, Nanoelectronics

1. Introduction

With scaling down the feature size in nanoranges, CMOS technology has faced serious problems and challenges such as high power densities, decreased gate control, short-channel effects and high sensitivity to process variations (Lin et al. 2009). These difficulties will restrict the suitability of the CMOS technology for low-power and high-performance applications, in the time to come. Therefore, scientists are working toward the emerging nanotechnologies such as Quantum Dot Cellular Automata (QCA) (Porod et al. 1999; Navi et al. 2010a), Single Electron Transistor (SET) (Abu El-Seoud et al. 2007, Sulieman et al. 2005) and Carbon Nanotube Field Effect Transistor (CNFET) (Keshavarzian et al. 2009b, Subash et al. 2009) as the possible successors to the conventional silicon-based MOSFET technology. However, due to the similarities between MOSFETs and CNFETs in terms of operation and intrinsic characteristics, CNFET seems to be more feasible and promising compared to the other nanotechnologies. In addition, another important characteristic of CNFET, which makes it more promising, is its unique one-dimensional band-structure which suppresses backscattering and causes near-ballistic operation (Lin et al. 2009).

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In general, CNFET has higher performance and lower power consumption compared to the silicon-based MOSFET and is very suitable for low-voltage and high-frequency applications. Another significant attribute of CNFET is that P-CNFET and N-CNFET, with the same device geometries, have the same mobilities and consequently the same current drive capabilities, which is very important for transistor sizing in the complex circuits (Cho et al. 2009).

In recent years, some CNFET-based circuits such as Multiple-valued logic circuits (Lin et al. 2009), (Keshavarzian et al. 2009b), (Raychowdhury et al. 2005), Galois field circuits (Keshavarzian et al. 2009a), and CNFET Full Adders (Navi et al. 2009b), (Navi et al. 2010b) have been proposed in the literature. However, considering all these structures, arithmetic circuits could be more of an interest on account of their comprehensive applications in the VLSI systems, such as processors, DSP architectures and micro/nano electronic systems (Molahosseini et al. 2010; Timarchi et al. 2009). Since the Full Adder cell is the fundamental core and the building block of most arithmetic circuits and is located on most parts of their critical paths, it has always been important to design high-speed and high-performance Full Adder cells and consequently low Power-Delay Product (PDP) complex arithmetic circuits (Navi et al. 2009a).

In this paper a high-speed and low-PDP CNFET-based Full Adder with a critical path consisting of only two transistors is presented for low voltages. The performance of the proposed design is evaluated in various situations and is compared with the other conventional and state-of-the-art 32nm-CMOS and 32nm-CNFET Full Adder cells of different styles which are reviewed briefly in this section.

The CMOS-Bridge fully symmetric Full Adder cell (Kavehei et al. 2008) (Figure 1(a)), which has 24 transistors, takes advantage of the high-performance bridge style. It produces the $\overline{C_{out}}$ (output carry) signal based on a CMOS style and generates the $\overline{Sum}$ signal from $\overline{C_{out}}$ by means of a bridge circuit. In addition, to generate C_{out} and Sum and for enhancing the driving capability, two inverters are utilized at the output nodes of this circuit. Despite the low power consumption of this design, its critical path includes six transistors which leads to long propagation delays.

The TG-CMOS Full Adder (Figure 1(b)) (Weste et al. 1993), which has 18 transistors, is the conventional transmission gate-based CMOS Full Adder cell and its critical path consists of four transistors.

The Hybrid1 Full Adder cell (Chang et al. 2005) (Figure 1(c)), which has 26 transistors, utilizes a high-performance 2-input XOR/XNOR circuit and a complementary CMOS style circuit and two inverters to generate the Sum and C_{out} outputs with driving capability.

The Hybrid2 Full Adder cell (Goel et al. 2006) (Figure 1(d)), which has 24 transistors, is composed of three modules. The first module is a high-speed XOR/XNOR circuit and produces balanced full-swing signals. The other two modules use these signals to generate the Sum and C_{out} outputs with driving capability. The critical path of the Hybrid1 and Hybrid2 Full Adders consist of four transistors.

In addition to these MOSFET-based Full Adder cells, some CNFET Full Adders have been presented in the literature, which have been designed based on capacitors, which could be CNCAPs (Budnik et al. 2006), and CNFET-based inverters (Navi et al. 2009b, Navi et al. 2010c).

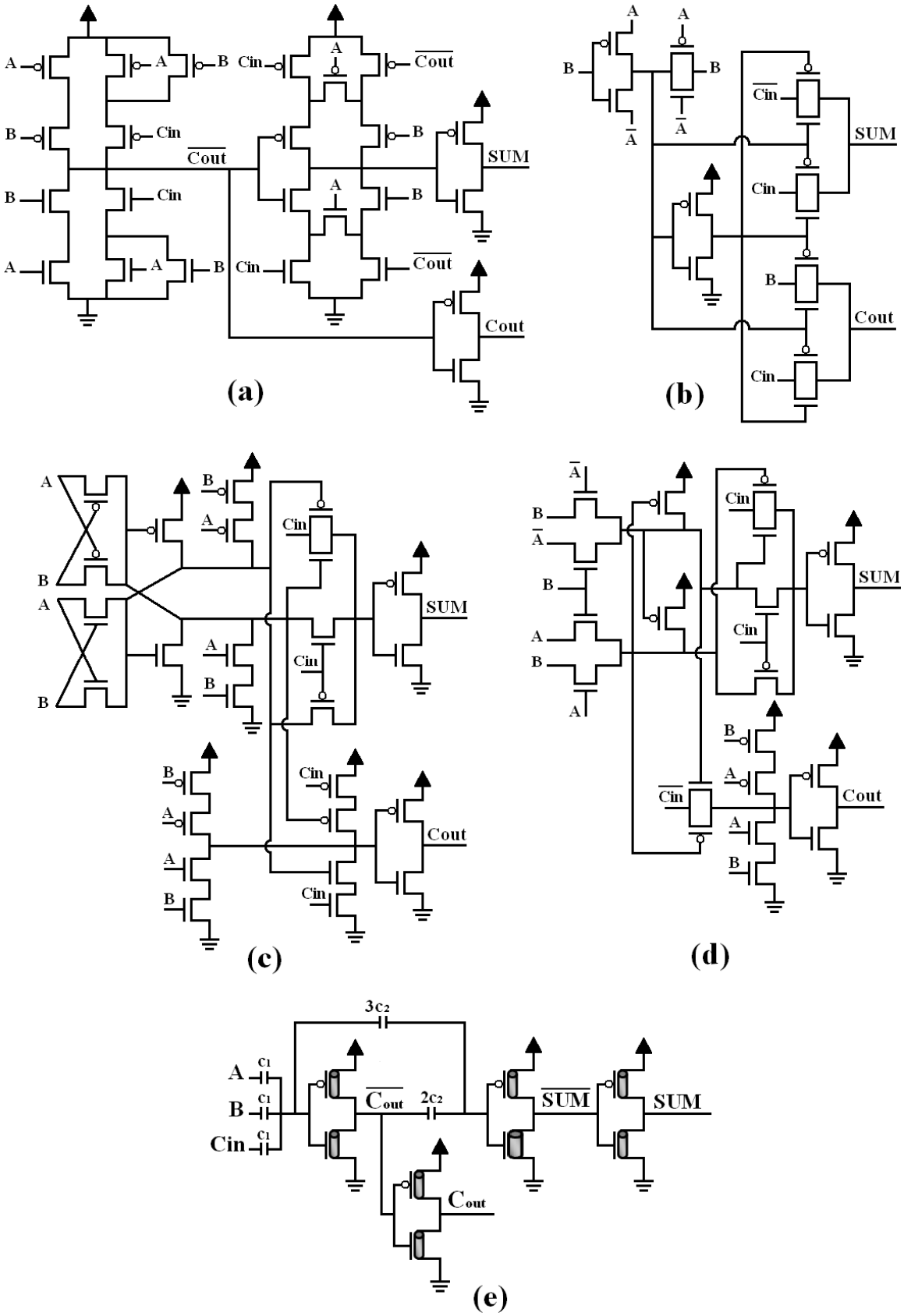

Figure 1. (a) CMOS-Bridge (b) TG-CMOS (c) Hybrid1 (d) Hybrid2 (e) CN3c2c

However, considering these designs, CN3c2c (Navi et al. 2010c) (Figure 1(e)), a Majority Function-based Full Adder cell, have shown better performance. This Full Adder is composed of five capacitors and four CNFET-based inverters. The first inverter acts as a majority detector on the input signals summation and produces $\overline{C_{out}}$. The second module uses another CNFET-based inverter to generate $\overline{Sum}$ by computing the majority of the summation of the inputs and two times of $\overline{C_{out}}$ signal. Moreover, two additional inverters are used for generating the Sum and C_{out} signals and enhancing the driving capability. Therefore, this design contains two capacitors and three CNFET inverters in its critical path and generates the Sum and C_{out} signals together with their complements.

In the reminder of this paper, in section 2 a brief review of the CNFET technology is presented. The proposed CNFET-based Full Adder cell is presented in section 3. The experimental results, analyses and comparisons are presented in section 4 and finally, section 5 concludes the paper.

2. Carbon Nanotube Field Effect Transistors

Carbon Nanotube (CNT) is a sheet of graphite which is rolled up along a wrapping vector. A CNT could be single-wall (SWCNT) or multi-wall (MWCNT) (McEuen et al. 2002). SWCNTs are composed of one cylinder whereas MWCNTs have more than one cylinder. A SWCNT could be metallic or semiconducting, depending on its chirality vector, which is determined by (n_1, n_2) indices and specify the arrangement angle of the carbon atoms along the nanotube (Lin et al. 2009). If n_1-n_2=3k ($k \in Z$), the SWCNT is conducting and otherwise it is semiconducting. In Carbon Nanotube Field Effect Transistors (CNFETs) one or more semiconducting SWCNTs are used as the channel of the device.

Figure2 (a) shows the schematic of a typical CNFET device. The distance between the centers of two adjoining SWCNTs under the same gate of a CNFET is called pitch, which directly impacts the width of the gate and contacts of the device. The width of the gate of a CNFET can be approximately calculated based on the following equation (Kim et al. 2009):

$$W_{gate} \approx Min(W_{min}, N \times Pitch) \quad (1)$$

where W_{min} is the minimum width of the gate and N is the number of nanotubes under the gate. Moreover, the current-voltage (I-V) characteristics of the MOSFET and CNFET devices are alike.

Similar to a MOSFET device, a CNFET has also threshold voltage which is the voltage required for turning on the device electrostatically through the gate. A great advantage of CNFET is that its threshold voltage (V_t) can be adjusted by changing the diameter of its CNTs. This practical characteristic makes CNFET more flexible than MOSFET for designing digital circuits and makes it very suitable for designing multi-V_t circuits. The threshold voltage of a CNFET is almost considered as the half bandgap and can be calculated by the following equation (Kim et al. 2009):

$$V_{th} \approx \frac{E_g}{2.e} = \frac{\sqrt{3}}{3}\frac{aV_\pi}{e.D_{CNT}} \approx \frac{0.43}{D_{CNT}(nm)} \quad (2)$$

where parameter a (≈ 0.249 nm) is the carbon to carbon atom distance, V_π (≈ 3.033 eV) is the carbon π-π bond energy in the tight bonding model, e is the unit electron charge, and D_{CNT} is the diameter of CNT. It can be concluded from Equation (2) that the threshold voltage of the CNFET is an inverse function of the diameter of CNT, which is calculated by the following equation (Kim et al. 2009):

$$D_{CNT} = \frac{a \times \sqrt{n_1^2 + n_2^2 + n_1 n_2}}{\pi} \approx 0.0783 \times \sqrt{n_1^2 + n_2^2 + n_1 n_2} \quad (3)$$

For instance, for a CNFET with the chiral numbers (n_1, n_2) = (19, 0), D_{CNT} is 1.487nm and subsequently its threshold voltages is 0.293V.

Three different kinds of CNFETs have already been presented in the literature. The first one is Schottky Barrier CNFET (SB-CNFET), which is shown in Figure 2(b). SB-CNFET is a tunneling device and works on the tenets of direct tunneling through a Schottky Barrier (SB) at the source-channel junction. The width of the barrier is regulated by the application of gate voltage and thus the transconductance of the device is reliant upon the gate voltage. This kind of CNFET is fabricated using direct contact of the semiconducting nanotube and the metal and consequently it has an SB at the CNT-metal junction. The main disadvantage of this technology is that the energy barrier at SB actually restricts the transconductance of the CNFET in the ON state and reduces the current delivery capability, which is a significant metric to the speed of a device. SB-CNFETs demonstrate strong ambipolar characteristics that restrict the usage of these devices in CMOS-like logic families. This type of CNFET is appropriate for moderate to high-performance applications. To overcome the mentioned drawback of SB-CNFET, there have been attempts to develop CNFETs, which would operate like normal MOSFETs but with higher performance. Therefore, Potassium doped source and drain CNT regions have been fabricated and unipolar characteristics and the field-effect behaviour has been reached. This type of CNFET which is called MOSFET-like CNFET (Figure 2(c)) operates on the tenet of barrier height modulation by application of the gate potential. The main advantage of MOSFET-like CNFET versus SB-CNFET is that its source-channel junction has no Schottky Barrier and hence, it has significantly higher ON current. As a result, MOSFET-like CNFETs are very suitable for ultra-high-performance digital applications. The third kind of CNFET, called the band-to-band tunneling CNFET (T-CNFET) (Figure 2(d)), has low ON currents and super cut-off characteristics and is very suitable for subthreshold and ultra-low-power applications (Raychowdhury et al. 2007), (Javey et al. 2004), (Javey et al. 2005).

Based on the mentioned pros and cons of the different types of CNFETs and also due to the further similarities between MOSFET-like CNFETs and MOSFETs in terms of operation and characteristics, this type of CNFET is utilized for designing the presented circuit.

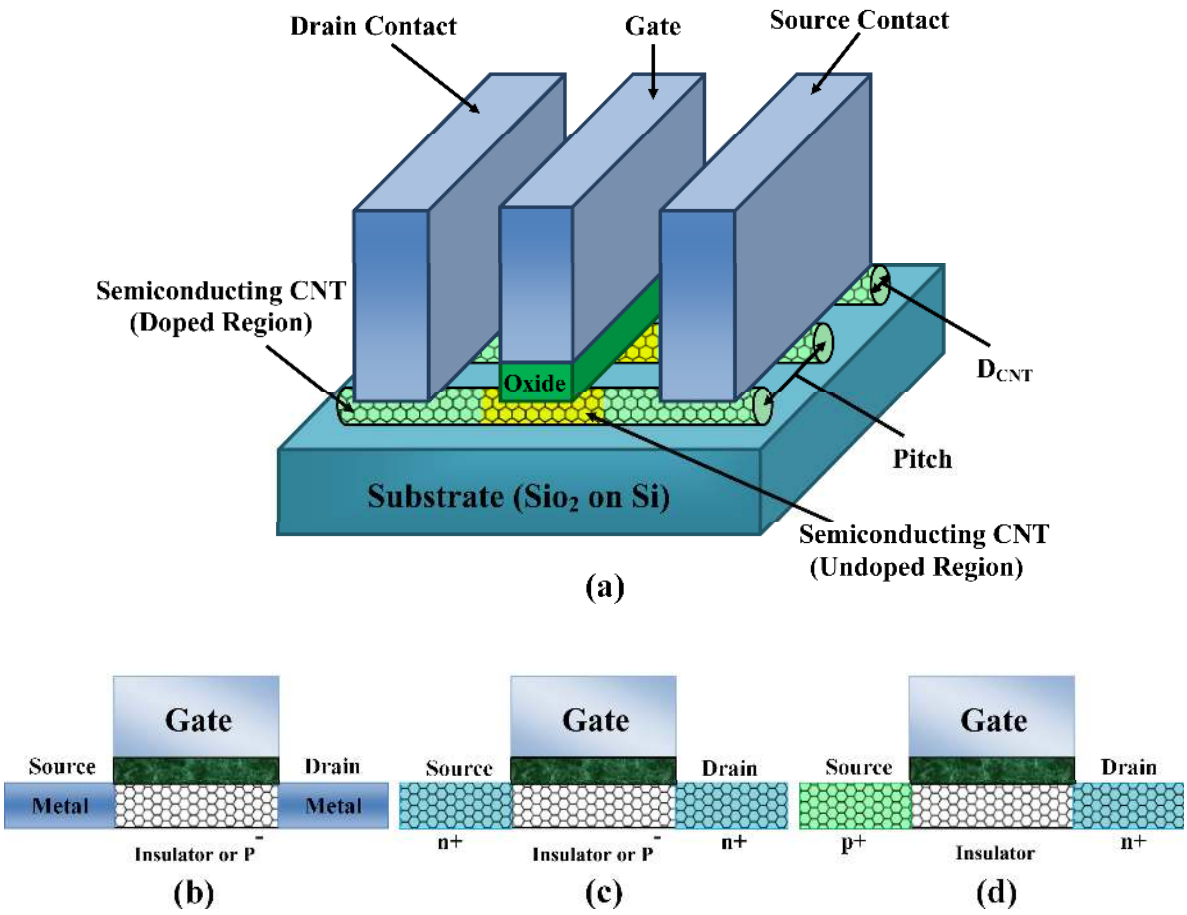

Figure 2. (a) Schematic diagram of a CNFET (b) SB-CNFET (c) MOSFET-like CNFET (d) T-CNFET

3. Proposed Full Adder Cell

The logic function of a 1-bit Full Adder cell with A, B, C_{in} (input carry) inputs and Sum and C_{out} (output carry) outputs is described by the following equations, in which $\odot$ symbol denotes the XNOR function:

$$Sum = XOR(A,B,C_{in}) = A.B.C_{in} + A.\overline{B}.\overline{C_{in}} + \overline{A}.B.\overline{C_{in}} + \overline{A}.\overline{B}.C_{in} \quad (4)$$
$$= A.(B \odot C) + B.(A \odot C) + C.(A \odot B)$$

$$C_{out} = Majority(A,B,C_{in}) = A.B + A.C_{in} + B.C_{in} \quad (5)$$

According to Equation (4) and Equation (5) the Full Adder cell can be designed based on two separate circuits, a 3-input XOR (Moaiyeri et al. 2010) and a 3-input Majority circuit, which generate Sum and C_{out} signals in a parallel manner. The proposed Full Adder cell, which is shown in Figure 3, is composed of two separate fully symmetric CNT pass-transistor networks to implement the Sum and C_{out} functions in a parallel

manner. The first network is a 3-input XOR circuit, which implements the Sum function by means of 10 CNFETs. This module implements Equation (4), with the shortest possible critical path and without using any complementary inputs. It is worth mentioning that shortening the critical path of the designs is the most efficient way to reduce the delay and power consumption at the same time. In addition, circuits with complementary inputs need additional inverters to complement the original inputs and most of them are not efficient.

In general, the output of this circuit has threshold loss in two cases only, when ABC="000" or ABC="111". To correct the voltage swing of the output node of the Sum generator circuit, some methods, such as using output buffers or using transmission gate networks instead of pass-transistor networks, could be utilized. Unfortunately, all of these solutions lead to lengthening the critical path of the designs and hardware redundancy, which consequently results in performance degradation. However, by utilizing CNFET nanotechnology, the intrinsic threshold voltage drop problem in this circuit can be resolved without any hardware redundancy.

According to Equation (2), the threshold voltage of CNFET is inversely proportional to the diameter of its carbon nanotube. As a result, threshold voltage can be reduced by increasing the diameter of the carbon nanotube, which could resolve the threshold loss problem and leads to better driving capability and higher speed. According to Equation (3), the diameter of a CNT can be regulated by adjusting its chiral number (n_1, n_2). As a result, in this design CNFETs with larger diameters ((n_1,n_2)=(55,0), D_{CNT}=4.306nm) are only utilized in two paths of the circuit to correct the voltage swing just when ABC="000" or ABC="111".

The second module of the proposed design is a Majority circuit which generates the C_{out} signal based on a direct implementation of Equation (5). The structure of this module is similar to the first one with its critical path consists of only two CNT pass-transistors and it has no complementary inputs. The same method as mentioned above can also be utilized to complete the voltage swing of the C_{out} generator circuit by using CNFETs with large diameters ((n_1,n_2)=(55,0), D_{CNT}=4.306nm).

The proposed circuit is simulated using output buffers at 0.65V supply voltage and 250MHz frequency. The input and output signals of the proposed design as well as the "high" and "low" voltage values are shown in Figure 4.

It is obvious that the value of voltage drop is very lower than the value of the threshold voltage in practice, when CNFETs are used. This is due to the very high-speed operation of CNFETs with large diameters in subthreshold region. CNTs with larger diameters have smaller band gaps, due to the fact that the energy band gap of a CNT is proportional to the inverse of its diameter. A smaller band gap intends that a CNFET composed of CNTs with larger diameters can exhibit higher on-currents, which leads to shorter delay times. CNTs with smaller diameters have higher drain/source resistance, which can be explained by the fact that at small diameters only the first sub-band is degenerate. In addition, CNFETs with larger diameters are less sensitive to process variations and leads to better manufacturability (Shahidipour et al. 2009). As described, this solution is based on unique properties of CNFETs and is not feasible and profitable in CMOS technology.

In addition, according to the results of this experiment, by utilizing CNFETs with the same device geometries on the critical path of the proposed design at its pull-up and pull-down networks, the high-to-low propagation delay (Tp_{HL}) and the low-to-high

propagation delay (Tp_{LH}) are almost the same for both Sum and C_{out} signals. It is worth mentioning that the Tp_{HL} and Tp_{LH} are 5.9ps and 6.1ps for the Sum signal and are 5.02ps and 5.08ps for the C_{out} signal, respectively. This fact is also based on another unique property of the CNFET device described in the previous sections.

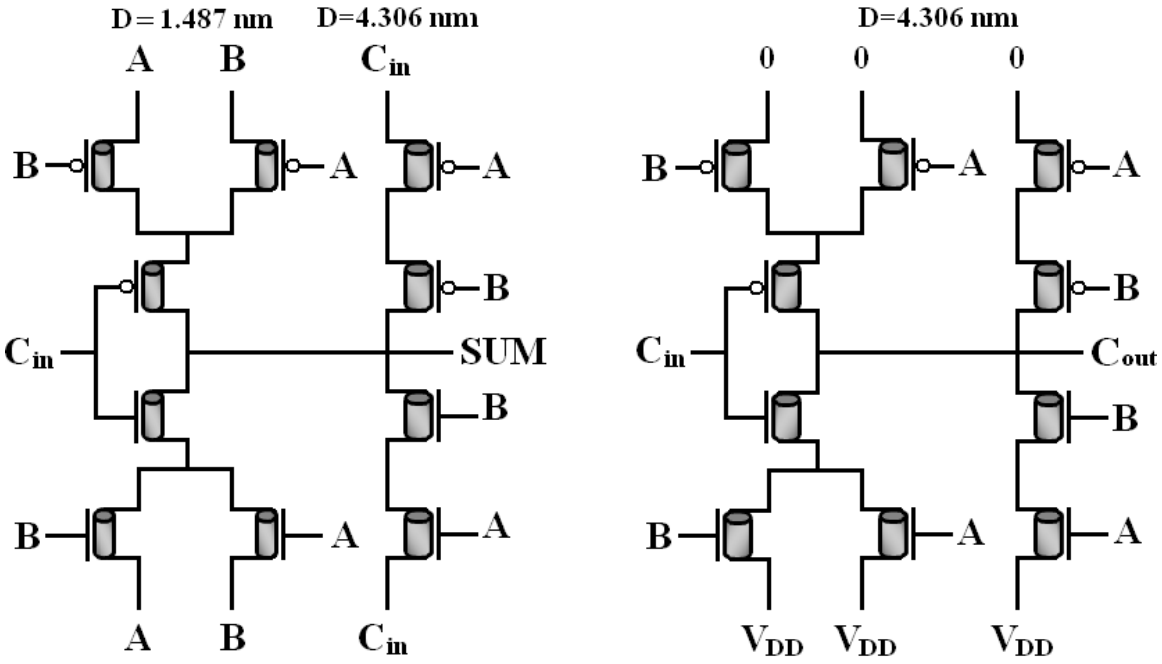

Figure 3. The Proposed CNFET-based Full Adder cell

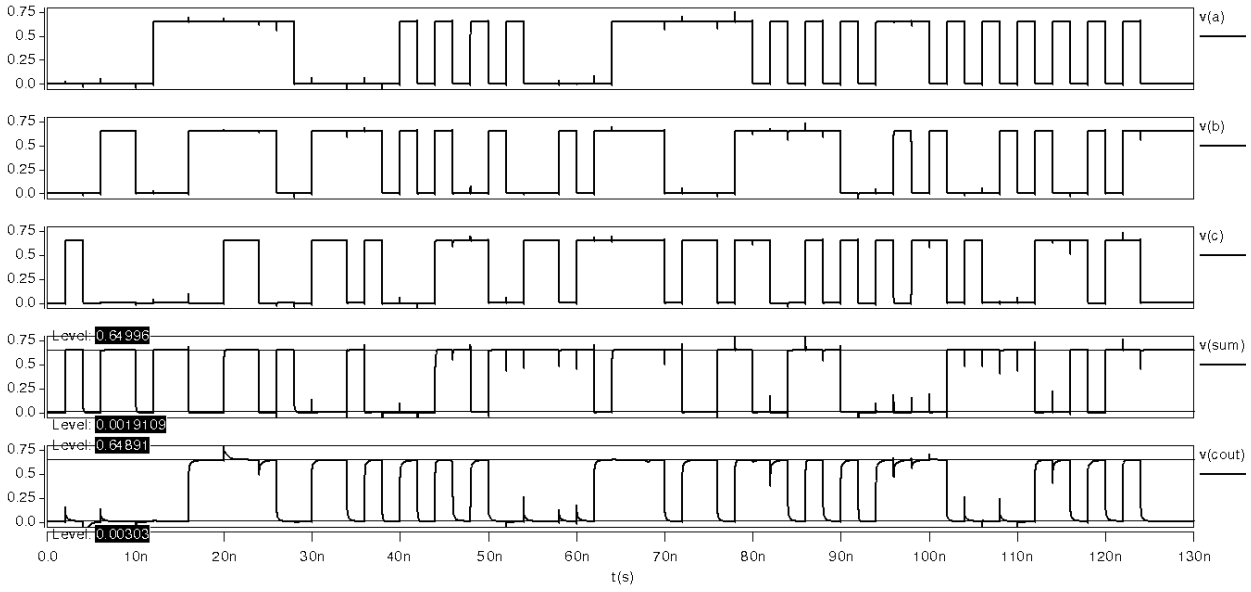

Figure 4. The input and output signals of the proposed design

As shown in Figure 3, the Sum and C_{out} generator modules of the proposed Full Adder cell have the same configurations and only the inputs at their drain nodes are different. Moreover, the great advantage of the proposed Full Adder cell is its short critical path, which consists of only two CNFETs, while the critical path of the other Full Adder circuits, previously presented in the literature, has at least consisted of three transistors. Therefore, this design is much faster than the others and is also more suitable for low-voltage applications.

4. Simulation Results Analysis and Comparison

4.1. Experimental Setup

In this section, the proposed designs are comprehensively evaluated in various situations and are compared with the other classical and state-of-the-art CMOS and CNFET-based Full Adders. All the designs are simulated using Synopsys HSPICE 2007 simulator tool with 32nm CMOS technology for CMOS circuits and the Compact SPICE Model (Deng et al. 2007a, b) for 32nm CNFET-based circuits, including all nonidealities. This standard model has been designed for unipolar, MOSFET-like CNFET devices, in which each transistor may have one or more CNTs. This model also considers Schottky Barrier Effects, Parasitics, including CNT, Source/Drain, and Gate resistances and capacitances and CNT Charge Screening Effects. The parameters of the CNFET model and their values, with brief descriptions, are shown in Table 1.

Table 1. CNFET Model Parameters

Parameter	Description	Value
L_{ch}	Physical channel length	32nm
L_{geff}	The mean free path in the intrinsic CNT channel	100nm
L_{ss}	The length of doped CNT source-side extension region	32nm
L_{dd}	The length of doped CNT drain-side extension region	32nm
K_{gate}	The dielectric constant of high-k top gate dielectric material	16
T_{ox}	The thickness of high-k top gate dielectric material	4nm
C_{sub}	The coupling capacitance between the channel region and the substrate	20pF/m
Efi	The Fermi level of the doped S/D tube	6eV

All of the CMOS circuits are sized for minimizing the PDP, based on the transistor sizing procedure of (Chang et al. 2005). Simulations are carried out at room temperature and various supply voltages, frequencies and loads are used for simulation. Complete input pattern with all the possible transitions from an input combination to another is applied to the circuits to measure their propagation delay. The delay of each circuit is calculated from the time that the input signal reaches $½V_{DD}$ to the time that the output signal reaches the same voltage level. All the transitions from one input to another are checked and the delay is measured for each transition and the maximum is reported as the delay of each circuit. The average power consumption during a long period of time is also considered as the power consumption parameter. In order to make a compromise between the power consumption and the delay of the circuits, the performance of the circuits can be evaluated by calculating the power-delay product (PDP), which is the multiplication of the average power consumption and the maximum delay. As a result, PDP could be an important parameter for evaluating and comparing the performance of the circuits.

4.2. *Performance Evaluation*

In the first experiment, the circuits are simulated at 0.8V, 0.65V, and 0.5V supply voltages and at 100MHz frequency with 2.1fF output load capacitors. The detailed results of this simulation are listed in Table 2. The best results at each voltage are demonstrated with bold-faced numbers. According to the experimental results, CNPTL (Proposed) has the shortest delay and the lowest PDP compared to the other designs at all supply voltages. It has also the lowest power consumption at 0.8V and 0.65V.

In order to evaluate the performance of the circuits in a demanding circumstance, all the circuits are simulated comprehensively at 250MHz frequency using 3.5fF output capacitor at the mentioned three supply voltages. The results of this experiment are listed in Table 3. Experimental results indicate that CNPTL (Proposed) once more has the shortest delay and lowest PDP compared to other designs at all supply voltages. It has also the lowest power consumption at all supply voltages.

Table 2. The results of the first experiment

V_{DD}(V)	0.5	0.65	0.8
	Delay (x10^{-12}s)		
CNPTL (Proposed)	**26.722**	**18.733**	**15.676**
TG-CMOS	238.44	90.097	56.272
CMOS-Bridge	591.62	199.95	130.20
Hybrid1	316.90	122.51	82.409
Hybrid2	309.41	116.80	82.048
CN3c2c	64.107	42.789	41.331
	Power (x10^{-7}W)		
CNPTL (Proposed)	1.2032	**1.7241**	**2.6224**
TG-CMOS	0.9715	1.9713	4.3871
CMOS-Bridge	0.8869	1.7560	3.2806
Hybrid1	**0.8861**	1.8298	3.9578
Hybrid2	0.9661	2.0086	4.4654
CN3c2c	2.1504	3.8263	5.5054
	PDP (x10^{-17}J)		
CNPTL (Proposed)	**0.3215**	**0.3229**	**0.4111**
TG-CMOS	2.3164	1.7761	2.4687
CMOS-Bridge	5.2475	3.5113	4.2714
Hybrid1	2.8080	2.2417	3.2616
Hybrid2	2.9892	2.3460	3.6638
CN3c2c	1.3786	1.6372	2.2754

In addition, to test the Full Adders as the building block of the larger structures, four cells of the proposed Full Adder are cascaded and simulated at 0.65V supply voltage. The delay, power consumption and PDP of this structure are 116ps, 0.19㎽ and 23aJ, respectively, whereas for instance these parameters are 427ps, 0.41㎽ and 174aJ, respectively for the four cascaded CMOS-Bridge cells. The results demonstrate that the proposed design can also operate with high performance in the larger structures.

To evaluate the driving capability of the circuits, they are simulated using various output load capacitors, ranged from 1.4fF up to 4.9fF, at 100MHz frequency and 0.65V supply voltage. The PDPs of the circuits are plotted versus load capacitor variation in Figure 5. According to the experimental results, the PDP of CNPTL (Proposed) is lower than the PDP of the other circuits for all output load capacitors.

Table 3. The results of the second experiment

V_{DD} (V)	0.5	0.65	0.8
Delay ($x10^{-12}$s)			
CNPTL (Proposed)	**41.055**	**28.059**	**24.04**
TG-CMOS	330.80	121.57	74.232
CMOS-Bridge	650.56	229.32	136.50
Hybrid1	388.28	168.06	116.58
Hybrid2	362.31	163.24	115.46
CN3c2c	73.677	51.235	39.738
Power ($x10^{-7}$W)			
CNPTL (Proposed)	**2.6733**	**4.1728**	**6.3074**
TG-CMOS	2.9707	5.2657	9.3550
CMOS-Bridge	2.7602	4.9340	8.5974
Hybrid1	2.7424	5.0029	8.8030
Hybrid2	2.8983	5.2486	9.4443
CN3c2c	4.0616	6.9714	18.471
PDP ($x10^{-17}$J)			
CNPTL (Proposed)	**1.0975**	**1.1708**	**1.5163**
TG-CMOS	9.8269	6.4017	6.9444
CMOS-Bridge	17.957	11.314	11.736
Hybrid1	10.648	8.4080	10.262
Hybrid2	10.501	8.5680	10.904
CN3c2c	2.9924	3.5718	7.3400

To evaluate the performance of the circuits at different frequencies, they are simulated at 100MHz to 500MHz and 0.65V supply voltage. The results of this experiment are plotted in Figure 6. It can be seen in Figure 6 that CNPTL has normal operation at different frequencies and can work reliably and with low power consumption at different frequencies. It can be also inferred from the results that CNPTL has the lowest average power consumption among the other cells at all frequencies and its power consumption increases slower, with the frequency increment, compared to the others.

To evaluate the immunity of the circuits to the ambient temperature variation, the circuits are also simulated in a vast range of temperatures from 0 ^{o}C to 70 ^{o}C at 0.65V supply voltage and at 100MHz frequency. The results of this experiment are plotted in Figure 7. It can be inferred from the experimental results that CNPTL has acceptable functionality and performance in a vast range of temperatures and it has the lowest PDP compared to other designs at all temperatures.

The driving capability of circuits is evaluated more precisely by simultaneous variations of both load capacitors and power supply voltage. The worst-case delay parameter situation occurs when low power supply voltages as well as high load capacitors are used. On the other hand, circuits consume much more power when the values of both power supply voltage and load capacitors increase. To examine this characteristic of the proposed circuit in detail, it is simulated at 100MHz using a large number of output load capacitors from 1.4fF to 5.6fF as well as a vast range of supply voltages from 0.8V to 0.4V. The results of this experiment are plotted in 3-D charts, which are shown in Figures 8 and 9. The results of these charts could be useful for better analyzing the driving capability of the proposed design. It can be inferred from the simulation results that the proposed Full Adder cell works with high performance at low voltages even with large load capacitors.

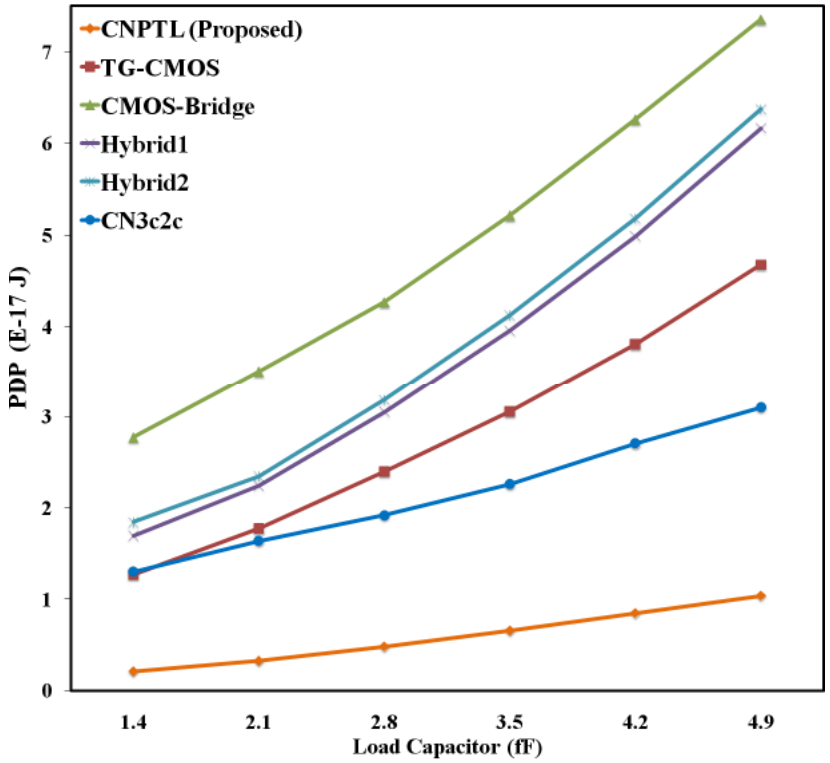

Figure 5. PDP of the circuits versus load capacitor variation

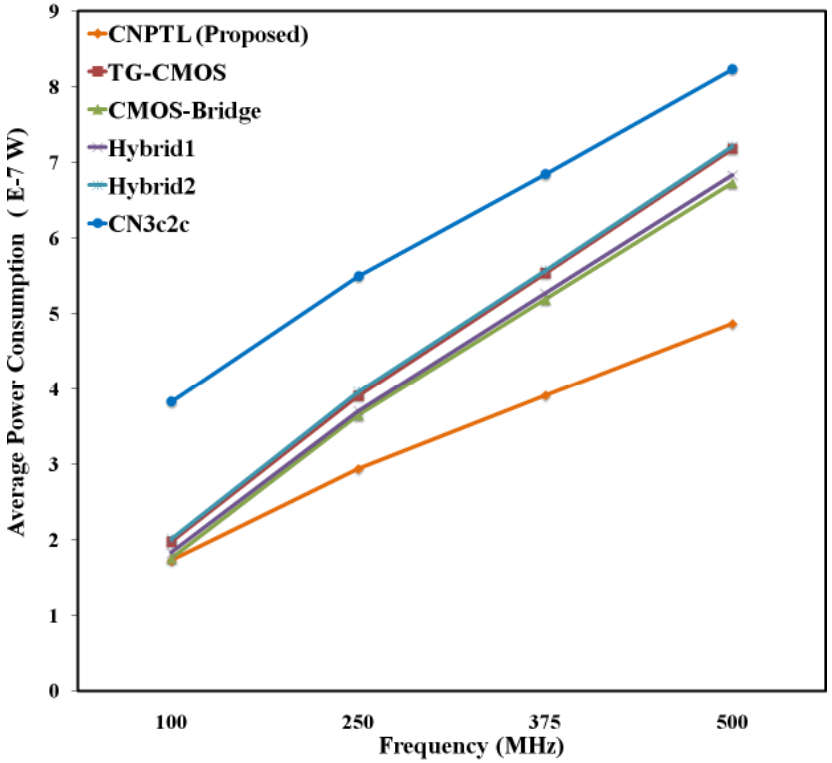

Figure 6. Power consumption of the circuits versus operating frequency

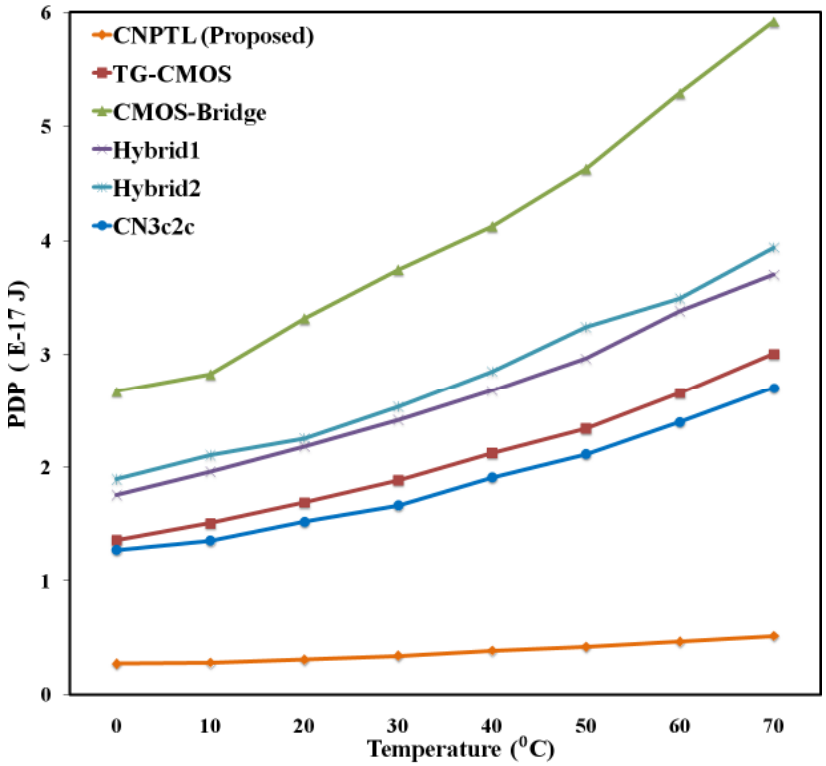

Figure 7. PDP of the circuits versus temperature variation

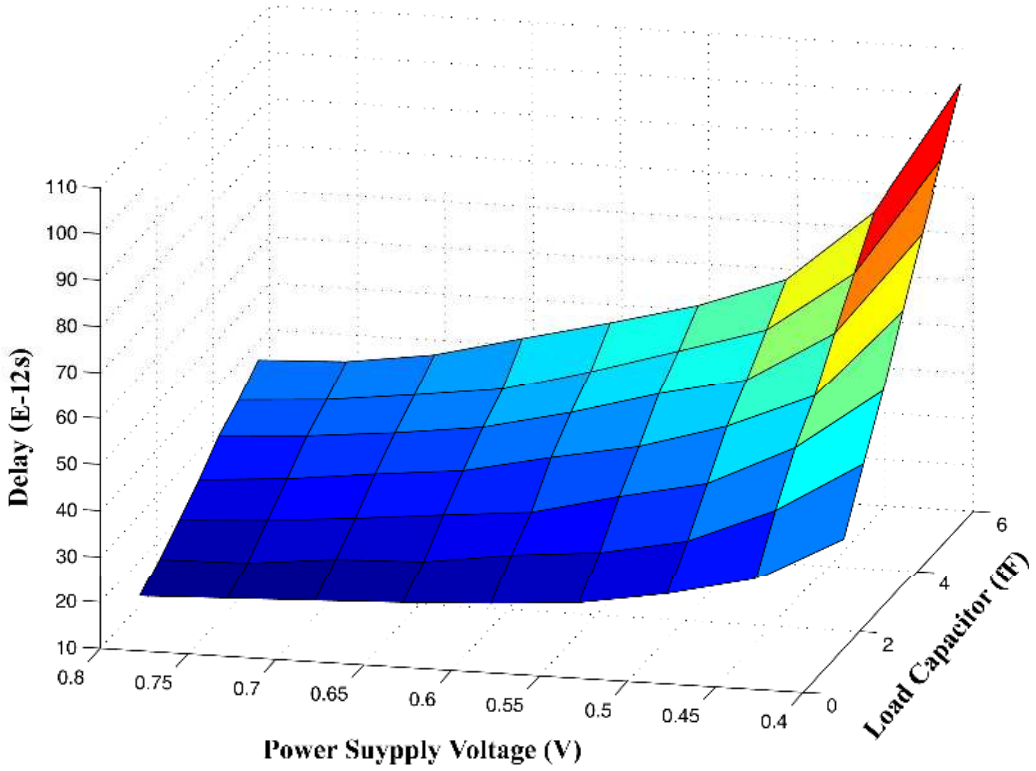

Figure 8. Delay of CNPTL (Proposed) versus supply voltage and load capacitor variations

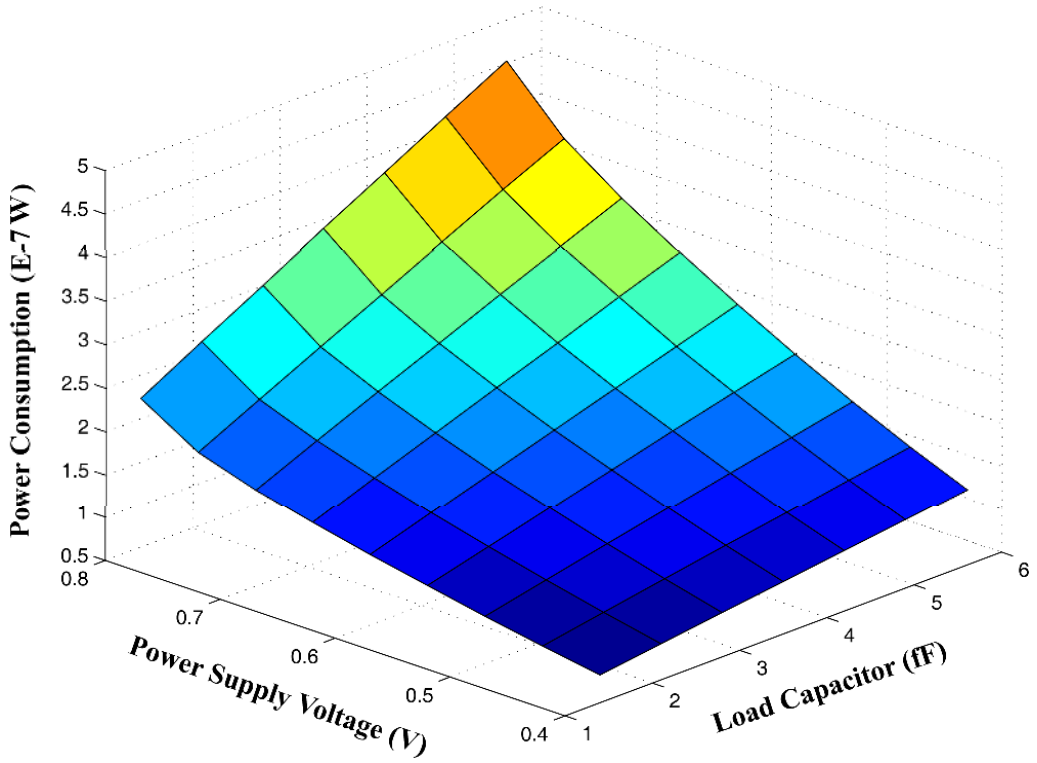

Figure 9. Power consumption of CNPTL (Proposed) versus supply voltage and load capacitor variations

4.3. Implementing MOSFET-based Full Adders using CNFETs

In this section two classical and state-of-the-art Full Adder cells, previously presented based on the MOSFET technology in the literature, i.e. TG-CMOS and Bridge-CMOS, are implemented using 32nm CNFET technology and their performance is evaluated. The diameters of the CNTs of these modified designs (TG-CNFET and CNFET-Bridge) are set as 1.487 nm. The simulation results of the proposed design and the CNFET versions of the TG and Bridge Full Adder cells are listed in Table 4.

Table 4. Simulation Results of the CNFET-based Full Adders (@ 250MHz and with 3.5fF load capacitor)

V_{DD} (V)	**0.5**	**0.65**
	Delay (x10^{-12}s)	
CNPTL (Proposed)	**41.055**	**28.059**
TG-CNFET	65.292	34.406
CNFET-Bridge	49.681	31.522
	Power (x10^{-7}W)	
CNPTL (Proposed)	2.8095	4.1728
TG-CNFET	**2.3204**	**3.8011**
CNFET-Bridge	2.6557	4.5283
	PDP (x10^{-17}J)	
CNPTL (Proposed)	**1.2691**	**1.1708**
TG-CNFET	1.5150	1.3078
CNFET-Bridge	1.3193	1.4274

Another performance parameter of the nanoscale circuits is robustness to the process variations. Random and systematic process variations are among the most major challenges regarding the design of nanoscale circuits. As the feature size of the devices scales down into the nanoranges, the process variation becomes a critical concern which negatively affects the speed, power consumption and reliability of the circuits. In this section, the delay, power consumption and PDP of the CNFET-based Full Adders are measured in the presence of process variations, i.e. deviations and mismatches in the diameter of the nanotubes of the carbon nanotube transistors. This variation has the most significant impact on the energy barrier of the CNFET devices and the performance of the CNFET-based circuits. For this purpose, Monte Carlo transient analysis with a reasonable number of 30 iterations for each simulation is conducted using the HSPICE simulator. The statistical significance of 30 iterations is quite high. If a circuit operates properly for all the 30 iterations, there is a 99% probability that over 80% of all the possible component values operate properly. Distribution of the diameters is assumed as Gaussian with 3-sigma distribution; a reasonable supposition for large numbers of fabricated CNTs (El Shabrawy et al. 2010).

The maximum variations of the delay, power consumption and PDP of the CNFET-based Full Adders versus CNT diameter variations, are demonstrated in Figures 10, 11 and 12, respectively. Considering the inaccuracy of fabrication techniques, a standard deviation from the mean value in the range of 0.04nm to 0.2nm is considered for each mean diameter value (Shahidipour et al. 2009). It can be concluded from the results that the performance of the proposed Full Adder is less sensitive to diameter variations, compared to TG-CNFET and CNFET-Bridge, specifically for the larger deviations.

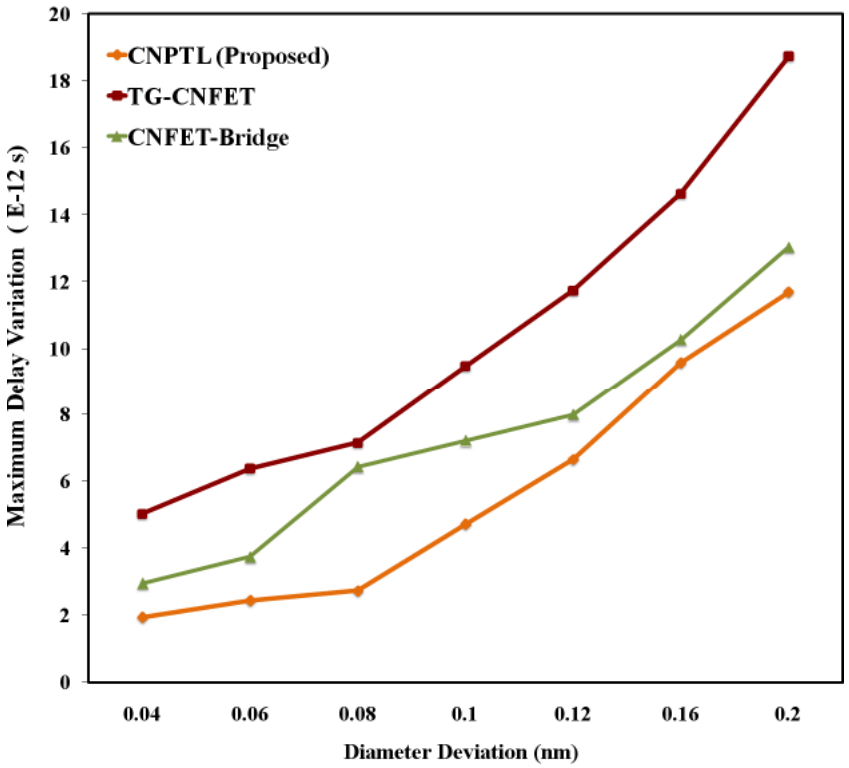

Figure 10. Delay variation of the circuits with respect to CNT diameter variations

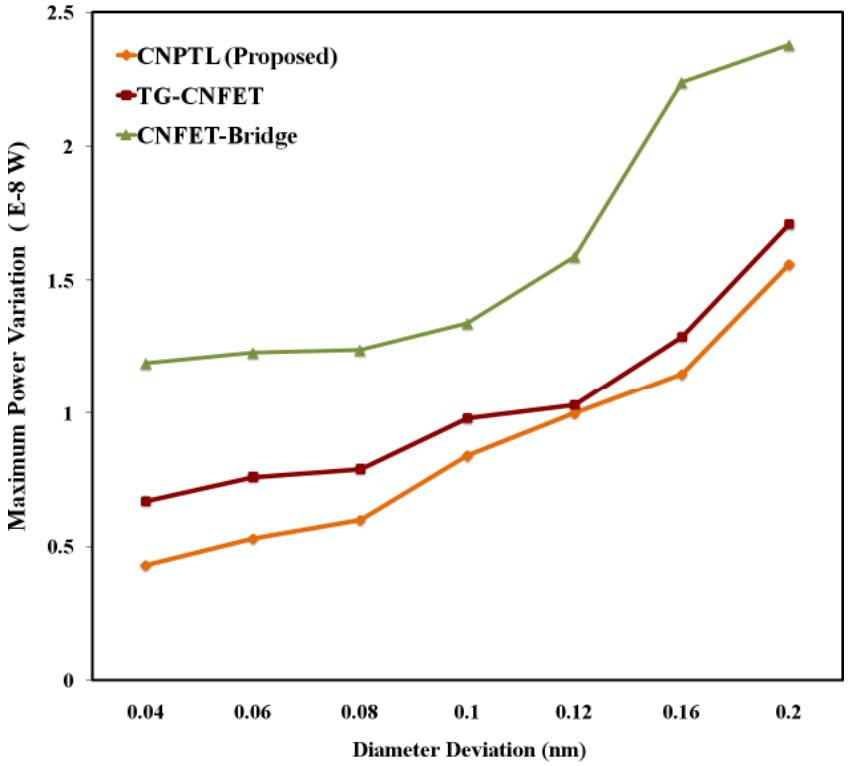

Figure 11. Power Consumption variation of the circuits with respect to CNT diameter variations

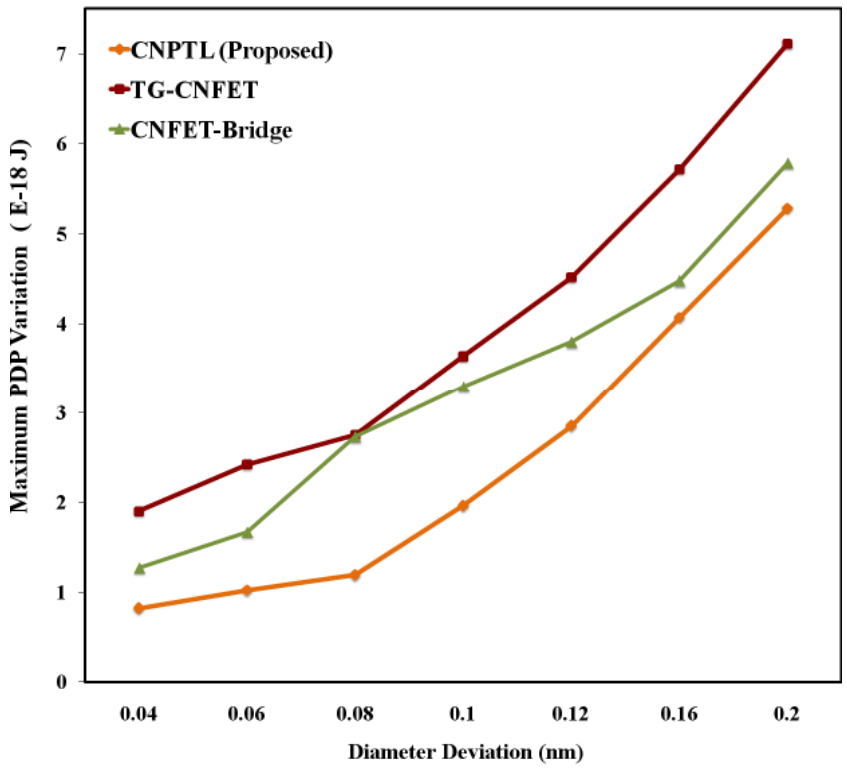

Figure 12. PDP variation of the circuits with respect to CNT diameter variations

5. Conclusion

In this paper, a high-speed and high-performance CNFET-based Full Adder cell for low-voltage applications has been proposed. The Sum and C_{out} generator modules of this Full Adder, which are fully symmetric and have the same hardware configurations, produce the Sum and C_{out} signals in a parallel manner. The great advantage of the proposed cell is its very short critical path, which consists of only two CNFETs. This leads to very short propagation delay and also makes this design appropriate for low-voltage applications. Results of the comprehensive simulations demonstrate considerable improvements in terms of delay, PDP and sensitivity to process variations in comparison with the other conventional and state-of-the-art 32-nm CMOS and CNFET-based Full Adder cells, in various situations.

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