Design and Analysis of a Novel Ultra-Low Power SRAM Bit-Cell at 45nm CMOS Technology for Bio-Medical Implants

JyotiYadav
VLSI Group, EECE
ITM University
Gurgaon, India

Neeraj Kr. Shukla
VLSI Group, EECE
ITM University
Gurgaon, India

Pulkit Bhatnagar
Design Platform/CCDS
STMicroelectronics
Greater Noida, India

Shilpi Birla
Department of EECE
SPS University
Udaipur, India

ABSTRACT
Bio-Implantable Microsystems such as the cardiac pacemaker, retinal and neural implant provides substitute for a missing biological part, support an impaired biological structure or even upgrade the existing biological system. These microsystems require ultra-low power miniature integrated circuit technology for long term reliable operation. For energy constraint applications like the implantable devices, the performance requirement are secondary factors while energy efficiency, low power, high density and high robustness are of primary concern. For low power operation, scaling the supply voltage into sub-threshold region is possible and is an effective technique for power reduction. Implantable devices require minimum energy consumption and prolonged battery lifetime. So these systems demand low leakage currents without sacrificing much on performance. In this work a new 9T MTIP3 SRAM Bit-Cell is proposed at 45nm CMOS technology using multi-threshold (MTCMOS) design technique. The static power saving in MTIP3 is 99.83% as compared to conventional 6T and 23.82% as compared to IP3 at VDD=0.8V. The dynamic power saving of read1 in MTIP3 is 86.37% as compared to 6T. The dynamic power saving of write1 in MTIP3 is 66.23% as compared to IP3. The access time of MTIP3 is 16.94% less than 6T. The energy saving during hold mode in MTIP3 is 99.5% as compared to 6T. Static Noise Margins are improved by 2.07% compared to IP3 at VDD =0.7V.

Keywords
6T SRAM, Bio-Implants, Microsystems, MTIP3 SRAM, Sub-threshold Region, Voltage Scaling.

1. INTRODUCTION
Due to technology scaling the current day IC's are becoming faster and denser. But faster circuits consume more power and hence reduces the battery lifetime of energy constraint applications like portable medical instruments and bio-implantable devices. These devices require minimum energy consumption and long battery lifetime. To improve the energy efficiency, supply voltage range (VDD) in these applications is placed near or below the threshold voltage (VT), known as the sub-threshold region [2]. SRAMs are one of the best choices for embedded memories in implantable applications as they are easily scalable in size and consume less power than register files and array of flip-flops. Sub-threshold memory designs are very attractive where less power consumption is the primary requirement and operating frequency is low (10-100KHz). In sub-threshold design, supply voltage is reduced below the device threshold voltage in order to achieve ultra-low power [1,3].

Bio Implantable SoC needs to consume less than 10A on average, if it needs to operate for 10 years on a single 1 A-hour battery. Meeting these power levels will open a large opportunity to diagnose and monitor various diseases. Ultra-low-power operation will reduce cost and size of these devices which leads to widespread use of portable medical devices, which in turn helps in prevention and cure of diseases [5].

The paper is organized as follows. In section II a brief background and review is presented of related research in field of bio-implantable memory design. Then we discuss the limitations of the conventional 6T SRAM operation in sub-threshold region in section III. Section IV proposes a novel 9T multi-threshold based SRAM bit-cell followed by the simulation, results and comparative study based on various performance parameters in section V. Finally, followed by conclusion in section VI.

2. LITERATUTE REVIEW
A wide variety of work is present in literature on Bio-Medical implants. Here is a glimpse of some bit-cell solutions for low power bio-medical embedded memory design. A number of power reduction techniques like sub-threshold, super-threshold, Multi-Vth, power gating, drowsy scheme, reverse body bias have been deployed in the past to reduce power and leakage for energy constraint applications like medical instruments and bio medical implants.

An integrated architecture level hardware for neural signal processing is designed by Narasimhan S. et.al [1] and an energy efficient ultra-low frequency sub threshold design using differential power reduction technique like clock gating and supply voltage gating is also proposed. High robustness, better yield, high energy efficiency is obtained at VDD=0.6V at frequency=33.33MHz at CMOS 70nm technology node.

Wang Bo et.al [2] proposed a multi-Vt, high energy efficiency better performance 8T SRAM at 65nm technology at VDD=0.4V using MTCMOS technique and various power reduction and performance boosting technique. This design using HVT, SVT, LVT transistors improves the energy efficiency by 33 times compared to SRAM using HVT devices.

Hashemian Maryam S. et.al [3] discussed a 6T super threshold design compared with 8T sub threshold design at 45nm CMOS technology node at VDD=1V and 0.4V respective. Supply gating technique is used in super threshold design to decrease static power consumption and higher thresholdtransistors are need to reduce leakage. The lowest energy obtained from the proposed design is 33.73 pJ at

highest frequency of 370 MHz. This technique reduces 27% SRAM energy without a huge impact on area and robustness.

Sense amplifier redundancy technique has been used to achieve low leakage, high density, high stability sub-Vt 8T SRAM by Verma N., et.al [4] at 65nm using VDD=0.35V. Buffered type read is used which ensures read stability and peripheral control enable sub-vt write, read without degrading cell's density.

SridharaSrinivasa R. et.al [5] presented an ultra-low power, better area, highly stable embedded processor platform chip at VDD=0.5V using fully differential sub threshold SRAM at 130nm CMOS technology consuming 5nW/Khz and retains data till 0.3V. Compared to 130nm 6T SRAM it employs a 2.5 times smaller bit cell, lower leakage and provide differential reads. A multipurpose header is used as write assist circuit that lower the supply voltage for the bit cell being written.

Sharifkhani M. et.al [6] improved the stability of cell in both read and write operation by controlling the cell access time and cell supply voltage. A 2048×20bit SRAM is implemented using 130nm CMOS technology at 100MHz and consumes less then 1mW in both read and write at 0.4V.

Kim Tea-H. et.al [7] enhanced the read and write performance better variation tolerance of 8T sub-threshold SRAM at 130nm CMOS at VDD=0.2V using reverse short channel effect. Long channel devices are used for the write access transistors and read path devices.

Schmitt trigger based 12T SRAM is reported by Chen Hu et.al [8] at 130nm CMOS using VDD=0.4V which is highly stable, more robust with 16% less power consumption and 45% better SNM compared to conventional 6T SRAM bit-cell. Structural change instead of sizing change is considered to enhance the robustness of the proposed design.

A small area DSP architecture is proposed by Marsam Eric D. et.al [9] at 180nm CMOS using VDD=1.2V at 3MHz frequency 1.79mW and occupies an area of 9.18mm2 with standby power consumption of 330µW.

Lee Shuenn Y. et.al [10] came out with a low power, wireless, small size, dual function monitoring and pacing implantable micro simulator SoC at 350nm CMOS technology node using VDD=1.2V having cardiac pacemaker. The power consumed by memory is 237nW. Rechargeable batteries with voltage 1.2V are used.

A 10T sub-threshold SRAM at 65nm is introduced by Calhounand Benton H. et.al [11] having low power, better energy efficient at VDD=0.4V for energy constraints applications like implantable systems. Separate read and write word lines are used. It provides dual advantage of minimum total energy consumption and minimum voltage at which SRAM can work in sub-threshold region.

3. LIMITATIONS OF CONVENTIONL 6T-SRAM BIT-CELL IN SUB-THRESHOLD DESIGNS

There are mainly four types of parametric failures which occurs in SRAM cells namely: read, write, access and hold failure. So, due consideration must be given to these factors while designing SRAM cells.

A. Read Failure

This failure occurs while reading the content of an SRAM cell. Suppose we are storing a value "0" at node Q and BLB is discharging through M5 and M1 as shown in Fig. 1. If the resistance of pull-down transistor M1 is higher than that of access transistor M5, a ripple voltage VQB is developed due to resistive divider formed by M1 and M5. If VQB exceeds the switching threshold of the inverter formed by M4 and M3, the cell state flips while reading. SNM (Static Noise Margin) is the amount of noise that the cell can bear before the state of the cell flips. Read SNM also comes down heavily because of the interference from the bit lines and flipping of the state of the cell. 6T SRAM can be operated at very low voltages provided that RSNM problem is removed. The read failure can be reduced by increasing the difference between the trip-point of the inverter associated with the node storing "1" and voltage rise at the node storing "0" [12].

B. Write Failure

During write, the value that has to be written into the cell is driven by bit lines. The word line WL goes high and the values are stored in the cell. Write failure occurs if the node storing "1" cannot be discharged through the access transistors while the wordline is on. The write ability of the cell fails due to increased variations and decreased signal levels. The write failure can be reduced by increasing the write access time and wordline on time which unfortunately makes SRAM slower [13].

C. Access Failure

This failure occurs if the voltage difference between the bitlines (BL and BLB) at the time when sense amplifier is fired remains below the offset voltage of the sense amplifier. Access failure occurs due to the reduction in current of bit-line discharging through the pass transistor and pull-down transistor. So a faster bitline discharge can be achieved by making the pull-down transistor stronger so as to reduce the resistance in discharge path. This leads to larger cell area which is not good for high density SRAMs.

D. Hold Failure

The hold failure occurs due to high-leakage in the path of pull-down NMOS transistors connected to the node storing "1". Due to technology scaling because of high leakage of the pull-down transistor, the node storing "1" reduces below VDD. If that voltage becomes lower than the trip-point of the inverter storing "0" flips the state of the cell in the hold mode. Hold failure can be avoided by reducing leakage in standby mode using high-Vth pull-down transistors. But it leads to increase in read delay.

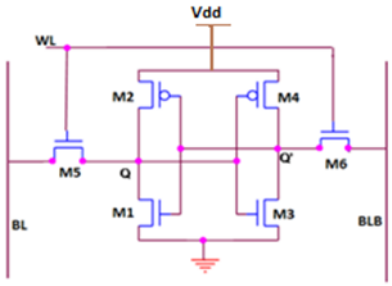


Fig. 1: Conventional 6T SRAM Schematic

With ever increasing need for implantable devices such as pacemakers, cochlear, retinal, dental implant for treatment of various diseases like sleep apnea, epilepsy, gastro intestinal disorder, auto immune disorders, we are facing technical challenges and need to reduce size, weight and power. We can explore design space and propose optimal design of embedded memory for bio implant applications for better area, high robustness, energy reduction and improved yield.

4. PROPOSED MTIP3 SRAM BIT-CELL

In [14], an IP3 SRAM Bit–Cell structure has been presented by Rakesh Kumar Singh et al. which uses drowsy scheme and pMOS stacking with ground. This cell reduces the power consumption (active, leakage, standby) with the small area penalty. The stack transistor is used one per row in the memory array so that area penalty of this transistor can be reduced.

We propose the next generation multiple threshold IP3 (MTIP3) cell as shown in fig.2, for ultra-low power applications such as those demanded in bio-medical devices. In this technique critical paths are preferred to be designed using lower-Vth devices while higher-Vth devices are favored in non-critical paths. The higher-Vth devices in non-critical paths reduce the leakage current and the lower-Vth devices maintain the required performance. MTCMOS technology has been usually adopted to achieve balanced design parameters such as cell stability, performance, write margin. MTCMOS provides circuit designers with more opportunities to optimize circuits in performance, power and energy. In SRAM design, read paths are considered as critical paths, limiting overall performance. Write paths are non-critical due to the faster operation speed than read paths. Therefore, lower-Vth devices have to be incorporated in read operation, and higher-Vth devices are employed in write paths. However, as supply voltage decreases, the write speed with higher-Vth devices degrades faster than the read speed with lower-Vth, eventually making the write paths critical. In this case, overall energy consumption needs to be carefully estimated since the degraded critical path delay from the write operation becomes more significant.

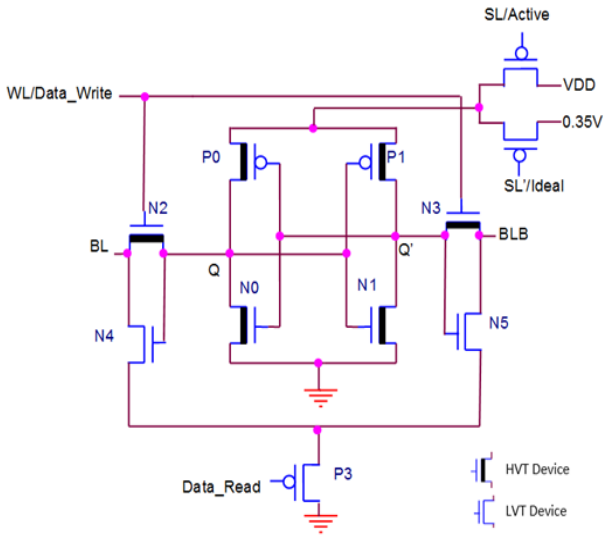


Fig. 2: Proposed MTIP3 SRAM Schematic

The MTIP3 SRAM cell structure comprises of two memory sub-cells i) the write sub-cell having Pull Down Transistors N0-N1, Access Transistors N2-N3 and Pull up Transistors P0-P1 is taken as high-Vth devices ii) the read-sub cell having Read Access Transistors N4-N5 and a Gated pMOS transistor P3 is taken as low-Vth devices. The write sub-cell performs the twin function of writing data into memory and other holding the data into the memory as described in [14].

Write mode- SL/Active is made 0 to supply voltage Vdd at the cell . To activate N2 and N3 WL is made 1 and SL'/Ideal is made 0 and Data_Read is given HIGH to cut-off the lower sub-cell P3 from the ground by deactivating pMOS. The data to be stored in the cell is applied at the BL and BLB to write the data into the upper sub-cell. The data is hold in the cell by making WL= 0. The access transistors N2 and N3 along with BL's are cut off from the upper sub-cell. This data is also feasible at the gates of the nMOS transistors N4 and N5. Now BL and BLB are given as HIGH. This will latch the data in the first memory sub-cell. Data_Read is kept HIGH so as the lower sub-cell is cut-off from the gated pMOS transistor P3.

Read mode- To apply drowsy supply voltage Vdd = 0.35V at the upper sub-cell, SL/Active is made 1 and SL'/Ideal is made 0. To deactivate the nMOS transistors N2 and N3 WL is given 0. Now the data is held in the cell by disconnecting the upper sub-cell from BL's. To connect the lower sub-cell to the ground for normal read operation activate pMOS P3 by applying Data_Read = 0. The lower sub-cell now is in the data read mode. The data is retained in the cell by applying low-power drowsy voltage Vdd=0.35V in the upper sub-cell. Thecells' stability is improved as a result of cells' improved read performance when the stored data at Q and Q' is not disrupted at the upper sub-cell. BL and BLB are made HIGH to read the data from the cell and the stored data can be accessed through the sense amplifier. This design can work at ultra-low voltage (Vdd=0.8V and Vdd=0.35V) and attain high stability i.e. improved noise margins, better energy efficiency, less access time.

Standby mode-To apply drowsy voltage Vdd = 0.35V, SL/Active is given 1 and SL'/Ideal is given 0 at the cell. This results in reduction of standby power of the cell. To disconnect the access transistors from the memory cell WL is applied LOW. To reduce the standby leakage apply Data_Read = 1 so as to keep the read sub-cell disconnected from the ground. The upper sub-cell is kept at drowsy voltage Vdd = 0.35V to retain the data in the cell. The lower sub-cell is also disconnected from the ground through P3 transistor. This in turn reduce the standby power leakage and the sub-threshold leakage current of the cell.

This technique can generate excessively slower write operation than read operation if Vth of the devices in the write paths is too high compared to that of the devices in the read ports. However, it leads to increase in process complexity.

5. SIMULATION RESULTS

The design and simulation work for 6T-SRAM, IP3-SRAM and proposed MTIP3-SRAM topologies have been carried-out with Cadence Virtuoso Environment using Spectre simulator to analyze the power consumption and other performance parameters at 45nm CMOS technology at temperature of 27oC for VDD=0.6V to 1.0V. The various performance parameters are discussed below.

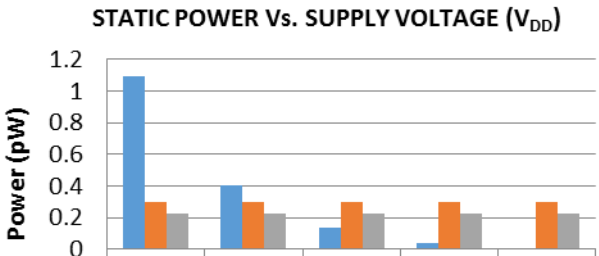
A. Static Power

In the standby mode the power dissipation is due to the standby leakage current. The static power of a CMOS circuit is determined by the leakage current through each transistor in off-state. MTIP3 is showing 99.83% better power saving as compared to 6T and 23.82% better power saving as compared to IP3 SRAM bit-cell at VDD=0.8V. Static power analysis of 6T vs IP3 vs MTIP3 is shown in fig. 3.

B. Dynamic Power

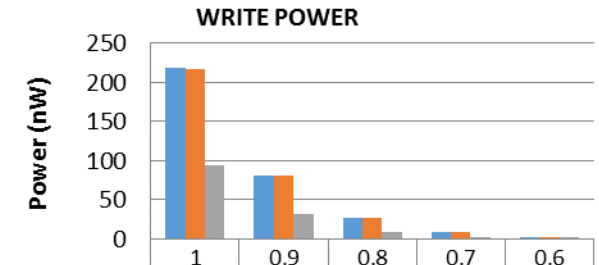
There are two components of dynamic power dissipation. One comes from switching power due to charging and discharging of load capacitance. The other is short circuit power due to nonzero rise and fall time of input waveforms. In case of write 1, MTIP3 is showing 65.83% better power saving as

compared to 6T and 66.23% better power saving as compared to IP3 SRAM Bit-Cell. While in case of read 1, MTIP3 is showing 86.37% better power saving as compared to 6T but is losing by 8.67% as compared to IP3 SRAM bit-cell at VDD=0.8V. Dynamic power analysis of 6T vs IP3 vs MTIP3 is shown in fig. 4 and fig. 5.



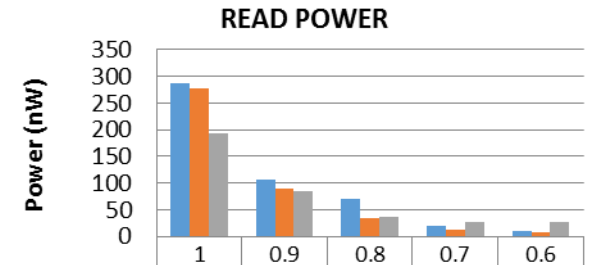
	1	0.9	0.8	0.7	0.6
6T	1.0938	0.40419	0.1353	0.03941	0.00963
IP3	0.298	0.298	0.298	0.298	0.298
MTIP3	0.227	0.227	0.227	0.227	0.227

Fig. 3: Static Power comparison 6T vs IP3 vs MTIP3



	1	0.9	0.8	0.7	0.6
6T(nW)	219.3	81.32	27.38	8.158	2.496
IP3(nW)	217.3	80.8	27.48	8.323	2.26
MTIP3(nW)	94.66	31.35	9.355	1.529	0.87

Fig. 4: Write Power comparison 6T vs IP3 vs MTIP3

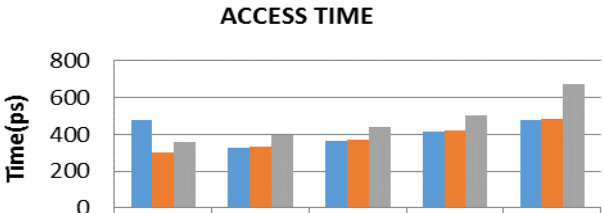


	1	0.9	0.8	0.7	0.6
6T(nW)	287.5	105.5	69.2	20.68	10.01
IP3(nW)	278.2	88.85	33.49	12.1	6.42
MTIP3(nW)	193.9	83.98	36.67	26.42	26.95

Fig. 5: Read power comparison 6T vs IP3 vs MTIP3

C. Access Time

It is the time required by a processor to access data and write data to and from memory. The minimum amount of time required to read a bit of data from the memory measured with respect to initial rising edge of clock in the SRAM read operation. MTIP3 is showing 16.94% less access time as compared to 6T but it is losing by 15.96% as compared to IP3 SRAM bit-cell. Access time analysis of 6T vs IP3 vs MTIP3 is shown in fig. 6.



	1	0.9	0.8	0.7	0.6
6T	479.5	327.7	365.7	413.3	480
IP3	299.5	331.7	370	418.7	485.8
MTIP3	356.8	394.1	440.3	501.4	675

Fig. 6: Access Time comparison 6T vs IP3 vs MTIP3

D. Stability

Stability of SRAM is decreasing with technology scaling, accurate estimation of data storage stability is an important step in SRAM design and test flows. Stability occupies a central role in SRAM operations. Stability in standby modes implies proper data retention, noise injection, and stability in read and write implies to non-destructive read and successful write.

a) Static Noise Margin

Input voltage to output voltage transfer characteristics can be used to define Noise Margin. Static Noise Margin (SNM) is the maximum amount of noise signals that a circuit can tolerate which does not change its initial state. Static Noise Margin of SRAM is the maximum amount of voltage noise that can be tolerated at cross inverters M1-M2 and M3-M4 output nodes without flipping state of cell. In case of hold, MTIP3 is showing comparable noise margins with respect to 6T but it is improving by 2.07% as compared to IP3 SRAM Bit-Cell at Vdd=0.7V. The SNM analysis of 6T vs IP3 vs MTIP3 is shown in fig. 7 and fig. 8.

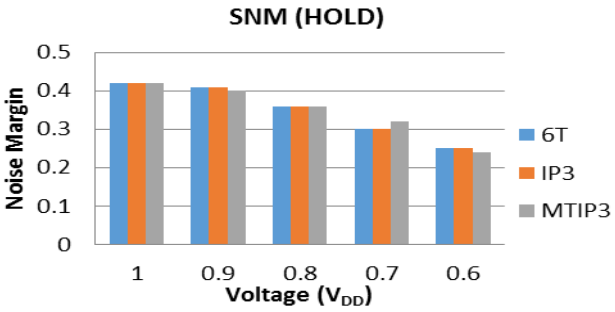


Fig. 7: SNM (Hold) comparison 6T vs IP3 vs MTIP3

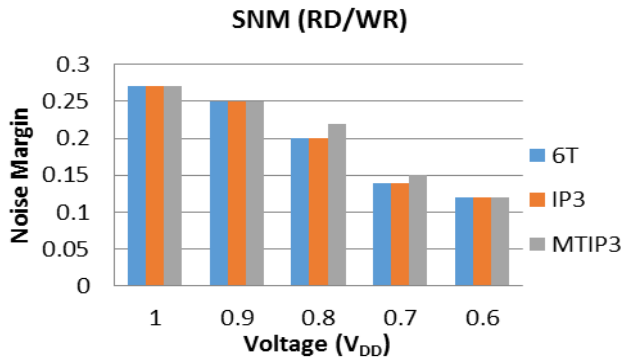


Fig. 8: SNM (RD/WR) comparison 6T vs IP3 vs MTIP3

b) N-Curve Analysis

To predict the overall cell stability and ability (read and write) N-curve is the latest developed technique which is becoming popular now a days. N curve analysis for stability defines static voltage noise margin (SVNM), static current noise margin (SINM), write trip voltage (WTV) and write trip current (WTI). In case of SVNM, MTIP3 is showing 0.5% better noise margins with respect to 6T and it is improving by 0.31% as compared to IP3 SRAM bit-cell. In case of SINM, MTIP3 is loosing by 57.531% with respect to 6T and 57.8% as compared to IP3 SRAM bit-cell. In case of WTV, MTIP3 is improving by 1% with respect to IP3 and loosing by 1% as compared to 6T SRAM. In case of WTI, MTIP3 SRAM Bit-Cell are compared. MTIP3 is loosing by 47.57% with respect to IP3 SRAM bit-cell. The N curve analysis of 6T vs IP3 vs MTIP3 is shown in fig. 9, fig. 10, fig. 11, and fig. 12.

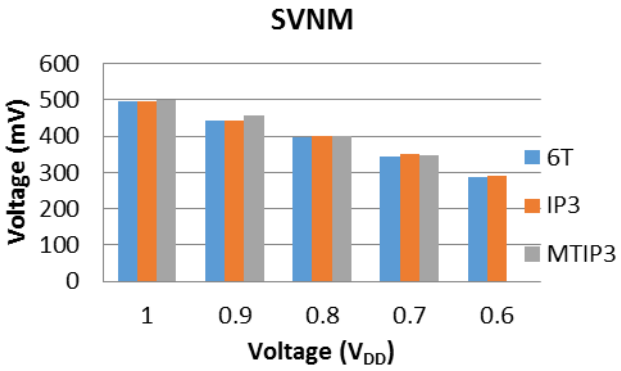


Fig. 9: SVNM comparison 6T vs IP3 vs MTIP3

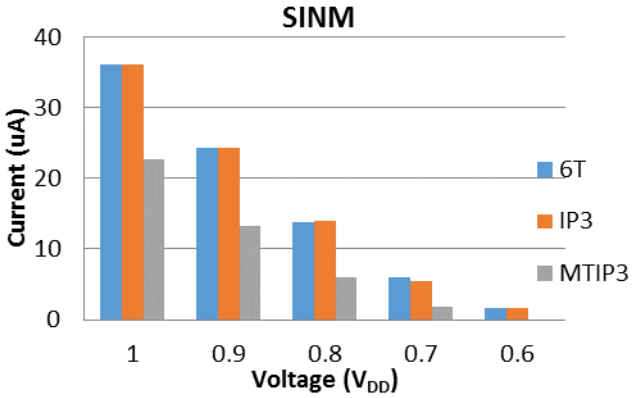


Fig. 10: SINM comparison 6T vs IP3 vs MTIP3

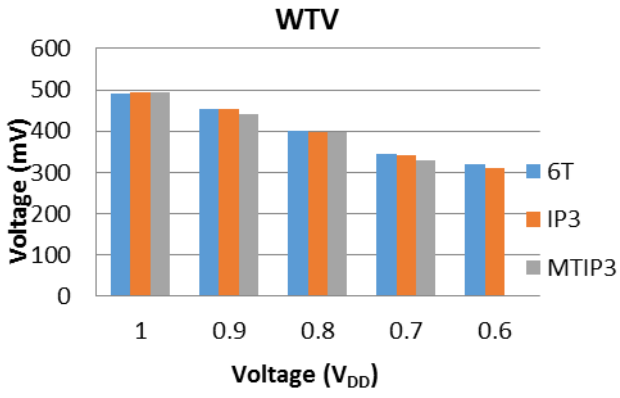


Fig. 11: WTV comparison 6T vs IP3 vs MTIP3

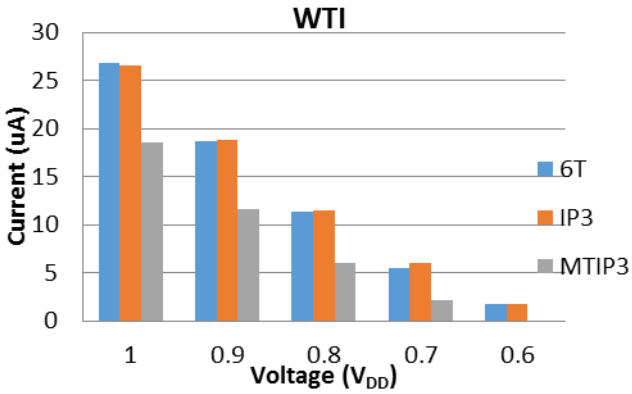


Fig. 12: WTI comparison 6T vs IP3 vs MTIP3

E. Energy

Energy consumption of an SRAM can be divided into two parts i) switching energy also called as dynamic energy ii) leakage energy also called as static energy. The correlation of power and performance is used to determine minimum energy point. The energy leakage and write comparison of 6T vs IP3 vs MTIP3 is shown in fig. 13 and fig. 14.

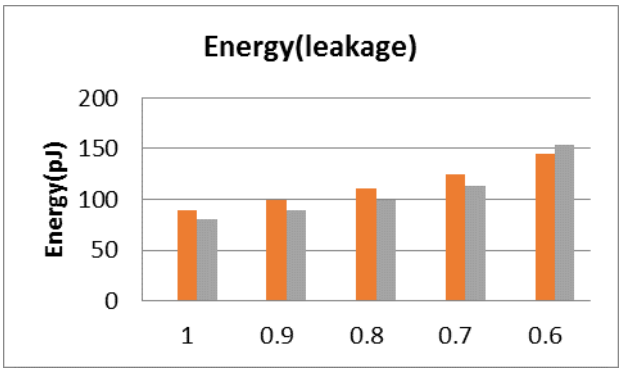


Fig. 13: Energy (leakage) comparison 6T vs IP3 vs MTIP3

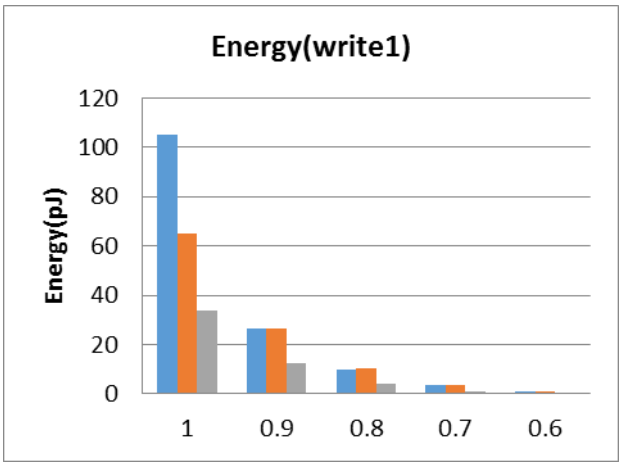


Fig. 14: Energy (write) comparison 6T vs IP3 vs MTIP3

6. COMPARISON

Voltage scaling is an effective method for minimizing the power consumption of SRAMs. In modern ICs, SRAMs occupies a significant portion of the total area and power, so the resulting total power savings are very significant. As we know conventional 6T SRAMs fail to operate at very low voltages in sub-threshold region because of reduced signal levels. A novel 9T MTIP3 SRAM Bit-Cell design has been

proposed in this work. The static power saving in MTIP3 is 99.83% as compared to 6T and 23.82% as compared to IP3 at VDD=0.8V.The dynamic power saving of write1 in MTIP3 is 66.23% as compared to IP3. The dynamic power saving of read1 in MTIP3 is 86.37% as compared to 6T. The access time of MTIP3 is 16.94% less than 6T but it is loosing by 15.96% as compared to IP3 SRAM bit-cell. Static Noise Margins are improving by 2.07% compared to IP3 at VDD =0.7V. N curve analysis for stability defines static voltage noise margin (SVNM), static current noise margin (SINM), write trip voltage (WTV) and write trip current (WTI). In case of SVNM, MTIP3 is showing 0.5% better noise margins with respect to 6T and it is improving by 0.31% as compared to IP3 SRAM bit-cell. In case of SINM, MTIP3 is loosing by 57.531% with respect to 6T and 57.8% as compared to IP3 SRAM bit-cell. In case of WTV, MTIP3 is improving by 1% with respect to IP3 and loosing by 1% as compared to 6T SRAM. In case of WTI, MTIP3 SRAM Bit-Cell are compared. MTIP3 is loosing by 47.57% with respect to IP3 SRAM bit-cell. The energy saving during hold mode in MTIP3 is 99.5% as compared to 6T. In case of write1, MTIP3 is loosing by 58.2% with respect to 6T SRAM Bit-Cell. In case of read1, MTIP3 is improving by 23.18% with respect to IP3 SRAM bit-cell.

Thus, simultaneous reduction of leakage current and better performance is achieved. The proposed design can work at ultra-low voltage (VDD=0.8V and VDD=0.35V). However, this technique can generate excessively slower write operation than read operation if Vth of the devices in the write paths is too high compared to that of the devices in the read ports. It also leads to increase in process complexity.

7. ACKNOWLEDGEMENT

The authors are grateful to their organization for their help and support to carry out this work.

8. REFERENCES

[1] Narasimhan S., Chiel H.J., and BhuniaSwarup, "Ultra-Low-Power and Robust Digital-Signal-Processing Hardware for Implantable Neural Interface Microsystems," IEEE Trans. Biomed. Circuits Syst., vol. 5, No. 2, pp. 169-178, Apr. 2011.

[2] Wang Bo, Zhou Jun, and Kim Tony T., "Maximization of SRAM Energy Efficiency Utilizing MTCMOS Technology," 4th Asia Symp. 2012 IEEE Quality Electronic Design Conf., Penang, pp. 35-40, 10-11 July 2012.

[3] Hashemian Maryam S.., and BhuniaSwarup, "Ultralow-Power and Robust Embedded Memory for Bioimplantable Microsystems," IEEE Computer Society, 26th Int. Conf. on VLSI Design and 12th Int. Conf. on Embedded Systems, Pune India, pp. 66-71, 5-10 Jan. 2013.

[4] Verma N., and Chandrakasan A.P., "A 256 kb 65 nm 8T Subthreshold SRAM Employing Sense-Amplifier Redundancy," IEEE J. Solid-State Circuits, vol. 43, No. 1, pp. 141-149, Jan. 2008.

[5] SridharaSrinivasa R., DiRenzo Michael, Lingam Srinivas, Lee Seok-Jun, BlázquezRaúl, Mxey Jay, GhanemSamer, Lee Yu-Hung, Abdallah Rami, Singh Prashant, and Goel Manish, "Microwatt Embedded Processor Platform for Medical System-on-Chip Applications," IEEE J. Solid-State Circuits, vol. 46, No. 4, pp. 721-730, Apr. 2011.

[6] Sharifkhani Mohammad and SachdevManoj, "An Energy Efficient 40 Kb SRAM Module With Extended Read/Write Noise Margin in 0.13 um CMOS," IEEE J. Solid-State Circuits., vol. 44, No. 2, pp. 620-630, Feb 2009.

[7] Kim Tea-Hyoung, Liu J., and Kim C.H., "An 8T subthreshold SRAM Cell Utilizing Reverse Short Channel Effect for Write Margin and Read Performance Improvement," IEEE Custom Integrated Circuits Conf., San Jose, pp. 241-244,16-19 Sept. 2007.

[8] Chen Hu, Jun Yang, Meng Zhang and Xiulong Wu, "A 12T subthreshold SRAM Bit-cell for Medical Device Application," Int. Cyber-Enabled Dis-tributed Computing and Knowledge Discovery Conf., Beijing, pp. 540-543, 10-12 Oct. 2011.

[9] Marsam Eric D., KubbaSundus, carichner Gordon A., "A DSP Algo for cochlear implants," Giraud B., Amara A., and Vladimirescu A.," Int. Symp. 2006 IEEE Circuits and Systems Conf., Island of Kos, pp. 657-660, 21-24 May 2006.

[10] Lee ShuennYuh, Su Mario Yu Cheng, , Liang Ming-Chun, Chen You-Yin, Hsieh Cheng-Han, Yang Chung-Min, Lai Hsin-Yi, Jou-Wei, and Fang, Qiang, "A Programmable Implantable MicrostimulatorSoCWithWireless Telemetry: Application in Closed-Loop Endocardial Stimulation for Cardiac Pacemaker," IEEE Trans. on Bio-Medical Circuits and Syst., vol. 5, No. 6, pp. 511-522, Dec. 2011.

[11] Calhounand Benton Highsmith and ChandrakasanAnantha P., "A 256-kb 65-nm Sub-threshold SRAM Design for Ultra-Low-Voltage Operation," IEEE J. Solid-State Circuits, vol. 42, No. 3, pp. 680-688, Mar. 2007.

[12] RamaniRamnathArun, and Choi Ken, "A Novel 9T SRAM Design in Sub-Threshold Region," IEEE Electro/Information Technology Int. Conf., Mankato US, pp. 1-6, 15-17 May 2011.

[13] Islam Aminul, Hassan. Mohd., "Variability Analysis of 6T and 7T SRAM Cell In Sub-45nm Technology," IIUM Engineering Journal, vol. 12, No. 1, pp 13-29, 2011.

[14] Singh R., Pattanaik M., and Shukla N., "Characterization of a Novel Low-Power SRAM Bit-Cell Structure at Deep Sub-Micron CMOS Technology for Multimedia Applications," Scientific Research, vol. 3 No. 1, pp. 23-28, Jan 2012.