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Design and Analysis of Low Power and High SFDR Direct Digital Frequency Synthesizer

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ABSTRACT Due to the advantages of fast frequency shifting, continuous phase shifting, fine frequency resolution, large bandwidth, and excellent spectral purity, the direct digital frequency synthesis (DDFS) technique is attracting more attention than ever before. Although the DDFS suffer from high power consumption, recent researches on the development of the low power DDFS (LP-DDFS) increases the feasibility of applying the DDFS to portable devices. To further accelerate the use of LP-DDFS, a new LP-DDFS design to significantly improve power efficiency is proposed and analyzed in this paper. In the new design, the dominant spur by truncation errors causing performance degradation has been also thoroughly considered. Since the existing dithering techniques for the truncation error problems can cause the additional performance degradation due to the side effects such as frequency offset and SNDR deterioration, an enhanced dithering technique is also proposed in this paper. The proposed technique includes a frequency compensation circuit and thus minimizes the truncation errors in the LP-DDFS with the minimal additional power consumption and SNDR degradation. Both theoretical and experimental analysis are conducted to verify the proposed design, where a prototype chip is fabricated and measured.

INDEX TERMS Direct digital frequency synthesizer (DDFS/DDS), dithering scheme, high spurious-free dynamic range (SFDR), low power design, Phase accumulator (PACC), pseudo-random binary sequence (PRBS).

I. INTRODUCTION

Since waveform generators are essential devices for many electronic devices, the demand for advanced waveform generators that can more accurately generate and control analog waveforms of various frequencies and profiles has been rapidly increasing. Typical examples are the agile low-phase noise variable-frequency source with excellent spurious performance for communications devices and the convenient and simple frequency generation for measuring instruments. Further, small and low power waveform generators have recently become the most important part in various portable devices. Since there are many different waveform generation techniques varied from phase locked loop (PLL)-based methods to ultra-high frequency synthesis, circuit designers can choose the most suitable method depending on their target applications. Among the various methods, direct digital frequency synthesis (DDFS) is one of the representative waveform generation technique having fast frequency switching, continuous phase switching, fine frequency resolution, large bandwidth, and excellent spectral purity. Owing to these advantages, the DDFS method has been used in a wide range of applications such as radar, military equipment, medical devices, and aircraft [1]–[3]. However, the DDFS method has the critical drawback in high power consumption, causing the difficulty of using it in portable (battery-powered) devices [4], [5]. Since the DDFS conventionally uses read-only-memory (ROM) for signal generation, the required ROM size gets also significantly increased as the performance requirements of the synthesizer increases. As a result,

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the increase in power consumption becomes unavoidable. To resolve this problem, active researches on the DDFS method and its hardware design have been steadily conducted, and the recent research results show that the power consumption level of DDFS can be lowered to the usage in portable devices. For example, the recent work [4] of the low power direct digital frequency synthesizer (LP-DDFS) consumes less than 130mW, which is much smaller than common mobile AP cores. Having the potential for lowering additional power consumption from the previous LP-DDFS [4], a new advanced LP-DDFS architecture is proposed in this paper. In the new LP-DDFS, CML-based circuit design is replaced with CMOS-based circuit through the theoretical and practical analysis of the dynamic and static power characteristics. Further, the proposed design is optimized by eliminating redundant logic and unnecessary blocks from the previous LP-DDFS and lastly fabricated as a prototype chip using 65nm CMOS process.

However, since truncation errors by the pipelined phase accumulator integrated in the proposed LP-DDFS cause dominant spurs degrading spurious free dynamic range (SFDR) performance, several state-of-the-art dithering methods [6]–[9] known as the most effective solution for reducing truncation errors are also analyzed with the proposed LD-DDFS. Although the dominant spurs caused by the truncation error appear as a white noise with the currently available dithering methods, frequency offset and degradation of signal-to-noise and distortion ratio (SNDR) are found to be problems. The frequency offset problem is due to the average of pseudo-random binary sequence (PRBS) affected by the length of itself, while the SNDR degrades because of the spectral leakage induced by the random signal injection. Therefore, to overcome the limitation of the current dithering methods, a new dithering technique based on frequency compensation to sufficiently suppress the truncated errors with the minimal additional power consumption and SNDR degradation is also proposed in this paper. In Section II the previous DDFS designs are reviewed and the proposed DDFS design is presented. Then, the detailed analysis of the dominant spur in the LP-DDFS is presented in Section III. Further, in Section IV and V, the proposed dithering method is presented and verified through both the simulation and experiment. It should be noted that the Section V primarily focuses on the experimental work regarding to the proposed dithering method, while the other sections mainly describe the proposed LP-DDFS architecture and new observations. Finally, Section VI concludes the paper.

II. DESIGN OF THE LOW POWER DDFS

A. CONVENTIONAL DDFS METHOD AND PREVIOUS LP-DDFS METHODS

FIGURE 1 shows the block diagram of a conventional DDFS consisting of a phase accumulator (PACC), phase-to-amplitude mapper (P2AM), and digital to analog converter (DAC). The PACC is used to generate phase information

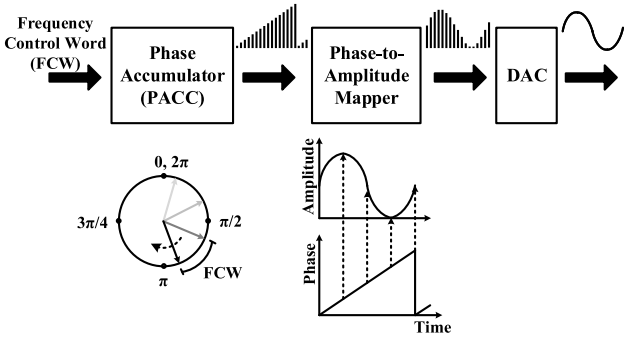

FIGURE 1. Block diagram of a conventional DDFS.

by accumulating digital input called the frequency control word (FCW). The P2AM is responsible for mapping the accumulated phase to the corresponding amplitude. The DAC converts digital sine wave into analog sine wave.

The PACC plays a key role in controlling the output frequency of the DDFS, F_{out}. As the digital output of the PACC overflows every 2π, F_{out} can be easily controlled by adjusting the FCW as follows

$$F_{out} = \frac{F_{clk} \times FCW}{2^N}, \tag{1}$$

where F_{clk} denotes the clock frequency. That is, the PACC produces the desired F_{out} according to the FCW, where the larger FCW accumulates the phase faster and the output frequency becomes higher. Since the original PACC structure consists of an N-bit adder with N-bit flip-flops (FFs) limiting the speed, the recent PACC designs including the proposed architecture usually adopts pipelining method instead.

The conventional DDFS uses a digital mapper for the P2AM as shown in FIGURE 2 (a) to convert the phase accumulated in the PACC into an amplitude and pass it to the DAC. The digital mapper is typically implemented with regular or compressed ROM. However, since the required ROM size has been increased exponentially with the evolution of DDFS, the required DDFS power consumption gets also significantly increased. As the P2AM became the

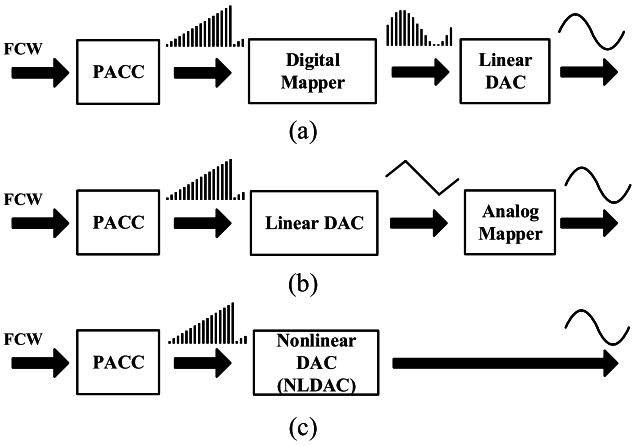

FIGURE 2. (a) DDFS using digital mapping block. (b) Using analog mapping block. (c) NLDAC-based DDFS.

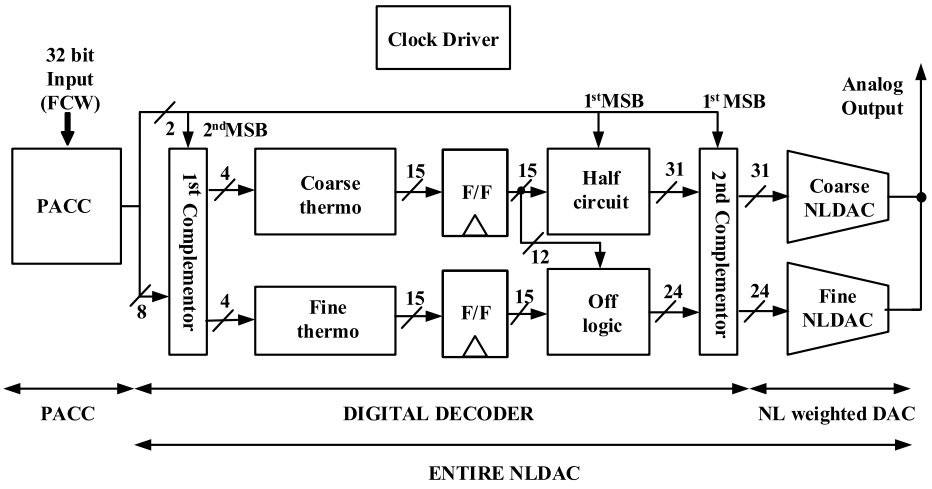

FIGURE 3. Block diagram of the proposed LP-DDFS.

most power-consuming block in the DDFS, previous studies on the LP-DDFS have focused primarily on reducing the power consumption of the P2AM. Although the attempts to replace the traditional ROM-based designs [10]–[16], including CORDIC [15]–[19], polynomials, and quadratic-based designs [20]–[23] have been suggested, they suffer from high design complexity and still power overhead. Then, another approaches for developing analog mapper to replace the digital mapper have been proposed [24]–[26]. In this new topology using the analog mapping block as illustrated in FIGURE 2 (b), the P2A conversion is performed through the post-DAC analog method, resulting in a significant power reduction. However, this approach undergoes a serious drawback of limited dynamic performance due to power, voltage, and temperature (PVT) variations.

More recently, a new approach to replace the P2AM and linear DAC with a sign weighted nonlinear DAC (NLDAC) have been proposed to achieve both low power and high performance [4], [27], [28]. FIGURE 2 (c) shows the basic structure of the NLDAC-based DDFS, where a nonlinear sign weighted DAC directly converts the output of the PACC to the desired sign wave. Because the NLDAC can be simply implemented with a thermometer decoder (decoding logic) and a nonlinear weighted DAC (current sources), its power consumption and design complexity are much less than the digital and analog mappers in the previous DDFS structures. From the former NLDAC-based DDFS proposed by the author of this paper [4], the design technique to significantly simplify the decoding logic in the NLDAC has been introduced. More specifically, the general operation of the NLDAC that divides the current source into coarse and fine phases to reduce the operating complexity has been focused. When segmentation is performed, additional logic circuits are inevitably required for each point that needs to be decoded, becoming new power and area overhead. To tackle this problem, the new technique called by the coarse phase based fine amplitude of NLDAC decoder grouping (C^2FAG) has been proposed to efficiently reduce the decoding point without affecting the performance. Further, the authors have proposed the low power technique for pipelined accumulators implemented with CML-based circuits. This method has been named as the multi-level momentarily activated bias (M^2AB) technique which effectively utilizes the fast speed characteristics of the CML-based circuits while reducing accompanying static power.

B. PROPOSED LP-DDFS DESIGN

The CML-based circuits used for the digital logic of the previous DDFS design in [4] allows the operation at higher frequencies with lower supply voltages than CMOS-based circuits. But, they consume a lot of static power because the current flows in one of two differential loads. For better understanding, the power consumption of the circuit $P_{Tech.}$ is divided into dynamic and static powers, $P_{dyn,Tech.}$ and $P_{static,Tech.}$ (i.e., *Tech.* implies either CML or CMOS), respectively. Then, the $P_{dyn,Tech.}$ and $P_{static,Tech.}$ can be expressed with supply voltage $V_{dd,Tech.}$, leakage current $I_{lkg.Tech.}$, and the target frequency of the DDFS f_{target} as follows

$$P_{dyn,Tech.}(V_{dd,Tech.}, f_{target}) = C_{eff.Tech.} V_{dd,Tech.}^2 f_{target}, \quad (2)$$

$$\text{and } P_{static,Tech.}(V_{dd,Tech.}) = I_{lkg.Tech.} \cdot V_{dd,Tech.}, \quad (3)$$

where $C_{eff.Tech.}$ is the effective capacitance of the *Tech.*-based circuit. According to the CML and CMOS characteristics, $V_{dd,CML}$ is smaller than $V_{dd,CMOS}$ and $\frac{I_{lkg,CML}}{I_{lkg,CMOS}}$ is larger than $\frac{V_{dd,CMOS}}{V_{dd,CML}}$. These characteristics imply that if P_{dyn} is much larger than P_{static}, using the CML-based circuits with lower V_{dd} may have the low-power advantage. For instance, this can happen when the DDFS operates with high V_{dd}, fast $f_{tareget}$, and/or large C_{eff}. However, in the opposite situation with relatively small f_{target} and/or C_{eff}, or P_{dyn} less than or equal to P_{lkg}, using CMOS-based circuit may be better to save power than CML-based circuit. For example, if the DDFS with 2GS/s target frequency same as in [4] is designed, P_{lkg} predominates and thus using CMOS-based circuit should be better than the CML-based circuit.

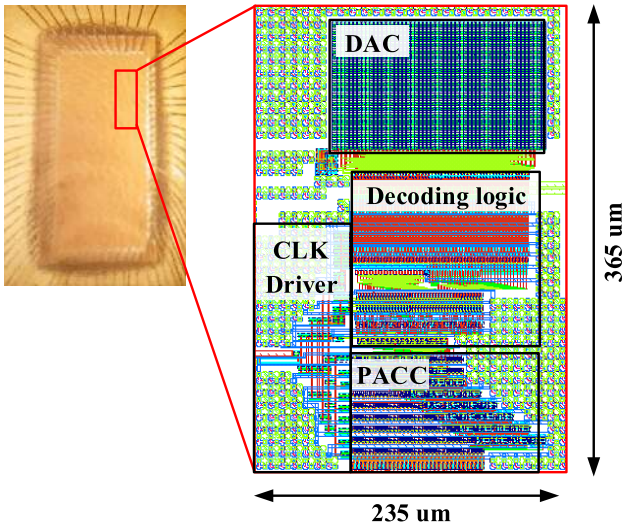

FIGURE 4. Die micrograph of the proposed LP-DDFS.

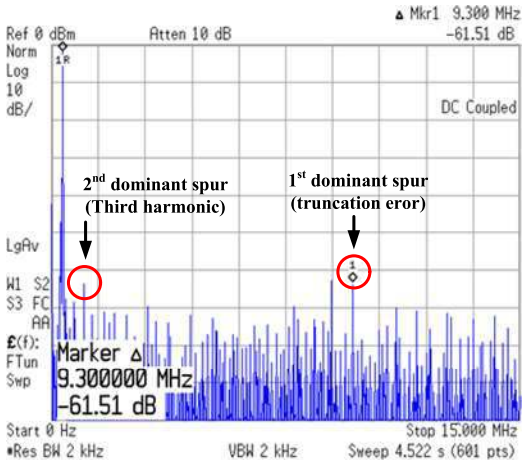

FIGURE 5. Measured spectra from the prototype chip.

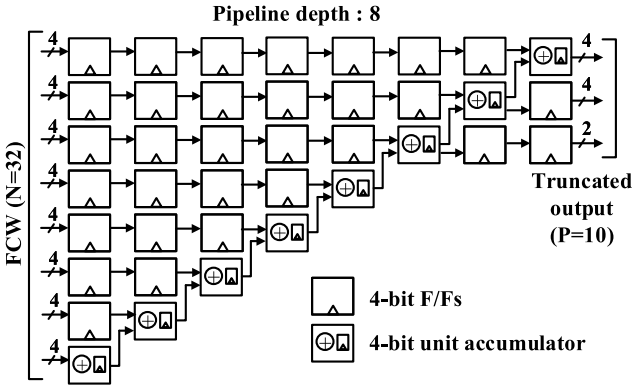

FIGURE 6. Block diagrams of the pipelined PACC.

Based on the abovementioned analysis, a new LP-DDFS with the CMOS-based circuit is designed in this paper. To complement the relatively low speed of the CMOS circuit, a low threshold voltage (LTV) CMOS technology and high speed FFs such as true single-phase clock (TSPC) are adopted. It is noted that although the CML is known to have the advantage of low switching noise in mixed signal circuits, this feature is irrelevant to the DDFS where the CMOS is only used in the digital logic. The block diagram of the proposed LP-DDFS is described in FIGURE 3, where the C^2FAG is still applied in the digital decoder. However, the M^2AB is omitted, because it is only for reducing static power consumption of the CML-based circuit. Then, FIGURE 4 shows the fabricated chip having the size of 235um x 365um by using 65nm CMOS process and the detailed layout. Compared to the previous LP-DDFS with CML circuits consuming 130mW, the proposed LP-DDFS consumes only 56.5mW saving power by 57%.

III. ANALYSIS FOR LOW SFDR IN THE LP-DDFS

Referring to FIGURE 5, the spectra show two dominant spurs occurred at the frequencies including the third harmonic and the spur caused by the decoder. The second dominant spur at the lower frequency is due to the third harmonic caused by non-linearity of DAC such as mismatch and timing error, and thus can be simply solved by fixing the non-linearity through a DAC modification. However, the first dominant spur at the higher frequency is caused by the truncation error. This means that even if the technique in [4] is applied to the decoder and NLDAC for high SFDR performance, spurs due to the PACC still become the dominant.

In order to achieve the potentially maximum performance of [4], the truncation error of the PACC should be controlled below 67.3dBc. To understand the truncation error, the structure of the PACC also used in the prototype chip shown in Figure 6 must be investigated. As aforementioned, the FCW is set according to the target application, and the larger FCW can control the DDFS output sine wave frequency finer. In this paper, the target FCW is set to 32-bit (N), as seen in the figure. Further, the PACC has an eight-depth pipelined structure that consists of eight 4-bit unit accumulators and 124 FFs. To meet the desired frequency of 2GS/s, the 4-bit adder (and thus 4-bit FF) is designed. At the output of the PACC, the 10-bit (P) output of the PACC is truncated into 2/4/4-bits. This truncated 10-bit is for the 9-bit resolution DDFS where the MST technique presented in [4] is applied. If higher resolution is required, the output of the PACC must be truncated to more bits, resulting in the increase in decoding logic with drastically increased power consumption.

FIGURE 7 (a) shows a MATLAB simulation result based on the non-truncated PACC and non-ideal decoding logic and the DAC. Here, the decoder logic makes the dominant spur which results in 67.3dBc SFDR. Then, to investigate the spurs due to truncation, the case where only the PACC is truncated while the other decoding logic and DAC blocks are set ideally not to generate additional spurs is simulated. Having the input (FCW) and output of the PACC as the N-bit and

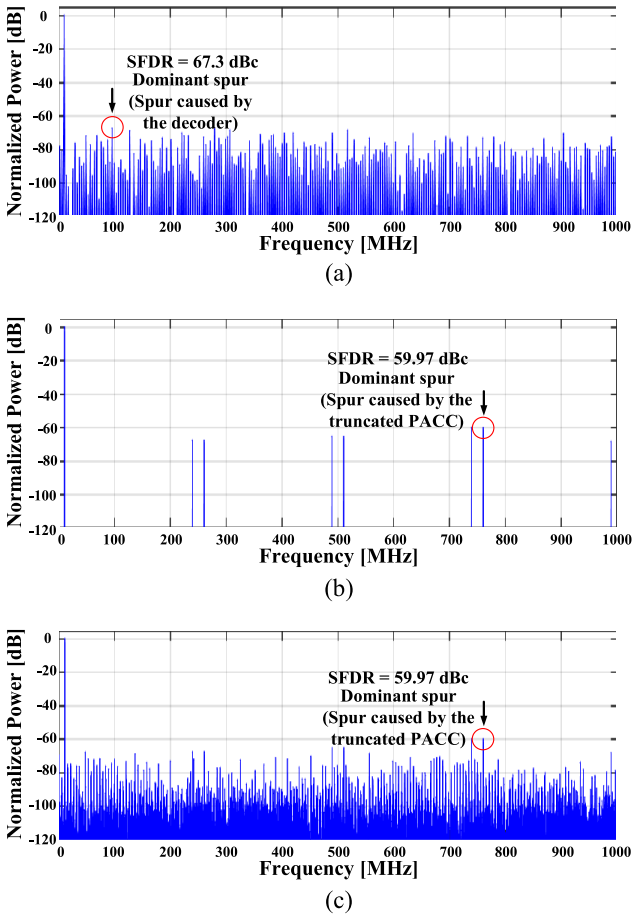

FIGURE 7. Simulation results of the dynamic performance by (a) non-truncated PACC and non-ideal decoder and DAC, (b) 10-bit truncated output PACC ($N = 13$, $P = 10$) and ideal decoder and DAC, and (c) 10-bit truncated output PACC ($N = 13$, $P = 10$) and non-ideal decoder and DAC.

P-bit (larger numbers are LSB), respectively, 1 is periodically displayed in the LSB of the PACC output at every 2^{N-P}. With the $N = 32$ and $P = 10$ as in proposed design, 1 is displayed for every 2^{22} clocks in the LSB of the output and generates truncation error. FIGURE 7 (b) shows the simulated truncation error for case of $N = 13$ instead of using $N = 32$ for saving the execution time. Then, the truncation error is accumulated during 8 ($= 2^{13-10=3}$) clocks and the phase error accumulated by the truncated bit is initialized at every 8 clocks. The truncation spurs occur at every 0.25GHz, which is 8 times less than 2GHz as clearly shown in FIGURE 7 (b). Further, the SFDR due to the truncated spur becomes 59.97dBc. Finally, the simulation for the truncated PACC and non-ideal decoder and DAC as seen in FIGURE 7 (c) shows the dominant spurs exactly matched to truncation spurs in FIGURE 7 (b) and the SFDR of 59.97dBc for the LP-DDFS.

Since the truncation spurs are found to be dominant limiting factor for the performance of the LP-DDFS, increasing the output resolution of the PACC can be easily considered to solve the problem. For example, if the truncation bit of the

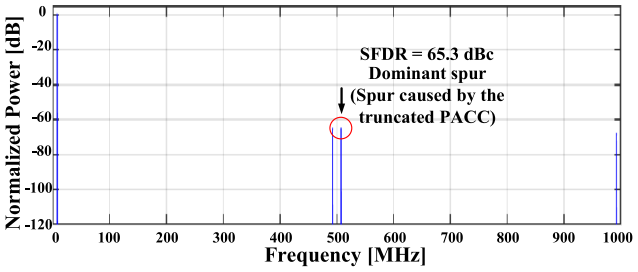

FIGURE 8. Simulation result from using a 11-bit truncated output PACC ($N = 13$, $P = 11$), ideal decoder, and ideal DAC.

PACC output increases from 10-bit to 11-bit, the truncation error will be accumulated during 2^{N-11} clocks. With the $N = 13$, the truncation spur occurs at every 0.5GHz and the phase error initialized at every 4 clocks. As shown in FIGURE 8, the SFDR increases from 59.97dBc to 65.31dBc. However, increasing the number of the truncated output bit of the PACC causes the latter block to be more complicated, and the power consumption due to these complicated blocks also eventually increases. This can be easily verified by the fact that the power consumption of the 10-bit LP-DDFS with 11-bit truncated output PACC ($N = 32$, $P = 11$) and the 9-bit LP-DDFS with 10-bit truncated output PACC ($N = 32$, $P = 10$) are 14.1mW and 10.2mW, respectively. That is, increasing only one-bit results in the 40% increase of power consumption. Moreover, the truncation spurs are remains as the major spurs limiting the performance of LP-DDFS. Instead of increasing the output resolution of the PACC, the dithering method can be an alternative solution [6]–[9]. The truncation error is periodically dithered and thus appeared as a white noise instead of the dominant spurs. Since the previous studies have shown the effectively mitigated truncation errors, several techniques are applied to the proposed LP-DDFS and analyzed through simulations. However, frequency offset and SNDR degradation are found to be side effects with the previously reported dithering methods due to the addition of PRBS signal to the FCW or PACC outputs. Therefore, a new dithering method is also proposed to overcome the drawbacks caused by the incompatibility of the previous methods with the proposed LP-DDFS.

IV. PROPOSED DITHERING METHOD

If the PRBS is inserted into the A^{th} FCW input, the offset of the output frequency, f_{offset} due to the PRBS can be expressed as follows,

$$f_{offset} = E(PRBS) \times \frac{F_{clk}}{2^A}, \tag{4}$$

where $E(PRBS)$ is the mean of the PRBS. According to the equation (4), f_{offset} can be calculated as $\frac{F_{clk}}{2^{A+1}}$ because $E(PRBS)$ is almost 1/2. Then, a frequency compensation circuit (FCC) to eliminate f_{offset} is proposed to obtain the desired frequency exactly as shown in FIGURE 9. The FCC compensates the foffset by subtracting the same weight as the $E(PRBS)$, $\frac{1}{2^{A+1}}$ through two A-bit adders. Here, each adder

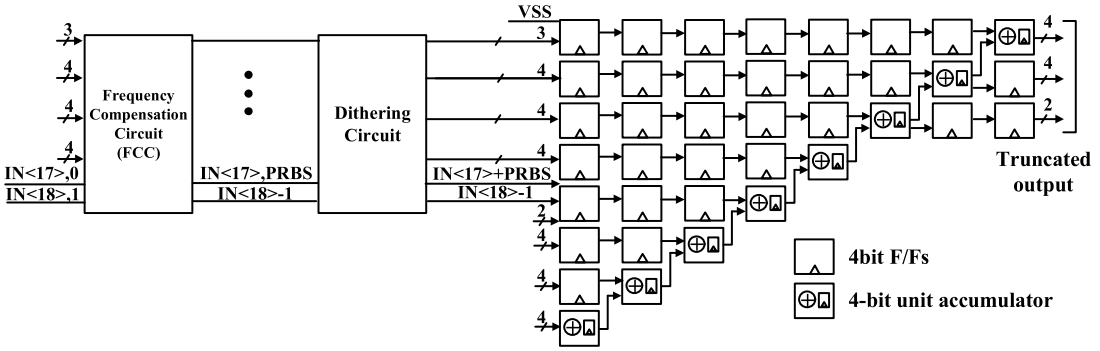

FIGURE 9. Block diagram of the PACC describing the proposed dithering method.

inserts the PRBS into the A^{th} FCW input and to subtract 1 from the $(A+1)^{th}$ FCW input. The proposed FCC is designed with 18-bit and its length depends on where the PRBS is added, A. It is noted that the FCC consumes significantly less power than the PACC because CMOS logic does not consume power when there is no data change. The FCC only operates below the bit where the first 1 of the is inserted. For example, if IN<18> is 1 in FIGURE 9, only one-bit adder operates. In the worst-case scenario, only a less than half the power is used because it has a shorter length than the PACC. As a result, the proposed FCC can effectively compensate the offsets with a minimal additional power consumption.

Then, the most important design factors of the dithering method, the length of the PRBS, L, and the position where the PRBS is added among the N-bit FCWs, A, must be investigated as well. First, it should be noted that the f_{offset} will not be perfectly compensated in case of that PRBS average is not exactly 1/2. More specifically, the $E(PRBS)$ cannot be 1/2, because the length of the PRBS is always odd. That is, the number of 1's and 0's cannot be equal and thus their difference is always only one regardless of the length of PRBS. An example that the PRBS length is 7 ($L = 7$) is described in FIGURE 10 where the 1's and 0's occur 64 and 63 times, respectively.

Then, this error is defined as $PRBS_{error}$, which can be expressed by

$$PRBS_{error} = \frac{2^{L-1}}{2^L - 1} - \frac{1}{2} = \frac{1}{2^{L+1} - 2}. \tag{5}$$

Since the f_{offset} due to $PRBS_{error}$ must be smaller than the frequency tuning resolution, the frequency tuning resolution (F_{out}/FCW) can be mathematically derived from the Eqn. (1) as follows.

$$\frac{F_{clk}}{2^N} > PRBS_{error} \times \frac{F_{clk}}{2^A} = \frac{1}{2^{L+1} - 2} \times \frac{F_{clk}}{2^A} \tag{6}$$

Referring to the above equation, L should be greater than 16, if $N = 32$-bit and $A = 16$-bit.

To compare the SFDR performances with different L and A, the 10-bit truncated output PACC is simulated as shown in FIGURE 11. The location to insert the PRBS and how to set its length can be determined by Figure 11. The dashed line

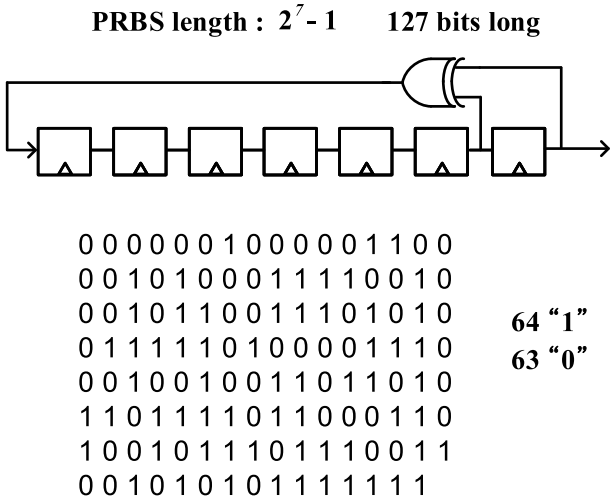

FIGURE 10. Block diagram for the PRBS length of $2^7 - 1$.

indicates the baseline performance based on the use of non-truncated PACC, non-ideally operating decoders and DAC. The others are set with the 10-bit truncated output PACC (P = 10) and ideally operating decoder and DAC to focus only on the PACC. Here, the baseline performance implies a fixed SFDR of 67.3 dBc regardless of the PRBS conditions. That is, the SFDR of the truncated PACC should be higher than 67.3dBc, so as not to make the PACC limiting the DDFS performance. If the SFDR of the truncated PACC is higher than 67.3dBc, the height of the SFDR becomes meaningless. Further, FIGURE 11 shows no difference in the performance when the PRBS length exceeds $2^{17} - 1$.

According to FIGURE 11, there are five candidates (with black dotted circles) that satisfy the SFDR performance of the target LP-DDFS. If the previously reported dithering methods are to be used, any one of the five can be chosen by only considering the SFDR performance. However, depending on which candidate is selected, the resulted SNDR can be varied due to the spectral leakage. More specifically, adding the PRBS signal to the FCW does not change the overall average frequency, but the instantaneous phase can change as if there is a jitter. This is shown in FIGURE 12, where the spectral difference between the cases with and without

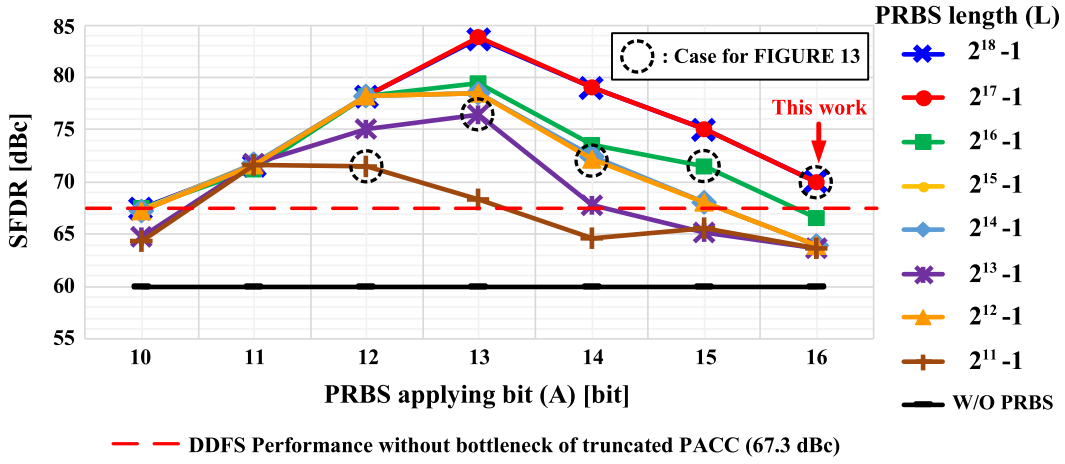

FIGURE 11. SFDR results simulated with varying PRBS conditions.

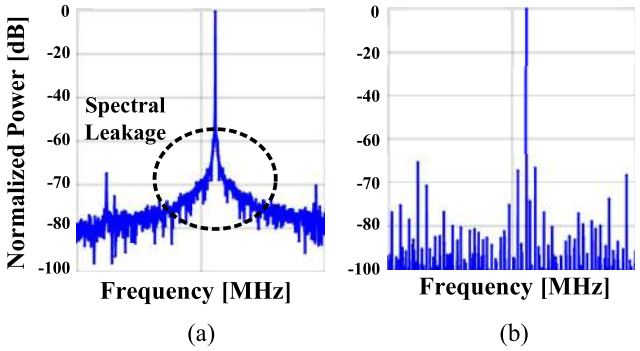

FIGURE 12. Simulation results of spectral leakage (a) with and (b) without the dithering method.

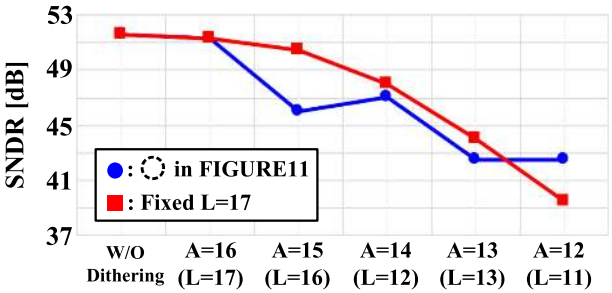

FIGURE 13. SNDR simulation results for the five candidates in FIGURE 11.

the dithering method is clear. Then, FIGURE 13 shows the SNDR results for the five candidates with the largest L of 17. Here, the higher the A is, the better the dithering effect and the worse the spectral leakage. Referring to the FIGURE 13, when $A = 16$, the SNDR becomes the best. Therefore, the PRBS into the 16^{th} FCW input ($A = 16$) is chosen with the PRBS length to be $2^{17} - 1$ ($L = 17$). This condition guarantees that i) the truncated spur is sufficiently dithered, ii) the frequency offset becomes smaller than the frequency tuning resolution, and iii) SNDR degradation is minimized.

V. EXPERIMENTAL WORK

To verify the effective performance of the proposed dithering method, three different case were experimentally analyzed. The first case was for the 10-bit truncated output PACC and ideally operating decoder and DAC, without the proposed dithering method being applied while the second case was applied with the proposed dithering method having the other conditions identical to the first case. Further, the third case was for the 10-bit truncated output PACC and non-ideally operating decoder and DAC with the proposed dithering method being applied. The simulated result for each case is shown in FIGURE 14. The dominant spurs were caused by the truncated PACC in both FIGURE 14 (a) and (b). The resulted SFDRs of the DDFS for the first and second cases were 59.97dBc and 70.80dBc, respectively. In FIGURE 14 (c), the dominant spurs were caused by the decoder and the SFDR of the DDFS was 67.52dBc. Since the truncated spurs had been dithered the performance was no longer limited and the proposed dithering method increases the power by only 0.7mW. Considering the original power consumption of the DDFS of 56.5mW, the power overhead of the proposed method was negligible.

Further, to compare between the 9-bit DDFS with the proposed dithering method and the 10-bit DDFS without the dithering method, the 10-bit DDFS was also simulated. The resulted SFDR of the 10-bit DDFS without the dithering method is 65.3 dBc, which was still slightly less (worse) than the 9-bit DDFS with the dithering method. However, the power consumption of the 10-bit DDFS increased significantly up to 14.1W. Finally, the figure-of-merit (FoM) was defined as follows [4], [26]

$$FoM = \frac{2^{\frac{SFDR}{6}} \times f_{target}[GHz]}{P_{total}[W]}, \tag{7}$$

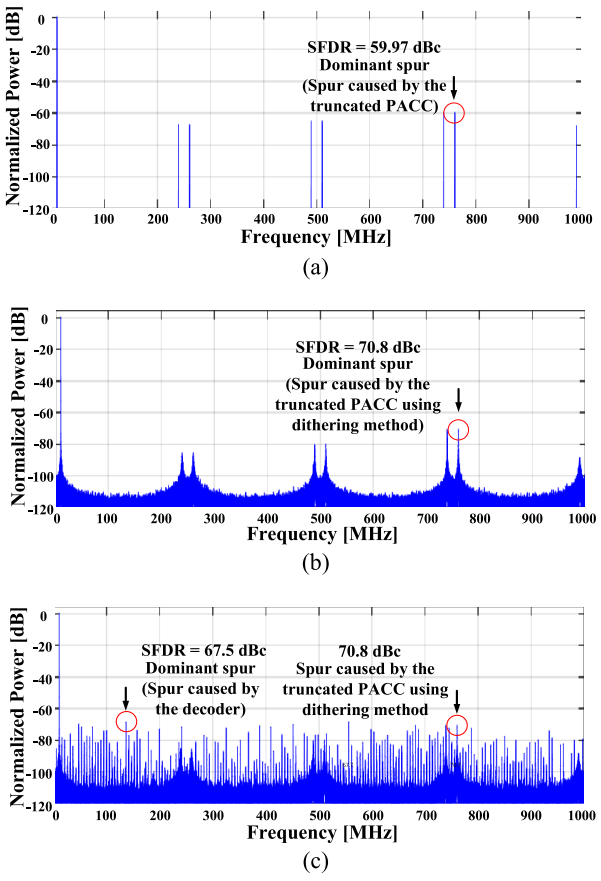

FIGURE 14. Simulation result of the SFDR performance of the LP-DDFS (a) with a truncated PACC and ideal decoder and DAC, and not using the proposed dithering method, (b) with a truncated PACC and ideal decoder and DAC, and using the proposed dithering method, and (c) with a truncated PACC and non-ideally operating decoder and DAC, and using the proposed method.

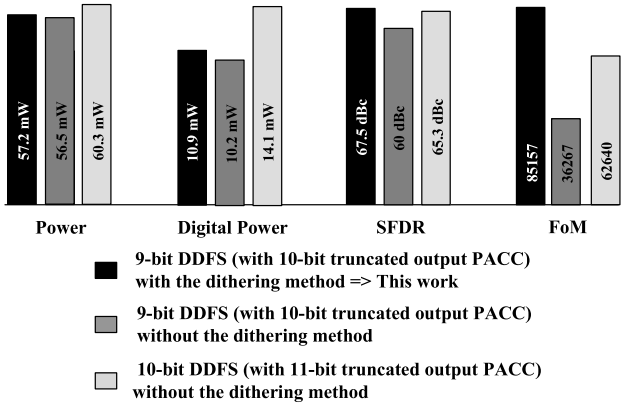

FIGURE 15. Performance comparisons: the 9-bit LP-DDFS design with the proposed dithering method vs. the other cases.

where P_{total} was the total power consumption including both dynamic and static power of the target LP-DDFS. The FoM of the 9-bit DDFS using the proposed dithering method was 85157, the highest as expected, while the 9-bit and 10-bit DDFS without the proposed method were 36267 and 62640, respectively. The comparisons results are summarized in FIGURE 15.

VI. CONCLUSION

In this paper, a new LP-DDFS design topology has been proposed and verified by analyzing the performance of the LP-DDFS as well as finding the performance constraints. The proposed architecture contained the optimized CMOS-based circuit in the LP-DDFS and thus improved the overall performance, power and area occupation. The new LP-DDFS design was fabricated as the prototype chip using 65nm CMOS process and demonstrated 57% reduction in power consumption. Further, the main constraints for the performance of the LP-DDFS, the pipelined PACC and its truncation errors, were analyzed, and thus a new dithering method that minimized the SNDR degradation effect and the frequency offset was also proposed. The PRBS circuit was inserted into the FCW input, and the truncated spurs were dithered periodically to make the spurs like white noise. Detailed procedure to determine where to insert the PRBS and how to determine its length was also presented. That is, all the processes from the LP-DDFS design with the performance analysis to the dithering method have been thoroughly covered with the theoretical and experimental analysis.

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