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Research Article

Design and Analysis of Nanoscaled Recessed-S/D SOI MOSFET-Based Pseudo-NMOS Inverter for Low-Power Electronics

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In this paper, a comparative analysis of nanoscaled triple metal gate (TMG) recessed-source/drain (Re-S/D) fully depleted silicon-on-insulator (FD SOI) MOSFET has been presented for the design of the pseudo-NMOS inverter in the nanometer regime. For this, firstly, an analytical modeling of threshold voltage has been proposed in order to investigate the short channel immunity of the studied device and also verified against simulation results. In this structure, the novel concept of backchannel inversion has been utilized for the study of device performance. The threshold voltage has been analyzed by varying the parameters of the device like the ratio of metal gate length and the recessed-source/drain thickness for TMG Re-S/D SOI MOSFET. Drain-induced barrier lowering (DIBL) has also been explored in terms of recessed-source/drain thickness and the metal gate length ratio to examine short channel effects (SCEs). For the exact estimation of results, the comparison of the existing multimetal gate structures with TMG Re-S/D SOI MOSFET has also been taken under study in terms of electrostatic performance, i.e., threshold voltage, subthreshold slope, and on-off current ratio. These structures are investigated with the TCAD numerical simulator from Silvaco ATLAS. Furthermore, for the first time, TMG Re-S/D FD SOI MOSFET-based pseudo-NMOS inverter has been designed to observe the device performance at circuit levels. It has been found that the device offers high noise immunity with optimum switching characteristics, and the propagation delay of the studied circuit is recorded as 0.43 ps.

1. Introduction

Incorporation of new technologies is going to be more crucial in the coming era of CMOS devices [1, 2]. Short channel effect has become the major problem in performance improvement at the nanotechnology node [3]. Various technologies have been reported recently regarding the improvement in the device performance at nanometre nodes such as FinFET, FD SOI, recessed-source and drain, and gate engineering [4–20]. In last few years, FinFET devices have gained popularity due to better short channel immunity [4]. However, the fin structure was found to be more complex as compared to FD SOI MOSFETs. The leakage and power consumption are drastically reduced by the use of the FD SOI structure [5–7]. Dielectric isolation in SOI MOSFET reduces parasitic capacitances and substrate leakage current, which tempted the device for analog and digital applications [8]. Since FD SOI MOSFET is associated with the problem of higher source/drain series resistance, the structure of single-metal gate (SMG) recessed-source/drain MOSFET was introduced [9, 10]. In Re-S/D-based device, the depth of source and drain is expanded in the buried insulated layer. It reduces capacitances and gives better drive current [11].

To increase the drive current capability, multimaterial gate [12–14] is associated with recessed-source/drain MOSFET. To reduce DIBL, hot carrier effect [15], and gate transport efficiency, the dual-metal gate (DMG) structure was acquainted in the papers [16]. In [17], TMG Re-S/D SOI MOSFET was proposed, in which work functions are in the descending order from the source end to drain end. Due to distinct work function of gate metal

contacts, there is a spike identified in the channel electric field. So the carrier transport efficiency is improved, and so the driving capability of the device is also improved [18]. There is suppressed hot carrier effect (HCE) due to high work function of the control gate than the screen gates.

The three metals in the gate structures give two step potential profile. It reduces DIBL and improves the current transit speed [19]. So, it enhances current-driving capability which ensures SCEs reduction. It can be the same threshold voltage with reduced doping due to gate engineering [20]. It assures immunity against mobility degradation and improved transconductance.

Moreover, use of portable devices in the integration of VLSI circuits requires low power and high speed. At the level of circuit design, the power reduction shifts towards the consideration of a different logic style. CMOS logic offers all requirement of lower and high speed, but in CMOS, the size of the PMOS transistor is larger than the NMOS transistor to balance the rise and fall time. Sometimes, in the logic circuits, it requires to reduce the area for some applications. It can be fulfilled by the use of pseudo-NMOS logic. It uses the n+ 1 transistor as compared to CMOS which uses $2n$ transistors in the logic circuit [21]. Here, TMG Re-S/D FD SOI MOSFET has been utilized for the performance analysis of aforesaid pseudo-NMOS inverter for low-power digital applications.

In this work, threshold voltage of triple-metal gate Re-S/D SOI MOSFET is analyzed for the first time, which is the extension of previous work [17] because surface potential is required to model the threshold voltage of the device. However, to describe the overall electrostatic performance of the device, the threshold voltage model is necessary. Here, analytical threshold voltage model for the device under consideration has been proposed by assuming certain parabolic approximations and verified against two-dimensional mathematical simulations. It is analyzed by varying device parameters like Re-S/D thickness, oxide thickness, and body thickness. Effect of DIBL for a different Re-S/D thickness has also been discussed. Threshold voltage, subthreshold slope, and on/off current ratio have been compared for SMG, DMG, and TMG. It is also investigated by 2D TCAD simulator Silvaco ATLAS [22]. Furthermore, the studied device has been analyzed for the design of the pseudo-NMOS inverter for the estimation of its switching behaviour.

Section 2 discusses the materials and methods of device design and the specifications. The analytical modeling has been presented in Section 3, and corresponding results are discussed in Section 4. Furthermore, the design and analysis of the pseudo-NMOS inverter is shown in Section 5, and the overall contribution is mentioned in Section 6.

2. Materials and Methods

The cross-sectional view of the TMG Re-S/D SOI MOSFET is shown in Figure 1, where L, t_{si}, t_{ox}, t_{rsd}, t_{box}, and d_{box} represent the channel length, silicon body thickness, oxide thickness, Re-S/D thickness, buried oxide (BOX) layer thickness, and S/D overlap over the BOX layer, respectively.

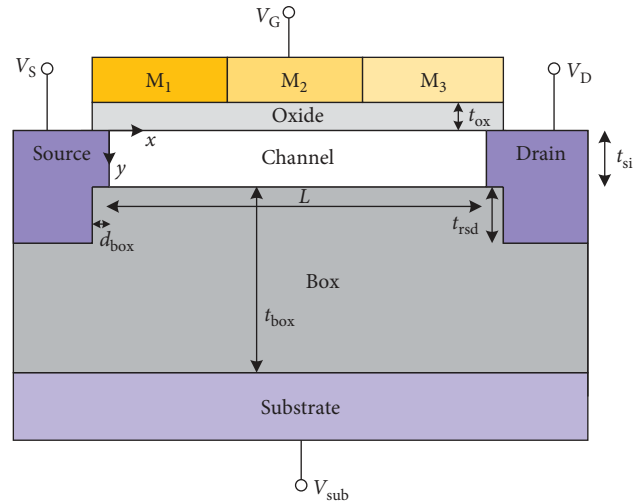

Figure 1: Cross-sectional view of TMG recessed-S/D UTB SOI MOSFET.

The x-axis is taken along the front oxide-channel interface, and y-axis is taken along the source-channel interface. The three metals of the gate are M_1(control gate), M_2(screen gate: first), and M_3(screen gate: second) in which Au, Mo, and Ti are the metal materials. The length of these three metals are termed as L_1, L_2, and L_3 where $L_1 + L_2 + L_3 = L$. N_a, N_d, and N_{sub} are concentration levels of the channel region, source/drain region, and substrate region. Also, under the zero bias condition, it is assumed that channel is fully depleted. The structures of single-metal, double-metal, and triple-metal gate are described in Table 1 for 90 nm channel length.

3. Analytical Modeling

The device under consideration is shown in Figure 1, for which under parabolic approximations, 2D Poisson's equation for the potential at the surface of the channel is presented as follows:

$$\frac{\partial^2 \varnothing_i(x,y)}{\partial x^2} + \frac{\partial^2 \varnothing_i(x,y)}{\partial y^2} = \frac{qN_a}{\varepsilon_{si}}, \tag{1}$$

where $i = 1$, 2, and 3 for region $1\,(0 \le x \le L_1)$, $2\,(L_1 \le x \le L_1 + L_2)$, and $3\,(L_1 + L_2 \le x \le L)$. ε_{si} is the silicon permittivity. The solution of (1) is defined as follows:

$$\varnothing_i(x,y) = \varnothing_{si}(x) + C_{i1}(x)y + C_{i2}(x)y^2, \tag{2}$$

where $\varnothing_{si}(x)$ is the surface potential at the SiO_2/Si interface. The coefficient $C_{i1}(x)$ and $C_{i2}(x)$ can be determined from the following boundary condition.

At the boundary line of region 1 and 2,

$$\left.\frac{\partial \varnothing_1(x,y)}{\partial x}\right|_{x=L_1} = \left.\frac{\partial \varnothing_2(x,y)}{\partial x}\right|_{x=L_1},$$
$$\left.\frac{\partial \varnothing_2(x,y)}{\partial x}\right|_{x=L_1+L_2} = \left.\frac{\partial \varnothing_3(x,y)}{\partial x}\right|_{x=L_1+L_2}. \tag{3}$$

At boundary line between SiO_2 and Si,

Table 1: Device structure of SMG, DMG, and TMG Re-S/D SOI MOSFET.

Device	L_1	L_2	L_3	$\varnothing_{M_1}$	$\varnothing_{M_2}$	$\varnothing_{M_3}$
SMG Re-S/D	90	—	—	4.8 eV (Au)	—	—
DMG Re-S/D	45	45	—	4.8 eV (Au)	4.6 eV (Mo)	—
TMG Re-S/D	30	30	30	4.8 eV (Au)	4.6 eV (Mo)	4.4 eV (Ti)

$$\begin{aligned}
\varepsilon_{si}\cdot\left.\frac{\partial\varnothing_1(x,y)}{\partial y}\right|_{y=0} &= C_{ox1}\cdot\frac{\varnothing_{s1}(x)-(V_{GS}-V_{FB1})}{L_1},\\
\varepsilon_{si}\cdot\left.\frac{\partial\varnothing_2(x,y)}{\partial y}\right|_{y=0} &= C_{ox2}\cdot\frac{\varnothing_{s2}(x)-(V_{GS}-V_{FB2})}{L_2},\\
\varepsilon_{si}\cdot\left.\frac{\partial\varnothing_3(x,y)}{\partial y}\right|_{y=0} &= C_{ox3}\cdot\frac{\varnothing_{s3}(x)-(V_{GS}-V_{FB3})}{L_3}.
\end{aligned} \tag{4}$$

Oxide capacitances C_{ox1}, C_{ox2}, and C_{ox3} and flat band voltage V_{FB1}, V_{FB2}, and V_{FB3} are defined in [17]. At the boundary line between the Si and BOX layer,

$$\begin{aligned}
\varepsilon_{si}\cdot\left.\frac{\partial\varnothing_1(x,y)}{\partial y}\right|_{y=t_{si}} &= C_{rsd1}\cdot\frac{V_s-V_{FB4}-\varnothing_{b1}(x)}{L_1}\\
&\quad+C_{rsd2}\cdot\frac{V_D-V_{FB4}-\varnothing_{b1}(x)}{L_1}\\
&\quad+C_{box1}\cdot\frac{V_{sub}-V_{FB5}-\varnothing_{b1}(x)}{L_1},\\
\varepsilon_{si}\cdot\left.\frac{\partial\varnothing_2(x,y)}{\partial y}\right|_{y=t_{si}} &= C_{rsd3}\cdot\frac{V_s-V_{FB4}-\varnothing_{b2}(x)}{L_2}\\
&\quad+C_{rsd4}\cdot\frac{V_D-V_{FB4}-\varnothing_{b2}(x)}{L_2}\\
&\quad+C_{box2}\cdot\frac{V_{sub}-V_{FB5}-\varnothing_{b2}(x)}{L_2},\\
\varepsilon_{si}\cdot\left.\frac{\partial\varnothing_3(x,y)}{\partial y}\right|_{y=t_{si}} &= C_{rsd5}\cdot\frac{V_s-V_{FB4}-\varnothing_{b3}(x)}{L_3}\\
&\quad+C_{rsd6}\cdot\frac{V_D-V_{FB4}-\varnothing_{b3}(x)}{L_3}\\
&\quad+C_{box3}\cdot\frac{V_{sub}-V_{FB5}-\varnothing_{b3}(x)}{L_3}.
\end{aligned} \tag{5}$$

Re-S/D capacitances C_{rsd1}, C_{rsd2}, C_{rsd3}, C_{rsd4}, C_{rsd5}, and C_{rsd6} and flat band voltage V_{FB4} and V_{FB5} are defined in [17]. $\varnothing_{bi}$ is the surface potential of the backchannel:

$$\begin{aligned}
&\text{at source side: } \varnothing_1(0,y) = V_{bi},\\
&\text{at drain side: } \varnothing_3(L,y) = V_{bi}+V_{DS},
\end{aligned} \tag{6}$$

where V_{bi} and V_{DS} are the barrier potential and drain-to-source bias. Threshold voltage is described as the gate voltage in which the minimum surface potential is equal to twice the Fermi potential. In the TMG structure, there are three metal gates with different work functions. The minimum surface potential is defined under the region of highest work function (control gate).

In the recessed-source/drain structure, backchannel inversion is also significant as compared to front channel inversion due to certain length of recessed-source/drain. Therefore, threshold voltage for the front and backchannel is analyzed in this modeling. Threshold voltage is described with a larger minimum surface potential.

3.1. Front Threshold Voltage. Surface potential at SiO_2/Si is calculated as follows [17]:

$$\frac{d^2\varnothing_{si}(x)}{dx^2}-G_{si}\varnothing_{si}(x)=H_{si},\quad i=1,2,3, \tag{7}$$

where G_{si} and H_{si} are defined in paper [17]. Now, the threshold voltage can be evaluated by following expression:

$$\varnothing_{s1,\min}\big|_{V_{GS}=V_{th}}=\varnothing_{s1}(x_{min})\big|_{V_{GS}=V_{th}}=2\varnothing_{F,si}, \tag{8}$$

where $\varnothing_{s1,\min}$ is the minimum surface potential at the front channel and x_{min} presents the position of minimum surface potential from the source side. It can be obtained as

$$\left.\frac{d\varnothing_{s1}}{dx}\right|_{x=x_{min}}=0, \tag{9}$$

where $\varnothing_{F,si}$ is the Fermi potential in the channel region and is defined as

$$\varnothing_{F,si}=\frac{kT}{q}\ln\left(\frac{N_a}{n_i}\right), \tag{10}$$

where n_i is the intrinsic carrier concentration. Solving equation (1) gives the following expression of threshold voltage:

$$V_{th}=\frac{-b_s+\sqrt{b_s^2-4a_sc_s}}{2a_s}. \tag{11}$$

The derived formulas of coefficients a_s, b_s, and c_s are shown in Appendix A.

3.2. Back Threshold Voltage. Surface potential at the SiO2/BOX interface is calculated as follows [17]:

$$\frac{d^2\varnothing_{bi}(x)}{dx^2}-G_{bi}\varnothing_{bi}(x)=H_{bi},\quad i=1,2,3, \tag{12}$$

where G_{bi} and H_{bi} are defined in [17]. Similarly, threshold voltage for the backchannel can be obtained by evaluating the following expression:

$$\varnothing_{b1,\min}\big|_{V_{GS}=V_{th}}=\varnothing_{b1}(x_{min})\big|_{V_{GS}=V_{th}}=2\varnothing_{F,si}, \tag{13}$$

where $\varnothing_{b1,\min}$ is the minimum surface potential in the backchannel and x_{min} presents the position of the minimum surface potential from the source side. It can be obtained as

$$\left.\frac{d\varnothing_{b1}}{dx}\right|_{x=x_{min}}=0. \tag{14}$$

Solving this equation gives the following expression of threshold voltage:

$$V_{th} = \frac{-b_b + \sqrt{b_b^2 - 4a_b c_b}}{2a_b}. \quad (15)$$

The derived formulas of coefficients a_b, b_b, and c_b are shown in Appendix B.

In the next section, the corresponding results has been discussed and verified against simulation results.

4. Results and Discussion

Analytical model of the threshold voltage for the studied structure has also been compared with TCAD ATLAS Simulator [21]. In the ATLAS simulation, different types of the physical model have been used like field-dependent mobility mode (FLDMOB), concentration-dependent mobility mode (CVT), and Fermi-Dirac statistical model. The doping profile is uniform. The device parameters have been chosen as per the ITRS roadmap. The device channel length (L) is 90 nm, and it has been varied from 20 nm to 300 nm in order to evidence the scaling challenges. The front oxide thickness (t_{ox}) is considered as 2 nm, buried oxide thickness (t_{box}) as 200 nm, silicon channel thickness (t_{si}) of 10 nm, and Re-S/D thickness (t_{rsd}) of 30 nm. The studied MOSFET is characterized with uniform source/drain concentration (N_d) of $10^{20}\,cm^{-3}$ and low bulk doping (N_{sub}) of $10^{15}\,cm^{-3}$.

4.1. Threshold Voltage. The comparative study of threshold voltage for SMG, DMG, and TMG Re-S/D SOI MOSFET is shown in Figure 2. One can find that TMG offers smallest roll off in threshold till 40 nm as compared to DMG and can be further optimized with the metal gate length ratio. Also, there is 14%-15% improvement in the TMG Re-S/D SOI MOSFET in threshold voltage and 0.5%–1% error in between simulation and model. Figure 3 shows the graph for the threshold voltage by varying length ratio of screen and control gates keeping the overall gate length constant. Roll off in threshold voltage is decreased by choosing a shorter screen gate length, but the effect of drain potential variation becomes considerable which indicates poor immunity to DIBL. So, the ratio ($L_1 : L_2$) can be optimized to reduce roll off in threshold voltage.

Figure 4 presents the graph of V_{th} with channel length, while recessed-source/drain thickness is a variable parameter. For a larger recessed-source/drain thickness, roll off is higher at a shorter channel length, which shows the reduction of gate controllability over the channel and so the SCEs. In the Re-S/D MOSFET, inversion in the backchannel occurs before inversion in the front channel. At zero recessed thickness, device behaves like conventional SOI MOSFET in which the front gate controls the channel. So recessed-source/drain thickness should be optimized for trade-off between the SCEs and the backchannel control. Figure 5 shows the graph of V_{th} versus channel length by varying work function values of three materials of gate. Threshold voltage is observed to be increased for higher values of work function and also have less roll off. When the difference between the work function is reduced, the channel will be more prone to drain voltage variation which shows more HCEs. So work function should be maintained to optimize between SCEs and HCEs.

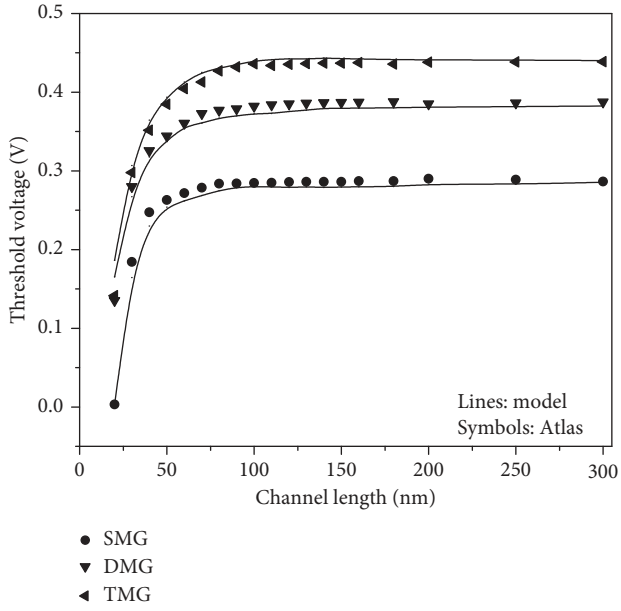

Figure 2: Comparison of threshold voltage for SMG, DMG, and TMG Re-S/D SOI MOSFET

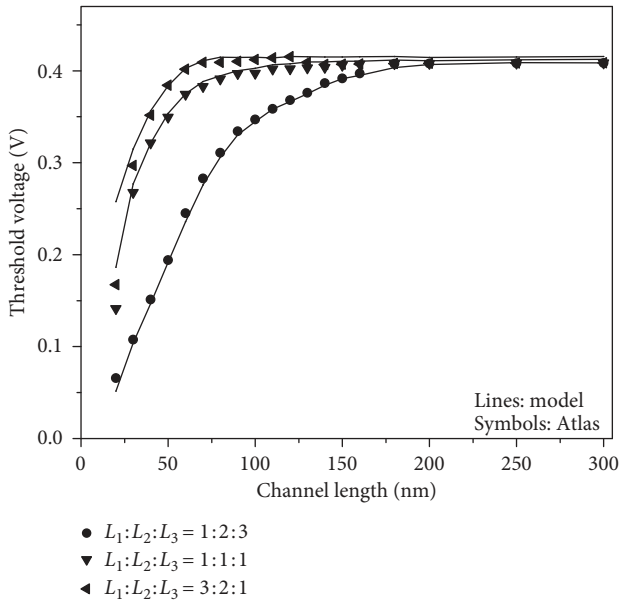

Figure 3: Threshold voltage for different ratios of control gate and screen gates of TMG Re-S/D SOI MOSFET.

Figure 6 shows the graph of DIBL versus channel length for varying the length ratio of control gate and screen gates, while the overall channel length is constant. The graph shows the reduction of DIBL at a shorter length of the control gate. It demonstrates that the structure will be less susceptible to DIBL when control gate length is kept lower. Figure 7 shows the graph of drain-induced barrier lowering (DIBL) plotted against channel length by varying the thickness of the recessed-source/drain region. Here, DIBL is the difference

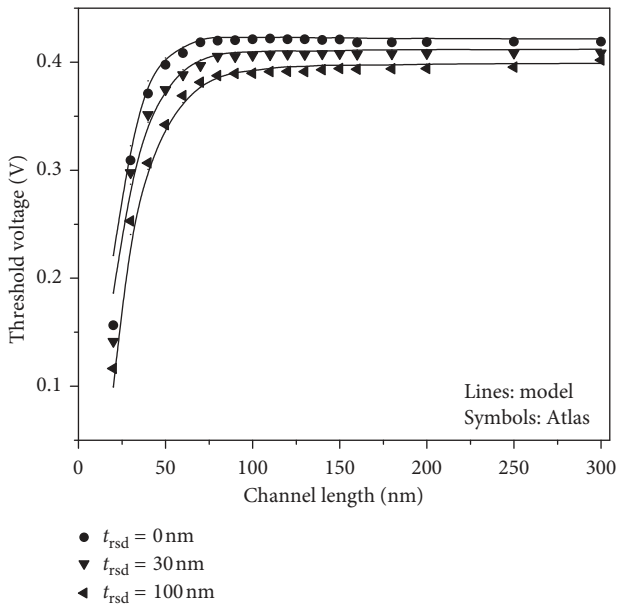

Figure 4: Threshold voltage for different values of recessed-source/drain thickness.

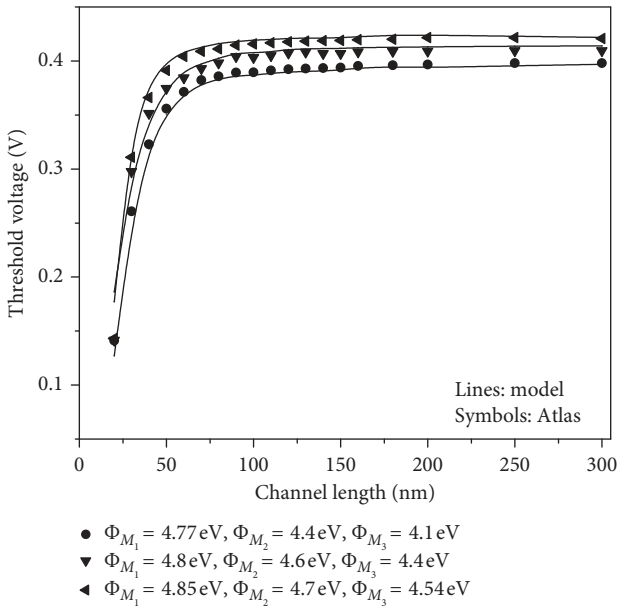

Figure 5: Threshold voltage for different sets of values of work functions for TMG Re-S/D SOI MOSFET.

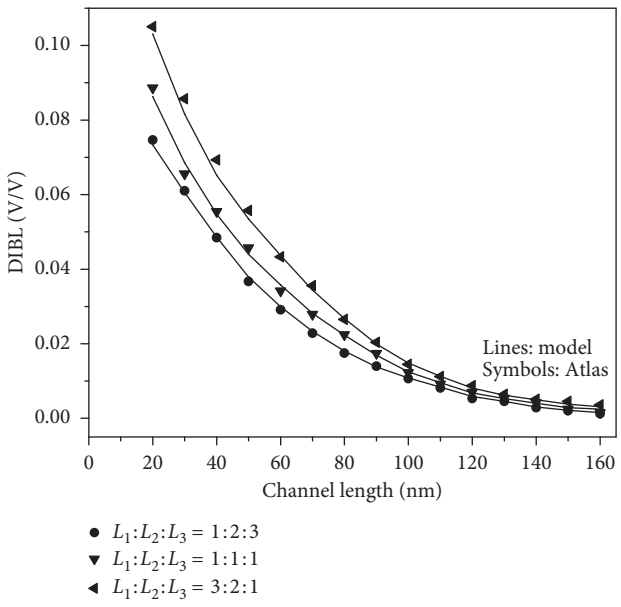

Figure 6: DIBL for the different ratios of control gate and screen gates of the TMG device.

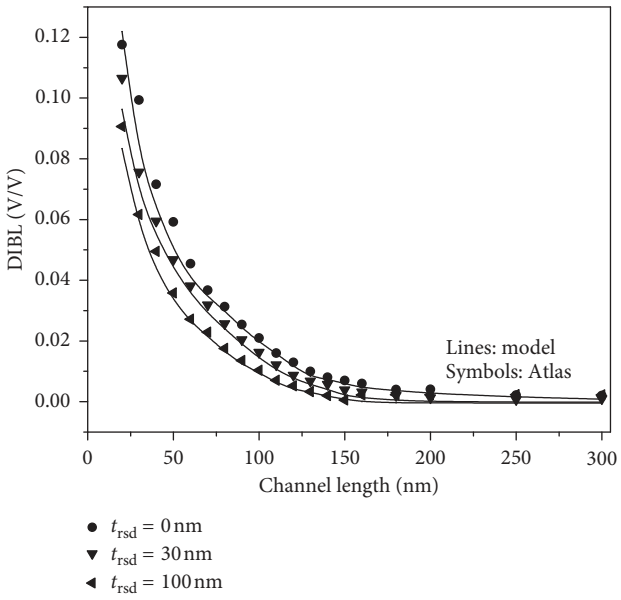

Figure 7: DIBL for the different values of recessed-source/drain thickness.

between the threshold voltage at drain to the source voltage value of 0.1 V and 0.05 V. It has been observed that DIBL is minimized by increasing the thickness of recessed-source/drain thickness.

4.2. Electrostatic Performance. The graph of drain current versus gate voltage for single, double, and TMG Re-S/D SOI MOSFET is shown in Figure 8. This graph reveals that the drain current is better in the case of TMG. This high current is due to high electric field, which results from three gate metals. The increment in the electric field at the edge of metals accelerates the carriers, which automatically enhances the transport efficiency of the carriers. There is 3–17% enhancement in the drain current for TMG recessed-S/D MOSFET. However, this signifies a lesser change as compared to SMG and DMG. Moreover, it is well known that the on-current behaviour of all the three devices depends upon recessed-S/D structure. This is the reason that all the three devices have almost the same on current behaviour due to recessed-S/D, and due to the TMG structure, electrostatic characteristics such as off-state leakage, threshold voltage, and DIBL will be improved. Figure 9 represents the on/off current ratio with respect to channel length. It shows that the

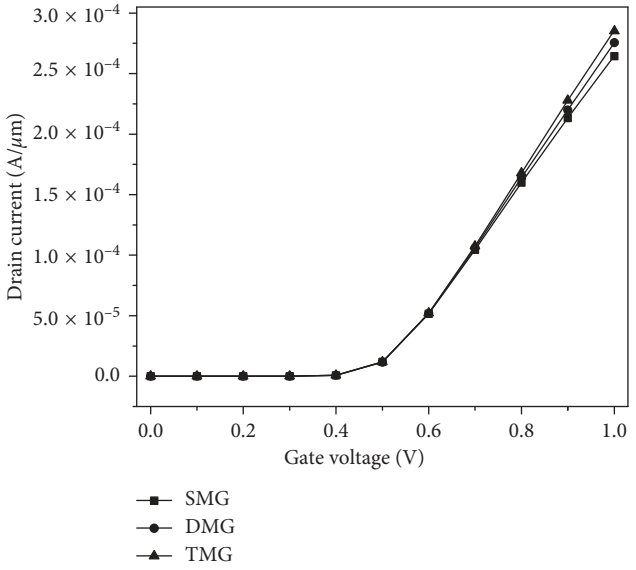

Figure 8: Drain current versus gate voltage for SMG, DMG, and TMG Re-S/D SOI MOSFET.

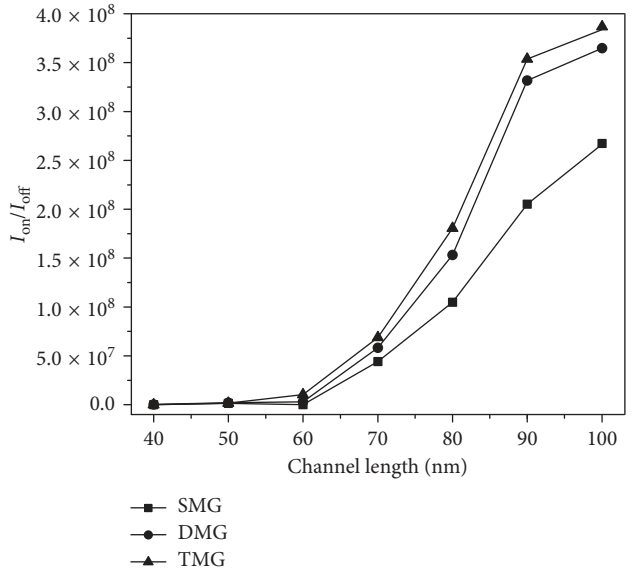

Figure 9: I_{on}/I_{off} at various channel lengths for SMG, DMG, and TMG Re-S/D SOI MOSFET.

switching (I_{on}/I_{off}) current ratio is higher for TMG than DMG and SMG. The peaks in the electric field are increased due to the two interface of metal gate. So the current transport efficiency becomes better in comparison to dual and single-metal gate. On/off current ratio is increased by the increasing gate length. As compared to studied DMG Re-S/D, there is 3–17% improvement in the on/off current ratio in TMG. Figure 10 is the graph of the on/off current ratio at a different value of oxide thickness. As shown in the graph, on/off current ratio is larger for a small value of oxide thickness. When the thickness is increased, on/off current ratio is decreased. It is due to the enhancement of on current as compared to off current. It presents the better current transport at a small oxide region thickness. I_{on}/I_{off} current

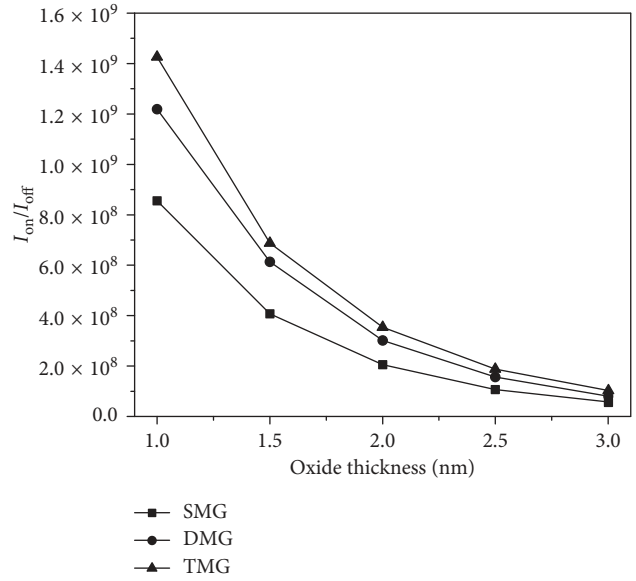

Figure 10: I_{on}/I_{off} for SMG, DMG, and TMG Re-S/D SOI MOSFET versus oxide thickness.

ratio for the TMG Re-S/D device is better as compared to DMG and SMG due to the better current transport.

On/off current ratio with the variation of the thickness of the Re-S/D region is shown in Figure 11. It shows the higher on/off current ration at zero Re-S/D thickness and lower at 100 nm thickness. Since at 0 nm thickness, the resistance value of the MOSFET is increased. So the thickness is slightly increased to optimize between resistance and current. It also shows the 2–10% better on/off current ratio for the TMG Re-S/D structure. Figure 12 represents the graph of subthreshold slope at different values of channel length. As shown in the graph, the subthreshold value is decreased towards higher channel length. The value of subthreshold slope is approximately 70 mV/dec at a higher channel length. It increases at a lower value due to high leakage. It also shows the lower value for TMG as compared to DMG and SMG Re-S/D SOI MOSFET. There is 0.5-6% decrease in the subthreshold slope for TMG as compared to DMG Re-S/D. Figure 13 presents the subthreshold slope with the variation of oxide thickness at 90 nm channel length. As shown in the graph, the subthreshold value is decreased by decreasing oxide thickness. The subthreshold value is between 60 and 73 mV/dec, which is approximately close to the ideal value of 70 mV/dec. Subthreshold slope for TMG is lower than that for DMG and SMG Re-S/D structures, which show that TMG is better immune to SCEs than DMG and SMG. It is observed that 0.7–1.5% reduction in the subthreshold slope for TMG Re-S/D SOI MOSFET. Subthreshold slope with the variation of Re-S/D thickness is represented in Figure 14. As shown in the graph, the subthreshold value is lower for 0 nm Re-S/D thickness, but it increases the series resistance of the MOSFET. The subthreshold value for 100 nm thickness is higher. So, Re-S/D thickness is kept in between to optimize between resistance and SCEs, i.e., at 30 nm. It also shows the 0.01–0.3% better results for the TMG Re-S/D device as compared to others.

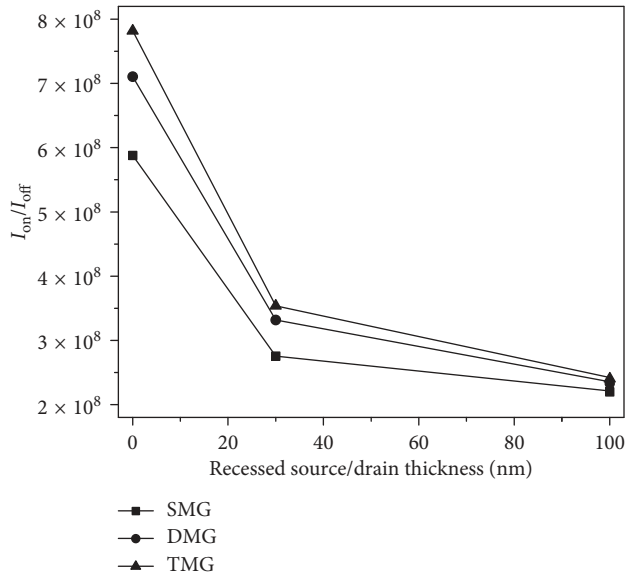

Figure 11: I_{on}/I_{off} for SMG, DMG, and TMG Re-S/D SOI MOSFET versus Re-S/D thickness.

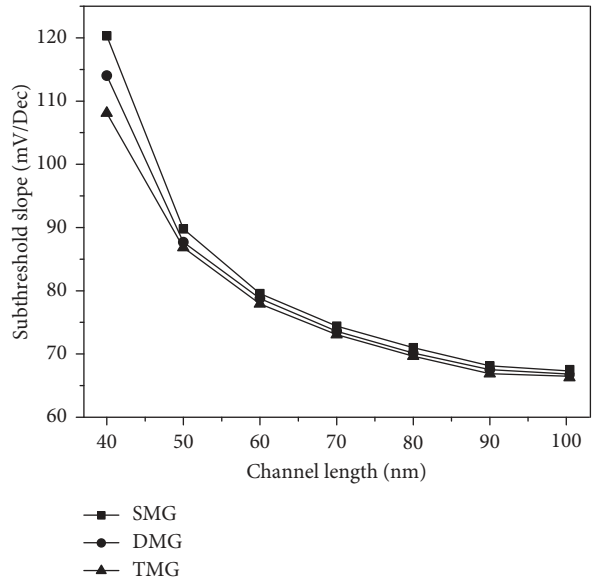

Figure 12: Subthreshold slope at a different channel length for SMG, DMG, and TMG Re-S/D SOI MOSFET.

The performances of the parameters are compared in Table 2. Table 2 is shown for 90 nm channel length in which threshold voltage has been approximately 14% improved for the TMG structure. There is 0.4–0.8% improvement in DIBL and subthreshold slope for TMG Re-S/D as compared to others, which shows better immunity to SCEs. For TMG Re-S/D MOSFET, it is observed to approximate 6% improvement in on/off current ratio and approximate 3% enhancement in transconductance. It shows that TMG Re-S/D MOSFET has superior current driving ability as compared to others.

Also, it is necessary to examine charge distribution at the interfaces of the three metal gates. As, in the channel, uniform charge density has been assumed for the modeling of the

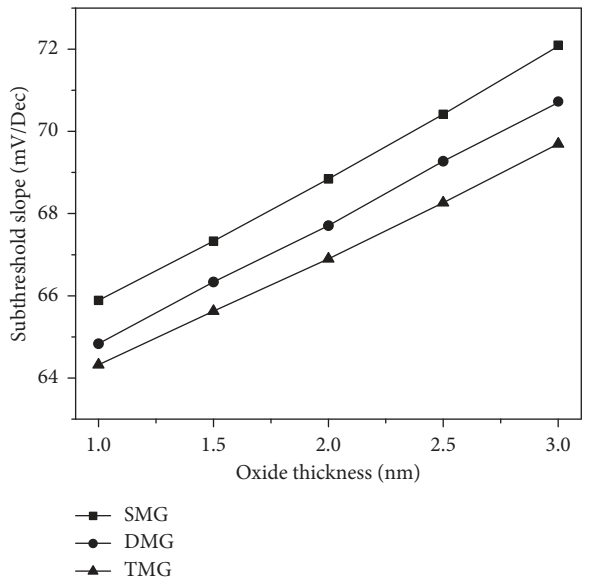

Figure 13: Subthreshold slope for SMG, DMG, and TMG Re-S/D SOI MOSFET versus oxide thickness at 90 nm channel length.

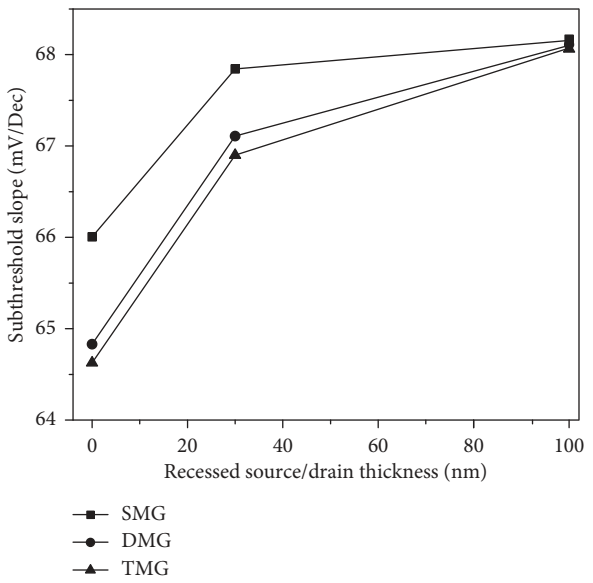

Figure 14: Subthreshold slope for SMG, DMG, and TMG Re-S/D SOI MOSFET versus Re-S/D thickness.

Table 2: Performance comparison of SMG, DMG, and TMG Re-S/D SOI MOSFET.

Parameters	SMG Re-S/D	DMG Re-S/D	TMG Re-S/D
Threshold voltage (V)	0.284	0.379	0.432
DIBL (mV/V)	24.8	24.6	24.5
Subthreshold slope (mV/dec)	68.1	67.5	66.9
I_{on}/I_{off}	2.052×10^8	3.316×10^8	3.537×10^8
Transconductance (S/μm)	5.559×10^{-4}	5.903×10^{-4}	6.041×10^{-4}

proposed device. The plot of carrier concentration vs. position along the channel is shown in Figure 15. It is clear from the plot that the device offers almost uniform charge density in the channel and even all the metal interfaces have equal charge distribution. The uniform charge density of 19.25 cm^{-3} and 19.40 cm^{-3} is observed at the first and second metal interfaces, respectively. These performance features of TMG Re-S/D FD SOI MOSFET have made it a suitable candidate for the analysis and design of today's low-power integrated circuits (ICs). In the next section, an attempt has been made to analyze the studied device performance in digital circuitry.

5. Design and Analysis of Pseudo-NMOS Inverter

Recently, pseudo-NMOS inverter has been accepted as the faster design as compared to the conventional inverter [23]. Here, TMG Re-S/D FD SOI MOSFET-based pseudo-NMOS inverter is designed by using PMOS and NMOS pairs, as shown in Figure 16. PMOS transistor is connected as pull-up load in which its gate is connected permanently to ground. Since it is not driven by any signals, it is always in the ON condition. NMOS is used as pull-down or driver circuit. Its gate is connected with input signals. It is equivalent to the operation of NMOS technology in the depletion mode. So, it is called pseudo-NMOS. In this circuit, PMOS works in the linear region, so it has low resistance and hence low time constant. However, NMOS works in the subthreshold region due to which it is fastest among other CMOS logic. It has the advantage of less area and high speed, but also it has the disadvantage of significant static power consumption.

The voltage transfer characteristics (VTC) of pseudo-NMOS inverter for TMG, DMG, and SMG recessed-S/D FD SOI MOSFET are shown in Figure 17. One can observe from the plot that the switching distance of TMG Re-S/D MOSFET is less as compared to DMG and SMG Re-S/D MOSFET. The TMG offers better characteristics due to the higher threshold and lesser threshold voltage variability as compared to DMG and SMG Re-S/D FD SOI MOSFETs. This will directly affect the noise immunity levels of SMG and DMG as compared to the TMG structure. So, the performance of TMG Re-S/D-based pseudo-NMOS is better as it responds rapidly. Furthermore, in order to analyze the scaling constraints versus switching characteristics of the TMG Re-S/D FD SOI MOSFET, this has been scaled down to 45 nm.

The VTC curve of the pseudo-NMOS inverter for TMG Re-S/D MOSFET at various channel lengths is shown in Figure 18. In short channel devices, barrier for electron injection from source to channel reduces due to overlapping of source and drain depletion regions. It leads to reduced threshold voltage. At the lower threshold voltage, NMOS transistor turns on earlier than the one with higher threshold voltage. Similarly, the PMOS transistor takes time to turn off. So, the switching distance is increased. So, threshold voltage varies with channel length. It reduces by reducing the channel length of the device. Therefore, switching distance is large for a smaller channel length. It is clear from the plot that the device resembles the inverter characteristics even if

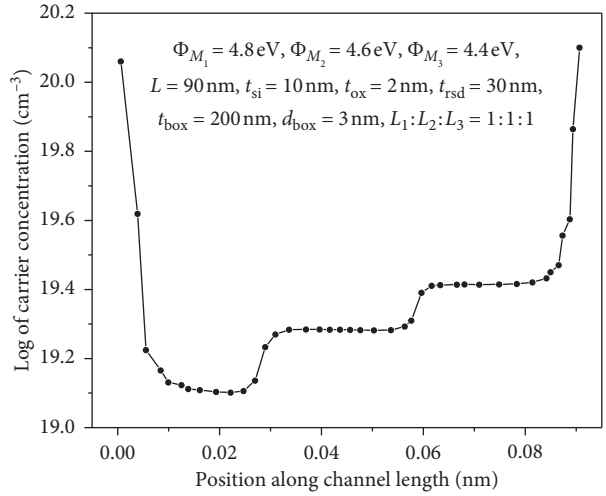

Figure 15: Carrier concentration along the position of channel length for TMG Re-S/D FD SOI MOSFET.

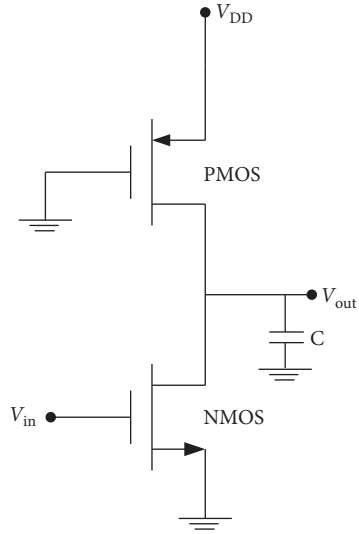

Figure 16: Pseudo-NMOS inverter.

it is scaled down to 45 nm. Moreover, the performance of the inverter at 90 nm channel length of TMG Re-S/D MOSFET is found to be better as its characteristics tend towards the ideal value and switching is faster. So, we have analyzed the device further at 90 nm channel length for its transient behaviour.

The transient analysis of pseudo-NMOS inverter for TMG Re-S/D FD SOI MOSFET is presented in Figure 19 at 90 nm channel length. In the transient analysis, input voltage has been given in pulse waveform with 0 to 1 V amplitude and 10 ps of cycle. As the supply voltage given in the inverter is 1 V, output voltage waveform switches between 0 and 1 V. The graph itself shows the inversion characteristics for input and output voltage, and the propagation delay between input and output switching is observed. When the output goes low to high value, the delay, i.e., τ_{plh}, is observed as 0.59 ps, and when the output goes high to low output, the delay, i.e., τ_{phl}, is observed as 0.27 ps. As the total propagation delay of the

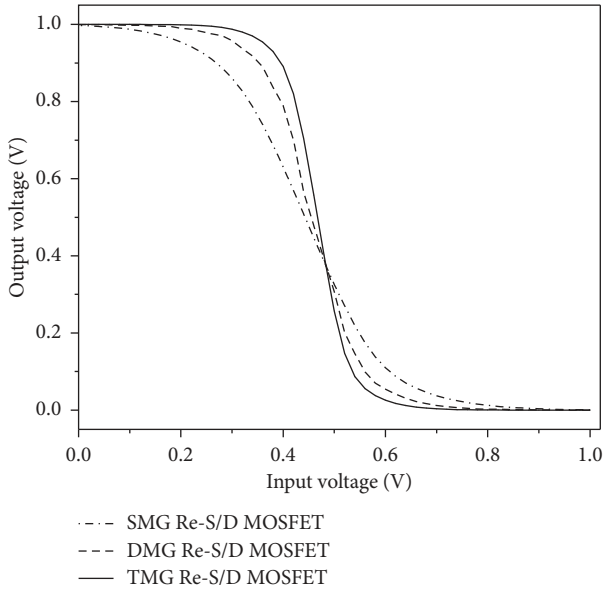

Figure 17: Voltage transfer characteristic curve of pseudo-NMOS for TMG, DMG, and SMG Re-S/D FD SOI MOSFET.

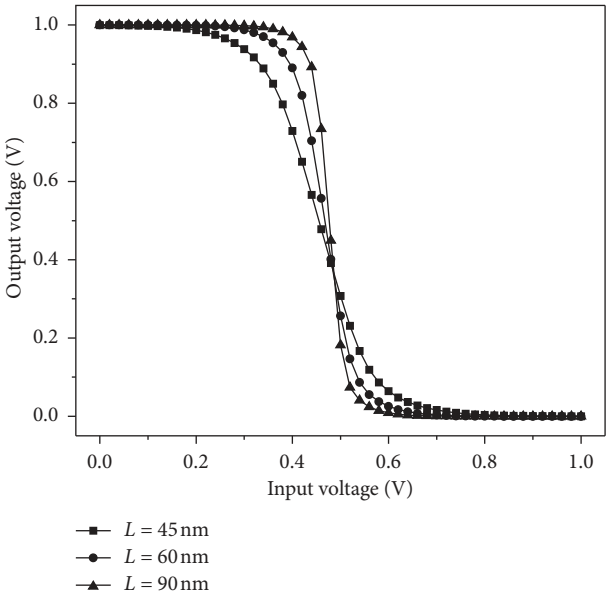

Figure 18: VTC curve of pseudo-NMOS for TMG Re-S/D FD SOI MOSFET at different channel lengths.

pseudo-NMOS is the average of τ_{phl} and τ_{plh}, the total delay comes as 0.43 ps. The comparison with the previous literature is shown in Table 3. This is very less for the circuit to be operated faster, and hence, the studied device could be optimized for high-speed applications.

6. Conclusion

In this contribution, design and analysis of recessed-S/D SOI MOSFET-based pseudo-NMOS inverter has been presented for low-power and high-speed applications. First, a comparison of threshold voltage and

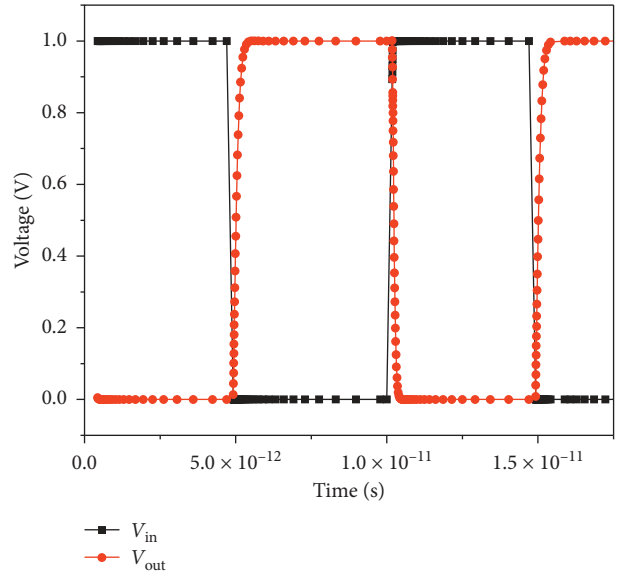

Figure 19: Transient analysis of pseudo-NMOS for TMG Re-S/D FD SOI MOSFET at 90 nm channel length.

Table 3: Comparison of delay of inverters at 90 nm channel length.

References	Inverter delay
Samanta et al. [24]	0.31 ns
Sing et al. [25]	9.43 ps
Rodoni et al. [26]	4.7 ps
Proposed pseudo-NMOS	0.43 ps

electrostatic performance has been discussed for single-metal, double-metal, and triple-metal gate recessed-source/drain (Re-S/D) SOI MOSFET. The model for threshold voltage helps to optimize the SCEs for short channel devices. The gate of three materials which are laterally joined shows better immunity to SCEs and DIBL which is the major concern of SOI MOSFET. The accuracy of the analytical model has been verified with the result of the two-dimensional TCAD simulator of Silvaco ATLAS, and it shows good agreement with 0.5–1% error in results. The comparison of threshold voltage indicates that the TMG-based device offers better immunity to SCEs than other Re-S/D SOI MOSFETs as less roll off seen in case of TMG. The TMG device provides significant reduction in the DIBL effect even if there are parameter variations. The enhancement in the drain current reveals that the TMG is better than the DMG and SMG Re-S/D SOI MOSFET in terms of current-driving capability. These advanced features of the TMG device made it a suitable candidate to further analyze it for high speed switching applications. For this, a pseudo-NMOS inverter has been designed and simulated using TMG Re-S/D FD SOI MOSFET. It is found that the inverter shows the excellent characteristics in case of TMG as compared to others as the TMG device resembles almost ideal VTC at $V_{dd} = 1$ V. The transient analysis shows that the studied circuit allows very less propagation delay of 0.43 ps. So, the device could be suggested for high-speed and low-power IC applications. Moreover, channel

engineering and the analysis of analog and high-frequency performances can be the future work of this device.

Appendix

A. Derived Coefficients of Front Threshold Voltage

$$a_s = \frac{Q_{s1}^2}{G_{s1}^2}\left(2r + \frac{2rd}{n_s} - 5\right) + \frac{Q_{s1}}{G_{s1}}\frac{Q_{s2}}{G_{s2}}\frac{2re}{n_s} + \frac{Q_{s1}}{G_{s1}}\frac{Q_{s3}}{G_{s3}}\frac{2rf}{n_s}, \tag{A.1}$$

$$\begin{aligned} b_s = {} & \frac{2P_{s1}Q_{s1}}{G_{s1}^2}\left(2r + \frac{2rd}{n_s} - 5\right) + \frac{P_{s1}Q_{s2} + P_{s2}Q_{s1}}{G_{s1}G_{s2}}\frac{2re}{n_s} \\ & + \frac{P_{s1}Q_{s3} + P_{s3}Q_{s1}}{G_{s1}G_{s3}}\frac{2rf}{n_s} + \frac{Q_{s2}}{G_{s2}}\frac{2reV_{bi}}{n_s} + \frac{Q_{s3}}{G_{s3}}\frac{2rfV_{bi}}{n_s} \\ & + \frac{Q_{s1}}{G_{s1}}\left(\frac{2rg}{n_s} + \frac{2rdV_{bi}}{n_s} - 8V_{bi} - 4\varnothing_{F,si}\right), \end{aligned} \tag{A.2}$$

$$\begin{aligned} c_s = {} & \frac{P_{s1}^2}{G_{s1}^2}\left(2r + \frac{2rd}{n_s} - 5\right) \\ & + \frac{P_{s1}}{G_{s1}}\left(\frac{2rg}{n_s} + \frac{2rdV_{bi}}{n_s} - 8V_{bi} - 4\varnothing_{F,si}\right) + \frac{P_{s1}}{G_{s1}}\frac{P_{s2}}{G_{s2}}\frac{2re}{n_s} \\ & + \frac{P_{s1}}{G_{s1}}\frac{P_{s3}}{G_{s3}}\frac{2rf}{n_s} + \frac{P_{s2}}{G_{s2}}\frac{2reV_{bi}}{n_s} + \frac{P_{s3}}{G_{s3}}\frac{2rfV_{bi}}{n_s} + \frac{2rgV_{bi}}{n_s} \\ & - 4\left(V_{bi}^2 + \varnothing_{F,si}^2\right), \end{aligned} \tag{A.3}$$

$$\begin{aligned} P_{s1} = {} & \frac{qN_a}{\varepsilon_{si}} - \frac{(V_S - V_{FB4})\cdot(2C_{rsd1}/C_1)}{t_{si}^2(1 + (2C_{si1}/C_1))} \\ & - \frac{(V_D - V_{FB4})\cdot(2C_{rsd2}/C_1)}{t_{si}^2(1 + (2C_{si1}/C_1))} \\ & - \frac{(V_{sub} - V_{FB5})\cdot(2C_{box1}/C_1)}{t_{si}^2(1 + (2C_{si1}/C_1))} \\ & + \frac{V_{FB1}\cdot((2(C_{si1} + C_1)C_{ox1})/C_1\cdot C_{si1})}{t_{si}^2(1 + (2C_{si1}/C_1))}, \end{aligned} \tag{A.4}$$

$$Q_{s1} = -\frac{(2(C_{si1} + C_1)C_{ox1})/C_1\cdot C_{si1}}{t_{si}^2(1 + (2C_{si1}/C_1))}, \tag{A.5}$$

$$\begin{aligned} P_{s2} = {} & \frac{qN_a}{\varepsilon_{si}} - \frac{(V_S - V_{FB4})\cdot(2C_{rsd3}/C_2)}{t_{si}^2(1 + (2C_{si2}/C_2))} \\ & - \frac{(V_D - V_{FB4})\cdot(2C_{rsd4}/C_2)}{t_{si}^2(1 + (2C_{si2}/C_2))} \\ & - \frac{(V_{sub} - V_{FB5})\cdot(2C_{box2}/C_2)}{t_{si}^2(1 + (2C_{si2}/C_2))} \\ & + \frac{V_{FB2}\cdot(2(C_{si2} + C_2)C_{ox2}/C_2\cdot C_{si2})}{t_{si}^2(1 + (2C_{si2}/C_2))}, \end{aligned} \tag{A.6}$$

$$Q_{s2} = -\frac{(2(C_{si2} + C_2)C_{ox2})/C_2\cdot C_{si2}}{t_{si}^2(1 + (2C_{si2}/C_2))}, \tag{A.7}$$

$$\begin{aligned} P_{s3} = {} & \frac{qN_a}{\varepsilon_{si}} - \frac{(V_S - V_{FB4})\cdot(2C_{rsd5}/C_3)}{t_{si}^2(1 + (2C_{si3}/C_3))} \\ & - \frac{(V_D - V_{FB4})\cdot(2C_{rsd6}/C_3)}{t_{si}^2(1 + (2C_{si3}/C_3))} \\ & - \frac{(V_{sub} - V_{FB5})\cdot(2C_{box3}/C_3)}{t_{si}^2(1 + (2C_{si3}/C_3))} \\ & + \frac{V_{FB3}\cdot(2(C_{si3} + C_3)C_{ox3}/C_3\cdot C_{si3})}{t_{si}^2(1 + (2C_{si3}/C_3))}, \end{aligned} \tag{A.8}$$

$$Q_{s3} = -\frac{(2(C_{si3} + C_3)C_{ox3})/C_3\cdot C_{si3}}{t_{si}^2(1 + (2C_{si3}/C_3))}, \tag{A.9}$$

$$\begin{aligned} d = {} & \frac{g}{V_{bi}} - \lambda_{f1}\lambda_{f2}\coth(\lambda_{f1}L_1)\coth(\lambda_{f2}L_2) \\ & - \lambda_{f1}\lambda_{f3}\coth(\lambda_{f1}L_1)\coth(\lambda_{f3}L_3), \end{aligned} \tag{A.10}$$

$$\begin{aligned} e = {} & \lambda_{f2}\lambda_{f3}\operatorname{cosech}(\lambda_{f2}L_2)\coth(\lambda_{f3}L_3) \\ & - \lambda_{f2}\lambda_{f3}\coth(\lambda_{f2}L_2)\coth(\lambda_{f3}L_3) - \lambda_{f2}^2, \end{aligned} \tag{A.11}$$

$$f = -\lambda_{f2}\lambda_{f3}\operatorname{cosech}, \tag{A.12}$$

$$\begin{aligned} g = {} & V_{bi}(\lambda_{f1}\lambda_{f2}\operatorname{cosech}(\lambda_{f1}L_1)\coth(\lambda_{f2}L_2) \\ & + \lambda_{f1}\lambda_{f3}\operatorname{cosech}(\lambda_{f1}L_1)\coth(\lambda_{f3}L_3) \\ & + \lambda_{f2}\lambda_{f3}\operatorname{cosech}(\lambda_{f2}L_2)\operatorname{cosech}(\lambda_{f3}L_3)), \end{aligned} \tag{A.13}$$

$$r = \coth(\lambda_{f1}L_1)\operatorname{cosech}(\lambda_{f1}L_1) + \operatorname{cosech}^2(\lambda_{f1}L_1). \tag{A.14}$$

The values of G_{s1}, G_{s2}, G_{s3}, n_s, λ_{f1}, λ_{f2}, and λ_{f3} are taken from [17].

B. Derived Coefficients of Back Threshold Voltage

$$\begin{aligned} a_b = {} & \frac{Q_{b1}^2}{G_{b1}^2}\left(2r' + \frac{2r'd'}{n_b} - 5\right) + \frac{Q_{b1}}{G_{b1}}\frac{Q_{b2}}{G_{b2}}\frac{2r'e'}{n_s} \\ & + \frac{Q_{b1}}{G_{b1}}\frac{Q_{b3}}{G_{b3}}\frac{2r'f'}{n_b}, \end{aligned} \tag{B.1}$$

$$\begin{aligned} b_b = {} & \frac{2P_{b1}Q_{b1}}{G_{b1}^2}\left(2r' + \frac{2r'd'}{n_b} - 5\right) + \frac{P_{b1}Q_{b2} + P_{b2}Q_{b1}}{G_{b1}G_{b2}}\frac{2r'e'}{n_b} \\ & + \frac{P_{b1}Q_{b3} + P_{b3}Q_{b1}}{G_{b1}G_{b3}}\frac{2r'f'}{n_b} + \frac{Q_{b1}}{G_{b1}}\left(\frac{2r'g'}{n_b} + \frac{2r'd'V_{bi}}{n_b}\right. \\ & \left. - 8V_{bi} - 4\varnothing_{F,si}\right) + \frac{Q_{b2}}{G_{b2}}\frac{2r'e'V_{bi}}{n_b} + \frac{Q_{b3}}{G_{b3}}\frac{2r'f'^{V_{bi}}}{n_b}, \end{aligned} \tag{B.2}$$

$$c_b = \frac{P_{b1}^2}{G_{b1}^2}\left(2r' + \frac{2r'd'}{n_b} - 5\right) + \frac{P_{b1}}{G_{b1}}\left(\frac{2r'g'}{n_b} + \frac{2r'd'^{V_{bi}}}{n_b} - 8V_{bi} - 4\varnothing_{F,si}\right) + \frac{P_{b1}}{G_{b1}}\frac{P_{b2}}{G_{b2}}\frac{2r'e'}{n_b} + \frac{P_{b1}}{G_{b1}}\frac{P_{b3}}{G_{b3}}\frac{2r'f'}{n_b} + \frac{P_{b2}}{G_{b2}}\frac{2r'e'^{V_{bi}}}{n_b} + \frac{P_{b3}}{G_{b3}}\frac{2r'f'V_{bi}}{n_b} + \frac{2r'g'^{V_{bi}}}{n_b} - 4\left(V_{bi}^2 + \varnothing_{F,si}^2\right), \tag{B.3}$$

$$P_{b1} = \frac{qN_a}{\varepsilon_{si}} - 2\left((-V_{FB1}) + (V_S - V_{FB4})\left[(C_{rsd1}/C_{ox1}) + (C_{rsd1}/C_{si1})\right] + (V_D - V_{FB4})\left[(C_{rsd2}/C_{ox1}) + (C_{rsd2}/C_{si1})\right] + (V_{sub} - V_{FB5})\left[(C_{box1}/C_{ox1}) + (C_{box1}/C_{si1})\right]\right) \times \left(t_{si}^2\left(1 + (2C_{si1}/C_{ox1})\right)\right)^{-1}, \tag{B.4}$$

$$Q_{b1} = -\frac{2}{t_{si}^2\left(1 + (2C_{si1}/C_{ox1})\right)}, \tag{B.5}$$

$$P_{b2} = \frac{qN_a}{\varepsilon_{si}} - 2\left((-V_{FB2}) + (V_S - V_{FB4})\left[(C_{rsd3}/C_{ox2}) + (C_{rsd3}/C_{si2})\right] + (V_D - V_{FB4})\left[(C_{rsd4}/C_{ox2}) + (C_{rsd4}/C_{si2})\right] + (V_{sub} - V_{FB5})\left[(C_{box2}/C_{ox2}) + (C_{box2}/C_{si2})\right]\right) \times \left(t_{si}^2\left(1 + (2C_{si2}/C_{ox2})\right)\right)^{-1}, \tag{B.6}$$

$$Q_{b2} = -\frac{2}{t_{si}^2\left(1 + (2C_{si2}/C_{ox2})\right)}, \tag{B.7}$$

$$P_{b3} = \frac{qN_a}{\varepsilon_{si}} - 2\left((-V_{FB3}) + (V_S - V_{FB4})\left[(C_{rsd5}/C_{ox3}) + (C_{rsd5}/C_{si3})\right] + (V_D - V_{FB4})\left[(C_{rsd6}/C_{ox3}) + (C_{rsd6}/C_{si3})\right] + (V_{sub} - V_{FB5})\left[(C_{box3}/C_{ox3}) + (C_{box3}/C_{si3})\right]\right) \times \left(t_{si}^2\left(1 + (2C_{si3}/C_{ox3})\right)\right)^{-1}, \tag{B.8}$$

$$Q_{b3} = -\frac{2}{t_{si}^2\left(1 + (2C_{si3}/C_{ox3})\right)}, \tag{B.9}$$

$$d' = \frac{g'}{V_{bi}} - \lambda_{b1}\lambda_{b2}\coth(\lambda_{b1}L_1)\coth(\lambda_{b2}L_2) - \lambda_{b1}\lambda_{b3}\coth(\lambda_{b1}L_1)\coth(\lambda_{b3}L_3), \tag{B.10}$$

$$e' = \lambda_{b2}\lambda_{b3}\operatorname{cosech}(\lambda_{b2}L_2)\coth(\lambda_{b3}L_3) - \lambda_{b2}\lambda_{b3}\coth(\lambda_{b2}L_2)\coth(\lambda_{b3}L_3) - \lambda_{b2}^2, \tag{B.11}$$

$$f' = -\lambda_{b2}\lambda_{b3}\operatorname{cosech}(\lambda_{b2}L_2)\coth(\lambda_{b3}L_3), \tag{B.12}$$

$$g' = V_{bi}\left(\lambda_{b1}\lambda_{b2}\operatorname{cosech}(\lambda_{b1}L_1)\coth(\lambda_{b2}L_2) + \lambda_{b1}\lambda_{b3}\operatorname{cosech}(\lambda_{b1}L_1)\coth(\lambda_{b3}L_3) + \lambda_{b2}\lambda_{b3}\operatorname{cosech}(\lambda_{b2}L_2)\operatorname{cosech}(\lambda_{b3}L_3)\right), \tag{B.13}$$

$$r' = \coth(\lambda_{b1}L_1)\operatorname{cosech}(\lambda_{b1}L_1) + \operatorname{cosech}^2(\lambda_{b1}L_1). \tag{B.14}$$

The values of G_{b1}, G_{b2}, G_{b3}, n_b, λ_{b1}, λ_{b2}, and λ_{b3} are taken from [17].

Data Availability

The data used to support the findings of this study are included within the article.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

Acknowledgments

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