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Design and analysis of power-CMOS-gate-based switched-capacitor DC–DC converter with step-down and step-up modes — Source link

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Published on: 01 Sep 2003 - International Journal of Circuit Theory and Applications (Wiley)

Topics: Boost converter, Circuit design, Electrical efficiency, Maximum power principle and Switched capacitor

Design and Analysis of Power-CMOS-Gate-Based Switched-Capacitor Boost DC–AC Inverter

Yuen-Haw Chang

***Abstract*—A multistage power CMOS-transmission-gate-based (CMOS-TG) quasi-switched-capacitor (QSC) boost dc–ac inverter is proposed and integrated with a boost dc–dc converter for a step-up application with ac or dc load. In this paper, using CMOS-TG as a bidirectional switch, the various topologies can be integrated in the same configuration for achieving two functions: boosting and alternating; boosting for getting a sinusoidal output in which the peak is the result of a many times step-up of the input; alternating to realize the positive/negative half sinusoidal of the output. The inverter does not require any inductive elements as inductor and transformer, so integrated circuit (IC) fabrication will be promising for realization. By using the state-space averaging technique, the large-signal state-space model of the inverter is proposed, and then both the static analysis and dynamic small-signal analysis are derived to form a unified formulation for inverter/converter. Based on this formulation, there are presented for theoretical analysis/control design, including steady-state power, conversion efficiency, voltage conversion ratio, output ripple percentage, capacitance selection, closed-loop control and stability, and total harmonic distortion (THD), etc. Finally, a six-stage QSC boost dc–ac inverter is simulated by PSPICE, and the simulations are discussed for some cases, including: 1) steady-state ac output, ripple percentage, and power efficiency; 2) transient response of the regulated inverter for load variation; 3) a practical capacitive load: electromagnetic luminescent (EL) lamp, and 4) efficiency, ripple percentage, and THD for different loads. The results are illustrated to show the efficacy of the proposed inverter.**

***Index Terms*—CMOS-transmission-gate-based (CMOS-TG), quasi-switched-capacitor (QSC), boost DC–AC inverter, state-space averaging technique, total harmonic distortion (THD).**

I. Introduction

With the coming of mobile-commerce generation, various portable electronic equipments have been produced and easily available, for example, PDA, notebook, cellular phone, digital camera, pager, e-book... etc. Such products emphasize some specific characteristics, for example, mobile convenience, integrated communication function, small volume, light weight, long-time high efficiency, and various sources (dc–dc/dc–ac). Recently, the portable systems always ask an increasing demand for a new dc–ac inverter module with small volume, light weight, high power density, high power efficiency, good regulation and reliability even if load/source variation happens. More researchers pay much attention to this topic about developing a more effective converter/inverter for step-up application with dc or ac load, for example, white light emitting diode and electromagnetic luminescent (EL) lamp, ultimately requiring dc–ac inverters realized on a chip by mixed-mode VLSI technology.

The common inverter always contains the magnetic elements, and so it results in the electromagnetic interference (EMI) problem. For avoiding the EMI effect, it is a quite excellent choice to adopt a switched-capacitor (SC) circuit scheme, containing only capacitors and transistors. Although the SC circuits lead to efficiency problem, it is the most excellent one of their advantages that the SC circuits do not require any magnetic elements (inductor/transformer), so the IC fabrication is not only promising but the EMI problem is also improved. The idea of SC circuit has existed for nearly half a century, and based on SC idea, Brugler suggested SC voltage multiplier [1], and then Lin and Chua presented topological generation and analysis of voltage multiplier [2]. The recent reinvention is mainly to take advantage of the active MOSFET switches for power conversion and output regulation. In 1990, the first SC step-down dc–dc converter was successfully proposed from Japan [3], [4]. Next, researchers followed this idea to get more extensions, including rectifier–inverter types, even for transient/steady-state analysis [5]–[7]. Nevertheless, some disadvantages still existed as: 1) since it has zero input current in the even period, such discontinuity results easily in the EMI problem and 2) since the voltage conversion ratio is usually predetermined by the circuit configuration, the ratio value cannot be regulated flexibly. In 1993, Cheong, Chung and Ioinovici suggested a new SC converter configuration, composed of two symmetric SC cells to operate cyclically in antiphase (charge–discharge) per cycle [8]. In the first half-cycle, the capacitors in one SC cell are in a charging phase by a constant voltage source, and at the same time the capacitors in the other SC cell discharge on the load. Then, in the second half-cycle, these two cells interchange their roles. Using pulsewidth modulation (PWM) technique, a new dc–dc converter followed on this idea, and then the output regulation was achieved by duty-cycle adjustment [9]–[11]. Although the output regulation was more flexible, some drawbacks still existed as: 1) the discontinuity still results in the EMI problem and 2) with duty-cycle control, a smaller output voltage always needs a small duty cycle, but such a short duration makes implementation more difficult.

In 1996, Chung and Ioinovici suggested a completely new converter scheme, called quasi-switched-capacitor (QSC) step-down converter, by using continuous input current control [12].

Manuscript received December 4, 2003; revised March 9, 2004 and April 12, 2004. This work was supported in part by the National Science Council of Taiwan, R.O.C., under NSC92-2213-E-324-004. This paper was recommended by Associate Editor A. Ioinovici.

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Digital Object Identifier 10.1109/TCSI.2004.835681

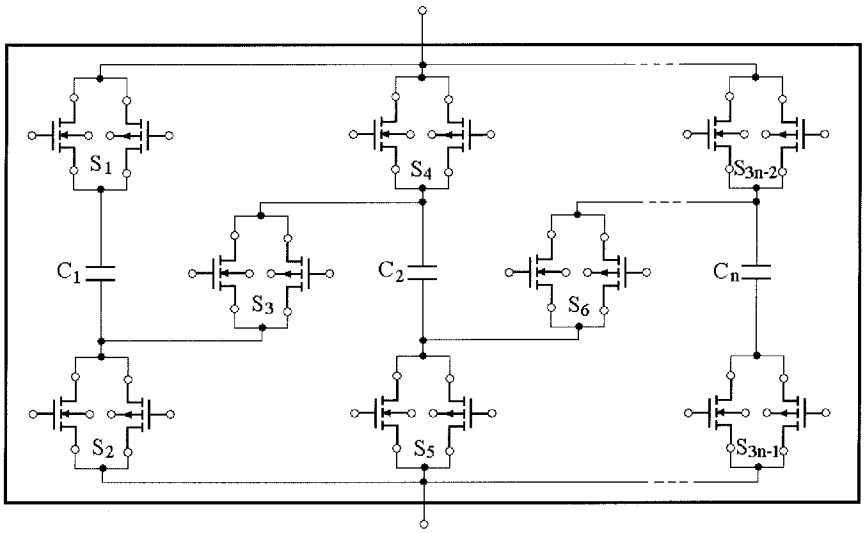

Fig. 1. n-stage SC cell.

This QSC converter scheme is similar to the one proposed in 1993, i.e., the QSC converter is also composed of two symmetric SC cells, and the two SC cells are also working in antiphase, but the most different one between them is to use a constant current source (current-mode control), not to use a constant voltage source as above. In this scheme, some active MOSFETs are working in pinch-off region, and they can be treated as current sources (controlled by the gate–source voltage of MOSFET), so as to increase the capacitor voltage linearly in a charging phase, not exponentially as above. Since the input current is constant continuously, not variant discontinuously as above, the EMI problem is much improved. Besides, the scheme utilizes these controlled current sources to adjust output voltage, and it belongs to current-mode control, not duty cycle, so the above short duration problem can be avoided. From 1999, researchers were concentrated on regulation improvement and capability enhancement [13]–[19]. Henry suggested a multistage design for improving voltage regulation and current capability [13]. For step-down, capacitors are connected in parallel in a discharging phase, and then the larger output current is produced for the heavier load [12]. For step-up, capacitors are in series in a discharging phase for higher output voltage [15]. In 2003, following up these ideas, Chang proposed a CMOS-TG QSC dc–dc converter with both step-down and step-up modes in one unified configuration [19].

II. Configuration of QSC Boost DC–AC Inverter

A. One n-Stage SC Cell Using Power CMOS-TG

Fig. 1 shows one n-stage SC cell, including n capacitors $(C_1, C_2 \ldots C_n)$, and $3n-1$ power CMOS-TG $(S_1, S_2 \ldots S_{3n-1})$. Each capacitor has capacitance C with equivalent series resistance (ESR) r_C, and similarly the output capacitor has capacitance C_o with ESR r_{Co}. The CMOS-TG $S_1, S_2 \ldots S_{3n-1}$ are treated as bidirectional switches, consisting of power PMOS and NMOS as shown in Fig. 2. The TG is controlled by two complementary signals v_g and $\bar{v}_g$. When v_g is at the lowest voltage V_L of circuit, the switch is turned off between $v_{\rm in}$ and $v_{\rm out}$. Contrary, when v_g is at the highest

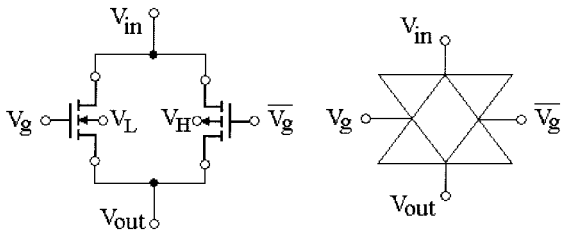

Fig. 2. Power CMOS transmission gate.

voltage V_H, the switch is in turn-on state. Here, it is notable that the turn-on resistance r_T of power-level CMOS-TG is quite small and constant because both channel resistances of pMOS and nMOS are connected in parallel (as the resistance of one MOSFET decreases, the resistance of the other MOSFET increases). Here, power CMOS-TG is adopted with increasing three advantages as follows. 1) It is much helpful to integrate step-up function of positive/negative half sinusoidal into one circuit configuration. 2) It gets higher efficiency since the turn-on resistance of CMOS-TG is constant and small enough to reduce power loss. 3) Since CMOS-TG can be operated at pretty high frequency, output ripple and THD are lessened possibly.

B. Configuration of n-Stage QSC Boost DC–DC Converter

Based on the above SC cell, a QSC boost dc–dc converter configuration is suggested as shown in Fig. 3, [12], [13]. The converter is mainly composed of two SC cells in parallel between source $\rm V_S$ and output v_o, denoted by cells A and B, and they are working cyclically in antiphase. For the first half-cycle [as topology of Fig. 4(a)], let $\rm QS_A$ be in pinch-off region as a controlled constant current source, turn off S_A and $\rm QS_B$, turn on S_B in triode region as a small resistor. Thus, n capacitors $C_{A1} \sim C_{An}$ in cell A are linearly charged in parallel by constant current source as circuit of Fig. 5(a). At the same time, n capacitors $C_{B1} \sim C_{Bn}$ in cell B are discharging in series on load R_L as circuit of Fig. 5(b). For the second half-cycle [as topology of Fig. 4(b)], cells $\rm A \sim B$ interchange their operations, and then vice versa. So, the theoretical waveforms can be figured out as

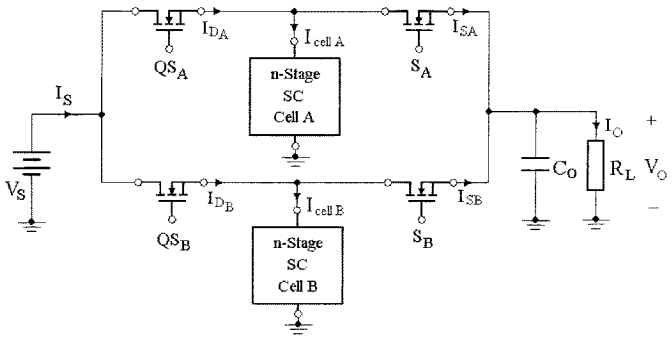

Fig. 3. Configuration of QSC boost dc–dc converter.

shown in Fig. 6. So, it is obvious that the duty cycle is fixed at 0.5 for each cell. With charging in parallel and discharging in series for n capacitors cyclically, the boost function can be realized for keeping output v_o up to $n \cdot \mathrm{V_S}$ ideally. In this research, such a dc–dc scheme is employed with increasing three advantages as follows. 1) Since QSC is adopted, input current $\mathrm{I_S}$ is continuous theoretically, so EMI problem is much improved. 2) Since the inverter contains only MOSFETs and capacitors, such a uniform characteristic is helpful to integrated circuit (IC) fabrication and design. 3) Since two cells work complementarily, such a constant duty cycle is useful to control design and theoretical analysis later.

C. Configuration of n-Stage QSC Boost DC–AC Inverter

Based on the above dc–dc scheme, a new n-stage QSC boost dc–ac inverter is suggested as shown in Fig. 7, mainly consisting of two n-stage SC cells A/B and a set of positive/negative dc voltage sources. Comparing the inverter of Fig. 7 with the converter of Fig. 3, the most different one between them is to employ dc-link voltage scheme for alternating positive/negative half-sinusoidal output. Actually, a single source $\mathrm{V_S}$ and an extra full-bridge topology are also able to form a pair of positive and negative sources. Here, for simplifying the circuit analysis process, we presume that a set of voltage sources is available for the moment.

For implementing ac output with frequency f (output cycle $T = 1/f$), we have two goals to do—boosting output and alternating output. First, one cycle T is divided into m time durations $\Delta T(\Delta T = T/m)$, and then the QSC boost dc–dc converter is employed in each of two time durations. In other words, within each of two time durations, the inverter behaves like a boost dc–dc converter (For one time duration, when cell A is working in a parallel-capacitor-charging phase, cell B is working in a series-capacitor-discharging phase. For the next one, cells A and B interchange their works). Thus, in each of time duration, the different output voltage can be boosted by the controlled current sources (drain currents of $\mathrm{QS}_{Ap}, \mathrm{QS}_{An}, \mathrm{QS}_{Bp}, \mathrm{QS}_{Bn}$), where $\mathrm{QS}_{Ap}, \mathrm{QS}_{Bp}$ can be used to handle positive half-sinusoidal and $\mathrm{QS}_{An}, \mathrm{QS}_{Bn}$ are for negative half-sinusoidal. So, a staircase sinusoidal output can be reconstructed by such the different boost and alternative voltage levels, and the theoretical waveforms of inverter are shown in Fig. 8. Thus, the SC switching cycle T_s is taken by two times of duration $\Delta T(T_s = 2 \cdot \Delta T)$, and the relationship between switching frequency $f_s(f_s = 1/T_s)$ and output frequency f is derived as

$$f_s = m \cdot f/2. \tag{1}$$

In this research, the proposed QSC boost dc–ac inverter scheme has some extra advantages as follows. 1) The switching frequency f_s can be flexibly selected as higher as possible, and then it results in the bigger m and the smaller duration ΔT, so it leads more excellent total harmonic distortion (THD). 2) The number of stage (n) is selected mainly relative to the times between ac output peak voltage and source voltage. The number of duration (m) is selected mainly relative to the desired THD. In this research, the values of n and m can be selected flexibly and independently. Due to the independent selection, it is not needed in our research to increase the number of stage for THD reduction, and the result is quite different from that of [18]. So, a smaller size and lower weight of the proposed inverter will be realized more possibly.

III. Formulation of QSC Boost DC–AC Inverter

In this section, a unified static analysis/dynamic small-signal analysis of n-stage QSC boost dc–ac inverter will be presented. For simplification, all capacitors in cells $\mathrm{A} \sim \mathrm{B}$ are selected by the same value: $C_{A1} = \cdots = C_{An} = C_{B1} = \cdots = C_{Bn} = C$, so each capacitor voltage in the same cell is assumed identical, denoted by $v_{C,A}(t)/v_{C,B}(t)$ for cells A/B respectively.

A. Formulation of n-Stage QSC Boost DC–DC Converter

First, let us look at the modeling of QSC boost dc–dc converter. When cell A is working in a charging phase as Fig. 5(a), QS_A is in pinch-off region and the capacitors in cell A are linearly charged in parallel by drain current $i_{D,A}(t), i_{D,A} = \mathrm{K} \cdot [v_{SG,A}(t) - \mathrm{V_T}]^2$, where K and $\mathrm{V_T}$ are the process parameter and the threshold voltage of MOSFET, so

$$v'_{C,A}(t) = \frac{1}{nC} \cdot i_{D,A}(t). \tag{2}$$

For keeping QS_A pinch-off, $v_{SG,A}/v_{DG,A}$ of MOSFET must be larger/smaller than $\mathrm{V_T}$, so the pinch-off condition can be derived as

$$\mathrm{V_S} > v_{C,A} + i_{D,A} \cdot (r_C + 2r_T)/n. \tag{3}$$

At the same time, cell B is in a discharging phase as Fig. 5(b), and S_B is in triode region, the capacitors in cell B are discharging in series on load R_L, and the equation is

$$\begin{bmatrix} v'_{C,B}(t) \\ v'_{Co}(t) \end{bmatrix} = \begin{bmatrix} -\dfrac{n \cdot (r_{Co} + R_L)}{C \cdot \Delta} & \dfrac{R_L}{C \cdot \Delta} \\ \dfrac{n \cdot R_L}{C_o \cdot \Delta} & -\dfrac{r_n + r_T + R_L}{C_o \cdot \Delta} \end{bmatrix} \cdot \begin{bmatrix} v_{C,B}(t) \\ v_{Co}(t) \end{bmatrix} \tag{4a}$$

$$[v_o(t)] = \begin{bmatrix} \dfrac{n \cdot r_{Co} R_L}{\Delta} & \dfrac{(r_n + r_T) \cdot R_L}{\Delta} \end{bmatrix} \cdot \begin{bmatrix} v_{C,B}(t) \\ v_{Co}(t) \end{bmatrix} \tag{4b}$$

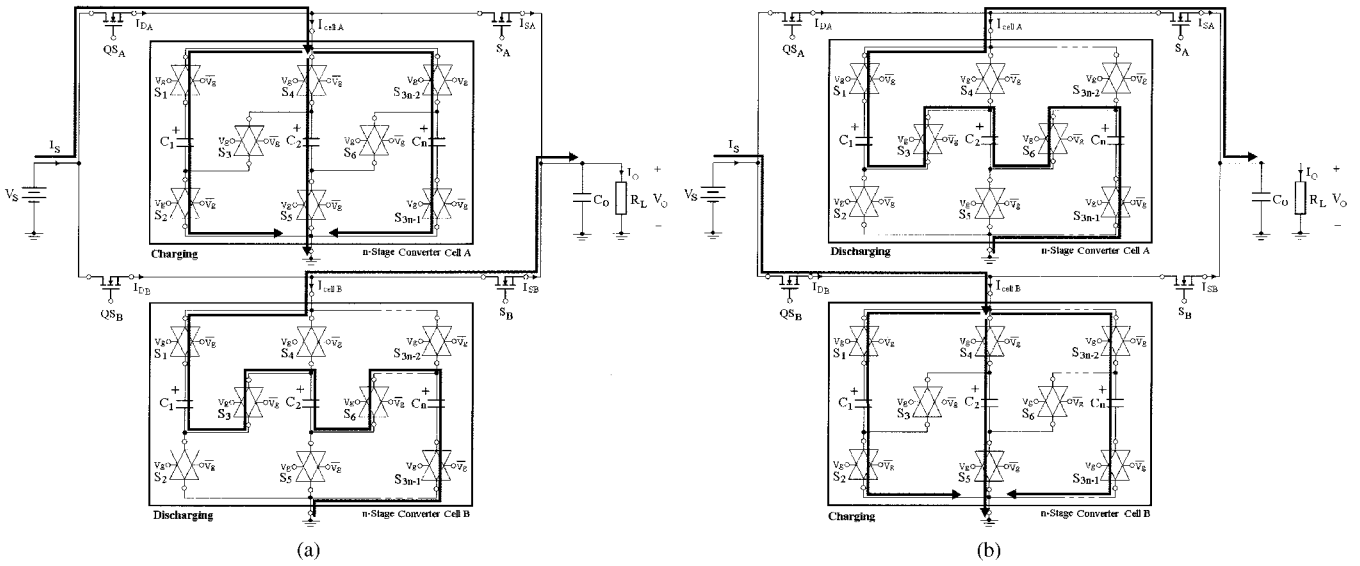

Fig. 4. (a) First half-cycle topology. (b) Second half-cycle topology.

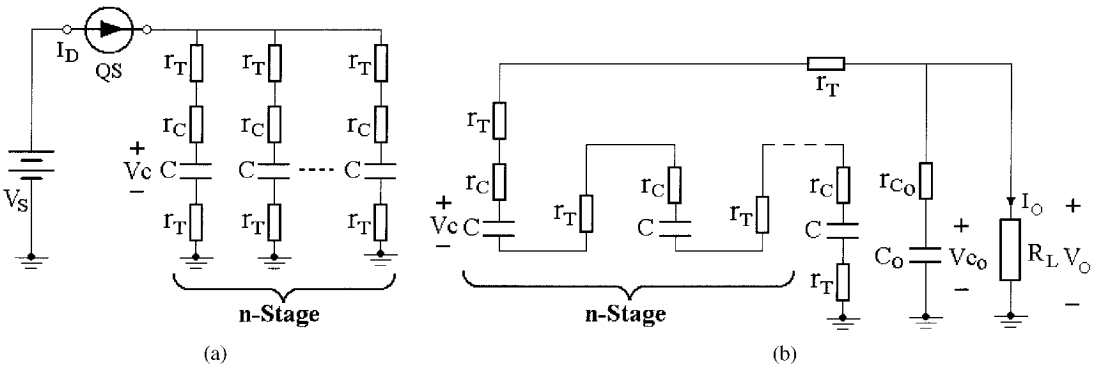

Fig. 5. (a) Topology in charging phase. (b) Topology in discharging phase.

where

$$r_n = nr_C + (n+1)r_T, \tag{5a}$$

$$\Delta = (r_T + r_n)(r_{Co} + R_L) + r_{Co}R_L \tag{5b}$$

in which $v_o(t), v_{Co}(t)$ represent output voltage and output capacitor voltages, respectively. By using state-space averaging technique (the duty cycle is 0.5) and taking the average of (2) and (4), the state-space equation of QSC boost dc–dc converter is

$$\begin{bmatrix} v'_{C,A} \\ v'_{C,B} \\ v'_{Co} \end{bmatrix} = \begin{bmatrix} -\dfrac{n\cdot(r_{Co}+R_L)}{2C\cdot\Delta} & 0 & \dfrac{R_L}{2C\cdot\Delta} \\ 0 & -\dfrac{n\cdot(r_{Co}+R_L)}{2C\cdot\Delta} & \dfrac{R_L}{2C\cdot\Delta} \\ \dfrac{n\cdot R_L}{2C_o\cdot\Delta} & \dfrac{n\cdot R_L}{2C_o\cdot\Delta} & -\dfrac{r_n+r_T+R_L}{C_o\cdot\Delta} \end{bmatrix} \cdot \begin{bmatrix} v_{C,A} \\ v_{C,B} \\ v_{Co} \end{bmatrix} + \begin{bmatrix} \frac{1}{2nC} \\ \frac{1}{2nC} \\ 0 \end{bmatrix} \cdot [i_D] \tag{6a}$$

$$[v_o] = \begin{bmatrix} \dfrac{n\cdot r_{Co}R_L}{2\Delta} & \dfrac{n\cdot r_{Co}R_L}{2\Delta} & \dfrac{(r_n+r_T)\cdot R_L}{\Delta} \end{bmatrix} \cdot \begin{bmatrix} v_{C,A} \\ v_{C,B} \\ v_{Co} \end{bmatrix} \tag{6b}$$

where $i_D(t)$ is the average of drain currents for cells A $\sim$ B($i_D(t) = 0.5 \cdot i_{D,A}(t) + 0.5 \cdot i_{D,B}(t)$). When cells A/B are working in the charging/discharging phase, the physical operation is $i_{D,A}(t) = \mathrm{K}\cdot[v_{SG,A}(t) - \mathrm{V_T}]^2, i_{D,B}(t) = 0$. When cells A/B are in the discharging/charging phase, the operation is $i_{D,A}(t) = 0, i_{D,B}(t) = \mathrm{K}\cdot[v_{SG,B}(t) - \mathrm{V_T}]^2$. Here, it is worthy to be concerned that drain currents $i_{D,A}(t), i_{D,B}(t)$ have only one direction, so the boosting function of dc–dc conversion can be achieved, but the alternating function of dc–ac conversion cannot be realized because there cannot produce reverse drain current in this dc–dc scheme of Fig. 3. So, a set of positive/negative dc-link sources is employed for alternating conversion later.

B. Formulation of n-Stage QSC Boost DC–DC Inverter

A set of positive/negative dc-link voltage sources is employed and combined with the above dc–dc scheme, and then a

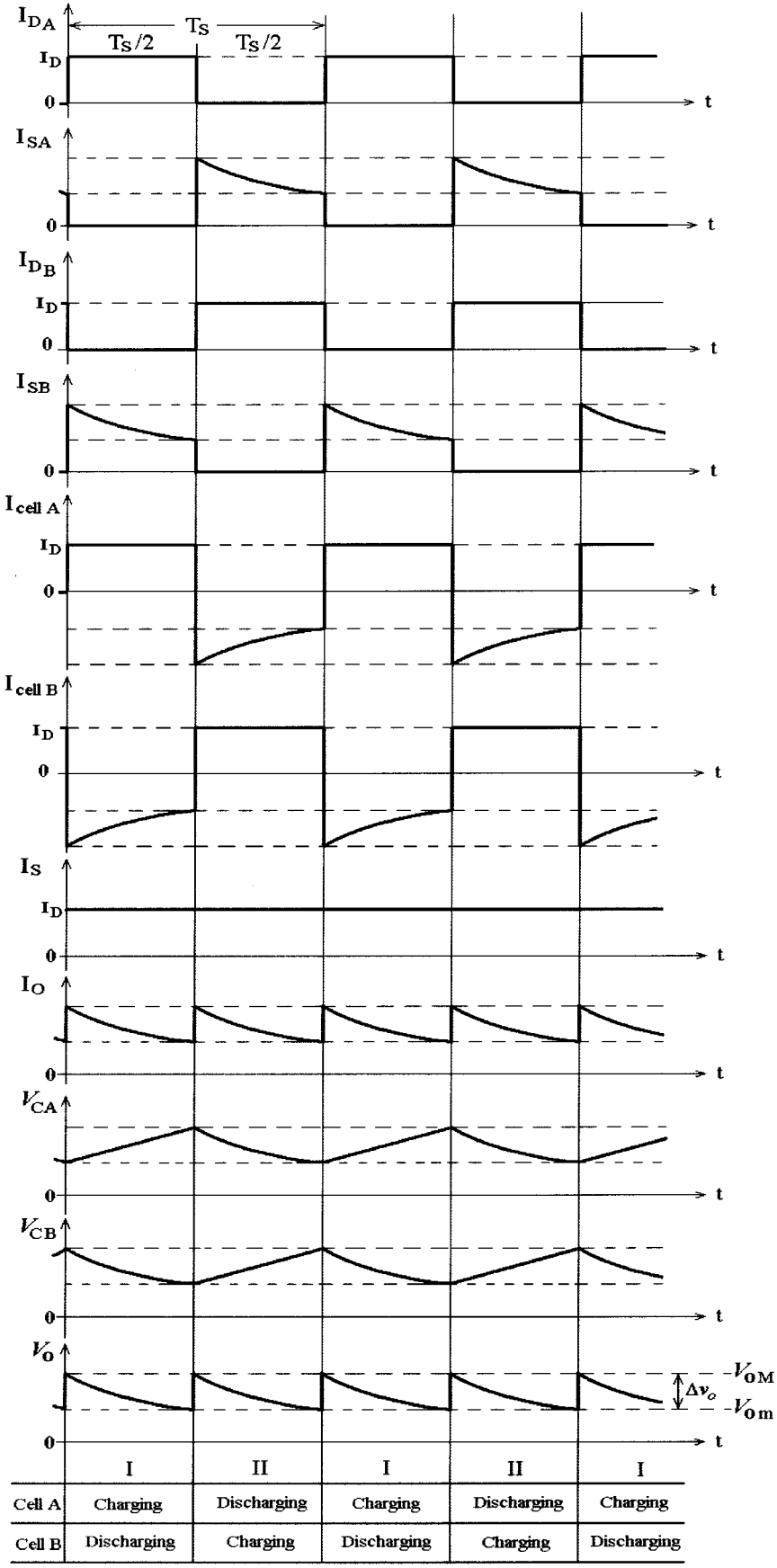

Fig. 6. Theoretical waveforms of QSC boost dc–dc converter.

new QSC boost dc–ac inverter is proposed as shown in Fig. 7. In the cell A of Fig. 7, there are two MOSFETs $\mathrm{QS}_{Ap}, \mathrm{QS}_{An}$ connected, respectively, with positive and negative sources ($+\mathrm{V_S}$ and $-\mathrm{V_S}$), and the connection of $\mathrm{QS}_{Bp}, \mathrm{QS}_{Bn}$ in cell B is

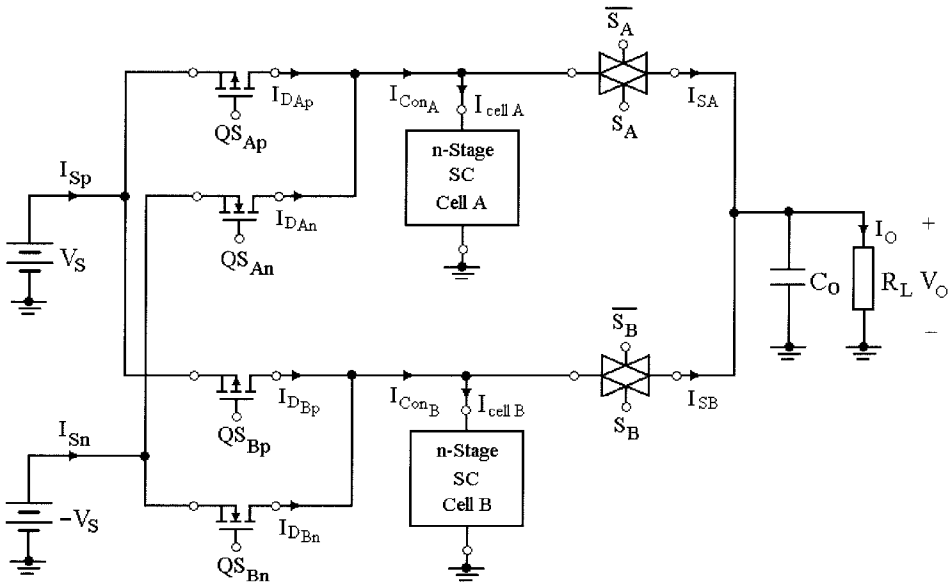

Fig. 7. Configuration of QSC boost dc–ac inverter.

similar to that in cell A. When positive-half sinusoid is desired, PMOS $\mathrm{QS}_{Ap}, \mathrm{QS}_{Bp}$ are working in antiphase, and the positive currents $i_{D,Ap}, i_{D,Bp}$ can be produced by $v_{SG,Ap}, v_{SG,Bp}$ based on the positive source $+\mathrm{V_S}$. When negative-half sinusoid is desired, NMOS $\mathrm{QS}_{An}, \mathrm{QS}_{Bn}$ are working in antiphase, and the negative currents $i_{D,An}, i_{D,Bn}$ are produced by $v_{GS,An}, v_{GS,Bn}$ based on the negative source $-\mathrm{V_S}$. Table I shows the scheduled timing operation between them (The same parameters are assumed by $\mathrm{K_p} = \mathrm{K_n} \equiv \mathrm{K}, \mathrm{V_{Tp}} = \mathrm{V_{Tn}} \equiv \mathrm{V_T}$ here). Thus, according to Fig. 7, control currents $i_{\mathrm{Con},A}, i_{\mathrm{Con},B}$ of cells $\mathrm{A} \sim \mathrm{B}$ are described by

$$i_{\mathrm{Con},A}(t) = i_{D,Ap}(t) + i_{D,An}(t) \tag{7a}$$

$$i_{\mathrm{Con},B}(t) = i_{D,Bp}(t) + i_{D,Bn}(t) \tag{7b}$$

where it is worthy to be concerned as follows. 1) Control currents $i_{\mathrm{Con},A}, i_{\mathrm{Con},B}$ are similar to drain currents $i_{D,A}, i_{D,B}$ of the dc–dc scheme. 2) Control currents $i_{\mathrm{Con},A}, i_{\mathrm{Con},B}$ contain both positive and negative current components $(i_{D,Ap}, i_{D,An}/i_{D,Bp}, i_{D,Bn})$, respectively.

By applying state-space averaging technique, based on dc–dc formulation of (6), a completely integrated state-space description of QSC boost dc–ac inverter can be derived as

$$x'(t) = A_{\mathrm{av}} \cdot x(t) + B_{\mathrm{av}} \cdot u(t) \tag{8a}$$

$$y(t) = C_{\mathrm{av}} \cdot x(t) \tag{8b}$$

where

$$x(t) = [v_{C,A}(t) \quad v_{C,B}(t) \quad v_{Co}(t)]^T \tag{9a}$$

$$u(t) = [i_{\mathrm{Con}}(t)] \tag{9b}$$

$$y(t) = [v_o(t)] \tag{9c}$$

TABLE I
TIMING OPERATION OF QSC MOSFETS $(f(v) = K \cdot [v - V_T]^2)$

QSC out		SC Cell A		SC Cell B	
		QS_{Ap}	QS_{An}	QS_{Bp}	QS_{Bn}
Positive-Half Sinusoid	Phase 1	$i_{D,Ap} = f(v_{SG,Ap})$	$i_{D,An} = 0$	$i_{D,Bp} = 0$	$i_{D,Bn} = 0$
	Phase 2	$i_{D,Ap} = 0$	$i_{D,An} = 0$	$i_{D,Bp} = f(v_{SG,Bp})$	$i_{D,Bn} = 0$
Negative-Half Sinusoid	Phase 1	$i_{D,Ap} = 0$	$i_{D,An} = -f(v_{GS,An})$	$i_{D,Bp} = 0$	$i_{D,Bn} = 0$
	Phase 2	$i_{D,Ap} = 0$	$i_{D,An} = 0$	$i_{D,Bp} = 0$	$i_{D,Bn} = -f(v_{GS,Bn})$

$$A_{\mathrm{av}} = \begin{bmatrix} -\dfrac{n(r_{Co}+R_L)}{2C\cdot\Delta} & 0 & \dfrac{R_L}{2C\cdot\Delta} \\ 0 & -\dfrac{n(r_{Co}+R_L)}{2C\cdot\Delta} & \dfrac{R_L}{2C\cdot\Delta} \\ \dfrac{nR_L}{2C_o\cdot\Delta} & \dfrac{nR_L}{2C_o\cdot\Delta} & -\dfrac{r_n+r_T+R_L}{C_o\cdot\Delta} \end{bmatrix} \tag{9d}$$

$$B_{\mathrm{av}} = \begin{bmatrix} \dfrac{1}{2nC} \\ \dfrac{1}{2nC} \\ 0 \end{bmatrix} \tag{9e}$$

$$C_{\mathrm{av}} = \begin{bmatrix} \dfrac{nr_{Co}R_L}{2\Delta} & \dfrac{nr_{Co}R_L}{2\Delta} & \dfrac{(r_n+r_T)R_L}{\Delta} \end{bmatrix} \tag{9f}$$

where $i_{\mathrm{Con}}(t)$ represents the averaging value of the control currents of cells A and B as

$$i_{\mathrm{Con}}(t) = 0.5 \cdot i_{\mathrm{Con},A}(t) + 0.5 \cdot i_{\mathrm{Con},B}(t). \tag{10}$$

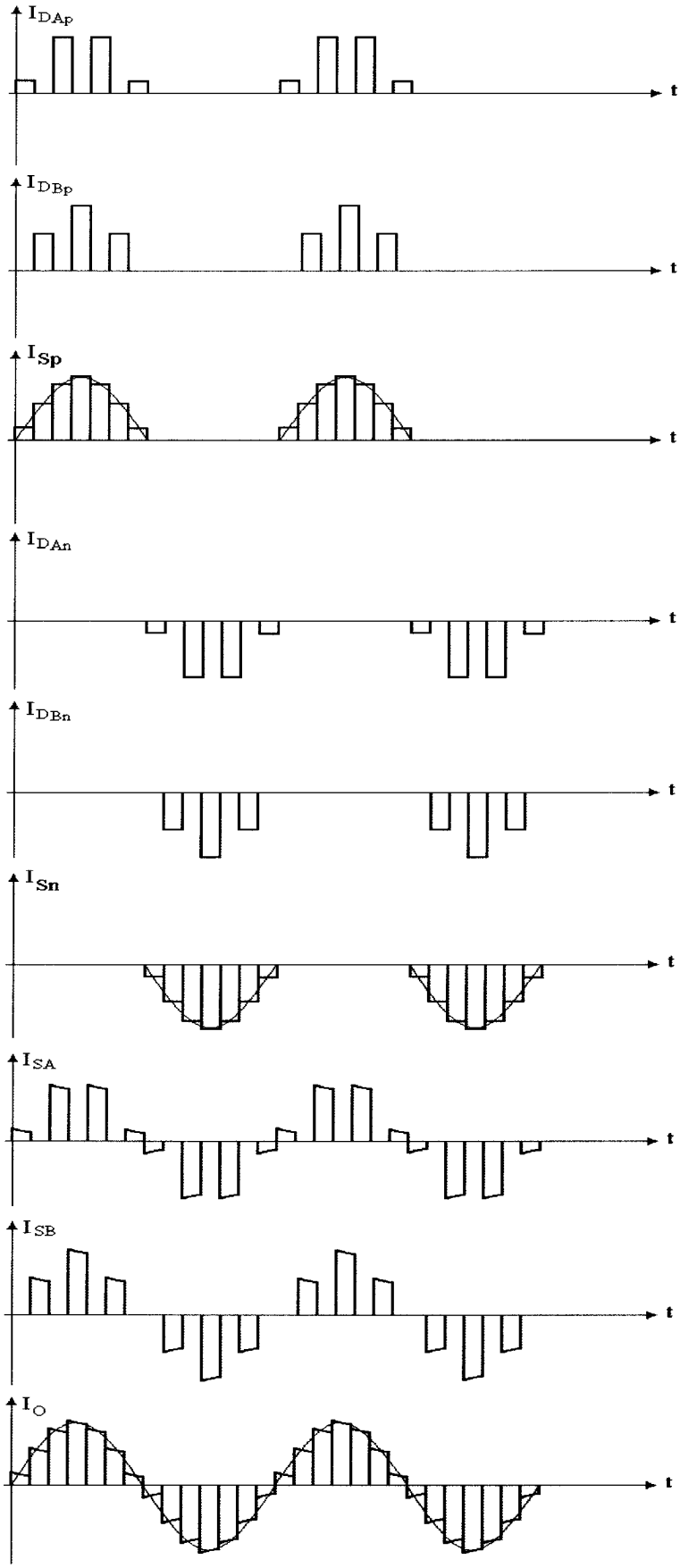

Fig. 8. Theoretical waveforms of QSC boost dc–ac inverter.

Here, it is found by analogy that i_{Con} is similar to the averaging drain current i_D of the dc–dc scheme. But, since i_{Con} is composed of $i_{\mathrm{Con},A}, i_{\mathrm{Con},B}$, which are with positive or negative components, i_{Con} is a bidirectional current so that the scheme

TABLE II
SIMPLIFIED TIMING OPERATION OF QSC MOSFETS

QSC out		SC Cell A		SC Cell B	
		QS_{Ap}	QS_{An}	QS_{Bp}	QS_{Bn}
Positive-Half Sinusoid	Phase 1	$v_{SG,Ap} = \lvert v_{Con}\rvert$	$v_{GS,An} = 0$	$v_{SG,Bp} = 0$	$v_{GS,Bn} = 0$
	Phase 2	$v_{SG,Ap} = 0$	$v_{GS,An} = 0$	$v_{SG,Bp} = \lvert v_{Con}\rvert$	$v_{GS,An} = 0$
Negative-Half Sinusoid	Phase 1	$v_{SG,Ap} = 0$	$v_{GS,An} = \lvert v_{Con}\rvert$	$v_{SG,Bp} = 0$	$v_{GS,An} = 0$
	Phase 2	$v_{SG,Ap} = 0$	$v_{GS,An} = 0$	$v_{SG,Bp} = 0$	$v_{GS,An} = \lvert v_{Con}\rvert$

is able to realize the alternative conversion. Besides, if $i_{\rm Con}$ is operated in single direction, then the boost dc–ac description of (8) shows the behavior of boost dc–dc converter as (6).

C. Static and Dynamic Analysis of Boost DC–AC Inverter

For static and dynamic analysis, all voltages and currents of (8) are composed of two parts: static signals and dynamic signals

$$\begin{aligned} v_{C,A}(t) &= \mathrm{V_{C,A}} + \hat{v}_{C,A}(t), v_{C,B}(t) = \mathrm{V_{C,B}} + \hat{v}_{C,B}(t) \\ v_{Co}(t) &= \mathrm{V}_{Co} + \hat{v}_{Co}(t), i_{\rm Con}(t) = \mathrm{I_{Con}} + \hat{i}_{\rm Con}(t) \\ v_O(t) &= \mathrm{V_o} + \hat{v}_o(t) \end{aligned}$$

where $\mathrm{V_{C,A}}, \mathrm{V_{C,B}}, \mathrm{V}_{Co}, \mathrm{I_{Con}}, \mathrm{V_o}$ represent the average signals within one time duration, and $\hat{v}_{C,A}, \hat{v}_{C,B}, \hat{v}_{Co}, \hat{i}_{\rm Con}, \hat{v}_o$ indicate the dynamic signals within one time duration. In other words, $\mathrm{V_{C,A}}, \mathrm{V_{C,B}}, \mathrm{V}_{Co}, \mathrm{I_{Con}}, \mathrm{V_o}$ can be treated as static operating signals within one time duration, and $\hat{v}_{C,A}, \hat{v}_{C,B}, \hat{v}_{Co}, \hat{i}_{\rm Con}, \hat{v}_o$ are regarded as dynamic small signals within one time duration. First, for static analysis, by substituting $x'(t) = 0$ of (8), static output voltage $\mathrm{V_o}$ and output current $\mathrm{I_o}$ can be derived as

- *Static operating output analysis:*

$$\mathrm{V_o} = -C_{\rm av} \cdot A_{\rm av}^{-1} \cdot B_{\rm av} \cdot u = \frac{1}{n} \cdot R_L \cdot \mathrm{I_{Con}} \tag{11a}$$

$$\mathrm{I_o} = \frac{\mathrm{V_o}}{R_L} = \frac{1}{n} \cdot \mathrm{I_{Con}}. \tag{11b}$$

Here, it is notable that both output voltage $\mathrm{V_o}$ and current $\mathrm{I_o}$ are functional relations with static control current $\mathrm{I_{Con}}$ (current-mode control), not directly affected by source voltage $\mathrm{V_S}$ theoretically. In other words, when $\mathrm{V_S}$ is decreasing a little, $\mathrm{V_o}$ and $\mathrm{I_o}$ cannot be affected immediately, and it is the reason that $\mathrm{V_S}$ is not directly connected to load R_L in any phase as Fig. 4(a) and (b), so the variation of $\mathrm{V_S}$ will not make immediate influence on $\mathrm{V_o}, \mathrm{I_o}$. That is one of advantages: it could have better robustness against source variation or noise.

For simplification, let us take a new cell capacitor voltage $v_C(t) = [v_{C,A}(t) + v_{C,B}(t)]/2$, and it also includes two parts: static operating signal and dynamic small signal as $v_C(t) = \mathrm{V_C} + \hat{v}_C(t)$. Substituting output matrix $C_{\rm av}$, static cell capacitor voltage $\mathrm{V_C}$ and output capacitor voltage V_{Co} can be also obtained as

$$\begin{aligned} \mathrm{V_C} &= \frac{\mathrm{V_{Ca}} + \mathrm{V_{Cb}}}{2} \\ &= -\frac{1}{2} \cdot [1 \quad 1 \quad 0] \cdot A_{\rm av}^{-1} \cdot B_{\rm av} \cdot u \\ &= \frac{1}{n} \cdot (r_m + r_T + R_L) \cdot \mathrm{I_{Con}} \end{aligned} \tag{12a}$$

$$\begin{aligned} \mathrm{V}_{Co} &= -[0 \quad 0 \quad 1] \cdot A_{\rm av}^{-1} \cdot B_{\rm av} \cdot u \\ &= \frac{1}{n} \cdot R_L \cdot \mathrm{I_{Con}}. \end{aligned} \tag{12b}$$

Next, let's derive the formulation for dynamic analysis. Around one static operating point, following by using the small-signal analysis, the dynamic small-signal state-space equation of QSC boost dc–ac inverter/dc–dc converter can be easily presented in (13), and consequently their small-signal transfer function can be also suggested in (14):

- *Dynamic small-signal state-space expression:*

$$\begin{bmatrix} \hat{v}_C'(t) \\ \hat{v}_{Co}'(t) \end{bmatrix} = \begin{bmatrix} -\dfrac{n(r_{Co} + R_L)}{2C \cdot \Delta} & \dfrac{nR_L}{2C \cdot \Delta} \\ \dfrac{nR_L}{C_o \cdot \Delta} & -\dfrac{r_T + r_n + R_L}{C_o \cdot \Delta} \end{bmatrix} \cdot \begin{bmatrix} \hat{v}_C(t) \\ \hat{v}_{Co}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{2nC} \\ 0 \end{bmatrix} \cdot [\hat{i}_{\rm Con}(t)] \tag{13a}$$

$$[\hat{v}_o(t)] = \begin{bmatrix} \dfrac{nr_{Co}R_L}{\Delta} & \dfrac{(r_n + r_T)R_L}{\Delta} \end{bmatrix} \begin{bmatrix} \hat{v}_C(t) \\ \hat{v}_{Co}(t) \end{bmatrix} \tag{13b}$$

- *Dynamic small-signal transfer function expression:*

$$\begin{aligned} G(s) &= \frac{\hat{v}_o(s)}{\hat{i}_{\rm Con}(s)} \\ &= \frac{\frac{r_{Co}R_L}{2C \cdot \Delta} \cdot \left(s + \frac{1}{r_{Co}C_o}\right)}{s^2 + \frac{nC_o(r_{Co} + R_L) + 2C(r_T + r_n + R_L)}{2CC_o \cdot \Delta} \cdot s + \frac{n}{2CC_o \cdot \Delta}}. \end{aligned} \tag{14}$$

Here, the small-signal open-loop model of the inverter has been presented as the above two forms, and then some compensation techniques can be applied, for example, state feedback or proportional compensation, to form a closed-loop feedback inverter system for more excellent performance.

IV. DESIGN AND ANALYSIS OF QSC BOOST DC–AC INVERTER

A. Output Power and Power Conversion Efficiency

According to Fig. 8, input currents $\mathrm{I_{Sp}}, \mathrm{I_{Sn}}$ through sources $+\mathrm{V_S}, -\mathrm{V_S}$ show positive/negative half-sinusoidal waveforms, respectively, and the average values of them can be expressed by: $\mathrm{I_{Sp}} = \mathrm{I_{S,m}}/\pi, \mathrm{I_{Sn}} = \mathrm{I_{S,m}}/\pi$ ($\mathrm{I_{S,m}}$ is the ac maximum peak value of $\mathrm{I_{Sp}}, \mathrm{I_{Sn}}$). Here, it must be under infinite m that complete half-sinusoidal of the input current exists. Actually, if the

switching frequency f_s is selected much larger than output frequency f, then m is regarded as almost infinite. So, the steady-state input power of the inverter is

$$\mathrm{P_i} = \mathrm{V_S} \cdot \mathrm{I_{Sp}} + \mathrm{V_S} \cdot \mathrm{I_{Sn}} = 2 \cdot \mathrm{V_S} \cdot \frac{\mathrm{I_{S,m}}}{\pi}. \tag{15}$$

According to the topology as Fig. 7, the maximum value of control currents $i_{\mathrm{Con},A}, i_{\mathrm{Con},B}$ is obviously identical to the maximum value $\mathrm{I_{S,m}}$ of input currents $\mathrm{I_{Sp}}, \mathrm{I_{Sn}}$. Then, based on (11b), the relationship can be obtained as $\mathrm{I_{o,m}} = \mathrm{I_{S,m}}/n$ ($\mathrm{I_{o,m}}$ is the ac maximum peak value of output current). So, the steady-state output power of the inverter is estimated as

$$\mathrm{P_o} = \frac{1}{2} \cdot \mathrm{V_{o,m}} \cdot \mathrm{I_{o,m}} = \frac{1}{2} \cdot \mathrm{V_{o,m}} \cdot \frac{\mathrm{I_{S,m}}}{n} \tag{16}$$

where $\mathrm{V_{o,m}}$ is the magnitude of ac output voltage, and it also represents the maximum value of boost output levels in all time durations. In addition, $\mathrm{V_{o,m}}$ is also regulated by control current $\mathrm{I_{Con}}$ based on (11a). With (15) and (16), the power conversion efficiency can be derived as

$$\begin{aligned}\eta = \frac{\mathrm{P_o}}{\mathrm{P_i}} &= \left(\frac{1}{2} \cdot \mathrm{V_{o,m}} \cdot \frac{\mathrm{I_{S,m}}}{n}\right) \Big/ \left(2 \cdot \mathrm{V_S} \cdot \frac{\mathrm{I_{S,m}}}{\pi}\right) \\ &= \frac{\pi}{4} \cdot \frac{1}{n} \cdot \frac{\mathrm{V_{o,m}}}{\mathrm{V_S}} = \frac{\pi}{4} \cdot \frac{1}{n} \cdot M\end{aligned} \tag{17}$$

where $M = \mathrm{V_{o,m}}/\mathrm{V_S}$ represents the boost voltage conversion ratio, and it can be also regulated by control current $\mathrm{I_{Con}}$. So, efficiency η increases with increasing voltage conversion ratio M. Due to n-stage scheme employed, the ratio M is not larger than n, so the maximum value of power efficiency can only be smaller than 78.5% theoretically, i.e., $\eta < \pi/4 = 78.5\%$.

B. Maximum Voltage Conversion Ratio and Maximum Power Efficiency

From the above discussion, output voltage $\mathrm{V_o}$ and current $\mathrm{I_o}$ are not directly affected by source $\mathrm{V_S}$. However, due to the natural drop of $\mathrm{V_S}$, it's more and more difficult to keep QS MOSFETs in pinch-off region, so it makes the limitation of control current $\mathrm{I_{Con}}$, and then it will indirectly affect $\mathrm{V_o}$ and $\mathrm{I_o}$. So, substituting $\mathrm{V_C}$ of (12a) into pinch-off condition of (3), the limitation of control current $\mathrm{I_{Con}}$ can be derived as

$$\mathrm{I_{Con}} < \mathrm{I_{Con,max}} = \frac{n^2 \cdot \mathrm{V_S}}{R_L + 2nr_C + (3n+2)r_T}. \tag{18}$$

When $\mathrm{V_S}$ is decreasing, the limitation of $\mathrm{I_{Con}}$ is also decreasing, so the range of output voltage $\mathrm{V_o}$ and current $\mathrm{I_o}$ are affected indirectly. Besides, the limitation of $\mathrm{I_{Con}}$ must be still required within the safe drain current $\mathrm{I_{D,safe}}$ of MOSFET. If not to do so, then maybe it makes the MOSFET burned out. Based on (11b), (16), and (18), the maximum output power is

$$\begin{aligned}\mathrm{P_o} < \mathrm{P_{o,max}} &= \frac{1}{2} \cdot R_L \cdot \mathrm{I_{o,m}^2} \\ &= \frac{n^2 R_L \cdot \mathrm{V_S^2}}{2 \cdot [R_L + 2nr_C + (3n+2)r_T]^2}.\end{aligned} \tag{19}$$

For analyzing the maximum power efficiency, substituting (11a), (11b), and (12a) into (3), the maximum voltage conversion ratio is

$$M < M_{\max} = \frac{nR_L}{R_L + 2nr_C + (3n+2)r_T}. \tag{20}$$

Combining (17) and (20), the maximum power conversion efficiency can be derived as

$$\begin{aligned}\eta < \eta_{\max} &= \frac{\pi}{4} \cdot \frac{1}{n} \cdot M_{\max} \\ &= \frac{\pi}{4} \cdot \frac{R_L}{R_L + 2nr_C + (3n+2)r_T}.\end{aligned} \tag{21}$$

If discussed in ideal case, the parasitic elements, like CMOS turn-on resistance r_T and capacitor ESR r_C, are small enough to be neglected almost, then the maximum voltage conversion ratio $M_{\max}$ of (20) is closed to n, and so the maximum power efficiency of (21) is also near to 78.5%.

C. Output Voltage Ripple Percentage and Total Capacitance Selection

Within two time durations, i.e., in one switching cycle ($T_S = 2 \cdot \Delta T$), the dc–ac inverter shows the behavior of the dc–dc converter. So, within one switching cycle, the voltage waveforms are quite similar to those of Fig. 6. In Fig. 6, output voltage $v_o(t)$ is decaying exponentially within each half-cycle repeatedly, and it can be described as

$$v_o(t) = V_{o\mathrm{M}} \cdot e^{-t/\tau}, \quad 0 \le t \le T_S/2 \tag{22}$$

where the maximum/minimum value of output voltage in one time duration is denoted by $V_{o\mathrm{M}}/V_{o\mathrm{m}}$, i.e., $V_{o\mathrm{M}} = v_o(0), V_{o\mathrm{m}} = v_o(\mathrm{T_S}/2) = V_{o\mathrm{M}} \cdot e^{-T_S/2\tau}$, in which τ represents the series-capacitor-discharging time constant as

$$\tau = [(r_T + r_n) \,||\, r_{Co} + R_L] \cdot [C/n + C_o]. \tag{23}$$

In Fig. 6, the variation of output voltage in one time duration can be defined as

$$\Delta v_o = V_{o\mathrm{M}} - V_{o\mathrm{m}} = V_{o\mathrm{M}} \cdot \left(1 - e^{-T_S/2\tau}\right). \tag{24}$$

By using (22), static average output voltage $\mathrm{V_o}$ within one time duration ΔT can be computed as

$$\begin{aligned}\mathrm{V_o} &= \frac{1}{T_s/2} \cdot \int_0^{T_S/2} v_o(t)\, dt \\ &= \frac{2}{T_s} \cdot V_{o\mathrm{M}} \cdot e^{-t/\tau}\Big|_0^{T_S/2} \cdot (-\tau) \\ &= 2f_s\tau \cdot \Delta v_o.\end{aligned} \tag{25}$$

The voltage ripple percentage can be defined and presented as

$$\begin{aligned}rp = \frac{\Delta v_o}{\mathrm{V_o}} \times 100\% &= \frac{1}{2f_s \cdot \tau} \\ &= \frac{1}{2f_s \cdot [(r_T + r_n) \| r_{Co} + R_L] \cdot C_T}\end{aligned} \tag{26}$$

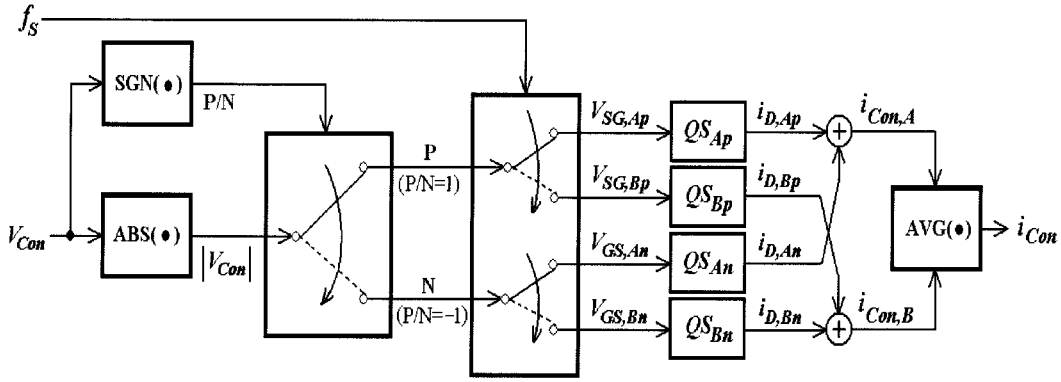

Fig. 9. Scheduled timing driver.

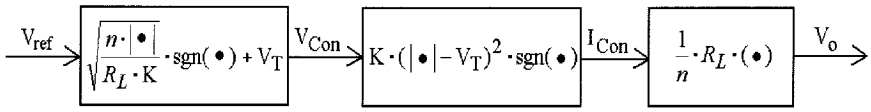

Fig. 10. Block diagram for static analysis.

where the total capacitance C_T is defined as $C_T = C/n + C_o$. The ripple percentage rp is increasing while the load is heavier, but it can be improved with increasing switching frequency f_s and total capacitance C_T. When the inverter is working in the unloaded case ($R_L \rightarrow \infty$), the ripple percentage will be almost near to zero. Obviously, if the maximum tolerant ripple percentage $\tilde{\text{rp}}$ is specified, based on (26), then the lower bound of total capacitance can be estimated as

$$C_T \geq \frac{1}{2f_s \cdot [(r_T + r_n) \,||\, r_{Co} + R_L] \cdot \tilde{\text{rp}}}. \tag{27}$$

D. Closed-Loop Control and Stability of QSC Inverter

According to the waveforms of Fig. 8, the relationship between control currents and voltages ($i_{D,Ap}, i_{D,An}, i_{D,Bp}, i_{D,Bn}$ and $v_{SG,Ap}, v_{GS,An}, v_{SG,Bp}, v_{GS,Bn}$) can be planned and scheduled for different two phases and two half-sinusoidal output, and then the result is shown in Table I as QSC boost dc–ac timing schedule. Here, for simplification of control design, according to Table I, four control voltages $v_{SG,Ap}, v_{GS,An}, v_{SG,Bp}, v_{GS,Bn}$ can be integrated and determined by a new control voltage variable v_{Con} for different timing intervals, and their relationship is shown in Table II, where v_{Con} will be basically composed of practical output voltage and desired reference sinusoid later. According to Table II, the overall relationship between i_{Con} and v_{Con} is described by the block diagram as shown in Fig. 9, and then using (7) and (10), the formulation between them can be derived as

$$\begin{aligned} & i_{\text{Con}}(t) \\ & = f(v_{\text{Con}}(t)) \\ & = \begin{cases} \text{K} \cdot (|v_{\text{Con}}(t)| - \text{V}_\text{T})^2 \cdot \text{sgn}(v_{\text{Con}}(t)), & |v_{\text{Con}}(t)| \geq \text{V}_\text{T} \\ 0, & |v_{\text{Con}}(t)| < \text{V}_\text{T} \end{cases} \end{aligned} \tag{28}$$

where $i_{\text{Con}}(t) = \text{I}_{\text{Con}} + \hat{i}_{\text{Con}}(t), v_{\text{Con}}(t) = \text{V}_{\text{Con}} + \hat{v}_{\text{Con}}(t)$, in which $\text{I}_{\text{Con}}, \text{V}_{\text{Con}}$ are static operating signals, and $\hat{i}_{\text{Con}}, \hat{v}_{\text{Con}}$ represent dynamic small signals. Based on (28), these relationships for static operating points/dynamic small signals are

$$\begin{aligned} \text{I}_{\text{Con}} &= f(\text{V}_{\text{Con}}) \\ &= \begin{cases} \text{K} \cdot (|\text{V}_{\text{Con}}| - \text{V}_\text{T})^2 \cdot \text{sgn}(\text{V}_{\text{Con}}), & |\text{V}_{\text{Con}}| \geq \text{V}_\text{T} \\ 0, & |\text{V}_{\text{Con}}| < \text{V}_\text{T} \end{cases} \end{aligned} \tag{29a}$$

$$\hat{i}_{\text{Con}}(t) = g_m \cdot \hat{v}_{\text{Con}}(t) \tag{29b}$$

where the trans-conductance of MOSFET is denoted by $g_m = 2 \cdot \sqrt{\text{K} \cdot |\text{I}_{\text{Con}}|}$. So, the static/dynamic closed-loop control of QSC inverter can be suggested as follows. 1) For operating signal view of static control, according to (11a), the static output voltage V_o is linearly regulated by control current I_{Con}, which is nonlinearly adjusted by control voltage V_{Con} as (29a). So, a nonlinear compensator is employed and presented as shown in Fig. 10, and then it is able to produce V_{Con} suitably for making output V_o closed to reference V_{ref}. 2) For small signal view of dynamic control, according to (14), the dynamic output voltage $\hat{v}_o$ is linearly regulated by dynamic control current $\hat{i}_{\text{Con}}$, which is also linearly adjusted by dynamic control voltage $\hat{v}_{\text{Con}}$ as (29b). So, a low-pass linear controller is adopted and suggested as shown in Fig. 11, in which a series proportional gain K_P is designed mainly for the compensation of the tracking error. Besides, there is a low-pass filter employed in the controller, and it is designed mainly for avoiding the possible high frequency noises, and thus, its cut-off frequency w_L can be suitably assigned according to the frequency band of noises.

Finally, the stability of QSC inverter is discussed. From (21), if load R_L is much larger than parasitic resistors r_T, r_C, r_{Co}, then power efficiency becomes quite closed to 78.5%. Basically, the requirement of $R_L >> r_C, R_L >> r_{Co}, R_L >> r_T$ is reasonable and desired for better performance (Assume that load R_L is about in Ω-level, and parasitic r_T, r_C, r_{Co} are

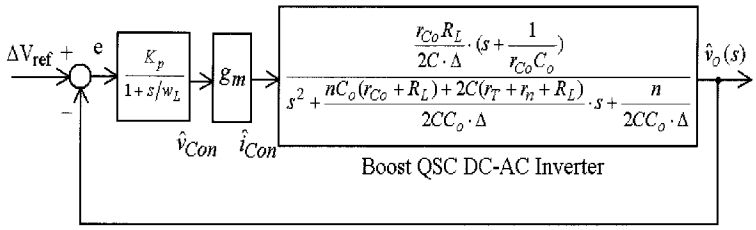

Fig. 11. Block diagram for dynamic analysis.

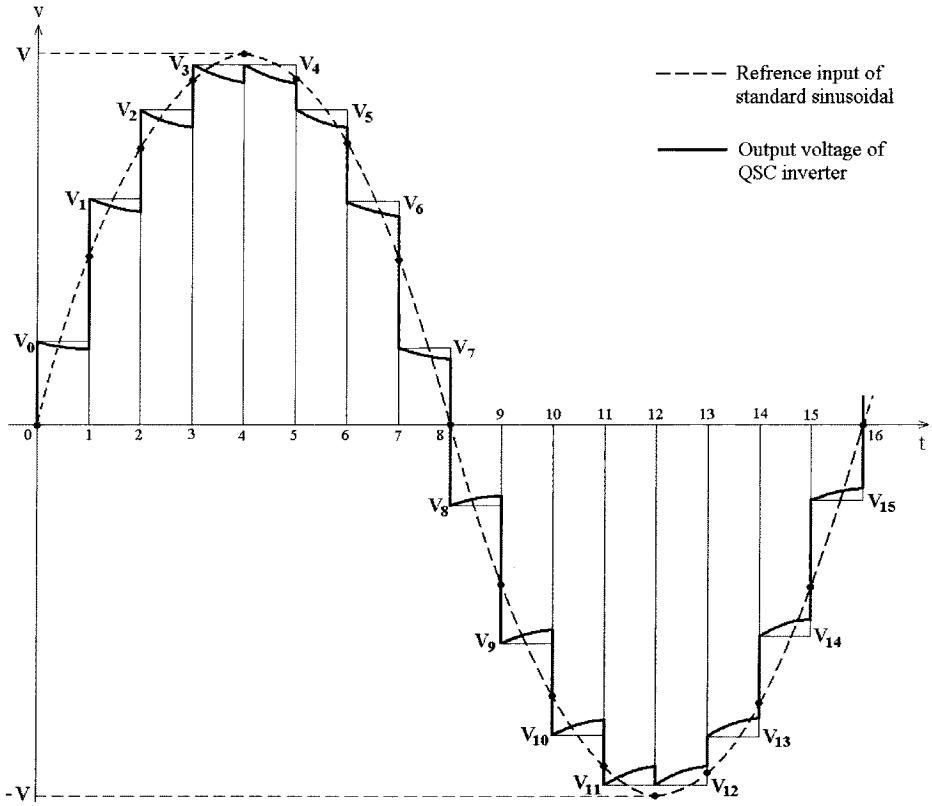

Fig. 12. Reference and output waveforms for THD analysis.

about in $m\Omega$-level). By combining (14) with this assumption, the second-order model can be reduced approximately into

$$G(s) \approx \frac{\hat{v}_o(s)}{\hat{i}_{\mathrm{Con}}(s)} = \frac{R_L/n}{(C_o + 2C/n)R_L \cdot s + 1} \tag{30a}$$

$$\mathrm{pole}_{\mathrm{dom}} = -\frac{1}{(C_o + 2C/n)R_L} \tag{30b}$$

where $\mathrm{pole}_{\mathrm{dom}}$ is the pole of the first-order model, and it also represents the dominant pole of the second-order QSC inverter. Since the dominant pole is located in the left half s-plane, it is obvious that the open-loop QSC inverter is locally stable. Since the variation of static operating point $\mathrm{I_{Con}}$ will not directly affect the dominant pole, the result almost ensures the global stability theoretically. So, it is an important one of advantages that inverter has an inherent good stability.

E. Total Harmonic Distortion of QSC Inverter

Fig. 12 shows the theoretical waveforms of reference input and practical output for QSC inverter. The reference input is a standard sinusoidal, denoted by $\mathrm{V_{ref}} = \mathrm{V} \cdot \sin(2\pi f \cdot t)$, and it also represents the desired output of QSC inverter. But, the practical output is shown as the bold real line of Fig. 12, which is almost similar to staircase waveform with discharging decay in each of time duration (For explanation simplification, the number of time duration is temporarily taken by $m = 16$ in Fig. 12). In the figure, $V_0, V_1, V_2 \sim V_{m-1}$ are exactly the initial values of discharging voltages for each of discharging time duration, and besides, they also represent the final values of charging voltages for each of charging time duration. Here, according to Fig. 12, these voltages $V_k, k = 0, 1, 2, \ldots, m-1$ are described and selected as

$$\begin{aligned} V_k &= \frac{\mathrm{V}}{2} \cdot [\sin(2\pi \cdot f \cdot k\Delta T) + \sin(2\pi \cdot f \cdot (k+1)\Delta T)] \\ &= \frac{\mathrm{V}}{2} \cdot \left[\sin\left(\frac{2\pi \cdot k}{m}\right) + \sin\left(\frac{2\pi \cdot (k+1)}{m}\right)\right] \end{aligned} \tag{31}$$

where $V_k = V_{k+m}$ holds due to the cycle waveform. Thus, based on (31), the practical output voltage waveform of QSC inverter can be described by

$$v_o(t) = \sum_{k=0}^{m-1} V_k \cdot \exp\left(-\frac{t - k\Delta T}{\tau}\right) \cdot P(t - k\Delta T) \tag{32}$$

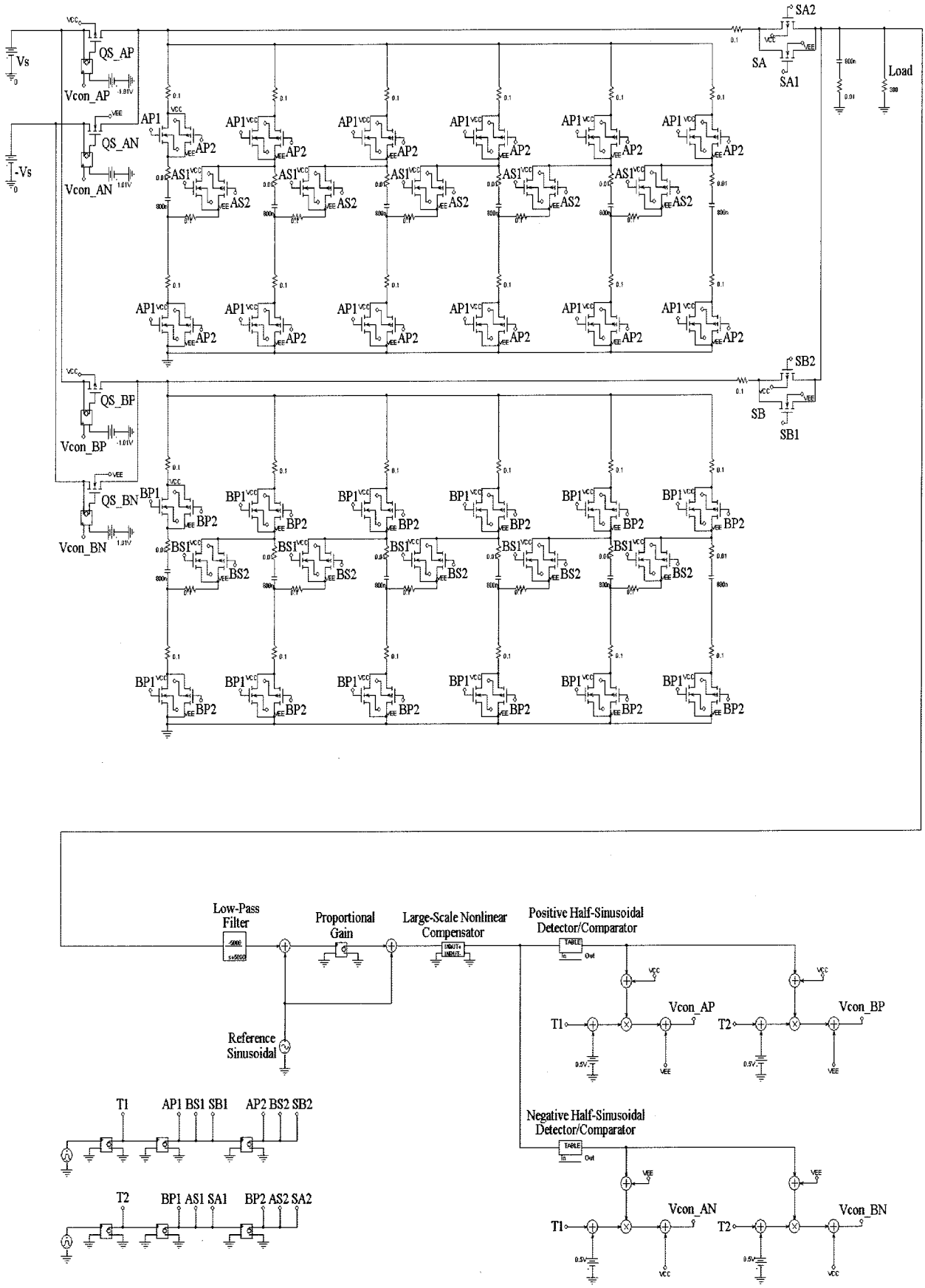

Fig. 13. Overall inverter circuit in PSPICE.

where $v_o(t) = v_o(t+T)$, and $P(t) = u_s(t) - u_s(t-\Delta T)$ is a pulse function with time duration ΔT. Next, the Fourier analysis of the practical output $v_o(t)$ is derived, and its analytic details are given in the Appendix. According to the result in

Appendix, the Fourier analysis of output $v_o(t)$ of inverter can be expressed as

$$v_o(t) = \sum_{n\in D} A_n \cdot \sin\left(\frac{2n\pi}{T}\cdot t\right) \tag{33}$$

where

$$A_n = \frac{A}{n} \tag{34a}$$

$$A = \frac{\sin(2\pi/m)}{2\pi/m}\cdot\left(1+\frac{T}{2m\tau}\right)\cdot \mathrm{V} \tag{34b}$$

$$D = \{n \,|\, n = 1, 2m\pm 1, 3m\pm 1, 4m\pm 1, \ldots\}. \tag{34c}$$

Using the THD definition and combining with (33), the THD of QSC boost dc–ac inverter can be described by

$$\begin{aligned}\mathrm{THD} &\equiv \frac{\sqrt{\sum_{n=2}^{\infty} A_n^2}}{A_1} \\ &= \frac{\sqrt{A_{m-1}^2 + A_{m+1}^2 + A_{2m-1}^2 + A_{2m+1}^2 + \cdots}}{A_1}.\end{aligned} \tag{35}$$

If the number of time duration (m) is selected quite large, then the approximation can be made as (36) (the approximation is satisfied when m is larger than 10). In fact, m is usually much larger than 10 because $f_s \gg f$ is employed.

$$\begin{aligned}A_{m-1}^2 + A_{m+1}^2 &= \left(\frac{A}{m-1}\right)^2 + \left(\frac{A}{m+1}\right)^2 \\ &= \frac{2A^2\cdot(m^2+1)}{(m^2-1)^2} \cong \frac{2A^2}{m^2}\end{aligned} \tag{36}$$

By applying (36) into (35), the THD is derived as

$$\begin{aligned}\mathrm{THD} &\cong \frac{1}{A}\cdot\sqrt{2A^2\cdot\left[\frac{1}{m^2}+\frac{1}{(2m)^2}+\frac{1}{(3m)^2}+\ldots\right]} \\ &= \frac{\pi}{\sqrt{3}}\cdot\frac{1}{m}.\end{aligned} \tag{37}$$

Here, it is obvious that THD can be improved with increasing the number of time duration (m). If the desired tolerant THD value THD_d and output frequency f are specified, based on (1) and (37), then the theoretical lower bound of switching frequency f_s can be suggested as

$$f_s > \frac{\pi}{2\sqrt{3}}\cdot\frac{f}{\mathrm{THD}_d}. \tag{38}$$

If THD_d is required lower, then the higher switching frequency f_s must be needed.

V. Example of QSC Boost DC–AC Inverter

In this section, a six-stage $(n = 6)$ QSC boost dc–ac inverter is made in circuit layout and simulated by PSPICE, and then the result shows the efficacy of the proposed inverter configuration. The main function of the dc–ac inverter is to convert dc source $\mathrm{V_S}$ (25 V) into ac output v_o (100 Hz, 100 V, rms, peak voltage 140 V) for supplying the standard load R_L (300 Ω). Based on the basic specifications, PSPICE tool (OrCAD v9.0) is employed for circuit design of the closed-loop QSC boost dc–ac inverter system, and then the overall inverter circuit is shown in Fig. 13. In this figure, T1 and T2 are a group of antiphase square waveform sources with switching frequency f_s of 1 MHz for the basic antiphase operation of cells A and B. In addition, symbols AP1, AS1, BP1, BS1, SA1, SB1, AP2, AS2, BP2, BS2, SA2, SB2 represent the control signals of CMOS-TG in inverter, and they are cyclically generated by T1 and T2 in accordance with the timing operation as Fig. 8. For realizing the QSC current-mode control, four control voltages Vcon_AP, Vcon_AN, Vcon_BP, Vcon_BN are generated by combining T1/T2 and positive/negative half-sinusoidal comparators. The gain K_P is designed for the tracking error compensation, and it is taken by 10 here. The low-pass filter is designed for avoiding the possible high frequency noises, and its cut-off frequency w_L is taken by 5000 rad/s here. All component parameters of QSC inverter adopted are listed in Table III. Now, based on the inverter of Fig. 13, the simulations will be discussed for some cases, including: 1) steady-state ac output, power conversion efficiency, and output ripple percentage; 2) transient response of the regulated inverter for load variation; 3) a practical capacitive EL lamp; and 4) power efficiency, output ripple percentage, and THD for various loads.

TABLE III
Component Parameters of QSC Boost DC–AC Inverter.

NMOS/PMOS	$\mathrm{K} = 3\,\mathrm{A/V^2}, \mathrm{V_T} = 1\mathrm{V}, \lambda = 0.001$
Controller	$w_L = 5000 rad/s, K_p = 10$
C_o, r_{Co}	$C_o = 0.8\mu F, r_{Co} = 10m\Omega$
C, r_C	$C = 0.8\mu F, r_C = 10m\Omega$
R_L	$R_L = 300\Omega$

First, the steady-state ac output voltage versus time is simulated for some different loads, and all the results are shown in Fig. 14(a)–(c). Fig. 14(a) shows the ac output waveform for supplying the standard load R_L of 300 Ω, and the results about steady-state efficiency, maximum ripple percentage, and setting time are obtained as: $\eta = 73.08\%, \mathrm{rp_{max}} = (\Delta v_o/\mathrm{V_o})_{\max} = 8.521\%$, and $t_S = 0.7$ ms. Similarly, Fig. 14(b)/(c) shows the ac output waveform for supplying the load R_L of 210 Ω/390 Ω, and the steady-state efficiency and maximum ripple percentage are also obtained as: $\eta = 70.79\%/\eta = 72.87\%, \mathrm{rp_{max}} = 8.581\%/\mathrm{rp_{max}} = 8.475\%$. So, the higher ac output can be successfully realized from the lower dc source by using the QSC inverter proposed. Comparing these results, it is observed that the ripple percentage becomes slightly larger/smaller when the load is heavier $(R_L : 300\ \Omega \rightarrow 210\ \Omega)/\mathrm{lighter}(R_L : 300\ \Omega \rightarrow 390\ \Omega)$. These above results show that the inverter has pretty good steady-state performances.

Secondly, the transient response of the regulated inverter for load variation will be discussed. Since it is possible that the load is unexpectedly increased/decreased, the regulation capability

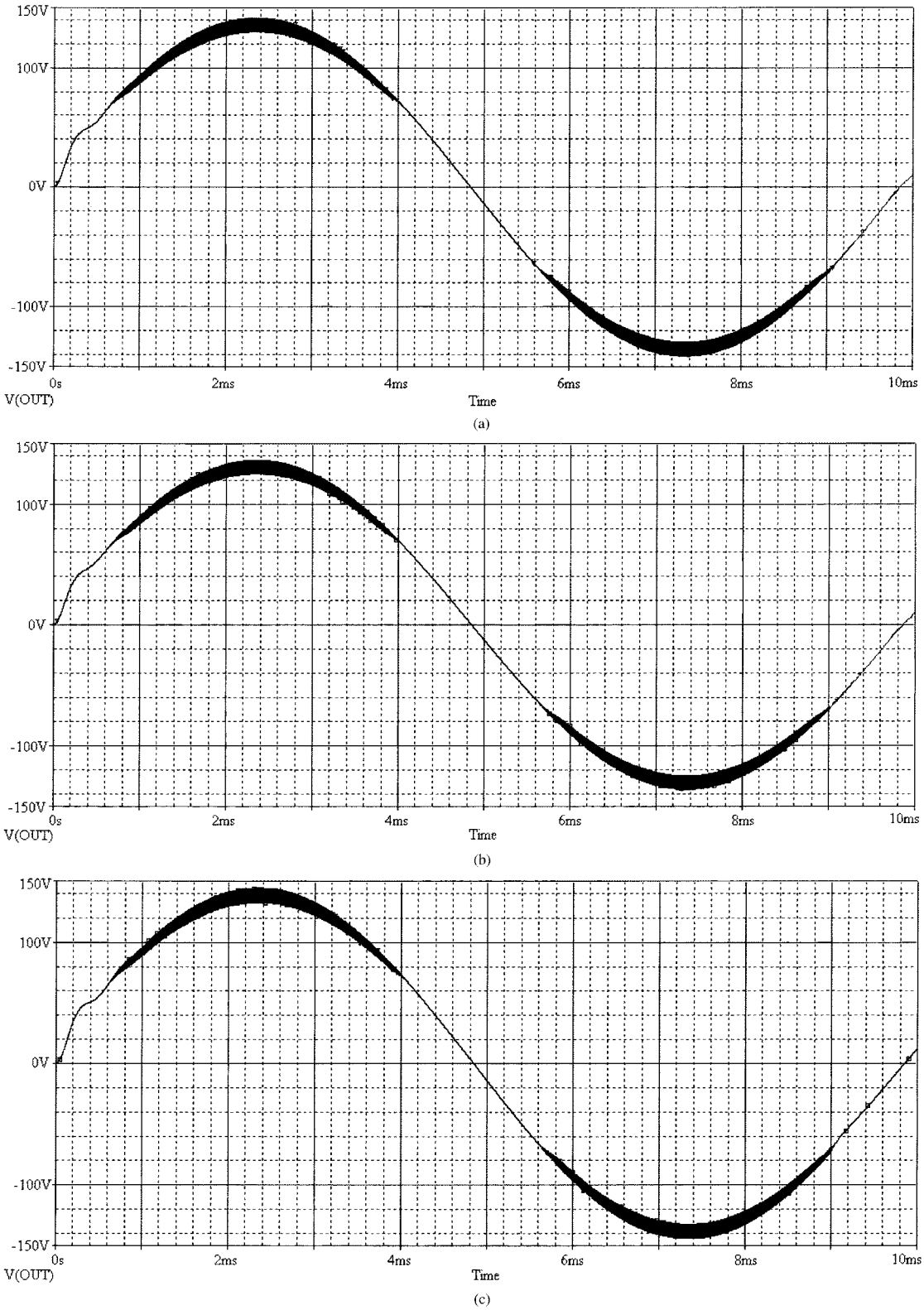

Fig. 14. ac output for load resistor of: (a) 300 Ω, (b) 210 Ω, and (c) 390 Ω.

of the inverter must be considered and emphasized. Here, it is assumed that the load R_L keeps on 300 Ω normally, and the same load is added at 7 ms and connected in parallel with the output terminals, and then the added load is removed away at 11 ms. In other words, the load is double heavier from 7 to 11 ms. Fig. 15(a) shows the overall output waveform versus time, and it is obvious that the output is still tracking reference sinusoidal no matter when the extra load is added in or removed away. Furthermore, to focus on the time of increasing/decreasing load, the graphics of output waveform is enlarged as

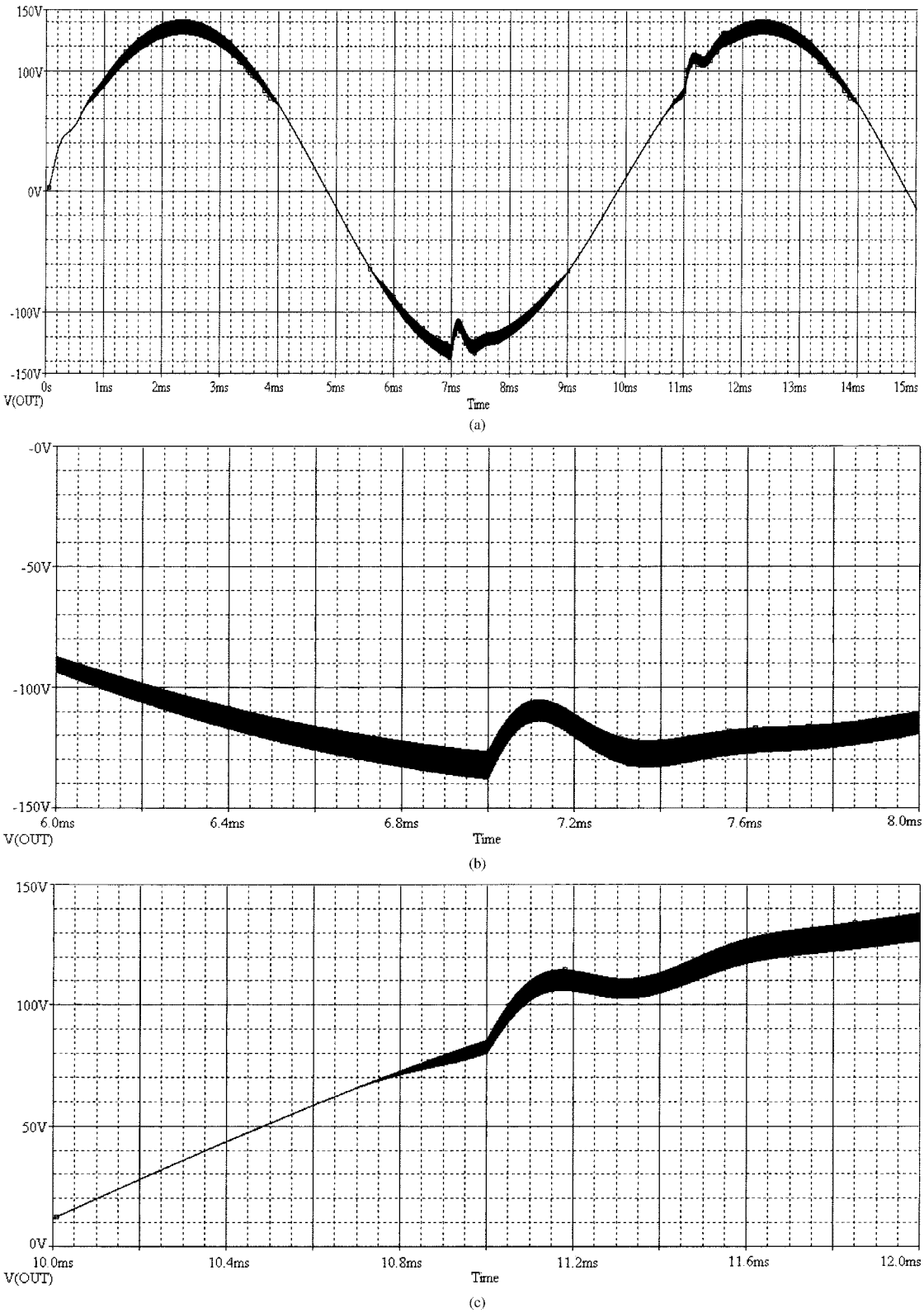

Fig. 15. (a) Transient regulation for load variation. (b) While adding the same load at 7 ms. (c) While removing the added load at 11 ms.

shown in Fig. 15(b)/(c), in which the output is tracking reference after passing a short setting time of 0.7 ms (7.0–7.7 ms/11.0–11.7 ms). The results show that the inverter has a pretty good transient regulation capability.

Thirdly, a capacitive load, EL lamp, is simulated and operated at different output frequencies. The equivalent circuit of the 5-in^2 EL lamp (100–1000 Hz, 100–120 V, rms) is shown as in Fig. 16. Exactly, due to the single directional input currents at source terminals, the proposed circuit can not take the power back to the sources. But, the proposed inverter has two CMOS-TG S_A, S_B connected between R_L and cells A $\sim$ B. Due to complimentary operation of S_A, S_B, at least one of them

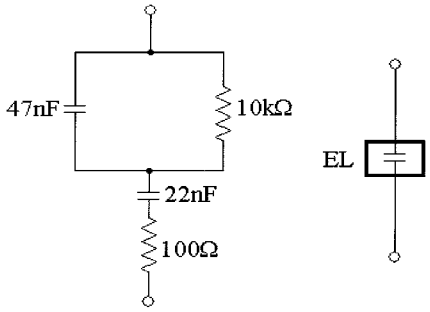

Fig. 16. Equivalent circuit of 5 in^2 EL lamp.

is turned on as a bidirectional switch at any time duration, and then it provides a bidirectional energy switching channel. So, when the load is capacitive or inductive, all the capacitors in cells A or B can be treated as energy buffers/tanks. So, the proposed inverter could handle as the capacitive/inductive load is not too heavy. Here, a practical capacitive EL lamp is operated at different output frequencies (400 Hz/800 Hz), and the outputs are given in Fig. 17(a) and (b).

Finally, the power efficiency, output ripple percentage, and total harmonic distortion are simulated for different loads. For different load resistors with range of 30 Ω–570 Ω, the power efficiency, output ripple and THD of the proposed inverter are simulated as shown in Fig. 18(a)–(c), respectively. In Fig. 18(a), it is obvious that the power efficiency for load resistors of 120 Ω–480 Ω can be higher than 70%. In Fig. 18(b), the ripple percentage for load resistors of 120 Ω–570 Ω is lower than 9%. In Fig. 18(c), the THD for load resistors of 150 Ω–570 Ω is lower than 8.45%. These results show that it has good performances for wide-range loading.

VI. Conclusion

A multistage power CMOS-TG QSC boost dc–ac inverter is presented and integrated with a boost dc–dc converter for a step-up application with ac or dc load, for example, EL lamp. In this paper, using CMOS-TG as a bidirectional switch, the various topologies can be integrated in the same circuit configuration for achieving two functions: boosting and alternating. Finally, a six-stage QSC boost dc–ac inverter is simulated by PSPICE tool, and the results are illustrated to show the efficacy of the proposed inverter.

The following advantages of the proposed scheme are involved. 1) Since all elements in the inverter only contain MOSFETs and capacitors, such the uniform is helpful to IC fabrication. 2) Since QSC technique is adopted, input current is continuous, so EMI problem is much improved. 3) By using CMOS-TG as a bidirectional switch, it is much helpful to integrate both dc–ac and dc–dc functions in one unified configuration. 4) The turn-on resistance of power-level CMOS is pretty small, so it could get higher efficiency. 5) The CMOS gate is operated at high frequency, so the lower output ripple percentage can be expected. 6) Due to QSC current-mode control, source variation will not make immediate response on output voltage and current. So, it has good output robustness against source variation or noise. 7) Since the duty cycle is fixed at 0.5, such a constant duty cycle is much useful to model formulation, control design and theoretical analysis, even to fault detection and isolation (FDI) design [20]–[22] in the future. 8) Since the dominant pole is located in the left half s-plane, it is obvious that the open-loop QSC inverter is locally stable. Thus, the circuit scheme has an inherent good stability. However, the power loss still exists, and it results in heat problem. So, both the high-voltage high-power semiconductors and the extra thermal management devices are considered for protection of inverter circuit. It will be the future aim to figure out the higher power efficiency scheme for IC fabrication.

Appendix
Fourier Analysis of Output

The time duration ΔT is reasonably assumed much smaller than the discharging time constant $\tau(\Delta T \ll \tau)$ as the high switching frequency f_s is selected. So, the exponential term of (32) can be approximated by the first-order Taylor's series as

$$\exp\left(-\frac{t-k\Delta T}{\tau}\right)\cdot p(t-k\Delta T) \cong \left(1-\frac{t-k\Delta T}{\tau}\right)\cdot p(t-k\Delta T). \quad (39)$$

By substituting (39) into (32), $v_o(t)$ is divided into two parts

$$v_o(t) = v_{o1}(t) + v_{o2}(t), \quad (40a)$$

$$v_{o1}(t) = \sum_{k=0}^{m-1} V_k \cdot p(t-k\Delta T) \quad (41a)$$

$$v_{o2}(t) = \sum_{k=0}^{m-1} V_k \cdot \left(-\frac{t-k\Delta T}{\tau}\right)\cdot p(t-k\Delta T) \quad (41b)$$

where v_{o1} is a complete staircase sinusoidal term, and v_{o2} is a linear discharging decay term.

Fourier Lemma: If there exists q discontinuous points $t_1, t_2, \ldots, t_q$ on $(0, T]$ for periodic odd function $v(t)$ and its derivative $v'(t)$ ($v''(t) = 0$ is assumed), then Fourier series of $v(t)$ can be

$$v(t) = \sum_{n=1}^{\infty} b_n \cdot \sin\left(\frac{2n\pi}{T}\cdot t\right), \quad n \in N = \{1,2,3,\ldots\} \quad (41a)$$

$$b_n = \frac{1}{n\pi}\sum_{k=1}^{q}\left[J_k \cdot \cos\left(\frac{2n\pi}{T}\cdot t_k\right) - \frac{T}{2n\pi}\cdot J'_k \cdot \sin\left(\frac{2n\pi}{T}\cdot t_k\right)\right] \quad (41b)$$

where

$$J_k = J(t_k) = v(t_k^+) - v(t_k^-) \quad (42a)$$

$$J'_k = J'(t_k) = v'(t_k^+) - v'(t_k^-). \quad (42b)$$

- *Fourier analysis of complete staircase sinusoidal term* $\boldsymbol{v_{o1}}$:

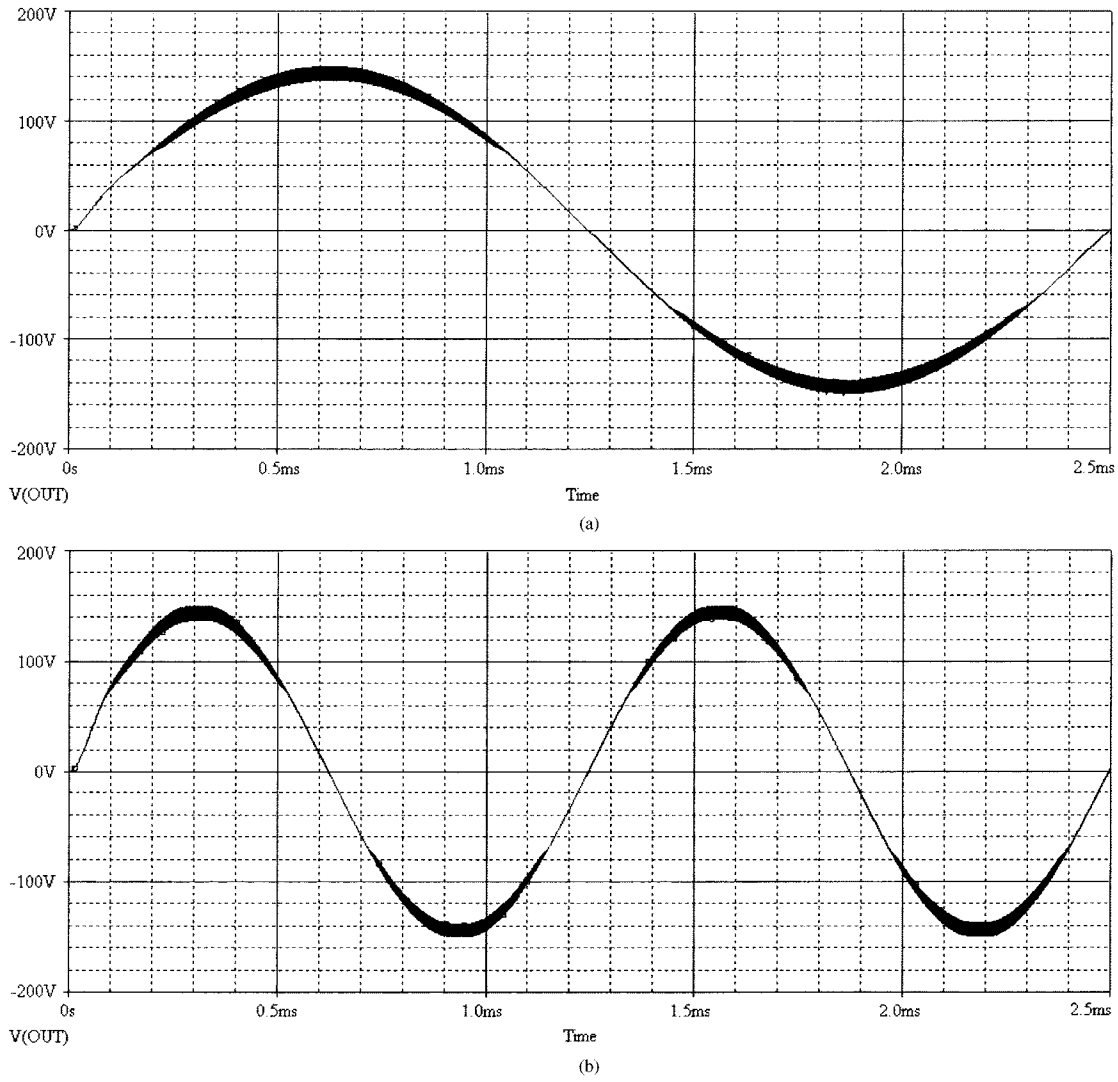

Fig. 17. EL lamp. (a) At 400 Hz, 100 V, rms. (b) At 800 Hz, 100 V, rms.

Due to complete staircase waveform of v_{o1}, the Fourier coefficients can be estimated just by $J_k(J'_k = 0)$, so

$$v_{o1}(t) = \sum_{k=0}^{m-1} V_k \cdot p(t - k\Delta T) = \sum_{n=1}^{\infty} b_{n1} \cdot \sin\left(\frac{2n\pi}{T} \cdot t\right) \tag{43}$$

where the Fourier coefficients of v_{o1} can be estimated by using *Fourier Lemma* as

$$\begin{aligned} b_{n1} &= \frac{1}{n\pi}\sum_{k=1}^{q} J_k \cdot \cos\left(\frac{2n\pi}{T} \cdot t_k\right) \\ &= \frac{1}{n\pi}\sum_{k=1}^{q} \{V_k - V_{k-1}\} \cdot \cos\left(\frac{2n\pi}{T} \cdot k\Delta T\right) \\ &= \frac{1}{n\pi}\sum_{k=1}^{q} \left\{\frac{\mathrm{V}}{2} \cdot \left[\sin\left(\frac{2\pi \cdot k}{m}\right) + \sin\left(\frac{2\pi \cdot (k+1)}{m}\right)\right]\right. \\ &\quad \left. - \frac{\mathrm{V}}{2} \cdot \left[\sin\left(\frac{2\pi \cdot (k-1)}{m}\right) + \sin\left(\frac{2\pi \cdot k}{m}\right)\right]\right\} \\ &\quad \cdot \cos\left(\frac{2n\pi}{T} \cdot \frac{kT}{m}\right) \\ &= \frac{1}{n\pi}\sum_{k=1}^{q} \frac{\mathrm{V}}{2} \cdot \left[2\sin\left(\frac{2\pi}{m}\right)\cos\left(\frac{2\pi \cdot k}{m}\right)\right]\cos\left(\frac{2n\pi}{m} \cdot k\right) \\ &= \begin{cases} \dfrac{\mathrm{V}}{n\pi} \cdot \sin\left(\dfrac{2\pi}{m}\right) \cdot \dfrac{m}{2}, & n \in D \\ 0, & n \notin D = \{n | n = 1, 2m \pm 1, 3m \pm 1, 4m \pm 1, \ldots\}. \end{cases} \end{aligned} \tag{44}$$

By combining (43) and (44), the Fourier series of v_{o1} can be

$$v_{o1}(t) = \frac{\sin(2\pi/m)}{2\pi/m} \cdot \mathrm{V} \cdot \sum_{n \in D} \frac{1}{n} \cdot \sin\left(\frac{2n\pi}{T} \cdot t\right). \tag{45}$$

- *Fourier series of linear discharging decay term* v_{o2}:

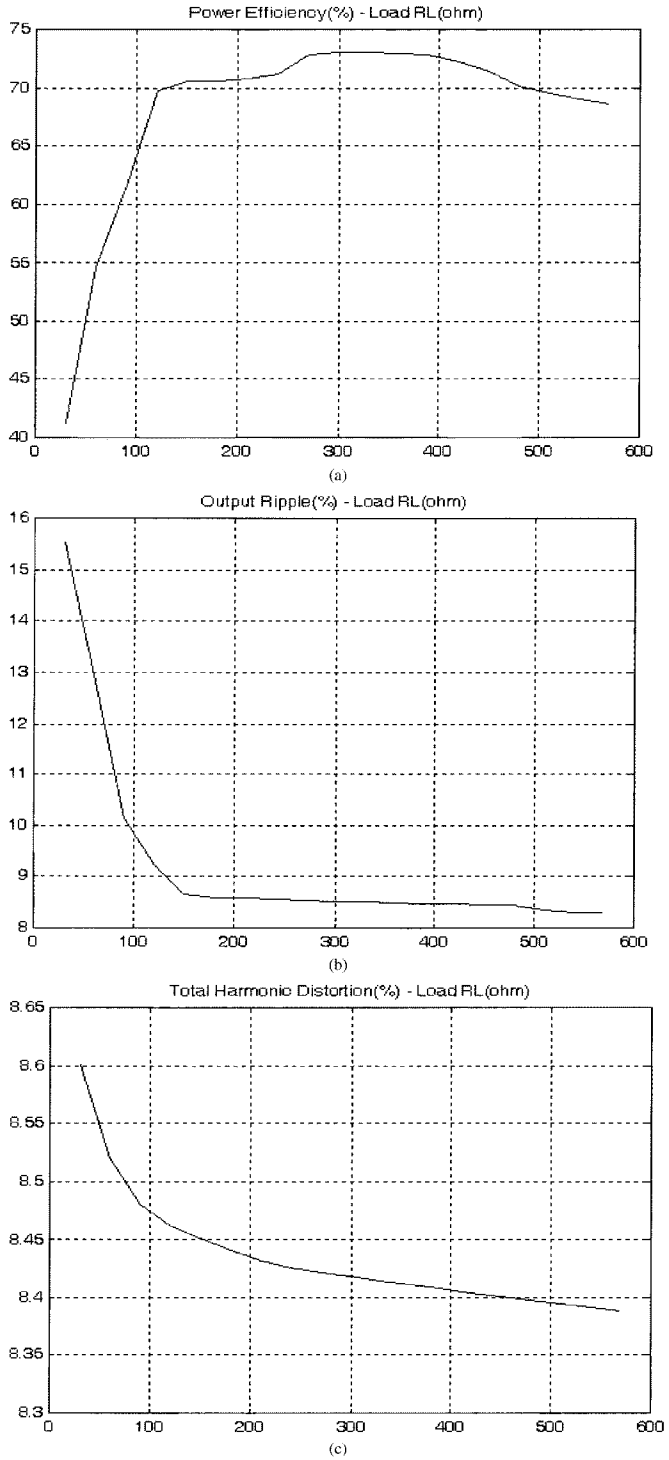

Fig. 18. (a) Power efficiency for different loads. (b) Output ripple percentage for different loads. (c) Total harmonic distortion for different loads.

Due to linear discharging decay term of v_{o2}, the Fourier coefficients are estimated by J_k and $J'_k (J''_k = 0)$, so

$$v_{o2}(t) = \sum_{k=0}^{m-1} V_k \cdot \left(-\frac{t - k\Delta T}{\tau}\right) \cdot p(t - k\Delta T) = \sum_{n=1}^{\infty} b_{n2} \cdot \sin\left(\frac{2n\pi}{T} \cdot t\right) \tag{46}$$

$$J_k = v_{o2}(t_k^+) - v_{o2}(t_k^-) = -\frac{T}{m\tau} \cdot V_{k-1} \tag{47a}$$

$$J'_k = v'_{o2}(t_k^+) - v'_{o2}(t_k^-) = \frac{V_k - V_{k-1}}{\tau}. \tag{47b}$$

By applying *Fourier lemma*, the Fourier coefficients of v_{o2} are

$$\begin{aligned} b_{n2} &= \frac{1}{n\pi} \sum_{k=1}^{q} \left[J_k \cdot \cos\left(\frac{2n\pi}{T} \cdot t_k\right) - \frac{T}{2n\pi} \cdot J'_k \cdot \sin\left(\frac{2n\pi}{T} \cdot t_k\right) \right] \\ &= \frac{1}{n\pi} \sum_{k=1}^{q} \left[\left(-\frac{T}{m\tau} \cdot V_{k-1}\right) \cdot \cos\left(\frac{2n\pi \cdot k}{m}\right) - \frac{T}{2n\pi} \cdot \left(\frac{V_k - V_{k-1}}{\tau}\right) \cdot \sin\left(\frac{2n\pi \cdot k}{m}\right) \right] \\ &= \frac{1}{n\pi} \sum_{k=1}^{q} \left\{ -\frac{T}{2m\tau} \cdot \mathrm{V} \cdot \left[\sin\left(\frac{2\pi \cdot (k-1)}{m}\right) + \sin\left(\frac{2\pi \cdot k}{m}\right) \right] \cdot \cos\left(\frac{2n\pi \cdot k}{m}\right) \right. \\ &\quad \left. - \frac{T}{2n\pi} \cdot \frac{\mathrm{V}}{\tau} \cdot \sin\left(\frac{2\pi}{m}\right) \cdot \cos\left(\frac{2\pi \cdot k}{m}\right) \cdot \sin\left(\frac{2n\pi \cdot k}{m}\right) \right\} \\ &= \frac{1}{n\pi} \cdot \left\{ -\frac{T}{2m\tau} \cdot \mathrm{V} \cdot \left[1 + \cos\left(\frac{2\pi}{m}\right)\right] \cdot \sum_{k=1}^{q} \sin\left(\frac{2\pi \cdot k}{m}\right) \cdot \cos\left(\frac{2n\pi \cdot k}{m}\right) \right. \\ &\quad + \frac{T}{2m\tau} \cdot \mathrm{V} \cdot \sin\left(\frac{2\pi}{m}\right) \cdot \sum_{k=1}^{q} \cos\left(\frac{2\pi \cdot k}{m}\right) \cdot \cos\left(\frac{2n\pi \cdot k}{m}\right) \\ &\quad \left. - \frac{T}{2n\pi} \cdot \frac{\mathrm{V}}{\tau} \cdot \sin\left(\frac{2\pi}{m}\right) \cdot \sum_{k=1}^{q} \cos\left(\frac{2\pi \cdot k}{m}\right) \cdot \sin\left(\frac{2n\pi \cdot k}{m}\right) \right\} \end{aligned} \tag{48}$$

According to discrete orthogonal property, ones can obtain

$$\sum_{k=1}^{q} \sin\left(\frac{2\pi \cdot k}{m}\right) \cdot \cos\left(\frac{2n\pi \cdot k}{m}\right) \cong 0 \tag{49a}$$

$$\sum_{k=1}^{q} \cos\left(\frac{2\pi \cdot k}{m}\right) \cdot \sin\left(\frac{2n\pi \cdot k}{m}\right) \cong 0. \tag{49b}$$

By employing (49), the Fourier coefficients of v_{o2} can be

$$b_{n2} \cong \begin{cases} \frac{\mathrm{V}}{n\pi} \cdot \frac{T}{2m\tau} \cdot \sin\left(\frac{2\pi}{m}\right) \cdot \frac{m}{2}, & n \in D \\ 0, & n \notin D \end{cases}. \tag{50}$$

By substituting (50) into (46), the Fourier series of v_{o2} can be

$$v_{o2}(t) = \frac{\sin(2\pi/m)}{2\pi/m} \cdot \mathrm{V} \cdot \frac{T}{2m\tau} \cdot \sum_{n\in D} \frac{1}{n} \cdot \sin\left(\frac{2n\pi}{T} \cdot t\right). \quad (51)$$

Finally, by combining (45) and (51), the Fourier analysis of the practical output $v_o(t)$ of QSC inverter can be derived as

$$v_o(t) = v_{o1}(t) + v_{o2}(t) = \sum_{n\in D} A_n \cdot \sin\left(\frac{2n\pi}{T} \cdot t\right) \quad (52)$$

$$A_n = b_{n1} + b_{n2} = \frac{A}{n} \quad (53a)$$

$$A = \frac{\sin(2\pi/m)}{2\pi/m} \cdot \left(1 + \frac{T}{2m\tau}\right) \cdot \mathrm{V}. \quad (53b)$$

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