Design and Analysis of Wide Frequency-Tuning-Range CMOS 60 GHz VCO by Switching Inductor Loaded Transformer

Wei Fei, *Student Member, IEEE*, Hao Yu, *Senior Member, IEEE*, Haipeng Fu, *Member, IEEE*, Junyan Ren, *Member, IEEE*, and Kiat Seng Yeo, *Senior Member, IEEE*

Abstract—To provide wide frequency tuning range (FTR) with compact implementation area, a new inductive tuning method is introduced in this paper for CMOS 60 GHz voltage controlled oscillator (VCO). The inductive tuning is based on a switching inductor-loaded transformer by configuring different current return-paths in the secondary coil of the transformer. Different from previous inductive tuning methods, the proposed VCO topology can achieve wide FTR for multiple sub-bands at 60 GHz within compact area by only one transformer. Two 60 GHz VCOs are demonstrated in 65 nm CMOS with design targets for the maximum FTR and the balanced phase noise in each sub-band, respectively. As measured by experiments, the first VCO (asymmetric) achieves a wide FTR of 25.8% from 51.9 to 67.3 GHz with phase noise variation of ±8.2 dB (−90.2 to −106.7 dBc/Hz at 10 MHz offset) in all sub-bands; and the second VCO (symmetric) realizes a low phase noise variation of ±2.5 dB (−105.9 to −110.8 dBc/Hz at 10 MHz offset) in all sub-bands with a FTR of 14.2% from 57.0 GHz to 65.5 GHz.

Index Terms—CMOS 60 GHz VCO, inductive tuning, loaded transformer, wide-tuning range.

I. INTRODUCTION

DURING last decade, substantial knowledge about the wide frequency bands at 60 GHz and beyond has been accumulated to develop the next generation big-data-rate wireless terminals [1]–[18]. The recent IEEE 802.15.3c standard for wireless local personal network (WPAN) has defined radio-frequency (RF) allocation composed of 4 RF sub-bands at 60 GHz, each with bandwidth of 2.16 GHz. Considering the large frequency range and also large process variation in nanoscale CMOS, the utilization of one single varactor for all 4-sub-band coverage has introduced grand challenge for 60 GHz VCO designed in CMOS process.

Multi-sub-band operation is normally adopted to enhance the total frequency tuning range (FTR) with reduced VCO gain (K_{VCO}) [1]. Conventionally, multi-sub-band operation is implemented with capacitive tuning by switched capacitor banks. When operation frequency scales up to 60 GHz, the parasitic capacitance from the capacitor bank becomes too large and the quality factor of capacitor becomes too low [1], [19]. Recently, inductive tuning has become a promising substitute to replace the capacitive tuning [1], [16], [19]–[25], and is normally implemented by a loaded transformer topology [1], [19], [20]. Besides a wide FTR, inductive tuning can also provide the benefit of isolated DC noise from the tuning element.

The loads on transformer for inductive tuning can be categorized into three types: resistor [1], capacitor [20], and inductor [19]. Wide FTR is then achieved by controlling the value of the load. However, traditional loaded transformer topologies suffer from various limitations. For example, resistor-loaded transformer has a nonlinear tuning-curve with large effective K_{VCO}, which can make PLL difficult to lock [1]. Capacitor-loaded transformer suffers from a narrow FTR due to the limited tuning range and poor quality factor of the varactor at high frequency region [20]. Inductor-loaded transformer requires the use of multiple number of transformers, which constraint the effective number of sub-bands due to layout size and design complexity [19].

A new inductor-loaded transformer is proposed in this paper to overcome the above limitations of inductive tuning by switching different current return-paths in the secondary coil of one transformer. Based on the proposed inductive tuning method, two types of CMOS 60 GHz VCOs were designed and measured. The first topology [17] targets for the maximum achievable FTR by an asymmetric layout implementation. The trade-off is relatively high phase noise variation due to the asymmetrical structure. The second topology targets for a balanced performance of both FTR and phase noise. With a symmetric layout implementation, both low phase noise and low phase-noise variation are achieved over all different sub-bands, while a large FTR can be still maintained.

The rest of paper is organized below. Section II shows a circuit analysis for loaded transformer based inductive tuning, upon which a new inductive tuning structure by switching current return-paths is proposed. Detailed performance analysis is then performed in Section III with a design optimization flow proposed based on the developed analysis. Two 60 GHz VCO
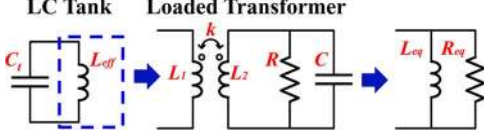
Fig. 1. Equivalent circuit model for inductive tuning of loaded transformer.

topologies are presented in Section IV, each with circuit realization. Simulation and measurement results for the two 60 GHz VCO prototypes are presented in Section V. The paper is concluded in Section VI.

II. LOADED TRANSFORMER FOR INDUCTIVE TUNING

A. Inductive Tuning Mechanism for Loaded Transformer

The mechanism of loaded transformers applied for inductive tuning can be explained by Fig. 1. The loaded transformer is utilized to tune the effective inductance (L_{eff}) in a LC-tank, while C_t consists of the total capacitance in the LC-tank. Note the 3 types of loaded transformers can all be approximately equalized to a RC tank and analyzed with the same equivalent circuit as shown in Fig. 1.

The transformer is assumed to be ideal with coupling factor k, and with L_1 and L_2 as the primary inductance and secondary inductance, respectively. The equivalent circuit with L_{eq} and R_{eq} can then be calculated as

$$
\begin{cases}
L_{eq} = L_1 \times \frac{R^2\left[1-\omega^2 C L_2(1-k^2)\right]^2+\omega^2 L_2^2(1-k^2)^2}{R^2(1-\omega^2 C L_2)[1-\omega^2 C L_2(1-k^2)]+\omega^2 L_2^2(1-k^2)} \\
R_{eq} = \frac{R^2 L_1\left[1-\omega^2 C L_2(1-k^2)\right]^2+\omega^2 L_1 L_2^2(1-k^2)^2}{R k^2 L_2}.
\end{cases}
\tag{1}
$$

Thus the oscillation frequency becomes

$$
\omega = \frac{1}{\sqrt{L_{eq}C_t}}.
\tag{2}
$$

For resistor or inductor-loaded transformer, the FTR of the equivalent circuit can be estimated by considering the two extreme conditions of R in Fig. 1:

$$
\begin{cases}
L_{eq\_max} = L_{eq}(R \to \infty) = L_1 \times \frac{1-\omega^2 C L_2(1-k^2)}{1-\omega^2 C L_2} \\
L_{eq\_min} = L_{eq}(R \to 0) = L_1(1 - k^2).
\end{cases}
\tag{3}
$$

By substituting (3) into (2), the FTR for LC-tank oscillation frequency can be obtained:

$$
\begin{cases}
\omega_{min} = \omega(R \to \infty) = \sqrt{\frac{\omega_1^2+\omega_2^2-\sqrt{\left(\omega_1^2+\omega_2^2\right)^2-4\omega_1^2\omega_2^2(1-k^2)}}{2(1-k^2)}} \\
\omega_{max} = \omega(R \to 0) = \frac{\omega_1}{\sqrt{1-k^2}},
\end{cases}
\tag{4}
$$

where $\omega_1 = 1/\sqrt{L_1 C_t}$ and $\omega_2 = 1/\sqrt{L_2 C}$. As shown in Fig. 1, ω_1 and ω_2 represent the resonant frequencies at the primary side and the secondary side of the transformer, respectively.

Note that ω_1 is pre-determined by parameters of the transformer and the LC-tank, while ω_2 would be affected by the load. By defining $\omega_2 = \alpha\omega_1$, where $\alpha > 0$ is the ratio between two resonant frequencies, we can further analyze the value of $\omega(R \to \infty)$ based on different α values. Since $\partial\omega(R \to \infty)/\partial\alpha$ stays positive for all α values, by taking the

extreme conditions for α, the range for $\omega(R \to \infty)$ can be estimated as

$$
\omega(R \to \infty) \approx \begin{cases} \omega_2, & 0 < \alpha \ll 1 \\ \omega_1, & \alpha \gg 1. \end{cases}
\tag{5}
$$

According to (5), when ω_2 is much higher than ω_1, $\omega(R \to \infty)$ equals to ω_1, indicating negligible dependence between value of $\omega(R \to \infty)$ and the load. However, as ω_2 drops, $\omega(R \to \infty)$ is decreased, approaching the value of ω_2 instead. This is actually the mechanism for frequency-tuning of capacitor-loaded transformer.

The effect of ω_2 value on the quality factor for the effective LC-tank must be considered, which can be easily derived from (1) as

$$
\begin{aligned}
Q_{eq} &= \frac{R_{eq}}{\omega L_{eq}} \\
&= \frac{R}{\omega L_2} \times \frac{\left(1-\frac{\omega^2}{\omega_2^2}\right)\left[1-(1-k^2)\frac{\omega^2}{\omega_2^2}\right]}{k^2} + \frac{\omega L_2}{R} \times \frac{1-k^2}{k^2}.
\end{aligned}
\tag{6}
$$

Note that here the loss from the transformer and the LC-tank is not included into the calculation and Q_{eq} quantifies the additional loss coupled from transformer load into the LC-tank. As (6) shows, this coupled loss is contributed by two portions. When $R \gg \omega L_2$, the first item on the right-side of the equation dominates. When $R \ll \omega L_2$, the second item dominates. Clearly, in the case of $\omega(R \to \infty)$, the first item should be considered. Unfortunately, as ω_2 drops, $\omega(R \to \infty)$ approaches the value of ω_2, forcing Q_{eq} degrades towards 0, which indicates a high degradation on the phase noise performance. As a result, the approach of lowering ω_2 value for larger FTR, suffers significant phase noise degradation. In fact, this is also one limitation for the capacitor-loaded transformer.

Therefore, for resistor or inductor-loaded transformer, the condition $\omega_1 \ll \omega_2$ is required in design optimization. The FTR can then be estimated by

$$
\text{FTR} = \frac{\frac{\omega_1}{\sqrt{1-k^2}} - \omega_1}{\frac{\omega_1}{\sqrt{1-k^2}} + \omega_1} \times 2 = \frac{1-\sqrt{1-k^2}}{1+\sqrt{1-k^2}} \times 2.
\tag{7}
$$

According to (7), to achieve a large FTR, a large k is required. Moreover, according to (6), Q_{eq} approaches infinity when R approaches 0 or infinity, but drops when R moves from the two boundaries. This can explain the performance degradation for resistor-loaded transformer since its major tuning region locates away from these two boundaries.

B. Proposed Inductor-Loaded Transformer by Switching Return-Path

According to Fig. 1 and (1), there are 4 variables: R, C, L_2, and k on the secondary coil of the transformer, which control the oscillation frequency. Resistor-loaded transformer tunes R, capacitor-loaded transformer tunes C, while inductor-loaded transformer tunes both L_2 and k. Conventionally, L_2 and k are tuned by switching on different combinations of transformers [19]. However, the large layout size of loop inductor and strong
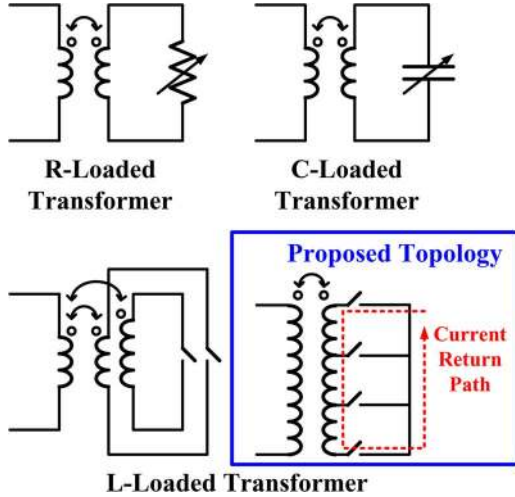
Fig. 2. Traditional resistor-, capacitor-, and inductor-loaded transformers and proposed new inductor-loaded transformer by switching current return-paths with only one transformer.

TABLE I
TRADE-OFFS BETWEEN DIFFERENT LOADED TRANSFORMER TOPOLOGIES

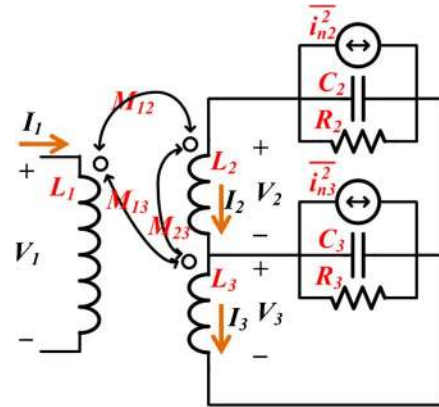| Topology	Benefits	Limitations
R-loaded transformer	• wide tuning range • large sub-band number	• large effective K_{VCO}
C-loaded transformer	• large sub-band number	• limited tuning range
Traditional L-loaded transformer	• wide tuning range	• limited sub-band number
Proposed L-loaded transformer	• wide tuning range	• asymmetric current return path

Fig. 3. Equivalent circuit model for the proposed loaded transformer.

magnetic coupling with adjacent devices limit the number of transformers. Moreover, as more transformers are used, magnetic coupling from different transformers tend to cancel each other, and hence make the tuning less effective. As a result, the number of sub-bands achieved by the conventional inductor-loaded transformer topology often limits to 4 (with 2 transformers used) and below.

In this paper, a new inductor-loaded transformer topology is proposed, which breaks through the limit of the conventional inductive tuning. The concept of the proposed topology can be explained in Fig. 2. Only one transformer is used for the new inductor-loaded transformer, with switches placed at various locations on the secondary coil. When some combination of switches are turned on such that a close-loop is constructed in the secondary coil, a current return-path forms. Different sized current return-paths generate different magnetic fluxes, which are fed back to the primary coil and hence result in multiple sub-bands.

C. Comparison With Traditional Loaded Transformers

Since the proposed topology can increase the number of sub-bands by simply adding more switches, the sub-band number can be easily designed to be larger than 4 with compact layout area when compared to the conventional inductor-loaded transformer.

Moreover, different from the resistor-loaded transformer that has a highly nonlinear tuning-curve and large K_{VCO}, the new inductor-loaded transformer achieves a much smaller K_{VCO} through multi-sub-band operation within linear tuning-curve. As a result, the phase noise performance can be improved with no PLL locking difficulty. The small K_{VCO} may also be used to trade for a wider tuning range, which can be easily realized by implementing with a large coupling factor k, as explained in (7).

In addition, as mentioned in Section II-A, frequency-tuning for capacitor-loaded transformer is realized by varying the value of C and thus ω_2. However, according to (6), as C increases or ω_2 drops, Q_{eq} is severely degraded. As a result, the FTR that can

be achieved is limited. What is more, the FTR for varactor or capacitor-bank is further limited by parasitic capacitance from switches and transformers.

Trade-offs between different loaded-transformer topologies are summarized in Table I. However, one design challenge is how to deal with asymmetric current return-paths in certain sub-bands, which will be discussed in detail in Section IV.

III. DESIGN ANALYSIS AND OPTIMIZATION

A. Model of Inductor-Loaded Transformer With Switches

Since both resistor and capacitor-loaded transformers have the loading at one fixed location on the secondary coil of the transformer, their circuit behavior can be fully emulated by the same equivalent circuit shown in Fig. 1. The inductor-loaded transformer, on the other hand, has switches located on several different locations on the secondary coil. When one part of the secondary coil is turned on and plays the major role in determining the effective inductance on the primary coil, the remaining part of the secondary coil can still affect the performance due to parasitic effect, which is ignored by the simple equivalent circuit in Fig. 1. As a result, one more comprehensive circuit model is developed in Fig. 3 that can provide a more comprehensive model for inductor-loaded transformer.

As shown in Fig. 3, three inductors (L_1, L_2, and L_3) are used to form the simplest topology, and are coupled with each other by the mutual inductances M_{12}, M_{13}, and M_{23}. The terminal voltage and loop current for each inductor are represented by (V_1, I_1), (V_2, I_2), and (V_3, I_3), respectively. The loaded inductance is varied by switching on different combinations of L_2 and L_3, with their switches represented by $(R_2, C_2, \overline{i_{n2}^2})$ and
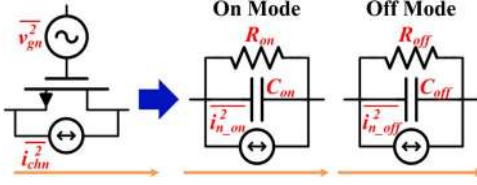
Fig. 4. Equivalent circuit model for switches. R_{on}, C_{on} and $\overline{\iota_{n\_on}^2}$ form the equivalent circuit of switch when it is turned on. R_{off}, C_{off} and $\overline{\iota_{n\_on}^2}$ form the equivalent circuit of switch when it is turned off.

TABLE II
SWITCH PARAMETERS EXTRACTED FROM CMOS 65 nm PROCESS

W_s (μm)	10	20	50	100	200	400
R_{on} (Ω)	41.4	20.5	8.16	4.07	2.04	1.02
R_{off} (Ω)	2.72K	1.36K	543	272	136	67.9
C_{on} (fF)	7.78	15.6	38.9	77.8	156	311
C_{off} (fF)	6.10	12.2	30.5	61.0	122	244

$(R_3, C_3, \overline{\iota_{n3}^2})$, respectively. The resulted L_{eq} and R_{eq} can then be calculated by solving the following equations

$$
\begin{cases}
I_1 = V_1 \times \left(\frac{1}{R_{eq}} + \frac{1}{sL_{eq}} \right) + \overline{\iota_{neq}} \\
V_1 = sL_1 I_1 + sM_{12} I_2 + sM_{13} I_3 \\
V_2 = sM_{12} I_1 + sL_2 I_2 + sM_{23} I_3 \\
V_3 = sM_{13} I_1 + sM_{23} I_2 + sL_3 I_3 \\
V_2 + V_3 + \frac{R_2 I_2}{1+sR_2 C_2} = \frac{R_2 \overline{\iota_{n2}}}{1+sR_2 C_2} \\
V_3 + \frac{R_3(I_3 - I_2)}{1+sR_3 C_3} = \frac{R_3 \overline{\iota_{n3}}}{1+sR_3 C_3},
\end{cases}
\tag{8}
$$

where an equivalent noise current $(\overline{\iota_{eq}^2})$ parallel to the LC tank can be transferred from the noise components of the switches.

B. Switch Design Parameters

To have the performance analysis in (8), we need to extract and optimize switch parameters for performance.

As shown in Fig. 4, switch state parameter in (8) is approximated by a RC-tank, where R_{on} and R_{off} are used to represent its effective resistance for the on and off states. What is more, the effective capacitances are represented by C_{on} and C_{off}. One can build a RC-library model for switches by extracting RC-values based on the 65 nm CMOS process by sweeping as listed in Table II. Note that since the minimum length of switch is used to minimize parasitic capacitance, the size of switch is determined by its width W_s.

For switch noise parameter in (8), the gate noise $(\overline{v_{gn}^2})$ and channel noise $(\overline{\iota_{chn}^2})$ of the switch are transformed to equivalent current noise sources $(\overline{\iota_{n\_on}^2}$ and $\overline{\iota_{n\_off}^2})$ that are parallelly added to the RC tank. Since transformer filters out the low frequency noise, flicker noise is not considered in the model for simplicity. As a result, the noise sources $(\overline{\iota_{n\_on}^2}$ and $\overline{\iota_{n\_off}^2})$ of the switch are estimated as thermal noise in equivalent model.

C. Performance Study

Based on the afore-developed switch and transformer models, performance for the proposed inductor-loaded transformer topology can be further analyzed to obtain the optimized

TABLE III
PARAMETERS FOR 60 GHz VCO DESIGN BASED ON PROPOSED LOADED
TRANSFORMER TOPOLOGY

Switch	Transformer			Other
W_s (um)	L_{prim} (pH)	L_{sec} (pH)	k	C_t (fF)
10~400	80	80	0.1~0.7	100

design with respect to switch sizing W_s. With extracted switch parameters such as in Table II, switch performance under various sizes W_s can be studied. Based on the design parameters summarized in Table III, we have the following detailed performance study.

Firstly, impact of switches to the FTR performance is studied in Fig. 5(a). Confirmed with our conclusion in (7), a larger coupling factor k leads to a wider FTR. When switch size is small, the FTR is also observed to increase with switch size. This can be explained by the analysis in Section II-A, where a larger C_{on} would raise the FTR when R_{off} is sufficiently large. However, as switch size further increases, R_{off} becomes too small to fully switch off the current return path, and FTR starts to decrease.

Secondly, impact of switches to phase noise performance can be also analyzed. Switches on loaded transformer degrade the phase noise performance from two aspects. It can decrease output signal power by reducing the effective Q factor in LC-tank; and also increase phase noise by transferring noise power to output nodes. These two aspects are analyzed in Fig. 5(b) and (c), by examining the minimum Q factor of the LC-tank and the maximum output noise spectral density at the offset frequency. One can observe that there is an optimal switch size for the minimum phase noise degradation.

D. Design Optimization Flow

As such, we present a design flow in Fig. 6 to optimize the specific performances of the proposed inductor-loaded transformer topology. The targeted frequency ($freq.$) and tuning range (FTR) define the minimum frequency (f_{min}) and maximum frequency (f_{max}) to be designed. With the proposed tuning topology, f_{min} is mainly determined by the inductance of the primary coil (L_{prim}) and the total capacitance in LC-tank (C_t). Due to the single-loop topology adopted for the proposed transformer, the inductance on its secondary coil (L_{sec}) can be accordingly determined.

Firstly, with the given FTR and targeted K_{VCO}, we can calculate the number of sub-bands (N_{band}) needed, thus determining how many switches are required as well as their locations on the secondary coil. Each sub-band is then to be fully covered by a varactor pair as fine tuning. Therefore the tuning capacitance (C_{tune}) is determined for varactor design. Besides C_{tune}, the rest part of C_t is mainly contributed from the parasitic capacitance in the cross-coupled transistors, which can help determine the transistor sizes.

Next, given L_{prim}, L_{sec}, and C_t, f_{max} is mainly determined by the coupling factor k of the transformer. For a specific k value, an optimized switch size can be found to minimize the phase noise (PN) as Fig. 5(b) and (c) shows. Note that since both phase noise and power consumption are related to the sizing and biasing of cross-coupled transistors, a few design
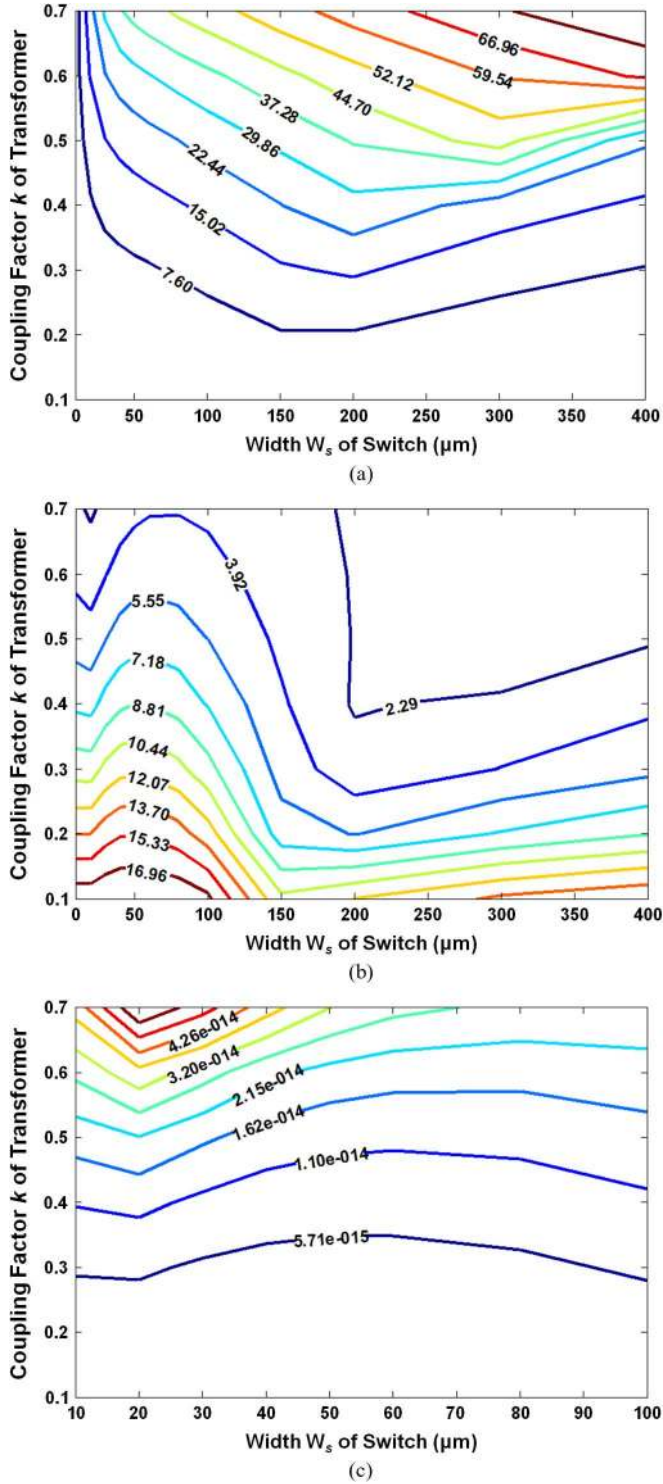
Fig. 5. Design optimization for (a) frequency tuning range, (b) the minimum quality factor in the tuning range and (c) the maximum output noise spectral density at 10 MHz offset in tuning range.

iterations are required to meet the targeted performance for all specifications.

IV. IMPLEMENTATION FOR WIDE-TUNING 60 GHz VCO

To realize multiple sub-bands for the proposed inductor-loaded transformer, switches are loaded at various locations on the secondary coil of one transformer. As the number of switches increases, the total capacitance and resistance loaded on the transformer increases and decreases, respectively. As analyzed in Section II-A, for the conditions when switches are turned off, both a larger C and a smaller R would weaken the domination of the terms $R^2[1 - \omega^2 C L_2(1 - k2)]2$ and $R21 - \omega2CL21 - \omega2CL21 - k2$ in (1), resulting in a smaller FTR. As a result, the number of switches loaded on the transformer should be minimized while providing enough sub-bands.

As a result, there are two topologies studied in this part. The first topology realizes the maximum number of sub-bands with the least number of switches, thus can achieve the maximized FTR. The penalty is an asymmetric layout implementation, which may cause certain degradation in the phase noise performance. The second topology adopts a symmetric layout implementation with the optimized tuning mechanism for the switches. Both phase noise and phase noise variation are thus improved. The penalty is the use of more switches than the first topology, leading to a relatively narrower FTR. These two topologies can be utilized for different applications with different design targets.

A. Asymmetric Implementation

The first proposed topology targets for the maximum FTR, with layout implementation shown in Fig. 7. A transformer is loaded with 4 switches (S1∼S4) at different locations. The inner loop is the primary coil, which serves as the inductor of the LC-tank. The outer loop is the secondary coil, which is loaded with 4 switches to control the current return-paths. Lengths of the 4 sections in the secondary coil are marked with unit length l. Different combinations of the switches and corresponding effective lengths of the current return-paths are summarized in Table IV. There are in total 7 modes or sub-bands established. For example, by turning on switches S1 and S2, the mode 3 is invoked with a current return-path formed with length $3l$. Moreover, as shown in Table IV, the effective length of return-path in secondary coil varies from 0 to $6l$ linearly, resulting in 7 evenly distributed sub-bands. Evenly distributed sub-bands can facilitate PLL design and also improve its performance.

Note that more sub-bands can be realized by implementing more switches but may also degrade the phase noise performance. As derived in Section II and III, a small switch R value is desired to minimize phase noise degradation. As such, the number of switches should be minimized when connected in serial in the activated current return-path. The proposed band selection method in Fig. 7 and Table IV can minimize the number of switches in the current return-path to be 2 or below for all selection modes.

With an asymmetric allocation of switches, this layout implementation realizes 7 sub-bands with only 4 switches. As a result, a maximized FTR can be achieved. The trade-off is that the asymmetric switch locations and current return-paths would have a large phase noise variation due to different current return-paths in each sub-band.

B. Symmetric Implementation

The second proposed topology targets for a balanced performance of both FTR and phase noise variation in each sub-band,
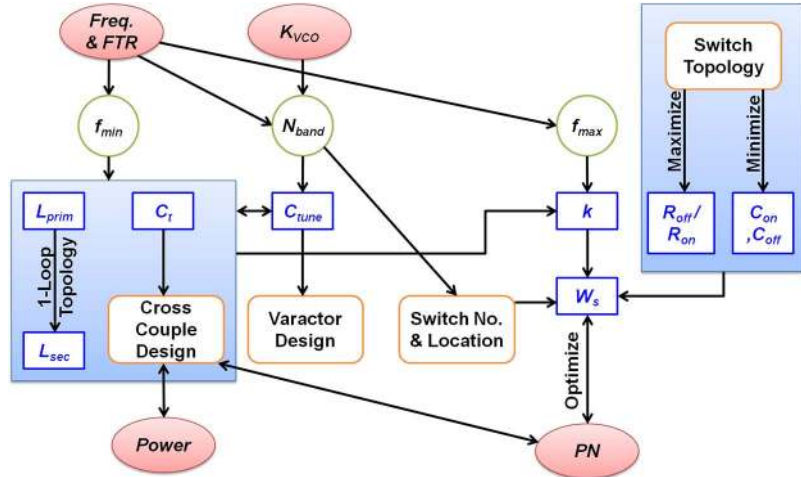
Fig. 6. Design optimization flow for wide-tuning VCO based on the proposed inductor-loaded transformer, where performance metrics are frequency, FTR, K_{VCO}, power, and phase noise.
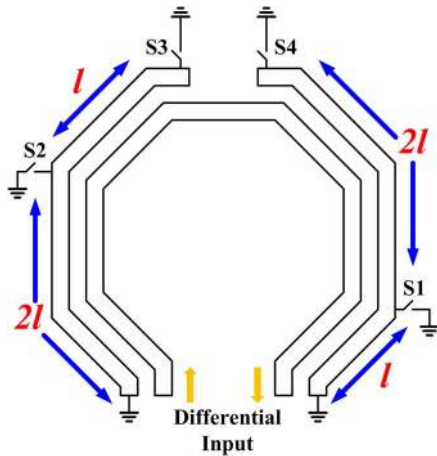

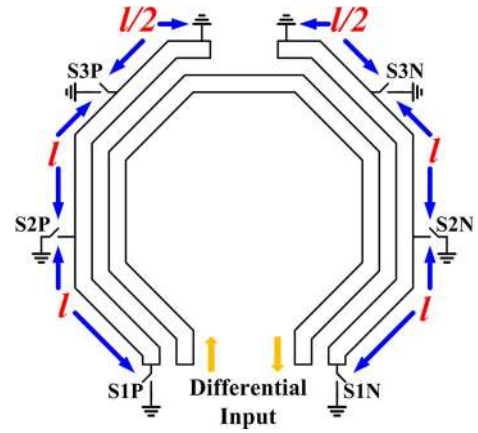Fig. 7. Asymmetric layout implementation for the proposed new inductor-loaded transformer [17].

Fig. 8. Symmetric layout implementation for the proposed new inductor-loaded transformer.

TABLE IV
EFFECTIVE RETURN PATH LENGTHS IN SECONDARY COIL FOR DIFFERENT
SUB-BAND SELECTION MODES IN ASYMMETRIC LAYOUT IMPLEMENTATION

Sub-band Selection Mode	0	1	2	3	4	5	6
On Switches	Nil	S1	S2	S1+S2	S1+S3	S2+S4	S3+S4
Effective Length of Return Path	0	l	$2l$	$3l$	$4l$	$5l$	$6l$

with symmetric layout implementation shown in Fig. 8. Since a symmetric topology with differential operation lowers undesired common-mode effects such as substrate and supply noise amplification and up-conversion [26], the phase noise performance is improved. In Fig. 8, the symmetric topology is realized by placing 3 pairs of switches (S1P/N∼S3P/N) on the secondary coil of transformer with vertical symmetry.

Note that with symmetric switch locations, if the current return-path is also configured symmetrically, the number of sub-bands is highly limited. For N pairs of switches, only $N+1$ sub-bands can be created. To realize a targeted FTR and K_{VCO}, more pairs of switches would then be required to generate enough sub-bands, which would add loss to the loaded transformer and degrade phase noise performance.

In this work, the following tuning scheme is designed to overcome the aforementioned challenge. As shown in Fig. 8, one switch on each side of virtual ground is turned on in all sub-band selection modes except the default mode 0 where all switches are off. Different sub-bands are then changed by shifting the ON-switch locations on each side alternately. In this fashion, the number of sub-bands created is nearly doubled while maintaining a small difference in the selected current return-path lengths on both sides. For N pair of switches, $2N$ sub-bands can be created.

One example is shown in Table V, 6 sub-bands are generated using 3 pairs of switches. The effective length of return-path in secondary coil varies from 0 to $5l$ linearly when the mode is switched from 0 to 5. In addition, the maximum difference in the effective length on both sides is maintained within l. As verified by measurement, this symmetrical configuration results in low

TABLE V
EFFECTIVE RETURN PATH LENGTHS IN SECONDARY COIL FOR DIFFERENT
SUB-BAND SELECTION MODES IN SYMMETRIC LAYOUT IMPLEMENTATION

Sub-band Selection Mode	0	1	2	3	4	5
On Switches	Nil	S3N+S3P	S2N+S3P	S2N+S2P	S2N+S1P	S1N+S1P
Effective Length of Return Path	0	l	$2l$	$3l$	$4l$	$5l$

phase noise with small variation across all sub-bands, while still maintaining a high FTR.

C. 60 GHz VCO Circuit

To verify the proposed inductive tuning, two VCO prototypes are designed at 60 GHz with both asymmetric and symmetric implementations. Both VCOs can provide multiple frequency sub-bands to cover the wide frequency band at 60 GHz.

As shown in Fig. 9, power supply is fed on the central tap. A varactor-pair is used for fine tuning within each sub-band. The LC-tank loss is compensated by a cross-coupled NMOS pair. Two output buffers are utilized for the power gain and isolation. The transformer is implemented with the top metal layer for high Q. To implement a proper k value, a gap size of 3.5 μm is designed between transformer primary and secondary coils in the asymmetric implementation, while a gap of 2.5 μm is selected for the symmetric implementation. Once the coupling factor of transformer is determined, an optimized switch size can be found. A size of 50 μm/60 nm is adopted for switch transistors in the asymmetric implementation, while a size of 64 μm/60 nm is adopted in the symmetric implementation. The size differences between two designs come from process and topology differences, as will be discussed in Section V-B.

With the tuning scheme proposed in Tables IV and V, there are 7 and 6 sub-bands generated by the two VCOs, respectively. While the asymmetric VCO provides a wider FTR due to more sub-bands and fewer loaded switches thus smaller parasitic capacitance, the symmetric VCO significantly improves the phase noise performance with highly suppressed phase noise variation and can still achieve a wide FTR.

V. EXPERIMENT RESULTS

A. Loaded-Transformer Simulation Results

1) Model Validation: The proposed model in Section III is used to analyze the asymmetrical implementation in Fig. 7. Transformer parameters are extracted from EM simulation, as summarized in Table VIII in Section V-B. C_t from Fig. 1 is adjusted to be 92 fF. Calculated VCO oscillation frequency and noise density contributed by switches are plotted in Fig. 10, both of which can roughly fit the simulation results from Cadence. This validates the proposed model. Note a larger deviation occurs at lower frequency bands, which is due to neglect of flicker noise in switch model, as will be addressed in Section V-B.

2) Comparison Between Loaded Transformer Topologies: The four topologies in Fig. 2 are simulated numerically in MATLAB for performance comparison. To achieve a fair
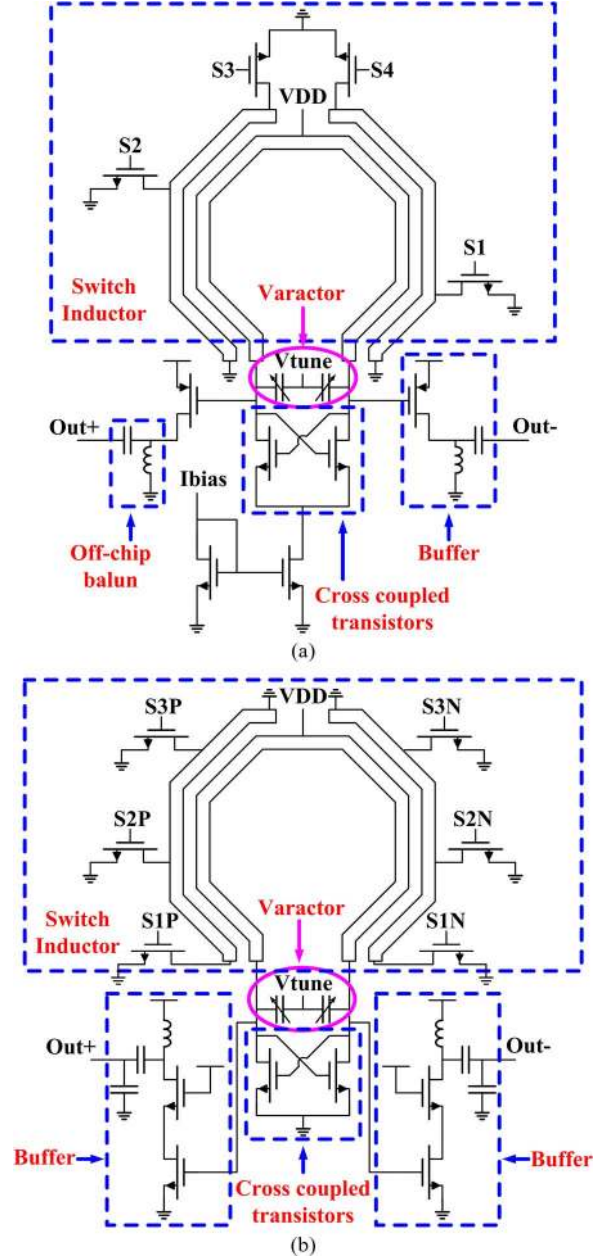

Fig. 9. Schematic of the 60 GHz inductive-tuning VCO with the inductor-loaded transformer implemented by switching current return-paths: (a) Asymmetric implementation [17], (b) symmetric implementation.

comparison, while both resistor and capacitor-loaded transformers are simulated by the equivalent circuit shown in Fig. 1, the inductor-loaded transformers are simulated based on more comprehensive models shown in Fig. 3 to consider parasitic effects on the secondary coil. Parameters derived in Section III-B are used to assist numeric analysis for the proposed inductor-loaded transformer topology. The same parameters are utilized to simulate resistor-loaded transformer (Table VI), with its resistance linearly varied between the on and off resistances (R_{on} and R_{off}) of the 50 μm switch in Table II. The linear change can be achieved by splitting the switch into parallel array of smaller switches [1]. Similarly, for the capacitor-loaded transformer, a switched capacitor bank can be used to obtain linear and large tuning range than single
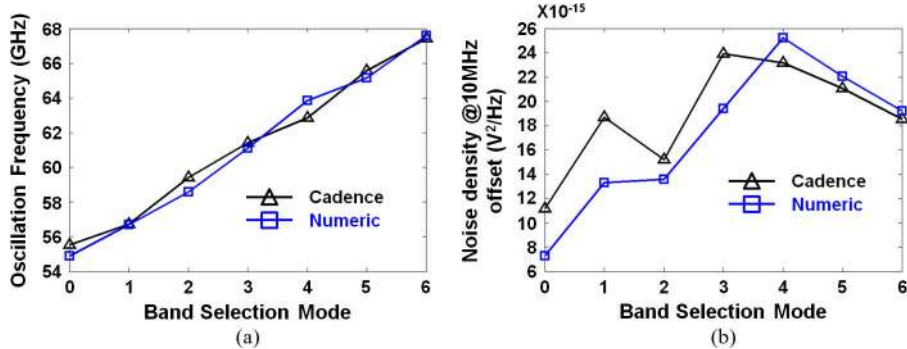
Fig. 10. Model validation: (a) oscillation frequency, (b) output noise density contributed by switches.
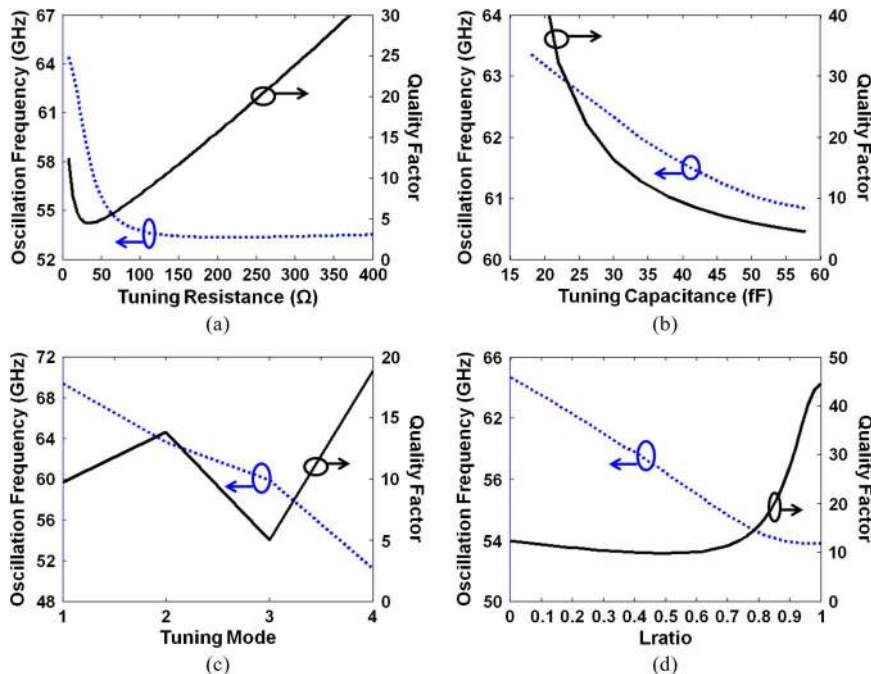

Fig. 11. Numeric simulation for tuning range and quality factor of different loaded transformers: (a) R-loaded transformer, (b) C-loaded transformer, (c) traditional L-loaded transformer, (d) proposed new loaded transformer.

TABLE VI
PARAMETERS FOR DIFFERENT LOADED TRANSFORMERS BIASED FOR 60 GHz
BAND OSCILLATION

Loaded Transformer	R-loaded	C-loaded	L-loaded	Proposed
L_{prim} (pH)	80	60	80	80
L_{sec} (pH)	80	60	N.A.	80
Coupling factor	k=0.5	k=0.5	k_{12}=k_{13}=0.5 k_{23}=0.4	k=0.5
L_{ratio}	N.A.	N.A.	0.3	0→1
C_{ratio}	N.A.	3.206	N.A.	N.A.

varactor. The penalty is the parasitic from the switches in the capacitor bank, which is also the major limitation for its tuning range. With the extracted switch parameters in Table II, the effective capacitance ratio when the switch is on and off for each bank ($C_{ratio} = C_{off}/C_{on}$) is analyzed. A value of 3.206 is obtained for C_{ratio} and is used for this analysis.

All loaded transformers designed to provide the same oscillation frequency in 60 GHz band. The adjusted parameters are summarized in Table VI, and the simulated tuning range and quality factor are shown in Fig. 11. To have a direct view of the extra loss coupled from the tuning elements into the LC-tank, similar definition of quality factor as (6) is used. With this definition, the quality factor represents how much degradation on the whole LC-tank quality factor (or phase noise performance) will be caused by the tuning elements loaded on the transformer.

Firstly, as Fig. 11(a) shows, the resistor-loaded transformer has a highly nonlinear tuning-curve with respect to tuning resistance. Most of the frequency tuning is realized in a narrow region of the tuning resistance, where the lowest quality factor also locates. Next, the capacitor-loaded transformer, as Fig. 11(b) shows, has a very linear tuning-curve. Besides its quality factor degradation in the lower frequency region, its major limitation is the narrow tuning range which comes from the limited tuning ability of varactor or capacitor bank. Lastly, for the traditional inductor-loaded transformer shown in Fig. 11(c), there are only 4 sub-bands within the tuning

TABLE VII
PERFORMANCE SUMMARY FOR DIFFERENT LOADED TRANSFORMER
TOPOLOGIES BASED ON NUMERIC ANALYSIS

Loaded Transformer	R-loaded	C-loaded	L-loaded	Proposed
Tuning Range	Large	Small	Large	Large
Linearity	Low	High	Medium	High
Quality factor Degradation	High	Medium	Medium	Low
Band number	Large	Large	Small	Medium

TABLE VIII
EM EXTRACTED PARAMETERS AT 60 GHz FOR ASYMMETRIC AND SYMMETRIC
LOADED TRANSFORMER IMPLEMENTATIONS

Loaded Transformer	L_1 (pH)	L_2 (pH)	M_{12} (pH)	k
Asymmetric	154.2	175.5	77.3	0.470
Symmetric	153.1	136.9	44.6	0.308

Fig. 12. Parameter extraction for two loaded transformer designs under various band selection modes.

range. Besides its limitation on the number of sub-bands that can be achieved, the inductor-loaded transformer also suffers from high degradation on quality factor in the middle region (mode 3) of its tuning range. Different from the resistor-loaded transformer, this degradation comes from magnetic coupling from L_3 to L_2 when L_2 is switched on and L_3 is off. Recall that multiple transformers needed by the traditional inductor-loaded transformer would cause large area overhead as well.

In contrast, the proposed inductor-loaded transformer does not have this degradation. Due to the single-loop topology adopted for the transformer, the coupling between different portions on the secondary coil is much weaker. As Fig. 11(d) shows, a linear tuning curve is obtained with a large FTR, and with low degradation on quality factor in the whole tuning range at 60 GHz by the proposed inductor-loaded transformer.

The performances of different loaded transformers are summarized in Table VII. The numeric simulations confirm with our observations in Section II-C that the proposed new inductor-loaded transformer can realize a wide FTR with high linearity and low K_{VCO} and also can achieve multiple sub-bands with compact size. What is more, low degradation on LC-tank quality factor and hence better VCO phase noise performance can also be maintained in the whole tuning range by the proposed inductor-loaded transformer. As shown in Fig. 11(d), a 20% FTR with linear tuning curve is achieved with a Q factor above 10 for all sub-bands.

B. VCO Circuit Simulation Results

The two 60 GHz VCOs discussed in Section IV-C are both implemented in CMOS 65 nm process. EM simulation (ADS-Momentum) is used for circuit design and verification before the fabrication. The asymmetric 60 GHz VCO is implemented in STM 65 nm 1P7M CMOS process, and the symmetric 60 GHz VCO is implemented in Global Foundries 65 nm CMOS 1P8M process.

1) Loaded Transformer Design: For a fair comparison, different transformer and switch sizes are designed for the two fabrications to achieve the same primary inductance L_1 as well as equivalent Q-factors Q_{eq}. In this way, similar oscillation frequency as well as similar loss introduced by loaded transformer can be ensured. The extracted parameters for both transformers are summarized in Table VIII, and the equivalent circuit parameters under various band selection modes are plotted in Fig. 12. Also note that a square shape is adopted for the second transformer for ease of switch allocation. Though an octagonal shape is theoretically less lossy, the effect is minimal for single-loop transformer at 60 GHz according to simulation.
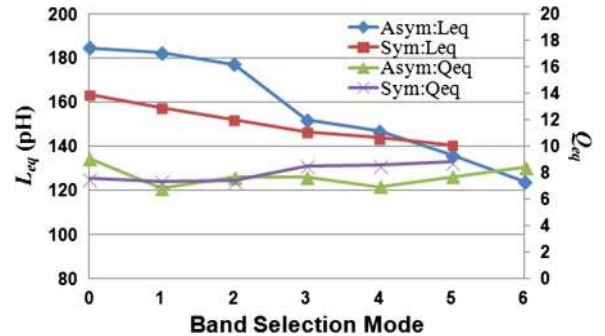
2) Phase Noise Analysis: To further analyze the proposed loaded-transformer influence on VCO phase noise (PN) performance, percentage of noise contribution from switches on loaded transformer to output is simulated and plotted in Fig. 13. Both asymmetric and symmetric loaded transformers were analyzed at offset frequencies of 1 MHz and 10 MHz.

Less noise contribution is observed for symmetric implementation compared with asymmetric implementation. Although similar Q_{eq} values in Fig. 12 indicate similar loss introduced by loaded transformers, a smaller k value means less noise coupling from switches, which gives better PN performance at the penalty of smaller FTR. As such, one can observe 4 dB improvement of average PN performance for symmetric loaded-transformer design.

The drain-to-source thermal noise from the "ON" switches in current return path is also analyzed in Fig. 13. In high frequency bands, where a large current return path is formed, thermal noise from "ON" switches dominate the total noise contribution. However, at lower frequency bands, where large portion of secondary coil is left floating, noise contribution from "OFF" switches not in the current return path comes in.

The deviation of total switch noise between 1 MHz offset and 10 MHz offset shows the role of flicker noise from switches. In our numeric analysis, flicker noise was ignored due to DC blocking and low up-conversion ratio of switches biased in triode region. However, a large AC signal on the secondary coil of transformer could drive the switch towards saturation region with negative voltage swing, leading to higher up-conversion ratio. In lower frequency bands, where large portion of secondary coil is left floating, a standing wave would be formed on the floating coil, introducing a large voltage swing at the floating end, which drives switches into saturation region. As a result, more flicker noise is up-converted and coupled to output. In higher frequency bands, the floating coil becomes shorter and the contribution of flicker noise from switches become negligible, as indicated in Fig. 13.
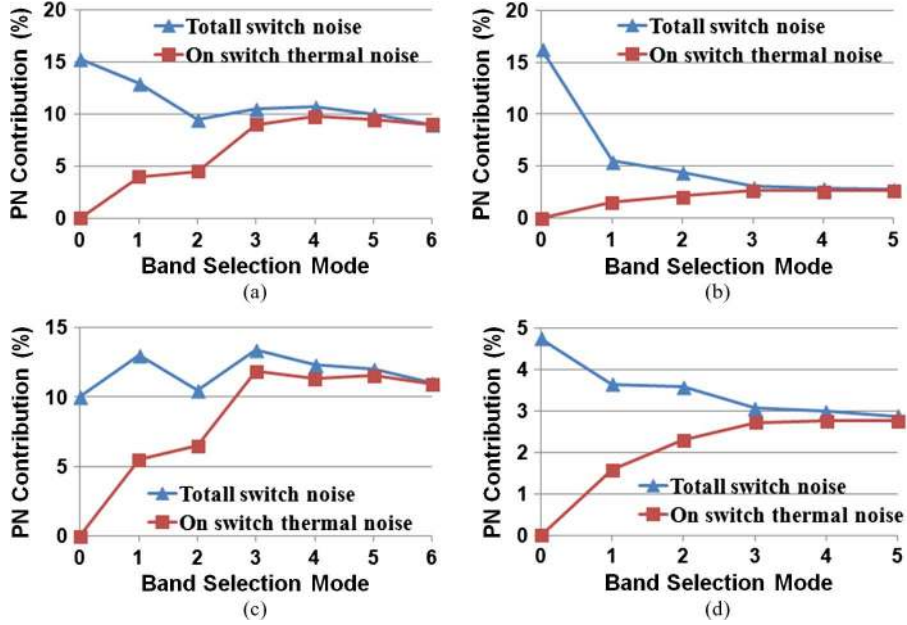
Fig. 13. Percentage of noise contribution from switches on asymmetric ((a) 1 MHz offset, (c) 10 MHz offset) and symmetric ((b) 1 MHz offset, (d) 10 MHz offset) loaded transformer implementations. Both total noise from all switches and drain-to-source thermal noise from "on" switches are plotted.

C. Fabrication Measurement Results

The measurements are then done on CASCADE Microtech Elite-300 probe station, with Agilent PNA-X spectrum analyzer, E5052 source signal analyzer, and 11970 V harmonic mixer. In asymmetric VCO, a 67 GHz bias-T is used to provide load to buffer. In symmetric VCO, the whole buffer is realized on-chip.

As mentioned in Section IV, there tends to be a large variation for VCO phase noise performance at different sub-bands due to the wide FTR and different switching conditions. Since a large phase noise variation across sub-bands would significantly degrade the PLL performance, we introduce a new phase noise (PN) performance in this work with the following equation

$$PN = \overline{PN} \pm \sigma_{PN}, \tag{9}$$

where $\overline{PN}$ and σ_{PN} are the mean and variation of phase noise across all sub-bands. The phase noise variation (σ_{PN}) can then be used as a new figure-of-merit for wide FTR VCO design at 60 GHz.

1) Asymmetric Implementation: The die photo for the designed asymmetric 60 GHz VCO is shown in Fig. 14. Decoupling capacitors are implemented by MIM capacitors and used to stabilize DC signals. The total area is $852 \times 451 \ \mu m^2$, which is mainly constrained by PADs. The core area takes only $163 \times 190 \ \mu m^2$.

With 1 V VDD and Vtune varied from 0.5 to 1.5 V, the obtained tuning curves under different sub-band selection modes are plotted in Fig. 15. The entire tuning range is divided into 7 sub-bands. Within each sub-band, a tuning range of 2.5~4.5 GHz is achieved by a small varactor. Evenly distributed sub-bands are preferred for the easy PLL implementation, which can be achieved by adjusting locations of switches. The obtained oscillation frequency varies from 51.9 to 67.3 GHz, which covers the whole 60 GHz band in IEEE 802.15.3c standard and provides a FTR of 25.8%. The effective K_{VCO} in each band varies
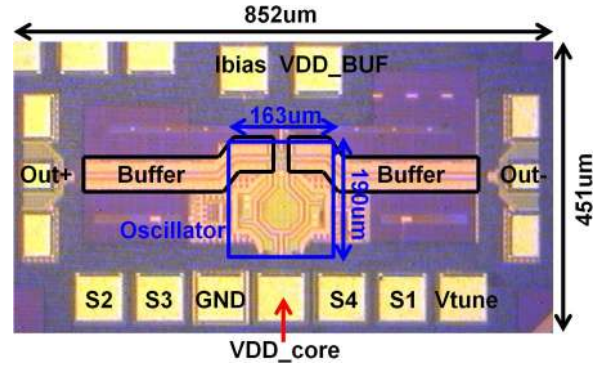

Fig. 14. Die photo for the 60 GHz asymmetric VCO with fabricated in STM 65 nm CMOS process [17].

from 2.1 to 3.8 GHz/V. Note the tuning voltage (0.5~1.5 V) is selected to provide maximum tuning range for varactor, and can be easily changed to 0~1 V by adding a serial capacitor between varactor and power supply.

A sample of phase noise plot is shown in Fig. 16(a). At 60 GHz, the phase noise is -106.7 dBc/Hz at 10 MHz offset. The measured phase noise performance for all modes is shown in Fig. 16(b). Due to the low output power, there is a deviation in phase noise from simulation. Moreover, as expected in Section IV-A, degradation in phase noise variation is observed in Fig. 16(b), which mainly comes from asymmetric sub-band selection topology. As a result, a large phase noise variation (σ_{PN}) of 8.2 dB is observed.

2) Symmetric Implementation: The die photo for the designed symmetric 60 GHz VCO is shown in Fig. 17. The VCO core occupies an area of $140 \times 220 \ \mu m^2$. The overall chip size is $840 \times 750 \ \mu m^2$, including the test buffer and all the pads.

The DC power dissipation of the VCO is 6 mW at supply voltage of 1.0 V. The low power consumption is due to the
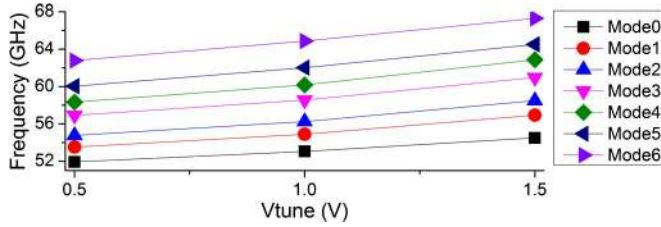
Fig. 15. Measured tuning curves under different band selection modes for the 60 GHz asymmetric VCO [17].

Fig. 18. Measured tuning curves under different band selection modes for the 60 GHz symmetric VCO.
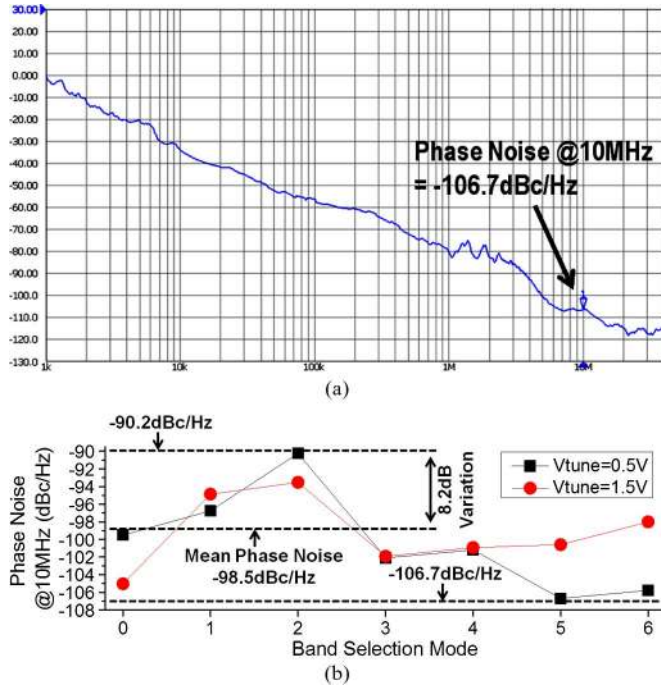

Fig. 16. Measured phase noise performance for the 60 GHz asymmetric VCO. (a) Phase noise at 60 GHz. (b) Phase noise variation for all selection modes [17].

Fig. 19. Measured phase noise performance for the 60 GHz symmetric VCO. (a) Phase noise at 60.8 GHz. (b) Phase noise variation for all selection modes.
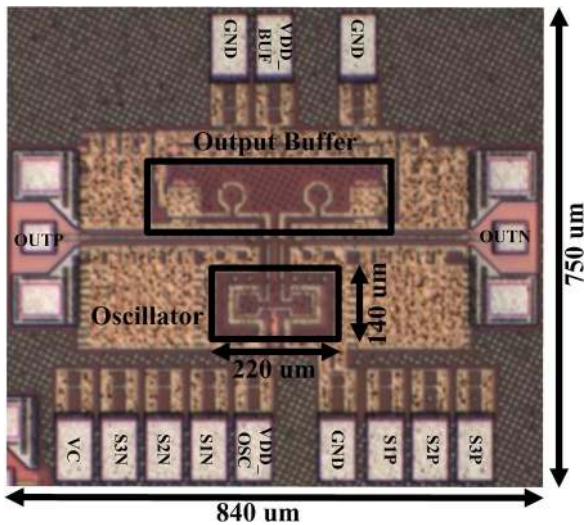

Fig. 17. Die photo for the 60 GHz symmetric VCO fabricated in Global Foundries 65 nm CMOS process.

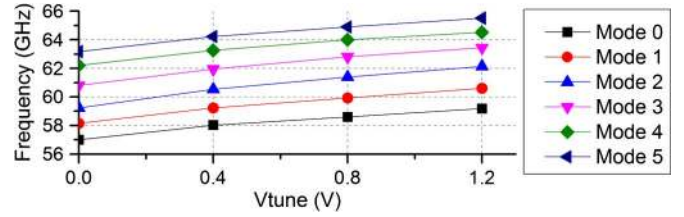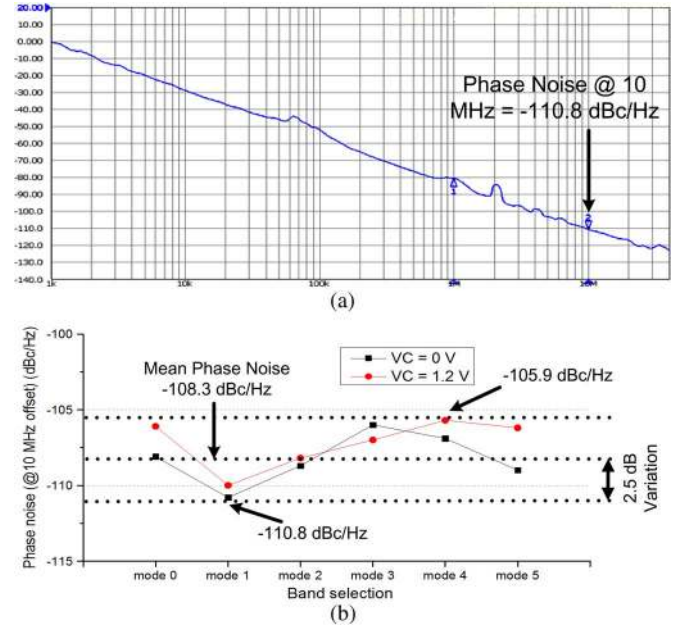designed high quality factor of the symmetrical transformer. Fig. 18 shows the measured tuning curves with dependence on the control voltages. One can observe that the VCO can exhibit 6 sub-bands with oscillation in a wide FTR from 57.0 GHz to 65.5 GHz, which covers the whole 60 bands in IEEE 802.15.3c standard. The tuning range is 8.5 GHz with 14.2% of the center frequency. The effective K_{VCO} in each band varies from 1.8 to 2.4 GHz/V.

Moreover, Fig. 19 shows the measured phase noise at 10 MHz offset frequency of the VCO. In the required frequency range (58.32–64.80 GHz), the phase noise at 10 MHz frequency offset is lower than -105 dBc/Hz. Both the mean phase noise ($\overline{PN}$) and phase noise variation (σ_{PN}) has been significantly improved over the first asymmetric design due to symmetric tuning adopted, with $\overline{PN}$ improved to -108.3 dBc/Hz and σ_{PN} reduced to 2.5 dB. Though the trade-off is reduced FTR, a large tuning range of 14.2% is still achieved. In addition, the measured spectra of the output signals under different modes are shown in Fig. 20. The starting frequency under different modes distribute evenly as expected, with a small variation from 1 GHz to around 1.6 GHz. Note that this variation could be further suppressed by adjusting switch locations.

As a summary, the comparison of both two VCO prototypes is made with the previously published 60 GHz VCOs in Table IX. The first asymmetric VCO is able to achieve a very wide FTR of 25.8% with the moderate figure-of-merits (FOM and FOM_t)
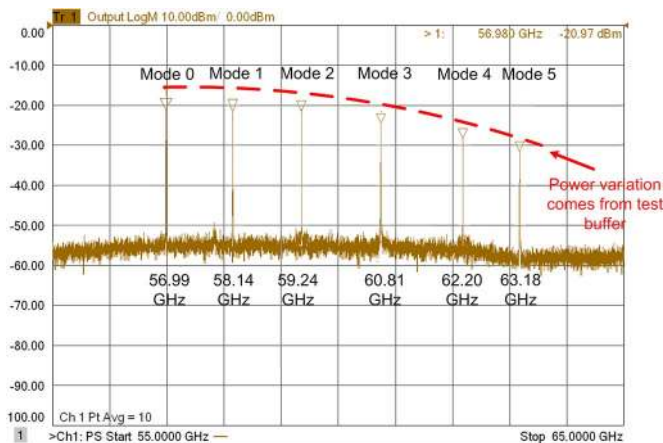
Fig. 20. Measured output spectrum of equally-spaced starting frequencies under 6 different modes for the 60 GHz symmetric VCO.

TABLE IX
PERFORMANCE SUMMARY AND COMPARISON OF WIDE-TUNING 60 GHz VCOS

		[27]	[28]	[29]	Asym. VCO Prototype [17]	Sym. VCO Prototype
Process (CMOS)		90 nm	65nm	65 nm	65 nm	65 nm
Freq. (GHz)	f_{OSC}	76.5	70.2	77	59.6	61
Freq. Tuning Range (%)	FTR	7.0	9.6	14.5	**25.8**	**14.2**
Phase Noise (dBc/Hz)	PN	−110.6	−106.0	−112	−106.7	−110.8
Phase Noise Mean (dBc/Hz)	$\overline{PN}$	−107.1	−99.5	−108.5	−98.5	−108.3
Phase Noise Variation (dB)	σ_{PN}	3.5	6.5	3.5	8.2	**2.5**
Power (mW)	P_{DC}	19.4	5.4	190	**5.4**	6.0
Area (mm²)	A	0.01	0.003	0.15	0.031	0.031
Figure of Merit (dBc/Hz)	$FOM^{(1)}$	−171.9	−169.1	−163.4	**−166.7**	**−176.2**
Figure of Merit (dBc/Hz)	$FOM_t^{(2)}$	−168.8	−168.8	−166.7	**−174.9**	**−179.3**

$^{(1)}$ $FOM = \overline{PN} - 20\log(100 \times f_{OSC}) + 10\log(P_{DC})$
$^{(2)}$ $FOM_t = \overline{PN} - 20\log(100 \times f_{OSC}) - 20\log(FTR/10) + 10\log(P_{DC})$

defined in ITRS. A large phase noise variation of 8.2 dB is observed because of asymmetric design. The second symmetric VCO shows improved phase noise with significantly reduced phase noise variation. The lowest phase noise variation (σ_{PN}) of 2.5 dB is achieved in the table with a phase noise mean ($\overline{PN}$) of −108.3 dBc/Hz while a high FTR of 14.2% is still maintained, leading to a state-of-art FOM_t of −179.4 dBc/Hz.

VI. CONCLUSION

A new inductive tuning by inductor-loaded transformer is proposed in this paper for wide frequency tuning range (FTR) VCO of all sub-bands at 60 GHz. Different from previously published inductive tuning methods, by configuring different current return-paths in the secondary coil of one transformer, wide multi-sub-band tuning can be achieved within compact area by only one transformer. With the use of the proposed new inductive tuning method, two VCO topologies are realized in 65 nm CMOS with design targets for the maximum FTR and the balanced phase noise performance, respectively. Measurement results show that the first VCO achieves a FTR of 25.8%

from 51.9 to 67.3 GHz, and a 10 MHz-offset phase noise varied from −90.2 to −106.7 dBc/Hz across all sub-bands; and the second VCO achieves a FTR of 14.2% from 57.0 GHz to 65.5 GHz, and a 10 MHz-offset phase noise varied from −105.9 to −110.8 dBc/Hz across all sub-bands. The demonstrated VCOs have shown great potential for integration in 60 GHz transceiver with wide FTR and small phase noise.

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Dr. Yu received the Best Paper Award from the ACM Transactions on Design Automation of Electronic Systems (ACM-TODAES'10), Best Paper Award nominations (DAC'06, ICCAD'06, ASP-DAC'12), Student Paper Competition Final List (SiRF'13, RFIC'13), and the Inventor Award from Semiconductor Research Cooperation. He is an associate editor and technical program committee member of several IEEE/ACM journals and conferences.

Haipeng Fu (S'06–M'12) received the B.S. degree in communication engineering from Harbin Institute of Technology, China, in 2007. He received the Ph.D. degree from Fudan University, Shanghai, China, in 2012.

He is currently working as research staff at Tianjin University, Tianjin, China. His research interests include RF and millimeter-wave IC design.

Junyan Ren (M'01) received the B.S. degree in physics in 1983 and the M.S. degree in electronics engineering in 1986, all from Fudan University, China.

He joined the Department of Electronics Engineering, Fudan University, in 1986 and the State Key Laboratory of ASIC and System in 1994. In 2000, he became a full Professor of Microelectronics at Fudan University. His research interests include CMOS RF/Mm-wave/mixed-signal design for wireless/optical communication, medical imaging system applications. He has granted over 20 patents, authored or co-authored over 150 technical papers.

Prof. Ren was the recipient of 1999 Distinguished Young Faculty Award and 2008 Excellent Subject Chief Scientists Award from Shanghai government, and 2004 Excellent Graduate Advisor Award from Fudan University. He is the Senior Member of China Institute of Communications.

Wei Fei (S'10) received the B.S. degree in Electrical and Electronic Engineering from Nanyang Technological University, Singapore, in 2007. He is currently working towards the Ph.D. degree in the School of Electrical and Electronic Engineering at Nanyang Technological University.

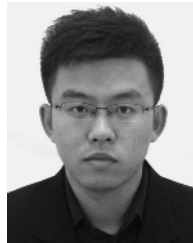His research interests include RF and millimeter-wave frequency IC design.

Hao Yu (M'06–SM'13) received the B.S. degree from Fudan University, Shanghai, China in 1999, and M.S. and Ph. D degrees from the Electrical Engineering Department, University of California, Los Angeles, CA, USA, in 2007, with a major in integrated circuit and embedded computing.

He was a Senior Research Staff at Berkeley Design Automation (BDA). Since October 2009, he has been an Assistant Professor at the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore. His primary research interests are 3D-IC and RF-IC at nano-tera scale. He has 100 peer-reviewed journal and conference publications.

Kiat Seng Yeo (M'00–SM'09) received the B.Eng. degree in electrical engineering (with Honors) and the Ph.D. degree in electrical engineering from Nanyang Technological University (NTU), Singapore, in 1993 and 1996, respectively.

He is an Associate Chair (Research) with the School of Electrical and Electronic Engineering, NTU. He is a widely known authority on low-power RF/millimeter-wave integrated circuit (IC) design and a recognized expert in CMOS technology. He has secured over S$30 M of research funding from various funding agencies and the industry over the last three years. He was the Founding Director of VIRTUS, a S$50 M research centre of excellence jointly set up by NTU and the Economic Development Board. He has authored or co-authored six books, three book chapters, and 320 international top-tier refereed journal and conference papers. He holds 25 patents.

Dr. Yeo is a Board member of the Singapore Semiconductor Industry Association He serves on the Editorial Board of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES. He holds or has held key positions in many international conferences, such as advisor, general chair, co-general chair, and technical chair. He was the recipient of the Public Administration Medal (Bronze) on National Day 2009 by the President of the Republic of Singapore and the Distinguished Nanyang Alumni Award in 2009 for his outstanding contributions to the university and society.