

Research Article

Design and Characterization of the Next Generation Nanowire Amplifiers

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Received 23 April 2008; Revised 20 October 2008; Accepted 30 November 2008

Recommended by Soo-Ik Chae

Vertical nanowire surrounding gate field effect transistors (SGFETs) provide full gate control over the channel to eliminate short-channel effects. This paper presents design and characterization of a differential pair amplifier using NMOS and PMOS SGFETs with a 10 nm channel length and a 2 nm channel radius. The amplifier dissipates $5 \mu\text{W}$ power and provides 5 THz bandwidth with a voltage gain of 16, a linear output voltage swing of 0.5 V, and a distortion better than 3% from a 1.8 V power supply and a 20 aF capacitive load. The 2nd- and 3rd-order harmonic distortions of the amplifier are -40 dBm and -52 dBm , respectively, and the 3rd-order intermodulation is -24 dBm for a two-tone input signal with 10 mV amplitude and 10 GHz frequency spacing. All these parameters indicate that vertical nanowire surrounding gate transistors are promising candidates for the next generation high-speed analog and VLSI technologies.

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1. INTRODUCTION

The speed of silicon integrated circuits is reaching beyond 100 GHz to enable wireless communications with wideband channels [1]. Even though the current VLSI technology has approached to its scaling limits necessitating a replacement technology, silicon-based devices are still favored to realize large-scale circuits and systems because of their low cost.

Downscaling of the bulk metal oxide semiconductor field effect transistors (MOSFETs) to nanometer dimensions has increased the leakage current and short-channel effects. Therefore, alternative silicon compatible transistor devices such as silicon on insulator (SOI) MOSFETs, FinFETs, and nanotube FETs have been investigated for improved performance [2].

Vertical surrounding gate field effect transistors (SGFETs) have full gate control around channel and have minimized short-channel effects [3]. The elimination of bulk in these transistors reduces latchup and substrate noise. The layout views of a vertical nanowire SGFET and a planar bulk MOSFET are shown in Figure 1 for comparison. Both transistors have identical channel widths of 13 nm and channel lengths of 10 nm and are designed with similar layout design rules. The area of the vertical transistor is

$(40 \text{ nm} \times 40 \text{ nm}) 1600 \text{ nm}^2$, and the area of the planar transistor is also 1600 nm^2 ($76 \text{ nm} \times 21 \text{ nm}$) with body contact.

2. HIGH-FREQUENCY MODELING

The three-dimensional view and the corresponding parasitic components of the vertical nanowire SGFET are shown in Figure 2. Only, the dominant parasitics are considered to simplify the circuit model.

The intrinsic transistor M is modeled using a BSIM-SOI compatible model to ensure that all the input and output transfer characteristics of the circuit and device simulators match each other. The parasitic capacitance between the source contacts and the metal gate is denoted as C_{gs2} in the figure. The parasitic capacitance, C_{gs1} , between the metal gate and the concentric source makes contact, and the junction well is the largest dominant capacitor of the SGFET device. The gate and drain capacitors (C_{gd1} and C_{gd2}) and the drain and source capacitors (C_{ds1} and C_{ds2}) can be lumped into C_{gd} and C_{ds} , respectively. Compared to planar bulk transistors, C_{gd} is very small and there is no junction to bulk capacitance, therefore, C_{ds} is quite linear. The well resistance, R_s , can be quite large and is the major drawback of the vertical SGFETs compared with planar transistors. The magnitude of this

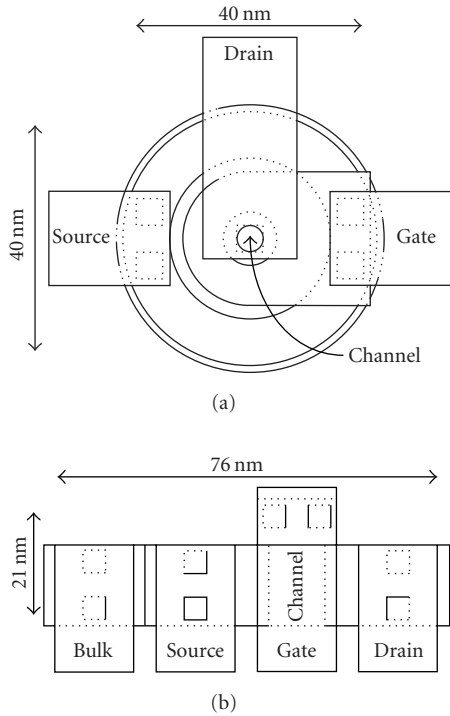


FIGURE 1: Layout views of (a) vertical nanowire SGFET and (b) planar bulk MOSFET.

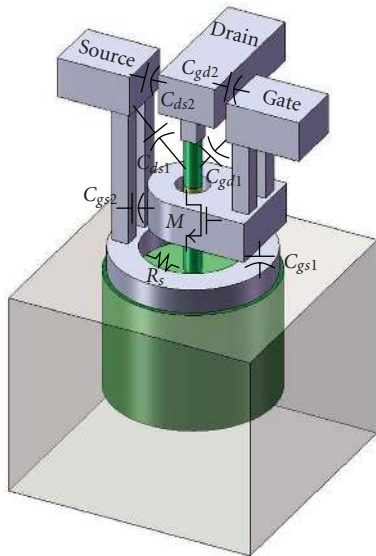


FIGURE 2: The 3D view of nanowire transistor.

resistance can be reduced drastically by placing a concentric (ring shape) source contact in parallel with the well, as shown in the figure.

The simplified parasitic components associated with NMOS and PMOS SGFETs are shown in Figures 3(a) and 3(b). For accurate circuit level simulations, the intrinsic SGFETs (M_n and M_p) are modeled using BSIM-SOI.

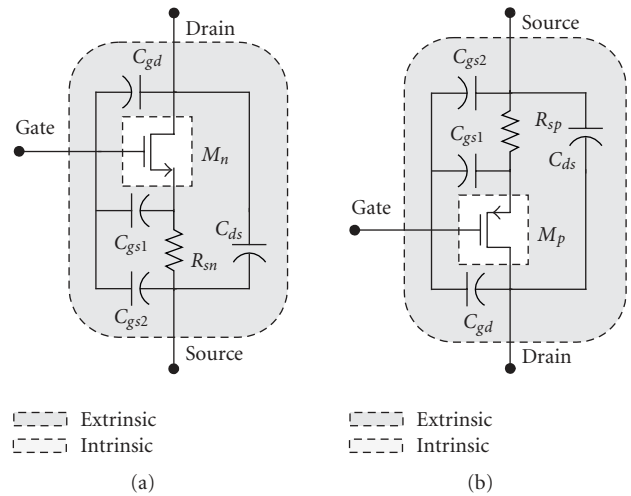


FIGURE 3: Simplified parasitic components of (a) NMOS and (b) PMOS SGFETs.

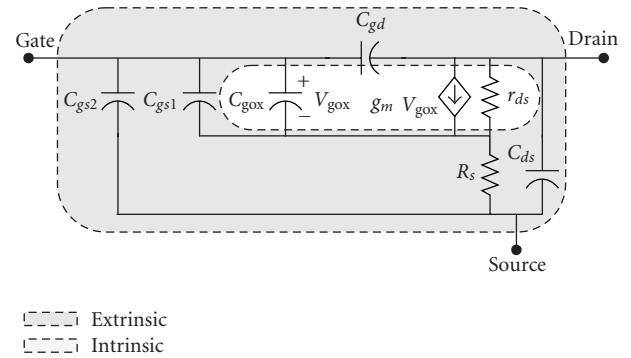


FIGURE 4: Linearized small-signal model of SGFET.

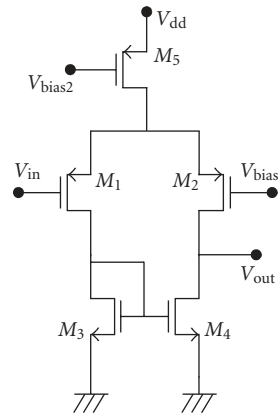


FIGURE 5: Schematic of a differential pair amplifier.

For simplified hand calculations and finding the AC parameters of the amplifiers, designed using SGFETs, the linearized small-signal model shown in Figure 4 can be used. Using this model at low frequencies, the DC voltage gain and output resistance of various amplifier stages can be calculated. The model shown in Figure 4 is valid for transistors biased in the active operating region, and transistor models

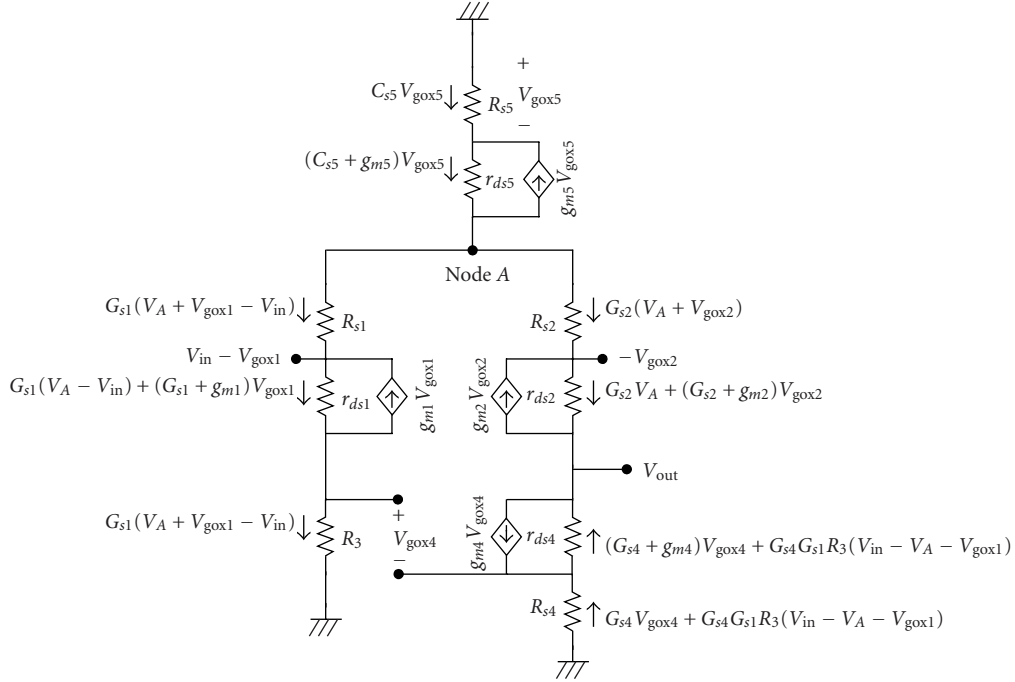


FIGURE 6: The low-frequency small signal model of the differential pair amplifier.

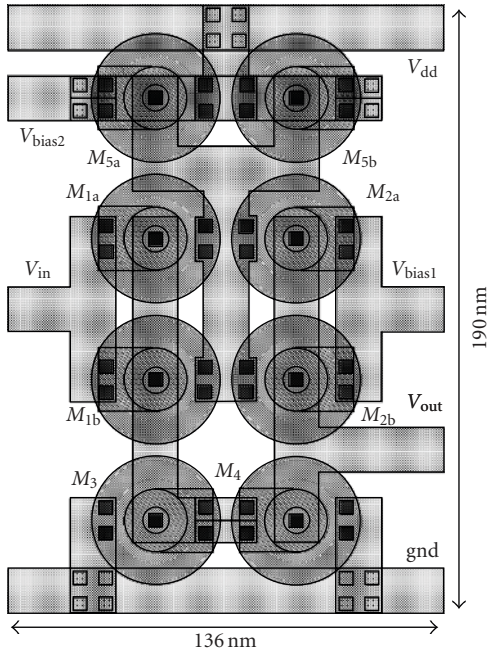


FIGURE 7: Layout of the differential pair amplifier.

in triode or cutoff regions can be easily constructed from this model by minor modifications.

3. DIFFERENTIAL-PAIR AMPLIFIER

The full gate control and the low leakage current of SGFETs make them suitable for many digital applications [4].

Operational amplifiers are one of the most important building blocks of analog integrated circuits, and differential-pair amplifiers are the input building blocks of any opamp, as shown in Figure 5. Therefore, the performance of a differential-pair amplifier, designed using SGFETs, needs to be measured before designing an opamp and will be investigated in this work. We design the input transistors of the differential pair amplifier using PMOS transistors to enable realizing the Miller stage using NMOS transistors and achieving higher gains.

The low-frequency small signal model of the differential pair amplifier designed using SGFETs is shown in Figure 6.

The layout of the differential pair amplifier realized using 3 metallization layers is presented in Figure 7. All interconnect parasitics are extracted and added to the amplifier netlist for postlayout simulations.

The resistor R_3 is given by

$$R_3 = R_{s3} + \left(r_{ds3} \parallel \frac{1}{g_{m3}} \right). \quad (1)$$

The voltage gain of the differential pair amplifier is given by

$$\frac{V_{out}}{V_{in}} = \frac{g_{m2}r_{ds2} + r_{ds2}(g_{m2} + G_{s2})/r_{ds5}G_{s2}}{1 - U_1/U_2}. \quad (2)$$

where U_1 denotes $g_{m2}r_{ds2}[r_{ds1}(g_{m1} + G_{s1}) + G_{s1}(R_{s3} + r_{ds3})/(1 + g_{m3}r_{ds3})]$ and U_2 denotes $g_{m1}r_{ds1}G_{s1}G_{s4}r_{ds4}(R_{s3} + r_{ds3})/(1 + g_{m3}r_{ds3})$.

For $G_s \gg g_m \gg g_{ds}$, the voltage gain is approximately given by

$$\frac{V_{out}}{V_{in}} \approx g_{m2}r_{ds2}. \quad (3)$$

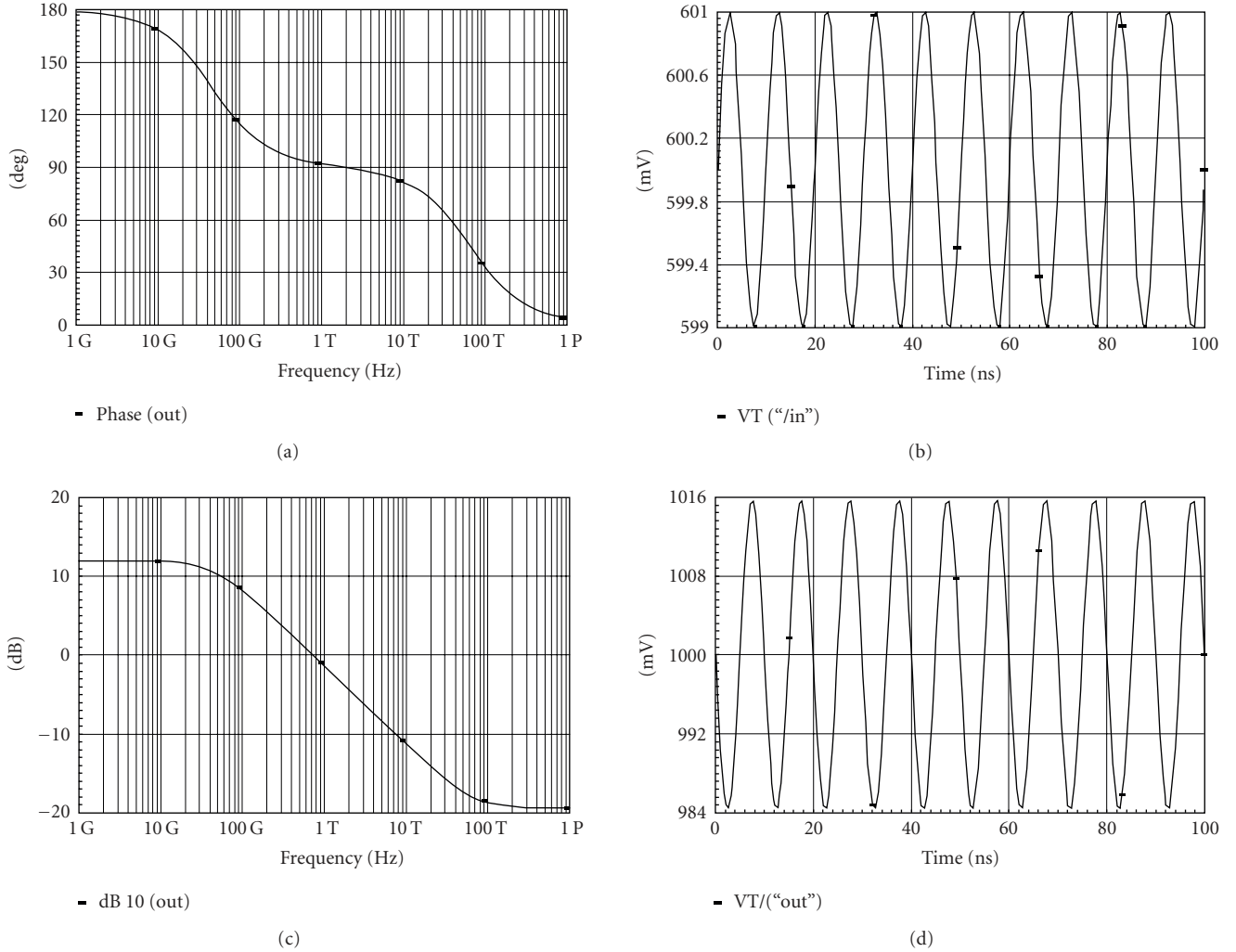


FIGURE 8: Frequency and transient responses of the differential pair amplifier.

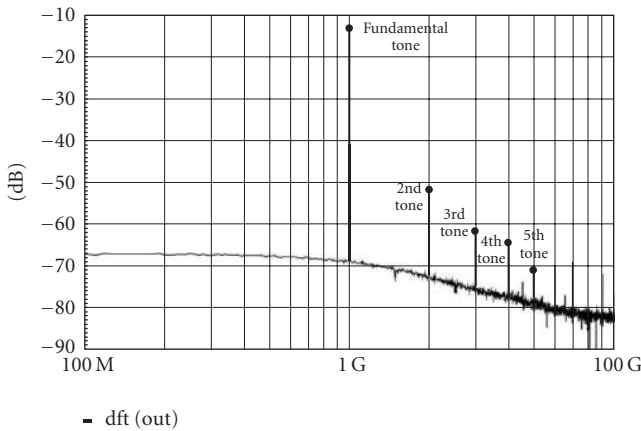


FIGURE 9: Spectrum of the output transient waveform.

For $G_s \gg g_m \gg g_{ds}$, the output resistance is approximately given by

$$R_{out} \approx \left[r_{ds2} \left(1 + \frac{g_{m2}}{g_{m1}} \right) \right] \parallel r_{ds4}. \quad (4)$$

The main transistors of the input differential pair amplifier are realized by parallel combination of two p-type SGFETs to ensure a large transconductance. The width of the metal interconnects is selected to be 14 nm to reduce their resistivity, and four parallel vias are used to connect metal-2 and metal-3 layers to minimize the signal loss. Each via with $4 \text{ nm} \times 4 \text{ nm}$ dimension and 36 nm height has a resistance of 400Ω . Overlap capacitance between metal-1 and metal-2 routing interconnects is 0.2 aF for $14 \text{ nm} \times 14 \text{ nm}$ dimension and 36 nm height. The layout area of the differential pair amplifier is $x = 136 \text{ nm}$ and $y = 190 \text{ nm}$.

4. POSTLAYOUT CHARACTERISTICS

The transient and frequency responses of the SGFET differential pair amplifier are shown in Figure 8. The amplifier provides a gain of 16 with the first pole located at 100 GHz and the second pole located at 100 THz. To attain high accuracy in the transfer functions of various analog circuits such as switch capacitor filters and amplifiers, it might be necessary to cascade multiple stages in nested Miller architectures and achieve a voltage gain higher than 1000.

TABLE 1: Postlayout characteristics of the differential pair amplifier.

Supply voltage	1.8 V
Maximum output linear signal swing	0.5 V
Input DC voltage level	0.6 V
Voltage gain (at 1 GHz)	16
Phase margin	>90°
Unity voltage gain cutoff frequency	5.1 THz
Third-order intermodulation distortion (10 mV two-tone signals with 1 GHz spacing)	-24 dBm
Second-order harmonic distortion	-40 dBm
Third-order harmonic distortion	-52 dBm
Total harmonic distortion	3%
Load capacitor	20 aF
Power dissipation	5 μ W
Area	136 nm \times 190 nm

The spectrum of the output waveform of the amplifier is given in Figure 9. It has very good linearity characteristics, and the total harmonic distortions of the amplifier are only 3% for ± 233 mV output swing. Such a high linearity is due to the source resistance, R_s , acting as the degeneration resistance and minimizing the harmonic distortions of input differential pair transistors.

The postlayout characteristics of the opamp are listed in Table 1. The good performance of the SGFET amplifier indicates that these transistors are good choices for future integration of high-speed and low-power analog and mixed signal circuits.

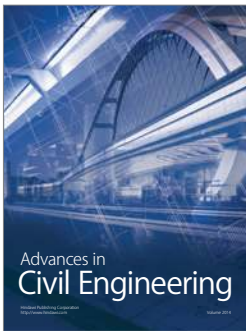
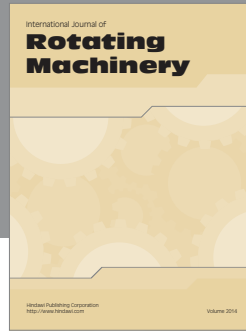
5. CONCLUSIONS

The design and characteristics of a differential pair amplifier designed using nanowire SGFETs and having channel length of 10 nm and channel radius of 2 nm were presented. The amplifier dissipates 5 μ W power and provides 5 THz bandwidth with a voltage gain of 16 and a distortion better than 3%. All these parameters indicate that vertical nanowire SGFETs are promising candidates for realizing next generation high-speed analog integrated circuits.

REFERENCES

- [1] B. Heydari, M. Bohsali, E. Adabi, and A. M. Niknejad, "Millimeter-wave devices and circuit blocks up to 104 GHz in 90 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 12, pp. 2893–2903, 2007.
- [2] A. Bindal, A. Naresh, P. Yuan, K. K. Nguyen, and S. Hamed-Hagh, "The design of dual work function CMOS transistors and circuits using silicon nanowire technology," *IEEE Transactions on Nanotechnology*, vol. 6, no. 3, pp. 291–302, 2007.
- [3] K. H. Cho, K. H. Yeo, Y. Y. Yeoh, et al., "Experimental evidence of ballistic transport in cylindrical gate-all-around twin silicon nanowire metal-oxide-semiconductor field-effect transistors," *Applied Physics Letters*, vol. 92, no. 5, Article ID 052102, 3 pages, 2008.

- [4] A. Bindal and S. Hamed-Hagh, "An exploratory design study of a 16×16 static random access memory using silicon nanowire transistors," *Journal of Nanoelectronics and Optoelectronics*, vol. 2, no. 3, pp. 294–303, 2007.



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