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Design and control of single-phase dynamic voltage restorer

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Abstract. Dynamic voltage restorer (DVR) is a custom power device used in electrical distribution system for power quality improvement. It ensures regulated voltage supply to the sensitive loads, even in case of voltage sag and swell disturbances in the distribution network. It is a series connected device and compensates voltage sag and swell by injecting a voltage with the help of a series transformer. The injection of an appropriate voltage component in the event of a voltage disturbance requires a certain amount of real and reactive power. Conventionally, DVR consists of an energy storage device, which supplies the required power over the limited duration of the sags. Large magnitude and long duration of sags lead to heavy financial investment in energy storage unit. To overcome this limitation, a single-phase back-to-back converter-based DVR is implemented in this work, which eliminates energy storage requirement. The integration of series and shunt converter makes the DVR capable of bidirectional flow of energy. Therefore, the key advantage of this topology is its capability to compensate for long-term voltage sag and swell. Modelling of the DVR and its controller design is included in this paper. The effectiveness of control schemes, protection schemes and starting sequence of operation of DVR is verified through detailed simulation studies. A scaled down laboratory prototype of DVR is developed. The viability of these schemes is confirmed by the experimental results generated from the laboratory prototype. Various challenges faced during the prototype development and corresponding solutions are also discussed in this paper.

Keywords. Custom power device; dynamic voltage restorer; in-phase compensation; voltage sag; voltage swell.

1. Introduction

Voltage sag and swells are considered to be one of the most severe disturbances to the sensitive loads [1]. Dynamic voltage restorer (DVR) has become popular as a cost-effective solution for the protection of sensitive loads from voltage sag and voltage swell. DVR injects voltage in series and synchronism with the grid supply voltage in order to compensate for voltage sag and swell [2]. DVR is connected in series with the line through an injection transformer. Figure 1 shows the single-line diagram of distribution system with DVR, which is connected in series with the feeder. When a short-circuit fault occurs at load 1, voltage at the distribution bus decreases. This leads to a sag in the voltage supplied to the sensitive load 2. To restore the voltage across this load, DVR is used [3].

During the period of voltage sag or swell, DVR injects the voltage so as to restore the load voltage to its normal value. During this operation, the DVR exchanges the active and reactive power with the load. In case of voltage sag, active power has to be supplied by DVR. This motivates the use of energy storage element in the DVR. Various energy storage devices such as batteries, capacitors, flywheels, etc. are used in DVR [4]. However, this increases the cost of DVR. Further, due to the presence of battery, regular maintenance is required.

A suitable controller is required in DVR to determine the phase and magnitude of the injected voltage and to restore the phase and magnitude of voltage across the sensitive load. Three popular techniques are (i) pre-sag voltage compensation, (ii) zero active power injection and (iii) in-phase voltage injection. In the pre-sag compensation technique, injection of both real and reactive powers is required. The difference between sag and pre-sag voltage is detected by DVR and appropriate voltage is injected to restore the magnitude and phase of load voltage to their pre-sag values [5, 6]. This technique is mainly used for loads that are sensitive to both voltage magnitude and phase

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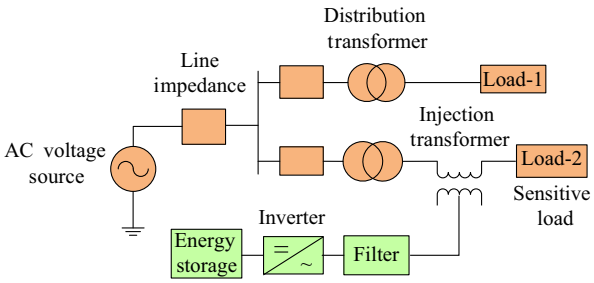

Figure 1. Single-line diagram of DVR connected in series with the feeder.

angle. This technique requires significant magnitude of injected voltage in case of large phase shift. Further, DVR should be capable of supplying/absorbing real power to/from the injection transformer. The second technique is zero active power injection [7]. Active power supplied by the DVR depends on the angle between the load current I_{Load} and the injected voltage V_{inj}. In this technique, these two vectors are maintained in quadrature, thereby ensuring zero active power injection by DVR. Only reactive power has to be supplied/absorbed by the DVR. This leads to elimination of energy storage device in the DVR, thereby reducing the cost. However, the sag compensation capability is limited in case of unity power factor loads. The following equation defines the magnitude of maximum voltage sag that this technique can compensate:

$$\Delta V_{\text{sag}} \leq V_L(1 - \cos\,\phi) \tag{1}$$

where V_L is the nominal load voltage and $\cos\phi$ is the power factor. It is clear that for the loads with poor power factor (p.f.), it is easier to compensate voltage sag without real power injection. Therefore, the proposed technique has limitation in compensating the voltage sag with loads having unity p.f. [5, 7, 8]. The third technique, in-phase voltage injection, requires minimum voltage injection to compensate either voltage sag or swell [3]. Further, this technique requires real power injection/absorption. However, the real power magnitude is smaller than that in case of pre-sag compensation technique.

Various circuit configurations and topologies are suggested for DVR applications in literature. A detailed comparison of various DVR topologies with their control strategies is provided in [4]. Control techniques used to compensate voltage sag, swell and harmonics are suggested in [9]. These control techniques minimize the rating of DVR. However, these techniques use dc battery storage and capacitor at the input of DVR, which increases the cost and size of DVR for long duration voltage sag/swell. Voltage sag/swell compensation scheme using pre-sag compensation technique is suggested in [10]. This scheme enables DVR to compensate sag/swell for longer duration. The transition to minimum active power (MAP) mode is carried out after the phase jump is compensated. However, the suggested method is not able to compensate deep voltage sag /swell. DVR based on multilevel inverter with adjustable dc-link voltage is proposed in [11]. A battery is connected to the input of DVR to provide active and reactive power support. The output of DVR has various output voltage levels, which improves the quality of output voltage during deep voltage sags. However, deep and long duration sags lead to increased size of battery. DVR topologies without energy storage are proposed in [12, 13]. The schemes suggested in [12, 13] use a matrix converter to compensate voltage sags of long duration. The energy required by the DVR during the voltage sag is extracted from the mains power supply. However, this technique is usable only for three-phase systems due to the use of a three-phase matrix converter. Single-phase DVR topologies without injection transformer are discussed in [14, 15]. These circuits are capable of compensating for voltage sag without energy storage. However, the current flowing through these circuits is higher as compared with that in the injection-transformer-based DVR. This may lead to additional conduction losses in the circuit. The DVR discussed in [16] uses a Z-type inverter to compensate voltage sag. A single-phase rectifier is connected at input of inverter to charge the dc-link capacitor. Due to unidirectional power flow, this scheme is not applicable for compensation of voltage swell.

This paper deals with the design of storage-less single-phase DVR based on two back-to-back-connected H-bridge converters. The load side converter, called series converter, is a single-phase PWM inverter, injecting the voltage in series with grid voltage. The in-phase voltage injection technique is used to provide compensation against voltage sag or voltage swell across the sensitive load. The shunt converter regulates the dc-link voltage by absorbing/supplying suitable active power to/from the grid. A detailed design of laboratory prototype of DVR and its performance on linear and non-linear loads is discussed in this paper. This paper is organized as follows. Section 2 describes the operation of DVR, modelling of converters, design of controllers and protection schemes used for DVR. Section 3 includes the system specification. Simulation and experimental results of DVR for linear and non-linear loads are also discussed in this section. Section 4 includes a detailed discussion of various issues faced during the development of DVR prototype. Section 5 includes the conclusions of this paper.

2. Design of DVR

This section discusses the operation, design and protection scheme of DVR.

2.1 *Operation of single-phase DVR*

The DVR consists of shunt and series converters connected via a common dc-link capacitor as shown in figure 2. The series converter is used to inject the voltage in series with grid voltage. The voltage injection takes place with the help of an injection transformer connected between the source and load. During voltage sag, a shunt converter is used to control the dc-link voltage and works as a unity power factor rectifier. The series converter acts as an inverter and generates constant ac output voltage. The injected voltage is in phase with grid voltage. During the sag, the active power required by DVR is harnessed from the source and flow of energy takes place from the shunt converter to series converter. Similarly, during voltage swell, power flows from the series converter to shunt converter. The injected voltage is out of phase with swell voltage. During voltage sag and swell, both converters generate switching frequency voltages along with the fundamental component. To filter out these switching harmonics, LC filters are used at input and output of shunt and series converters, respectively. The purpose of capacitor C_s connected at the input of shunt converter is to absorb high-frequency switching harmonics components in the inductor (L_s) current. This ensures that the current drawn/supplied to the grid from the shunt converter has less amount of high-frequency components. Figures 3 and 4 show the phasor diagrams of the injected voltage in case of voltage sag and swell, respectively. Figure 3 shows that in case of voltage sag, the injected voltage is in phase with the sag voltage. From figure 4, it is clear that when voltage swell occurs, injected voltage is out of phase with the swell voltage.

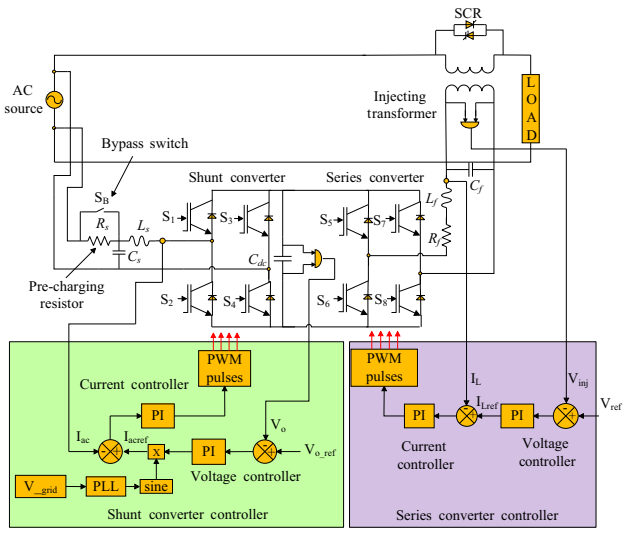

Figure 2. Single-phase DVR with series and shunt converters and their controllers.

2.2 *Phase-locked loop*

The phase-locked loop (PLL) discussed in [17] is used to detect phase angle and frequency of grid voltage. These parameters are required to ensure the performance of grid-connected systems according to the predefined standards during abnormal conditions like voltage sag, swell, notches, phase jumps, harmonics, etc. Figure 5 shows a block diagram of the PLL. The principle of PLL is based on generation of an orthogonal voltage system. These orthogonal voltage vectors are transformed to the *d-q* reference frame. The error between the actual and reference *q*-axis voltage is minimized by a proportional integral (PI) controller. The phase angle is generated by integrating the output of PI controller and constant angular frequency. For generation of orthogonal voltages v' and qv' from the grid voltages v, a second-order generalized integrator (SOGI) is used.

2.3 *Control scheme*

The controllers for shunt and series converters are shown in figure 2. A cascaded voltage- and current-controller-based control scheme is used in both converters. In case of shunt converter, the reference dc-link voltage is compared with the actual voltage to generate error. This error is processed by the PI controller to generate reference current magnitude, which is multiplied with a sinusoidal signal to generate reference ac current signal. The sinusoidal signal is of same phase and frequency as that of grid voltage and is generated by the PLL. An inner current controller is used to ensure that ac current is equal to this reference value.

For the series converter, the reference ac output voltage of the converter is determined by the grid voltage and its nominal value. This reference ac voltage waveform is processed by a suitable voltage and current controller to ensure that the injected voltage is equal to this reference value.

2.4 *Modeling of series and shunt converter*

In this section, mathematical modelling of the series and shunt converters is carried out. The equivalent circuit of series converter is shown in figure 6. By applying Kirchhoff's voltage law (KVL) in this circuit, the inverter voltage mv_o and injected voltage on the primary side of the transformer, v_{inj}, and capacitor current i_c of filter are related by following relations:

$$mv_o = i_L R_f + L_f \frac{di_L}{dt} + v_{\text{inj}} \tag{2}$$

$$v_{\text{inj}} = i_c R_c + \frac{1}{C_f} \int (i_c dt) \tag{3}$$

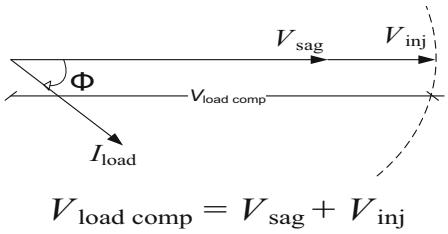

Figure 3. Voltage injected in series with grid voltage during voltage sag condition.

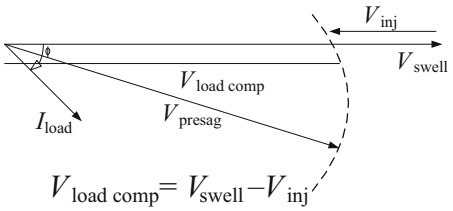

Figure 4. Voltage injected out of phase with grid voltage during voltage swell condition [17].

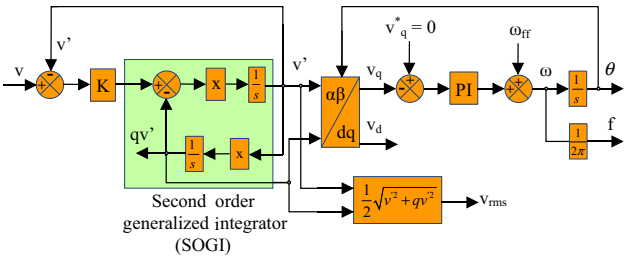

Figure 5. Block diagram of PLL used in DVR for phase angle detection.

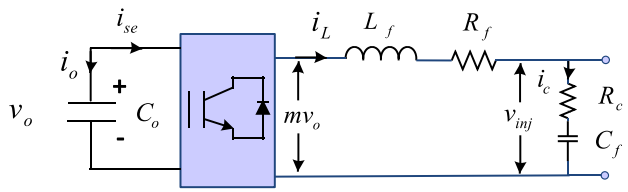

Figure 6. Equivalent circuit of series converter.

where m is the control input to the series converter, i_L is the inductor current of series converter, v_{inj} is the output voltage of the series converter and v_o is the dc-link voltage. L_f and C_f are, respectively, the filter inductance and capacitance. R_f and R_c are the equivalent series resistance (ESR) of inductor and capacitor, respectively. Taking Laplace of (2) and (3) gives

$$\hat{m}(s)V_o = \hat{i}_L(s)(R_f + sL_f) + \hat{v}_{\text{inj}}(s) \tag{4}$$

$$\hat{v}_{\text{inj}}(s) = \hat{i}_c(s)\left(R_c + \frac{1}{sC_f}\right) \tag{5}$$

where V_o is the average value of dc-link voltage. Similarly, the equivalent circuit of shunt converter is shown in figure 7. By applying KVL in this circuit, the voltage v_{in}, shunt converter output voltage v_o, input current i_{ac} and dc-link capacitor current i_o are related by following relations:

$$v_{ac} = i_{ac}R_s + L_s\frac{di_{\text{ac}}}{dt} + v_{\text{in}} \tag{6}$$

$$v_o = \frac{1}{C_o}\int (i_o dt) \tag{7}$$

where L_s and R_s are inductance and its ESR, respectively. C_o is the dc-link capacitance. Taking Laplace of (6) and (7) gives

$$\hat{v}_{\text{ac}}(s) = \hat{i}_{\text{ac}}(s)(R_s + sL_s) + \hat{v}_{\text{in}}(s) \tag{8}$$

$$\hat{v}_o(s) = \frac{1}{sC_o}\hat{i}_o(s). \tag{9}$$

2.5 *Controller design for series converter*

Figure 8 shows a block diagram of inner current and outer voltage control loop of the series converter [18]. The transfer function of PI controller is given by

$$H_i(s) = K_p + \frac{K_i}{s}. \tag{10}$$

Using (4) and (5), the plant transfer function of current control loop in series converter is given as

$$G_{\text{ise}}(s) = \frac{\hat{i}_L(s)}{\hat{m}(s)} = \frac{sC_f V_{\text{dc}}}{s^2L_fC_f + s(R_f + R_c)C_f + 1}. \tag{11}$$

Since the value of R_c is very small as compared with R_f, R_c can be neglected in (11). A time delay exists in the current control loop because of the sample and hold circuit of analog to digital converter (ADC) and updating rate of modulation signal in the digital signal processor (DSP) [19]. The cumulative time delay T_d in the current control loop is approximated by the following expression:

$$G_d(s) \approx \frac{1}{1 + sT_d}. \tag{12}$$

Taking into account the effect of time delay, the Bode plot of closed loop transfer function of current control loop is shown in figure 9. Using (5), the plant transfer function of voltage control loop in series converter is as follows:

$$G_{\text{vse}}(s) = \frac{\hat{v}_{\text{inj}}(s)}{\hat{i}_c(s)} = \frac{1}{sC_f + R_c}. \tag{13}$$

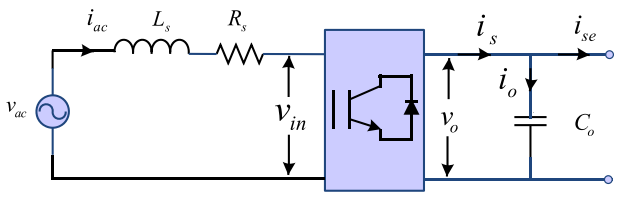

Figure 7. Equivalent circuit of shunt converter.

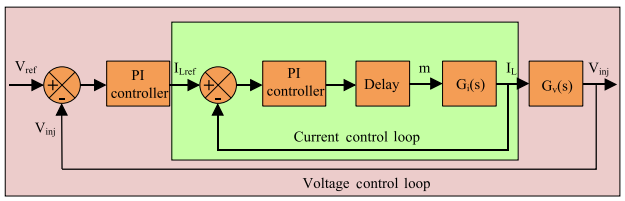

Figure 8. Block diagram of series converter control scheme.

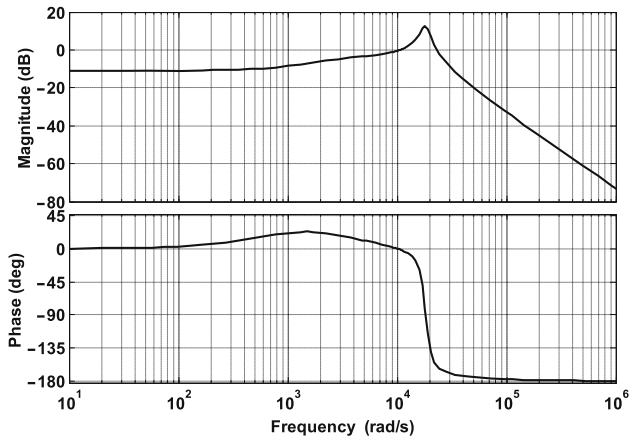

Figure 9. Bode plot of closed loop transfer function $\hat{i}_L/\hat{i}_{Lref}$ for series converter.

Taking into account the effect of time delay, the PI controller and dynamics of inner current controller, the Bode plot of voltage closed loop transfer function is shown in figure 10.

2.6 *Controller design for shunt converter*

The shunt converter maintains the dc-link voltage constant during voltage sag and swell compensation. The dc-link voltage is sensed with the help of a voltage sensor. Output of voltage controller is compared with shunt converter inductor current to generate reference signal. This reference signal maintains a constant dc-link voltage. Figure 11 shows a block diagram of inner current and outer voltage control loop [20]. Using (8), the plant transfer function of current to inverter voltage in shunt converter is given by

$$G_{\text{ish}}(s) = \frac{\hat{i}_{\text{ac}}(s)}{\hat{v}_{\text{in}}(s)} = -\frac{1}{sL_s + R_s}. \tag{14}$$

Considering the time delay in current control loop of shunt converter, the Bode plot of closed loop transfer function, $\hat{i}_{\text{ac}}/\hat{i}_{\text{acref}}$ is shown in figure 12. Using (9), the plant transfer function of outer control loop in shunt converter is given by

$$G_{\text{vsh}}(s) = \frac{\hat{v}_o(s)}{\hat{i}_o(s)} = \frac{1}{sC_s}. \tag{15}$$

Considering the effect of time delay, PI controller and dynamics of inner current controller, the Bode plot of closed loop transfer function of voltage control loop is shown in figure 13. The linearized relation between $\hat{v}_{in}$ and $\hat{v}_o$ is given as follows:

$$\hat{v}_{\text{in}}(s) = n\hat{v}_o(s) \tag{16}$$

where n is the modulation index of shunt converter. Using (14)–(16), the relation between $\hat{i}_o$ and $\hat{i}_{ac}$ is given by

$$\frac{\hat{i}_o(s)}{\hat{i}_{\text{ac}}(s)} = -\frac{sC_o}{n(R_s + sL_s)}. \tag{17}$$

The relation among $\hat{i}_s(s), \hat{i}_o(s)$ and $\hat{i}_{\text{se}}(s)$ is given by

$$\hat{i}_s(s) = \hat{i}_o(s) + \hat{i}_{\text{se}}(s). \tag{18}$$

Taking $\hat{i}_{\text{se}}(s)$ as disturbance input, the relation between $\hat{i}_s(s)$ and $\hat{i}_{\text{ac}}(s)$ is

$$\frac{\hat{i}_s(s)}{\hat{i}_{\text{ac}}(s)} = -\frac{sC_o}{n(R_s + sL_s)}. \tag{19}$$

2.7 *Protection schemes*

Different protection schemes are incorporated in DVR for its safety and to ensure reliable supply to the loads.

In case of overload, the load current exceeds its rated value. A bypass scheme is incorporated in DVR. During bypass operation, the secondary of the injection transformer is shorted through an anti-parallel silicon-controlled rectifier (SCR) pair, as shown in figure 2. During this mode, the transformer works in zero voltage injection mode. Control logic is implemented, which turns on the SCRs in case load current exceeds its safe limit. The overload limit is set to 125% of the rated load current. DVR is capable of handling this overload current for 600 s, therefore, bypass SCRs are turned on after 600 s of 125% overloading. The current–time characteristic used for overload protection is shown in figure 14. From the characteristic, it is clear that the time

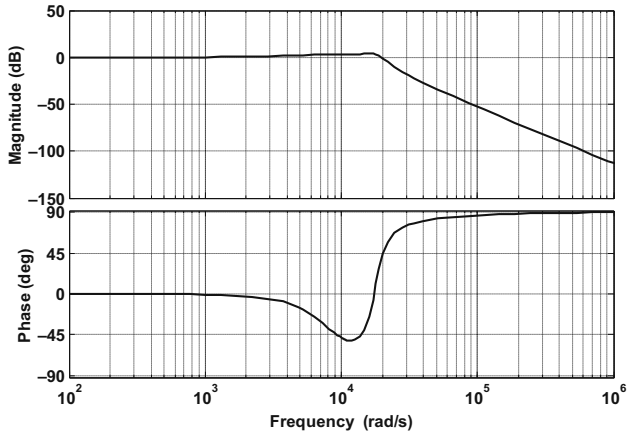

Figure 10. Bode plot of closed loop transfer function $\hat{v}_{inj}/\hat{v}_{ref}$ for series converter.

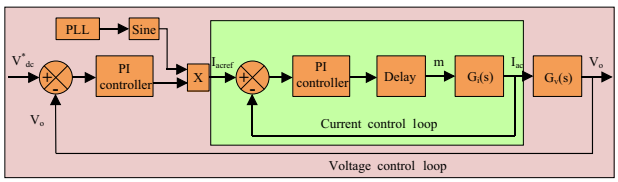

Figure 11. Block diagram of shunt converter control scheme.

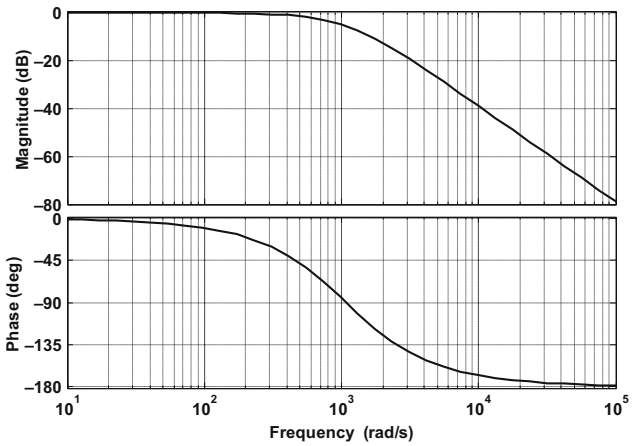

Figure 12. Bode plot of plant transfer function $\hat{i}_{ac}/\hat{i}_{acref}$ for shunt converter.

duration after which bypass operation should take place decreases with increase in value of load current above its rated value.

During starting of the DVR, the dc-link capacitor is completely discharged. Due to the high value of capacitor, a large magnitude of current can flow through the shunt converter at starting of DVR. To limit this initial current, a resistor is connected in series with shunt converter at starting of DVR, called as a pre-charging resistor R_s, as shown in figure 2. As dc-link voltage becomes equal to the peak of ac voltage, R_s is bypassed with the help of a relay connected in parallel with R_s.

The DVR compensates the voltage in the range 185–265 V (rms). If the voltage to be compensated exceeds this limit, the DVR is turned off. To turn off the DVR, the pulses supplied by the DSP to the converters are stopped and load is supplied by the bypass SCRs.

2.8 *Starting sequence of DVR*

The following steps are adopted during starting of the DVR. At starting, the IGBTs of both the converters are kept off and bypass SCRs are kept on. Charging of dc-link capacitor takes place through the pre-charging resistance. As capacitor voltage becomes equal to the peak value of ac voltage, the pre-charging resistor is bypassed through a relay. At the same instant, soft start operation to build dc-link voltage up to 400 V is initiated. Voltage and current controllers determine the switching sequence of the shunt converter. As soon as the dc-link capacitor reaches 400 V, the switching pulses to the series converter are released. The SCRs connected across the series transformer are turned-off.

3. Development of DVR prototype

In this section, the development of a DVR prototype is discussed.

3.1 *System parameters*

This DVR is designed to compensate both voltage sag and swell in the range of 185 V (rms) to 265 V (rms), and maintains the load voltage to 230 V. The DVR is designed to cater 5 kVA load. The power rating of the injection transformer is decided by the voltage to be injected and the load current flowing through the secondary of injection transformer. The current flowing through secondary of injection transformer is the same as that of the load, since they are connected in series. However, the voltage injected on the secondary of the transformer is limited [45 V(rms)]; therefore, the power rating of injection transformer is much less than that of the load. The power rating of injection transformer used for voltage compensation in the specified range is 1.5 kVA for rated load of 5 kVA. The specifications of DVR are shown in table 1.

3.2 *Simulation results*

To implement the control strategies and protection schemes discussed in previous sections, a detailed

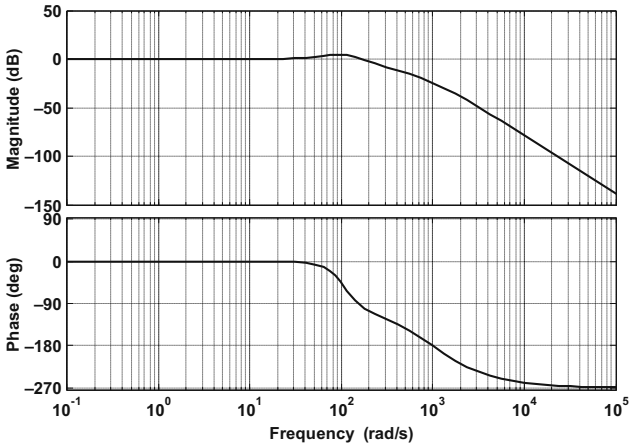

Figure 13. Bode plot of plant transfer function $\hat{v}_o/\hat{v}_{\text{oref}}$ for shunt converter.

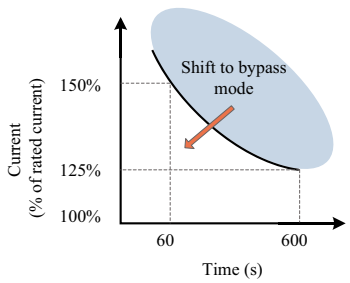

Figure 14. Current–time characteristic of overload protection.

Table 1. Specifications of DVR.

Power rating	5 kVA
Nominal output voltage	230 V
Frequency	50 Hz
Voltage compensation range	185–265 V

simulation study of DVR is accomplished in MATLAB/Simulink. Parameters of the system and controller are given in tables 2 and 3, respectively. The performance of the DVR during voltage sag and swell condition is determined for both, linear and nonlinear loads. Figure 15 shows the performance of the DVR with resistive load during voltage sag. Up to 0.4 s, the value of grid voltage is 230 V (rms). A sag in source voltage occurs at $t = 0.4$ s. The value of sag voltage is 185 V (rms) and the duration of the voltage sag is from 0.4 to 0.6 s. However, the load voltage remains constant at 230 V (rms). During voltage sag, real power flows from the shunt converter to series converter. Similarly, figure 16 shows the performance of DVR with swell in grid voltage for resistive load. The swell in voltage occurs from 0.4 to 0.6 s. Even during this period, the load voltage is regulated to 230 V (rms). During swell, power is transferred from the series converter to shunt converter.

Figure 17 shows the performance of the DVR with electronic load (non-linear load) for voltage sag. The duration of voltage sag is the same as that for linear load. The electronic load is a single-phase full-wave diode bridge rectifier. The diode bridge rectifier is designed for load current of crest factor 3.08. The load voltage is compensated and maintained at the rms value of 230.5 V shown by red trace.

Figure 18 shows the transient response of the DVR for sudden change in load. To test the transient performance of DVR, a sag in grid voltage of the same magnitude and duration as those for linear load is provided. Load is changed from no-load to full-load and vice versa at 0.45 and 0.55 s, respectively. During transients, load voltage remains constant, equal to 230 V (rms). However, due to load shedding, the dc-link voltage rises momentarily. After a duration of 70 ms, dc-link voltage is restored to its normal value of 400 V. Therefore from these waveforms, it is clear the bidirectional AC/DC/AC converter is able to compensate both voltage sag and voltage swell for linear and nonlinear loads.

3.3 *Experimental results*

To validate the simulation results, a 5 kVA prototype of DVR is developed, and shown in figure 19. The system parameters are shown in table 4. This section discusses the experimental results and performance analysis of DVR. The experimental results are presented for shunt converter, series converter and with back-to-back-connected converter. The set-up is also tested for bypass operation implemented with anti-parallel SCRs. The 5 kVA DVR prototype is realized by using three voltage sensors, three current sensors, two IGBT modules (each module having six IGBTs) and one anti-parallel SCR pair for bypass

Table 2. Parameters of LC filter for both side converters.

Parameter	Inductor	Capacitor
Shunt converter	1.693 mH	10 µF
Series converter	0.9 mH	10 µF

Table 3. Controller parameters.

	Voltage loop		Current loop	
Parameter	K_P	K_I	K_P	K_I
Shunt controller	1	100	0.5	0.1
Series controller	0.1	1000	0.1	100

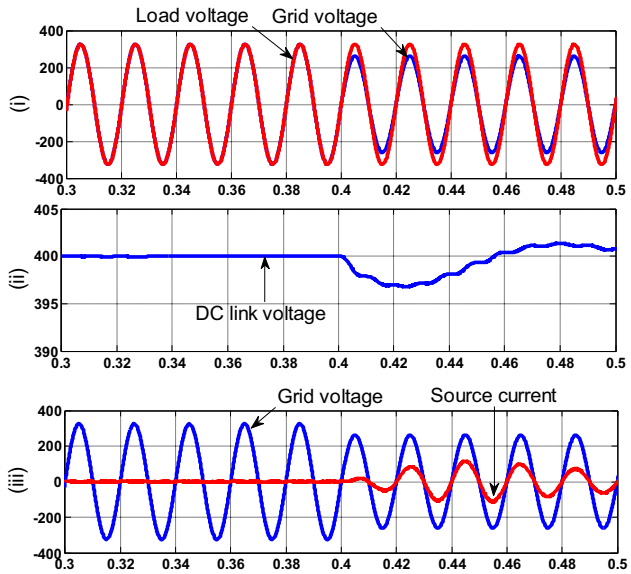

Figure 15. Voltage sag with resistive load. Trace (i) (red) load voltage (200 V/div), (blue) grid voltage (200 V/div), trace (ii): dc-link voltage (10 V/div), trace (iii): (blue) grid voltage of source side converter (100 V/div), (red) source current (10 A/div). *X*-axis 20 ms/div.

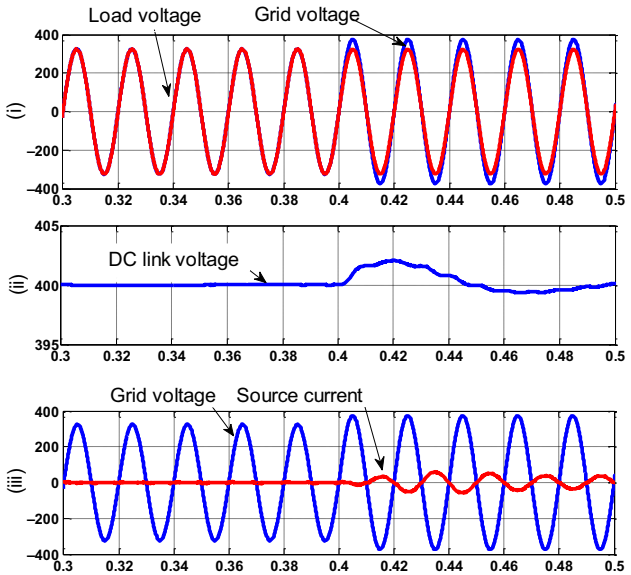

Figure 16. Voltage swell with resistive load. Trace (i): (red) load voltage (200 V/div), (blue) grid voltage (200 V/div), Trace (ii): dc-link voltage (2 V/div); Trace (iii): (blue) grid voltage of source side converter (100 V/div), (red) source current (10 A/div). *X*-axis: 20 ms/div.

operation and relay with the pre-charging resistor. The voltage sensors are used for sensing grid voltage, voltage of dc-link capacitor and output voltage of series converter. The current sensors are used for sensing inductor current of shunt converter, inductor current of series converter and load current. The DSP is used to implement all control algorithms and for generating the switching pulses for both converters. DSP is used because of its advantages in cost, speed and flexibility in programming over analog controllers and other digital platforms. To control the converters, a 32-bit TMS320F2808 Texas Instruments DSP is used. Switching frequency used for both converters is 7.5 kHz. Figure 20 shows a schematic of the various interconnections among the hardware modules within DVR.

Firstly, the shunt converter is separately tested for resistive load of 1 kW. Figure 21 shows waveforms of grid voltage, grid current and voltage between IGBT legs of shunt converter. For a grid voltage of 215 V (rms), the output dc voltage of active rectifier is 400 V. The value of dc-link capacitor is 2 mF. The series converter is a single-phase voltage source inverter and also tested separately for no load. Figure 22 shows the waveforms of inverter output voltage, inductor current and inverter output available after LC filtering. For the dc-link voltage of 250 V, the fundamental component of output voltage of inverter is 177 V(rms). After filtering, the output is almost sinusoidal in nature.

The DVR including both converters connected together is tested for a resistive load of 1 kW rating. The DVR is tested for voltage sag of 187 V (rms) with the same loading as in the previous case. Figure 23 shows waveforms of the grid voltage, load voltage, source current and inductor current of series converter. For the grid voltage of 187 V(rms), the load voltage is regulated at 227 V(rms). The FFT spectrum of source current is shown in figure 24. The source current THD is found to be 3.7%.

Similarly, the DVR is tested for voltage swell of 265 V(rms) with resistive load of 1 kW. Figure 25 shows the waveforms of the grid voltage, source current, load voltage and inductor current of series converter. For the grid voltage of 265 V(rms), the load voltage is regulated at 234 V(rms).

Table 5 shows THD of grid voltage, grid current, load voltage and load current for normal value of grid voltage, sag and swell conditions. Power factor of the grid supply and efficiency of DVR are evaluated for these cases and shown in table 5. The power factor of grid supply is almost unity in all the three cases.

4. Technical challenges in developing a laboratory prototype

Following are some of the important issues faced in preparing prototype.

4.1 *False activation of over-current protection*

A three-phase FSBB20CH60C IGBT module is used for shunt and series converter. The module is equipped with built-in gate drivers with various protection features,

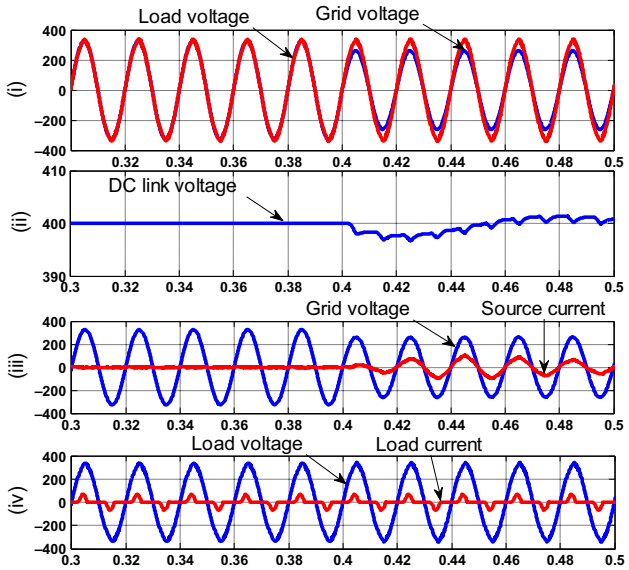

Figure 17. Voltage sag with electronic load. Trace (i) (red) load voltage (200 V/div), (blue) grid voltage (200 V/div), trace (ii): dc-link voltage (10 V/div), trace (iii): (blue) grid voltage of source side converter (200 V/div), (red) source current (10 A/div), trace (iv): (blue) load voltage (200 V/div), (red) load current (10 A/div). *X*-axis: 20 ms/div.

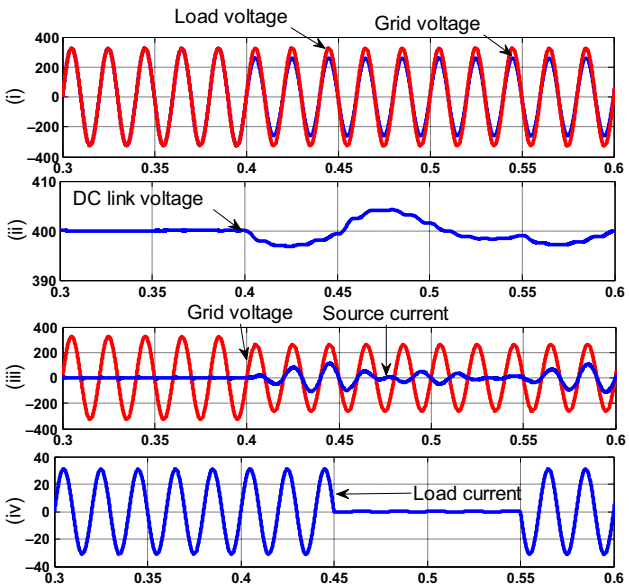

Figure 18. Load transient during voltage sag for resistive loading. Trace (i): (red) load voltage (200 V/div), (blue) grid voltage (200 V/div), trace (ii): dc-link voltage (20 V/div), trace (iii): (red) grid voltage of source side converter (200 V/div), (blue) source current (10 A/div), trace (iv): (blue) load current (20 A/div). *X*-axis: 50 ms/div.

including under-voltage lockouts, over-current shutdown and fault reporting. The built-in driver circuit translates the incoming logic-level gate inputs to the high-voltage,

Figure 19. Laboratory prototype of DVR.

Table 4. Parameters of the LC filter for both-side converters.

Parameter	Inductor	Capacitor	Resistance
Shunt converter	2.5 mH	10 μF	0.19 mΩ
Series converter	2.3 mH	10 μF	0.112 mΩ

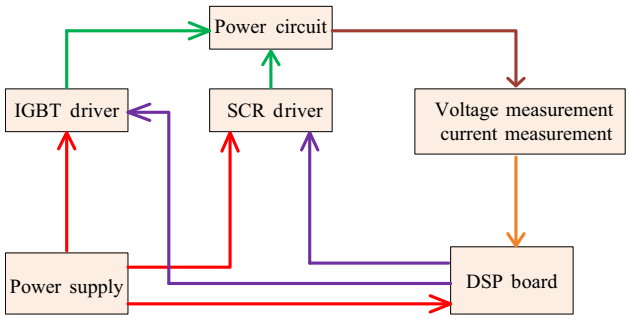

Figure 20. Block diagram of hardware scheme of DVR.

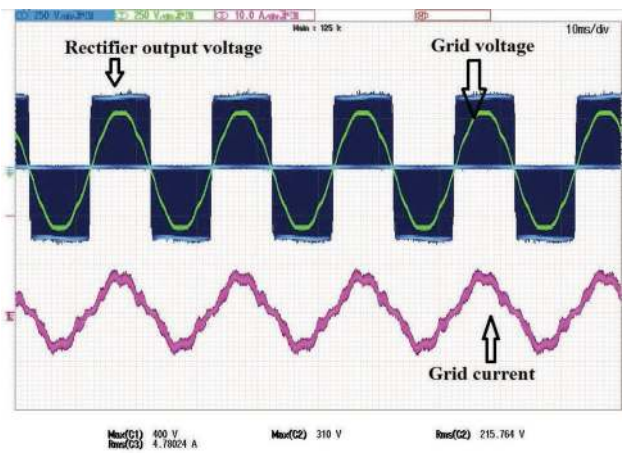

Figure 21. Waveforms of shunt converter with 1 kW dc load: rectifier output voltage (250 V/div), grid voltage (250 V/div) and grid current (10 A/div). X-axis: 10 ms/div.

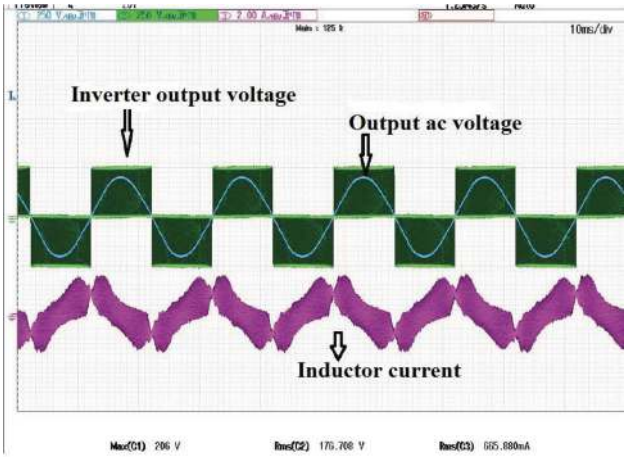

Figure 22. Waveforms of series converter on no load: output ac voltage (250 V/div), inverter output voltage (250 V/div) and inverter inductor current (2 A/div). X-axis: 10 ms/div.

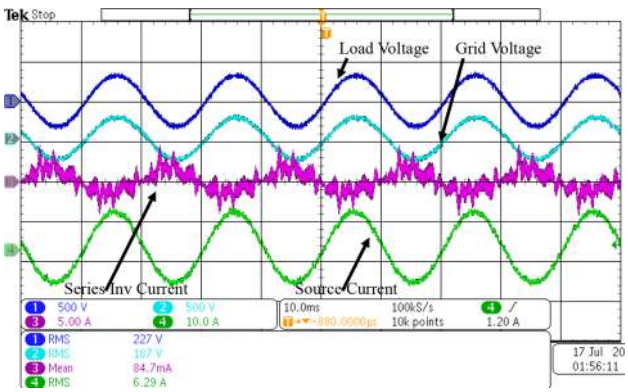

Figure 23. Waveforms of shunt and series converter with sag in grid voltage: load voltage (navy blue, 500 V/div), grid voltage (sky blue, 500 V/div), series converter current (pink, 5 A/div) and source current (green, 5 A/div) during sag in grid voltage for resistive load. *X* axis: 10 ms/div.

high-current driver signals required to properly drive the module's internal IGBTs. These modules are sensitive to noise. The noise signal appearing across the +15 V supply causes false operation of switches. Capacitors are extensively used for bypassing/decoupling. The filtering of noise signal is affected by ESR value of capacitor since ceramic capacitors have low value of ESR and low value of lead inductance when used in surface mounted technology (SMT). Therefore, SMT ceramic capacitors are considered a good choice for filtering high-frequency noise. Also these capacitors should be placed as close as possible to the IGBT module for effective filtering of noise signals [21]. Figure 26 shows the placement of these capacitors along with IGBT module in the printed circuit board (PCB). The capacitors are placed at some distance from the IGBT module. The noise signals are observed at the fault pin of the IGBT module that triggered the fault protection and IGBTs turned off. In figure 27, during the negative half cycle, IGBTs are off, due to which the inverter voltage becomes zero. This forces the inductor current to deviate from its reference value. After predefined time, IGBTs start normal operation. This issue is resolved by placing decoupling capacitors near the IGBT module.

4.2 *High inductor current due to PLL*

The PLL discussed in section 2.2 is used to detect phase angle and frequency of grid voltage. The phase angle is generated by integrating the output of PI controller and constant angular frequency. The PLL algorithm is implemented in the DSP. The value of phase angle is stored in a register of DSP. Since the angle value constantly increases, overflow of register occurs at a certain point of time. When this happens, a sudden change in the value of angle occurs. During this process, the PWM signals generated by the DSP are not as expected. This leads to uncontrolled increase in inductor current, which may damage the IGBT module. Therefore the angle of PLL should not be allowed to increase beyond the value of 2π rad. Figure 28 shows the reversal of PWM pulses followed by the sharp increase in inductor current.

4.3 *High auxiliary current in IGBT module due to regulated power supply*

The built-in gate driver circuit of IGBT module requires a dc voltage of 15 V. When this voltage is provided using commercially available regulated dc supplies, there exists a capacitance of 5 nF between the earth and output terminals of the supply. This high capacitance value provides a low-

Table 5. THD values of the DVR for input current, input voltage, output current, output voltage, power factor, efficiency and voltage regulation.

Source voltage (V)	Input current THD (%)	Input voltage THD (%)	Output current THD (%)	Output voltage THD (%)	Input side power factor	Efficiency (%)	Voltage regulation (%)
185	3.7	2.7	2.7	2.7	1	94.2	1
230	5.4	3	3.1	3.2	1	98.52	0.8
265	5.04	3	3.6	3.5	0.99	93.95	1.3

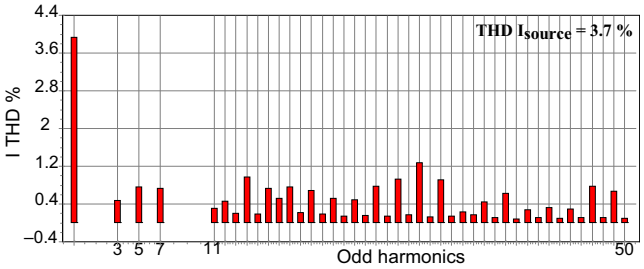

Figure 24. Harmonic spectrum of grid current in case of voltage sag with resistive load.

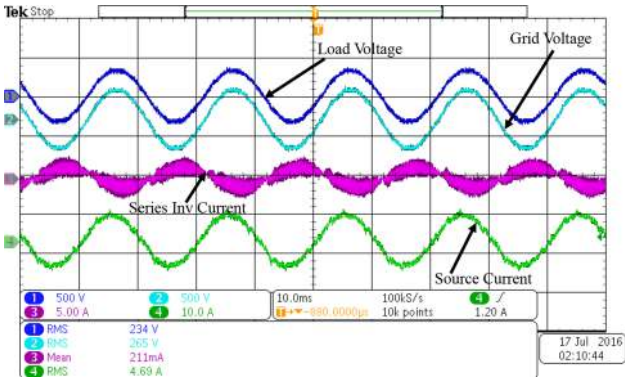

Figure 25. Waveforms of shunt and series converter with swell in grid voltage: load voltage (navy blue, 500 V/div), grid voltage (sky blue, 500 V/div), series inverter current (pink, 5 A/div) and source current (green, 5 A/div). *X* axis: 10 ms.

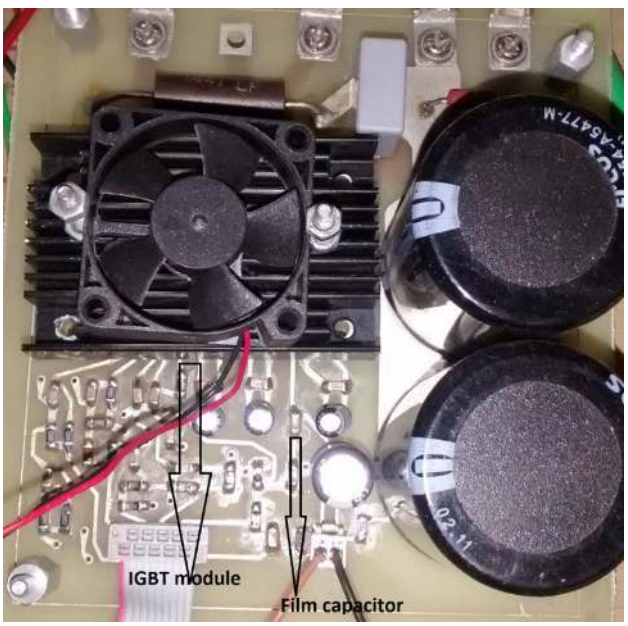

Figure 26. Wrong placement of film-type capacitors.

impedance path to high-frequency currents, which flow via grid neutral to the earth. The total current is on the order of 1–2 A, which can damage the gate driver circuit. To avoid

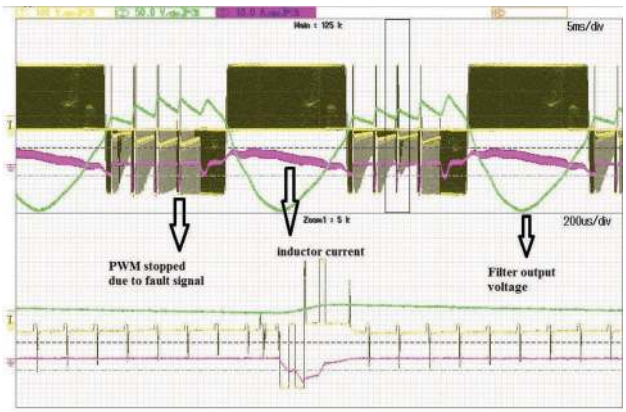

Figure 27. Effect of misplaced capacitor on firing of IGBT.

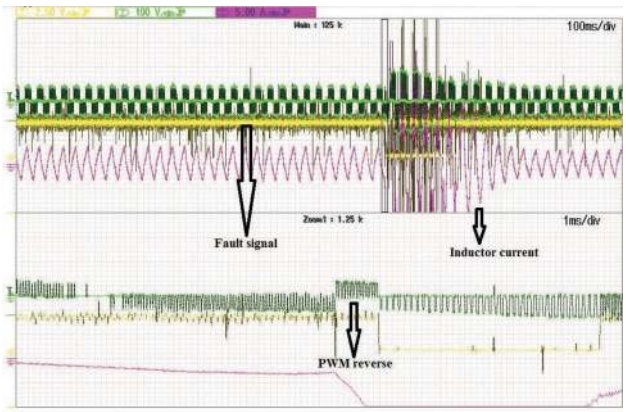

Figure 28. Reversal of PWM pulses and rise of inductor current.

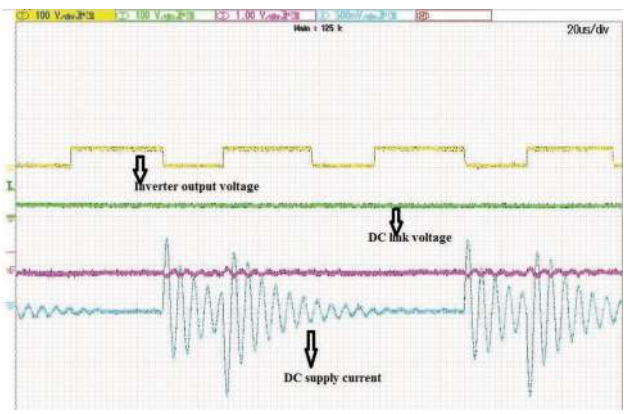

Figure 29. Auxiliary supply current for IGBT module by the commercially available regulated dc power supply.

this problem, an isolated power supply of ±15 V is obtained with the help of a step-down transformer and linear regulator IC. Using this method, the capacitance between system earth and output terminals is reduced to 0.2 nF, thereby limiting the flow of high frequency current. Figures 29 and 30 show the waveforms with a

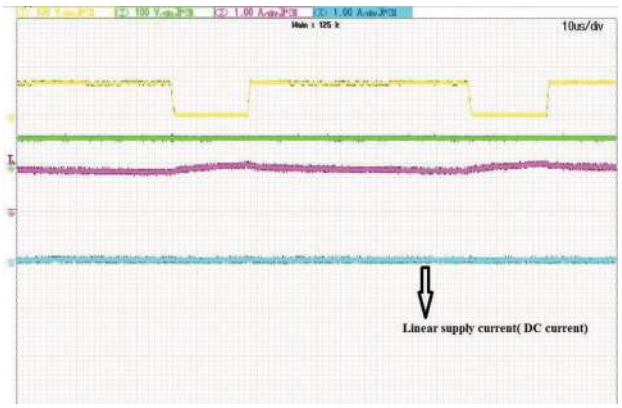

Figure 30. Auxiliary supply current for IGBT module by the designed linear power supply.

commercially available dc supply and laboratory designed linear power supply, respectively. Use of a suitable switch mode power supply instead of the linear power supply would lead to reduction of its size. However, appropriate design must ensure low value of capacitance between earth and its output terminals.

5. Conclusion

Power quality problems, such as sag and swell, can have adverse impact on the performance of critical loads. These power quality problems can even cause undesired turning-off of these loads. To address these issues, a DVR without energy storage element to compensate the voltage across load is designed. H-bridge converters connected in back-to-back configuration with a common dc-link capacitor are used to compensate the load voltage against sag and swell. The load voltage is compensated by injecting a voltage in series with supply voltage with the help of an injection transformer connected between supply and load. The modelling of converters is discussed and their controllers are designed with the help of the Bode plot technique. Various protection schemes are also incorporated in DVR. The performance of DVR is tested by detailed simulation studies in Matlab/Simulink. Simulation results are shown for voltage sag and swell with linear and non-linear loads. To validate the simulation results, a 5 kVA laboratory prototype of DVR is developed. From the experimental results, it is concluded that DVR is successfully able to compensate for voltage sag and swell. Voltage regulation across the load is found to be within $\pm 2\%$. The technical challenges faced during the development of the prototype are also discussed in detail.

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