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DESIGN AND FPGA IMPLEMENTATION OF DIGITAL PULSE COMPRESSION FOR BAND–PASS RADAR SIGNALS

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The paper presents fully digitized approach for band-pass discrete coded radar signals. The emphasis is to use one generalized reconfigurable compressor for several different types of signals and different types of receivers. It fits for direct radio frequency receiver (RF) as well as for intermediate frequency (IF) receiver. The system implementation on field programmable gate area (FPGA) let us eliminate special chips previously needed. From the experimental results it is known that this approach appears to work well for matched and mismatched pulse compression and it outstands when time-bandwidth product (TB) is of order 1000. A precision of 14 bits has been considered in the input signal and 16 bits in the filter coefficients. It gives the dynamic range of 78 dB and the quantification error less than 0.012 %.

K e y w o r d s: digital down converter, digital pulse compression, FPGA mismatched filter, sidelobes reduction

1 INTRODUCTION

Pulse compression is used in radar and sonar to increase the signal energy transmitted without sacrificing neither range resolution, nor encountering excessively high peak powers [1]. First implemented with analog sweep generators and correlators, pulse compression is today almost exclusively performed with digital signal processing hardware and software. Thanks to the advent of dedicated hardware multipliers in field- programmable gate arrays (FPGAs), these devices now challenge general-purpose programmable digital signal processors (DSPs) for signal processing tasks in many DSP applications. Instead of a few multiplier engines found in most DSPs, FPGAs now contain even hundreds of dedicated hardware multipliers. Compared with the iterative multiplications performed by program loops in DSPs, multiplications in FPGAs can be executed in parallel. For example, low cost Spartan 3A-DSP chip we used has 84 dedicated multipliers with accumulators (MAC) which works well at 250 MHz clock. It delivers unprecedented processing power of 21 GMACs (Giga MAC-operations per second).

The major disadvantage of compression is that the compressed pulse has range sidelobes (self-clutter), which limit the range resolution for closely spaced objects. The problem of sidelobes suppression has been recognized as a major problem of pulse compression techniques [1, 2]. First techniques for sidelobes suppression were based on mismatched receiver. The main objective is to design filter which simultaneously performs compression and mismatching, according to given criteria. Such solutions are economical and also obtain better overall results.Different methods of filters mismatching can be roughly classified into two classes of filters. First one, that suppress maximal sidelobes (MX filters) and second, that suppress RMS sidelobes (LS and similar ones). The original algorithms are presented in [3] IRLS (Iterative Reweighted Least Square) and in [4] DIRLS (Doppler optimized IRLS). These new filters combine properties of MX and LS filters and enable considerable simplification of the designing procedure and, what is more important, they can be applied to all types of sequences.

Sidelobes suppression is still unsolved problem generally. Some new techniques are presented in [5]. Adaptive approaches can be found in [2, 6].

Another group of methods for sidelobes suppression was based on complementary sequences. Implementations of compressors for complementary sequences in ultrasound systems have been proposed in [7, 8]. This technique is more Doppler shift sensitive than mismatched one, so its usage is limited on relatively small Doppler shift. An approach with exploiting of complementarity of Barker's sequences set is proposed in [9].

The FPGA implementation of radar compressor in chirp radars based on coordinate rotation digital computer (CORDIC) are proposed in [10]. The application of this compressor in high frequency (HF) radar direct receiver is presented in [11]. We propose simple band-pass compression procedure under some circumstances for pulse duration T, the carrier frequency f_0 and signal bandwidth B: (1) Signal is discrete coded (means the radar pulse is divided into N sub-pulses when $N = TB$); (2) The carrier frequency and signal bandwidth satisfies proposition that $f_0/B - 1/2$ is an integer. According to band-pass signal sampling theory [12, 13] it can be proven that under these conditions signal can be sampled by minimal frequency of $f_s = 2B$ without aliasing. After decimation by factor of 2 and alternating two time series, quadrature (I/Q) base-band signal sequences are obtained and base-band compression is provided. So the advantages of the proposed method are as follows

(1) It fits for direct radio frequency receiver (RF) as well as for intermediate frequency (IF) receiver;

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(2) The architecture reduces system complexity with less analog devices;

(3) The digital down conversion owns less I/Q disbalanse;

(4) Using one generalized reconfigurable compressor for several different types of signals and different type of compressors, matched or mismatched.

Section 2 presents the signal processing procedure for the discrete coded band-pass radar signal; Section 3 describes the hardware implementation of the algorithm described in previous section; System experiment results are considered in Section 4 and, finally, the conclusions are outlined in Section 5.

2 SIGNAL MODEL AND HYPOTHESIS

Denote the discrete coded radar signal in the transmitted period as

$$S(t) = \begin{cases} \cos[2\pi f_0 t + \theta(t)]\,, & t \in [0, T]\,, \\ 0\,, & t \in (T, T_r)\,, \end{cases} \tag{1}$$

where f_0 is carrier frequency, T_r is one transmitted pulse period and the phase $\theta(t)$. Discrete coding means that the phase $\theta(t)$ has the same shape in each sub-pulse interval T_{sp}, where $T_{sp} = T/N$ and $N = TB$ where N is the number of sub-pulses. Now, the phase is changing according to

$$\theta(t) = \theta_0 + \sum_{j=0}^{N-1} \theta_j g(t - kT_{sp})\,, \tag{2}$$

where θ_0 is constant phase, θ_j is phase in j-th sub-pulse and $g(t)$ is sub-pulse shaping waveform width of T_{sp}. It is rectangle pulse as usual so the phase is constant during the sub-pulse interval. Discrete chirp j-th sub-pulse phase is

$$\theta_j = \pi k T_{sp}^2 j^2, \tag{3}$$

where $k = B/T$ is chirp slope. Nowadays, the phase shift keying (PSK) is often used technique for intra-pulse modulation. The phase of discrete PSK radar pulse takes values from set of K equidistant points on trigonometric circle

$$\theta_j = \Delta\theta\, c_j\,, \tag{4}$$

where discrete phase increment is $\Delta\theta = 2\pi/K$ and c_j is code sequence length of $N = TB$ and $c_j \in \{0, 1, \ldots, K-1\}$. Assuming that the backscattering echo has a delay time τ and the amplitude attenuation factor is A, then the echo can be denoted as

$$S_R(t) = AS(t-\tau) = A\cos[2\pi f_0(t-\tau) + \theta(t-\tau)]\,. \tag{5}$$

Here we will process the RF echo signal in all-digital method. This signal has been digital down converted. Today, using of digital down converters is preferred in radar techniques because of their low I/Q imbalance. There are no analog parts in this case. The signal is sampled and the next operations (quadrature mixing or Hilbert transform and filtering) are done by digital signal processing techniques. According to [12, 13] allowed regions for sampling frequency f_s due to avoid aliasing are defined as

$$\frac{2f_0 + B}{m+1} \le f_s \le \frac{2f_0 - B}{m}\,, \tag{6}$$

where $m \in N_0$ and $m \le \lfloor f_0/B - 1/2 \rfloor$ where $\lfloor X \rfloor$ means round X to the nearest integers towards zero. When $m = 0$, the Niquist theorem for base-band signal sampling are obtained. When m is maximal, the minimal value for f_s is obtained. Provide this case, namely

$$m = f_0/B - 1/2\,, \quad m \in N\,, \tag{7}$$

the lowest value of sampling frequency is obtained, $f_s = 2B$. Discrete version of signal from (5) becomes

$$\begin{aligned} S_R[n] &= AS(n/f_s - \tau) \\ &= A\cos[2\pi f_0(n/f_s - \tau) + \theta(n/f_s - \tau)] \\ &= A\cos[2\pi B(m - 1/2)(n/2B - \tau) + \theta(n/f_s - \tau)] \\ &= A\cos[(2m-1)n\pi/2 - \pi(2m-1)\tau B + \theta(n/f_s - \tau)] \\ &= A\cos[(2m-1)n\pi/2]\cos[\theta_n - \theta_1] \\ &\quad - A\sin[(2m-1)n\pi/2]\sin[\theta_n - \theta_1]\,, \end{aligned} \tag{8}$$

where $\theta_1 = (2m-1)\pi\tau B$ and it is constant in the transmitted period, and $\theta_n = \theta(n/f_s - \tau)$ is the baseband phase information as we wanted. Dividing $S_R[n]$ on even and odd samples we get

$$\begin{aligned} &S_R[n] = \\ &\begin{cases} A\cos[(2m-1)i\pi]\cos[\theta_{2i} - \theta_1]\,, & n = 2i\,, \\ -A\sin[(2m-1)(2i-1)\pi/2]\sin[\theta_{2i-1} - \theta_1], & n = 2i-1 \end{cases} \\ &\qquad = \begin{cases} (-1)^i A\cos[\theta_{2i} - \theta_1]\,, & n = 2i \\ (-1)^i A\sin[\theta_{2i-1} - \theta_1]\,, & n = 2i-1\,. \end{cases} \end{aligned} \tag{9}$$

Considering we have two samples per sub-pulse interval ($f_s = 2B$) and phase is constant that time, it follows that $?_{2i} = ?_{2i-1}$. Now, from (9) it is clear that even samples are an alternate series of direct component samples and odd samples are an alternate series of quadrature component samples of complex baseband radar signal $x[i]$, sampled by $F_s = 2B/2 = B$

$$x[i] = (-1)^i (S_R[2i] + j\, S_R[2i-1])\,. \tag{10}$$

That simplifies the DDC block task. It has to disjoin stream out of ADC at two sub-series (even and odd) and to alternate them.

Generally, the compression filter has FIR structure length of $N = TB$, with complex coefficients $h[i]$. The filter response $y[k]$ is convolution between the input signal $x[i]$ and filter coefficients $h[i]$. Matched filter coefficients vector is mirror conjugate version of the applied baseband signal vector. Coefficients of mismatched filter we used are computed by DIRLS algorithm described in [4].

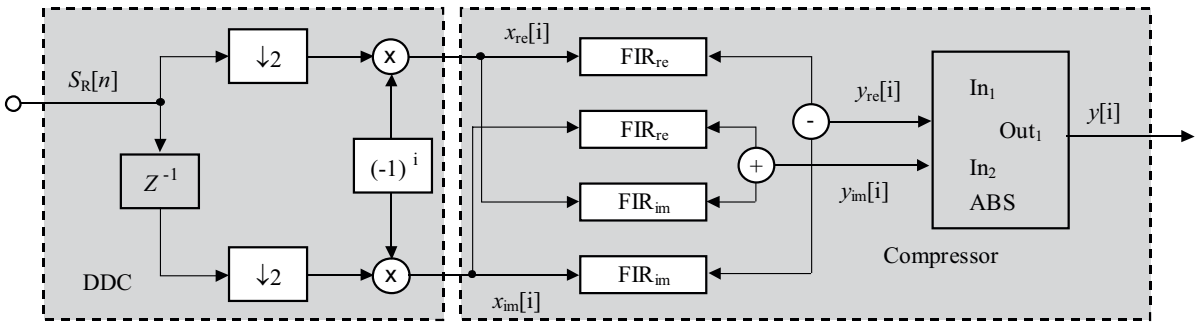

Fig. 1. Complex band-pass signal compressor

3 HARDWARE DESIGN AND FPGA IMPLEMENTATION

The hardware design of pass-band compressor has been divided into two modules perfectly differentiated: one block for digital down conversion of band-pass radar signal to its base-band version, and one base-band compression block. This structure is shown in Fig. 1. In practice, the multiplications in DDC block can be reduced to additions and subtractions because of the binary nature of the coefficients $(-1)^i$. For base-band pulse compression in our model we used four FIR filters (the first two with coefficients as real part and another two with coefficients as image part of complex compressor h[i]) with real and imaginary parts of signal $x[i]$ at the input. The real part of pulse compression is calculated by subtracting the outputs of FIR 1 and FIR 4, and the imaginary part by adding FIR 2 and FIR 3 outputs. Finally, the absolute value (ABS) of the complex signal is calculated applying the ABS CORDIC algorithm, which lets get the pulse compression. We use the Xilinx IP CORDIC core for ABS CORDIC algorithm implementation and Xilinx IP FIR Compiler core for FIR filters implementation [14]. The core support for up to 256 sets of coefficients, with 2 to 1024 coefficients per set and on-line coefficient reload capability. It means that one core can realize the pulse compression for wide set of signal types and wide set of compressors for each signal. The only resources that are increasing are memory blocks for the coefficients saving. We realize two types of compressors, the matched and DIRLS mismatched one, but the same design can easily be applied to the other types.

3.1 Hardware resources estimation

The most critical element in our compressor architecture is Xtreme DSP slice which provides an 18-bit × 18-bit multiplier, 18-bit pre-adder, 48-bit post-adder/accumulator, and cascade capabilities for various DSP applications [14]. The number of DSP slices utilized by the FIR compiler is primarily determined by the number of coefficients $N = TB$, and the hardware oversampling rate k_{os}, defined by the the maximal clock frequency ($F_{\max}$) to sample frequency ($F_s = B$) ratio $k_{os} = \lfloor \frac{F_{\max}}{B} \rfloor$ where $\lfloor X \rfloor$ means round X to the nearest integers towards zero. Each input stream can use the full k_{os} clock cycles to process the $N = TB$ filter coefficients. This gives $\lceil TB/k_{os} \rceil$ multiply- accumulate DSP slice (where $\lceil X \rceil$ means round X to the nearest integers towards infinity). The partial products must be summed together, so an additional accumulator DSP slice per stream is required. Our core provides four input streams, each using $\lceil TB/k_{os} \rceil + 1$ DSP slices. This gives a total of N_{DSP} slices. Maximal resource utilization is attained when ratios $F_{\max}/B$ and TB/k_{os} are integers. In that case

$$N_{DSP} = 4\frac{TB^2}{F_{\max}} + 4\,. \tag{11}$$

This gives the following limitations for the FPGA compressor implementation: $1 \leq TB \leq TB_{\max} B \leq F_{\max}$

$$\frac{TB^2}{F_{\max}} \leq \frac{N_{DSP\,\max}}{4} - 1\,. \tag{12}$$

The first limitation is determined by maximal FIR filter length determined by Xilinx tool and minimal TB product determined by uncertainty principle. In Xilinx IP FIR Compiler 3.5 maximal FIR filter length ($TB_{\max}$) is 1024. In recent versions it is expanded to 2048. The second condition is determined by maximal clock frequency. The third limitation is defined in (13).

The compressor is implemented and verified on NuHorizons Spartan 3A-DSP evaluation board. The Spartan-3A DSP family architecture consists of five fundamental programmable functional elements [14]: XtremeDSP Slices, RAM Blocks, Configurable Logic Blocks (CLBs), Input/Output Blocks (IOBs) and Digital Clock Manager (DCM) Blocks. We have used the FPGA chip XC3SD1800A. It has $N_{DSP\,\max} = 84$ DSP48A. The functional elements of the Spartan-3A DSP family architecture works well at $F_{\max} = 250$ MHz.

3.2 Performance of hardware implementation

It is necessary to consider the quantification error introduced by the hardware implementation shown in Section 3.1. In order to do that, the values of the input sequence are normalized in the $[-1, 1]$ range. A fixed point format has been used in the encoding of the numeric values. From now on, a precision of 14 bits has been considered in the input signal $x[i]$ (1 bit for the integer value

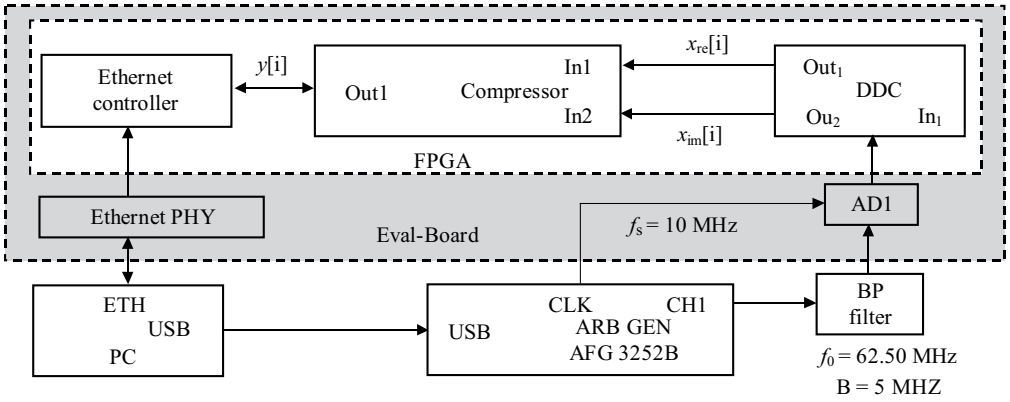

Fig. 2. Experimental setup

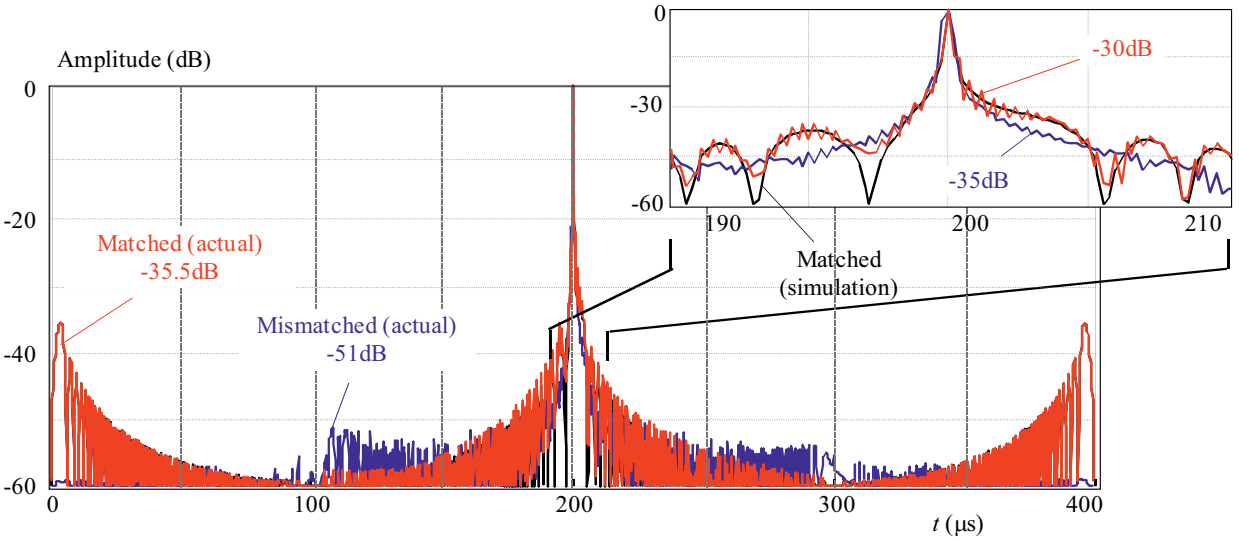

Fig. 3. Actual filters responses for discrete linear chirp TB=1000 (log scale)

and 13 for the fractional part). It gives the dynamic range of 2^{26} or 78 dB. For the FPGA families that include DSP slice this implementation structure takes advantage of the capabilities of the Xilinx DSP slice, however this also places a restriction on the output width limiting it to 48 bits. We designed the compressor for 14-bit width of the input signal, the filter coefficients are 16-bit and maximal filter length is 10-bit (1024). The maximal width of the output signal $y[i]$ is $14 + 16 + 10 = 40$ bit, so 48-bit accumulator is sufficient in order to avoid any kind of overflow or truncation in the consecutive arithmetic operations. At the end, after the CORDIC, the output signal is truncated to 16-bit width, so the quantification error is less than 2^{-15} or 0.004 %.

4 EXPERIMENTS AND RESULTS

The framework of the hardware implementation is shown in Fig. 2. An arbitrary waveform generator (Tektronix AFG 3252B) is used to form the band-pass discrete chirp signal. After band-pass filtering, signal is sampled by an AD converter. The compressor is implemented and verified on a Spartan 3A-DSP evaluation board by NuHorizons. This platform contains many peripherals. We used 14-bit width AD converter that operates on maximal 125 MHz (LTC2285) and 10/100 Ethernet PHY KSZ804. The results are presented by sending UDP packets to PC via 100BaseT Ethernet. The packets contain 16-bit samples of matched filter output and mismatched filter output. Two RAM blocks in form of FIFO (as a part of Ethernet controller) are used to collect the values of this three types of signals. When FIFOs are full, the Ethernet controller starts sending packets. A host application on the PC side receives packet, convert signal in logscale, and shows the results.

In the test scenario we tested compressor performance when long waveforms with large TB products were applied. We used the radar data with the following parameters: signal is linear FM (chirp), signal bandwidth is $B = 5$ MHz, and the pulse duration is $T = 200\,\mu$s, so TB product is 1000. Carrier frequency is 62.5 MHz, so condition (7) is satisfied. Input signal is Doppler shifted at 1 kHz in order to verify hardware design in realistic scenario. The implementation of the compressor for this type of signals occupies all 84 XtremeDSP slices in the Spartan 3A-DSP FPGA. It satisfies relation (13). The other elements are not critical.

Figure 3 shows the actual signals obtained by the designed hardware module. These signals are nearly equal to the ideal ones obtained by simulation. The error is less than 1.5 dB in near sidelobes significant region. It is effect of imperfect sampling and band-pass filtering when the phase in a sub-pulse interval is slightly changing so $\theta_{2i} \neq \theta_{2i-1}$ and equation (9) is not full satisfied. But $\theta_{2i} \approx \theta_{2i-1}$ and error is acceptable. In far sidelobes region, error is not noticeable. When mismatched filter is applied, it is clear that sidelobes are significantly smaller. Near sidelobes suppression is 5 dB apropos far sidelobes suppression of 25.5 B.

5 CONCLUSION

The paper presents fully digitized approach for band-pass discrete coded radar signal compression when carrier frequency and signal bandwidth satisfies proposition that $f_0/B-1/2$ is an integer. The hardware design has been divided into two modules: one block for simple digital down conversion of the band-pass radar signal to its base-band version, and one base-band compression block. The computational load has been analysed, modifying the signal bandwidth and the length of the used signal sequences.

We choose discrete chirp and DIRLS mismatched filter for verification of the proposed design. Also, it fits for arbitrary discrete coded spread spectrum waveforms and the other types of mismatched filters. From the experimental results it is known that this approach appears to work well for matched and mismatched pulse compression and it outstands when time-bandwidth product (TB) is of order 1000 at bandwidth of 5 MHz.

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