Design and Evaluation of FinFET based SRAM Cells at 22nm and 14nm Node Technologies

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ABSTRACT
In today's world scenario more than 85-90% of the chip area is mainly occupied by memory. There is a need for faster and reliable memory system for various integrated devices from computers to various handheld devices. The memory devices such as SRAM, DRAM etc. were served by the traditional MOSFETs till to date but as the demand of the better performing and the compact modeling of the integrated devices are causing the failure of MOSFETs operations. The MOSFET scaling is suffered by Short Channel Effects (SCE's). SRAM is one of the memories mainly used in the cache memory of devices. It must be faster, less power consuming and reliable but this is affected by CMOS scaling causing process variations. Here in this paper the alternate solution to the issues faced by MOSFET based SRAM is overcome by FinFET based SRAM. A 6T short gated FinFET based SRAM is taken for the study and the spice models are created at 22nm and 14nm using Predictive Technology Models (PTM) and simulated using HSPICE. The performance is analyzed in terms of Static Noise Margin (SNM), power and delay for the 6T SRAM. The results shows FinFET based SRAM is faster, reliable and the power consumption is significantly reduced and offers good trade-offs at lower technology nodes.

General Terms
Memory design, FinFET

Keywords
SRAM Cell, FinFET, CMOS, SNM, PTM Read delay, Write delay

1. INTRODUCTION
The past 4-5 decades CMOS scaling from one technology node to the next node has given improved performance. This enabled in developing smaller, faster and powerful digital systems. But scaling of bulk CMOS is facing a lot of challenges due to material and process technology limits [1]. As per 2011 International Technology Roadmap for Semiconductors (ITRS) there are many challenges to be addressed to the increased scaling of bulk CMOS include Short Channel Effects (SCE's), such as sub-threshold leakage, Drain Induced Barrier Lowering (DIBL) and gate-dielectric leakage etc. The system reliability and system performance are affected due to challenges of CMOS scaling.

The above said challenges will become more prominent as CMOS scaling approaches atomic and quantum-mechanical physics boundaries.

Many Researchers and scientists are working on CMOS scaling and alternate material ideas of semiconductors to overcome the above said challenges and trying to serve all the purposes of electronics and computer age. We have novel devices called FinFETs which are double-gate field-effect transistors and are capable of overcoming the scaling obstacles [1,2]. One of the most important features of FinFETs is that the front and back gates helps in effective controlling the electron flow through the channel hence reduce the short channel effects [5-10].FinFET technology is strong candidate for future Nano electronics due to its high-performance, low power consumption, reduced susceptibility to process variations, and ease of manufacturing using current processes.

Because of FinFETs, the possibility of scaling down the node technology to 10nm and beyond is a reality. Thus FinFET is a promising candidate to bridge the technology gap between bulk CMOS and other novel devices, such as Graphene FETs and CNTFETs. FinFETs can be a replacement for bulk-CMOS transistors in many ways. Its lower leakage current /standby power property makes FinFETs a desirable option for memory sub-systems designs. Memory modules are widely used in most digital and computer systems. Leakage power is very important parameter in memory cells since most memory applications access only one or very few memory rows in a given time. The majority of memory cells draw only leakage power. In microprocessors and controllers the clock circuit power consumption due to memory devices (i.e, cache memory, register, and pipeline registers) accounts for nearly 51% of the total power[6]. The application of FinFET technology to memories can save significant power; increase the tolerant capacity of the memory device and faster operations could be achieved. The sections of this paper are divided as follows: section 2 gives a brief description of the FinFET technology and device parameters, section 3 discuss about the performance metrics of the SRAM cell, section 4 describes about the FinFET based 6T SRAM and its working involving the write and read assist circuits. The results and discussions are detailed in the section 5, section 6 gives the conclusion.

2. FINFET TECHNOLOGY & DESIGN PARAMETERS
The FINFET based transistors offers good tradeoff for power as well offering interesting delay. The Figure 2.1 shows the 3D structure of multi-FIN based field effect transistors.

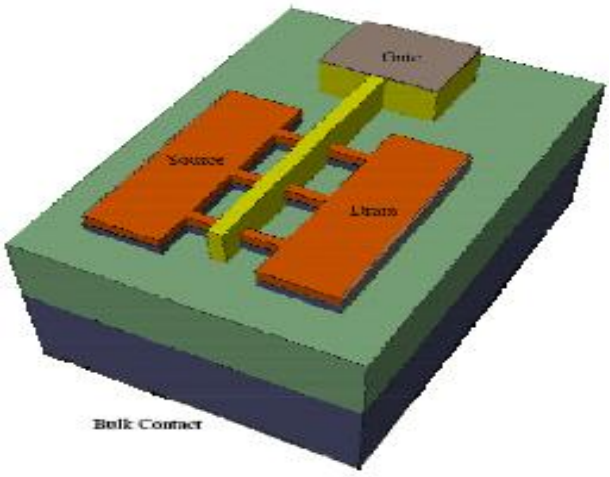

Fig 1. 3D Multi-FIN Based Field Effect Transistor Structure [12]

Fig 1 shows a simple structure of FinFET, it is a 4 terminal device comprising of source and drain connected by a channel, the channel is wrapped around by multiple gates, in this case we consider 2 gates namely forward and backward gates or front and back gates. A FinFET is like a FET, but the channel has been "turned on its edge" and made to stand up hence structure gave the name for the device as FinFET. FinFETs may be substituted into a former bulk-CMOS design by merely shorting the front- and back-gates together during device fabrication to allow only one gate connection per FinFET. This transistor configuration is often called shorted gate (SG).

The device parameters considerations are one of the important steps in developing a spice model and then simulating it. Commonly used FinFET simulation models available to the research community are the Predictive Technology Model (PTM)[7] and BSIM-CMG/BSIM-IMG[8]. Table1 shows the values of FinFET parameters used in this work. The values of the parameters shown in table 1 are considered with respect to PTM.

Table.1 Design considerations[15]

PARAMETER	**22nm FinFET**	**14nm FinFET**
Gate Length (Lg)	22nm	14nm
Supply Voltage	0.9v	0.8v
Thickness of Fin (tfin)	10nm	10nm
Height of Fin (hfin)	30nm	23nm
Thickness of oxide (tox)	1.4nm	1.3nm

The device parameters mentioned here are important in designing any circuit using FinFET. Technologies nodes are defined based on the gate length, as the device is scaled down the supply voltage, oxide thickness and height of the fin is also scaled down to meet the requirements and to avoid the scaling issue such as velocity saturation. The design considerations are purely done on the geometric description of FinFET device structure[13-15]. There will be a lot of variations in changing the values of any of these parameters mentioned. In our study we have focused on these 5 parameters mentioned in the table.

3. SRAM CELL PERFORMANCE METRICS

3.1 Static Noise Margin

Static Noise Margin (SNM) is one of the most important metric for SRAM memory cell. SNM affects both read and write margin, which is related to the threshold voltages of the NMOS and PMOS devices of the SRAM cell. The SNM is defined the minimum noise voltage present at each of the cell storage nodes necessary to flip the state of the cell. SNM parameter can be better understood by drawing the inverter characteristics and then mirroring it on itself and measuring the maximum square between them. For stability of the SRAM cell, good SNM is required that depends on the value of the cell ratio, pull up ratio and also supply voltage. Driver transistor is responsible for 70 % value of the SNM. Cell ratio is the ratio between sizes of the driver transistor to the load transistor during the read operation.

Pull up ratio is also nothing but a ratio between sizes of the load transistor to the access transistor during write operation.

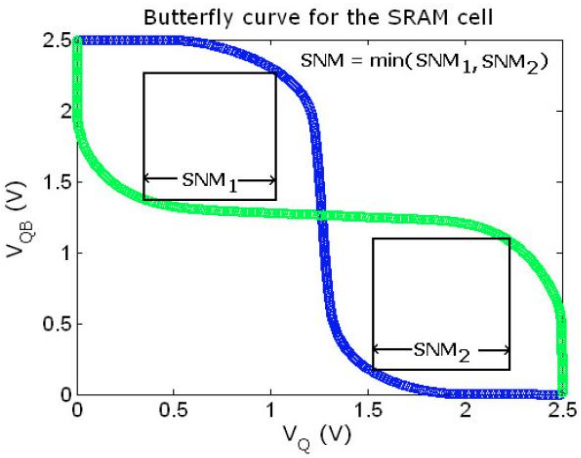

Fig.2. SRAM butterfly curve

Cell Ratio = (W1/L1) / (W5/L5) – During Read operation Pull up Ratio = (W4/L4) / (W6/L6) – During Write operation SNM, affects both read and write margins that are directly related to the threshold voltages of NMOS and PMOS devices [9]. To increase SNM, we can increase the threshold voltages of PMOS and NMOS however, that increase is limited and also having a threshold voltage that is very high makes the devices difficult to operate as it becomes hard to flip the MOSFET. Hence we turn to the use of FinFETs for enhancement of metrics that will make SRAM performance better. In our study we have calculated SNM at standby mode of the FinFET based 6T SRAM cell using graphical method by simulating the FinFET SRAM spice model in HSPICE. SNM should be high for a device to perform smoothly and produce valid outputs.

3.2 Power

Power consumption and dissipation is one of the major performance metric of SRAM [11]. The MOSFET based SRAM fails to operate when it is scaled down to the nanometer regime of technology node, causing high power consumption and dissipation of the SRAM cell . The power consumed by the FinFET based SRAM cell at 22nm and

14nm technology nodes are studied here. The system trade-offs of power are also observed here. The power consumption often relates to the supply voltage and hence as we scale down the FinFET, the power consumption of the entire circuit must also decrease but in few cases the dissipation of power may increase because of the density of the integrated device. Hence understanding the metric power is important here.

3.3 Delay

The delay of the SRAM cell can be measured in terms of the write and read delay of the circuit [11]. The write delay is the time taken by the SRAM circuit to write a bit of data into the memory i.e the latch circuit. The read delay is the time taken for extracting the stored bit of data from the latch to output. The read delay also depends upon the sense amplifier circuitry used for reading the output, if the sensing is fast then obtaining the outputs will be also fast. The write and read delays are obtained for FinFET based SRAM cell at 22nm and 14nm node technologies. Again the system trade-offs between power, area and delay are studied here.

4. SRAM MEMORY

4.1 Static Random Access Memory[SRAM] Cell

It is one of the most commonly used type of semiconductor memory that uses a bi-stable latching circuitry to store each bit, it is static in nature and different from D-RAM which is dynamic and is refreshed periodically. SRAM is volatile and will lose its data if it is not powered. It is used in PCs, workstations and other peripheral equipment alike internal CPU caches, hard disk buffers etc.

There are two types of SRAM cells:

1. Asynchronous SRAM
2. Nonvolatile SRAM

SRAMs are also classified on the basis of the transistor type used to build an SRAM. BJTs are very fast but consume a lot of power, then came the MOSFET bases SRAMs which replaced the BJTs and served all the operations with higher performance. The need of better performance and scaling down the size of MOSFET with reduced short channel effects paved the way for the idea of FinFET based SRAMs. The FinFET based 6T SRAM circuit is shown in fig 4.2. Looking at the circuit diagrams we can clearly understand the presence of double gates namely forward and backward gates in the FinFET based SRAM cell[12,13,18]. In our study we have considered the double gate short gated FinFET SRAM cell where the forward and backward gate are shorted and provided with the gate input. This gives better channel control and the failure of MOSFET at nanometer regime technology node can be overcome.

4.2 FinFET based SRAM Cell

The data storage cell, i.e., the 1-bit memory cell in static RAM arrays, invariably consists of a simple latch circuit with two stable operating points (states). Depending on the preserved state of the two-inverter latch circuit, the data being held in the memory cell will be interpreted either as a logic "0" or as a logic "1" .To access (read and write) the data contained in the memory cell via the bit line, we need at least one switch, which is controlled by the corresponding word line, i.e., the row address selection signal usually, two complementary access switches consisting of nMOS pass transistors are implemented to connect the 1-bit SRAM cell to the complementary bit lines (columns). This can be likened to turning the car steering wheel with both left and right hands in complementary directions.

The circuit structure of the full FinFET static RAM cell is shown in Figure 3, along with the pFET column pull-up transistors on the complementary bit lines. The most important advantage of this circuit topology is that the static power dissipation is even smaller; essentially, it is limited by the leakage current of the pFET transistors. A FinFET memory cell thus draws current from the power supply only during a switching transition. The low standby power consumption has certainly been a driving force for the increasing prominence of FinFET SRAMs.

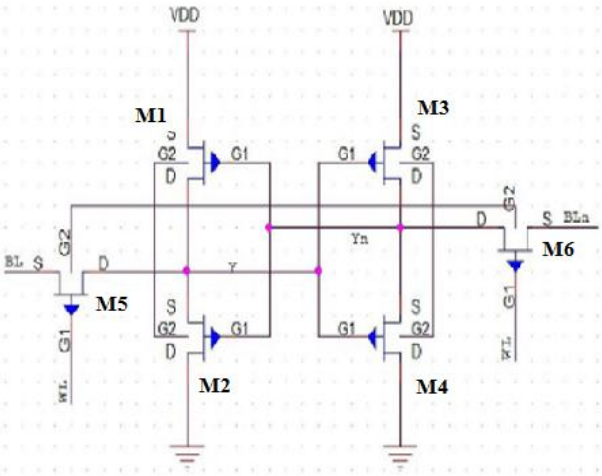

Fig.3. FinFET based 6T SRAM [12]

5. RESULTS AND DISCUSSIONS:

The spice models of FinFET SRAM are first created for 22nm and are simulated using HSPICE and the simulation waveforms are viewed using the cosmos cope. The simulation waveforms for write and read delays are as shown below in Fig 4 and Fig 5 respectively

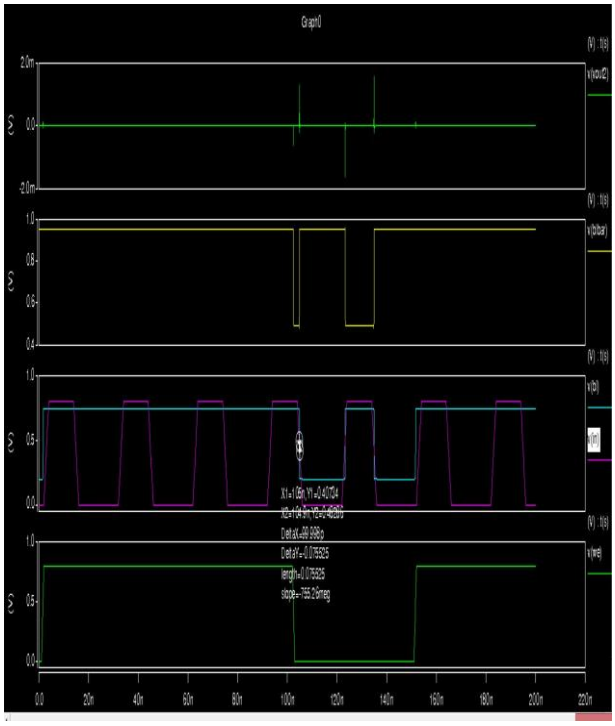

Fig.4. Write delay for 22nm FinFET based SRAM

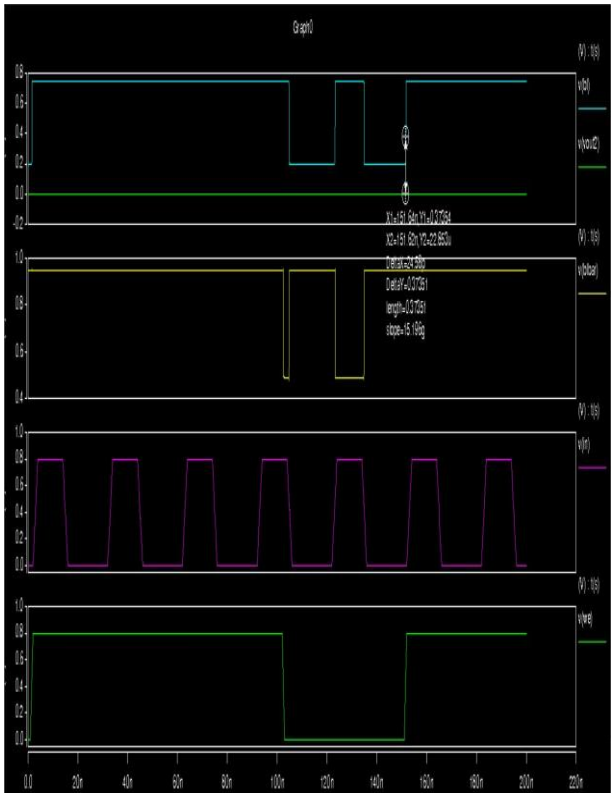

Fig.5. Read delay for 22nm FinFET based SRAM

Then the models are modified for 14nm and the process is repeated.

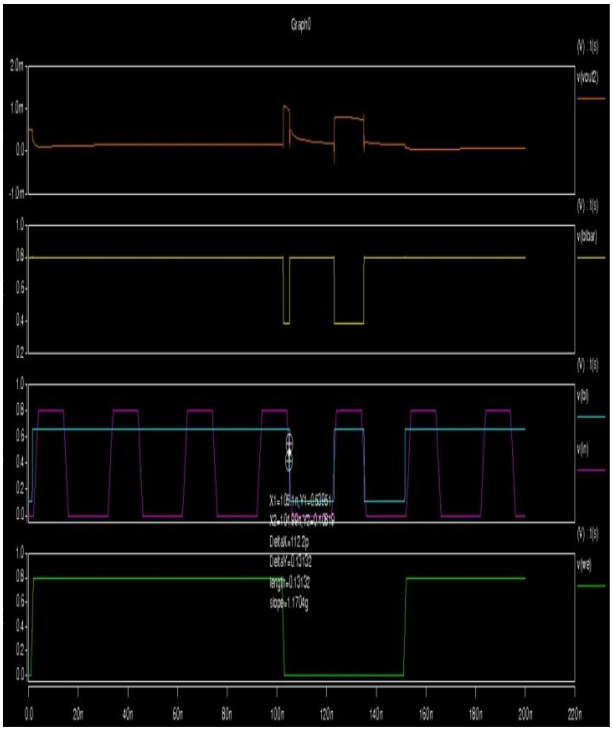

Fig.6. Write delay for 14nm FinFET based SRAM

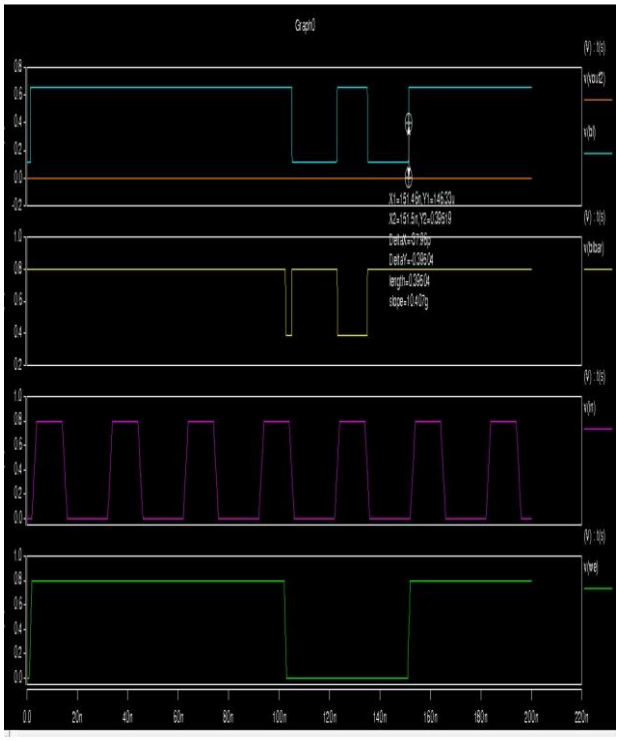

Fig. 7: Read delay for 14nm FinFET based SRAM

Fig. 6 and 7 shows the read and write operation for the FinFET based 6T SRAM at 14nm. The voltage used is 0.8v.

Here the word enable (we) acts as a control signal. When the word enable is low, write operation is done. When the word enable is high the data what was written will be sensed by the sense amplifier. The read operation is performed when word enable is high Fig. 8 and 9 shows the butterfly curves for FinFET based 6T SRAM cell at 22nm and 14n respectively. This shows the Static Noise Margin (SNM) at standby mode values obtained in each case of the SRAM cell. These butterfly curves are obtained using the graphical method plot in HSPICE. The SNM values are read from the DeltaY value, considering the fig.8 the DeltaY value shows 0.20738 in volts, hence the SNM value obtained for 22nm FinFET 6T SRAM is 207.38 mV. Similarly considering Fig.9 we can see the DeltaY value obtained is 0.18467 in volts, hence the SNM obtained for 14nm FinFET 6T SRAM cell is 184.67mV.

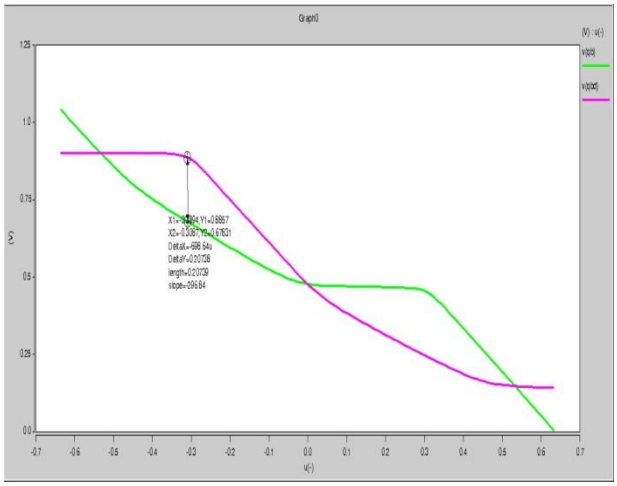

Fig.8.Butterfly curve for FinFET based 6T SRAM at 22nm

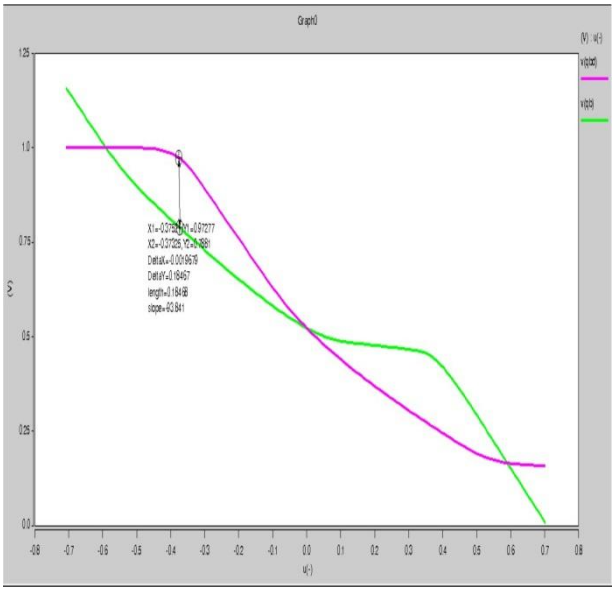

Fig.9: Butterfly curve for FinFET based 6T SRAM at 14nm

The average and maximum power consumed by the FinFET SRAM cell at 22nm and 14nm and the read and write delay is measured and it is tabulated in Table 2. The plotted graphs in fig.10 shows the comparison of the all the parameter values measured for the SRAM circuits. Here we can see the system trade-offs between power, area and delay of the FInFET SRAM circuit. As we scaled down the FinFET device from 22nm to 14nm the area has been reduced hence enabling the integration of more components for more operations and better multiple features. The second trade-off is with delay where the speed of the operation in terms of the write and read has been reduced quite a little in the 14nm SRAM compared to that of the 22nm model but the power consumption is more in case of the 22nm circuit but less in the 14nm FinFET SRAM. The SNM obtained shows that the FinFET based SRAM is reliable at lower technology nodes and the read and write operations of the SRAM cell will run smoothly.

Table 2 Results for FinFET based 6T SRAM Cell

PARAMETER	14nm 6T SRAM	22nm 6T SRAM
Static Noise Margin (SNM)	184.67mV	207.38mV
Avg Power	30.1870uW	35.2259uW
Max Power	63.0222uW	79.0756uW
Write Delay	112.2ps	99.98ps
Read Delay	37.96ps	24.58ps

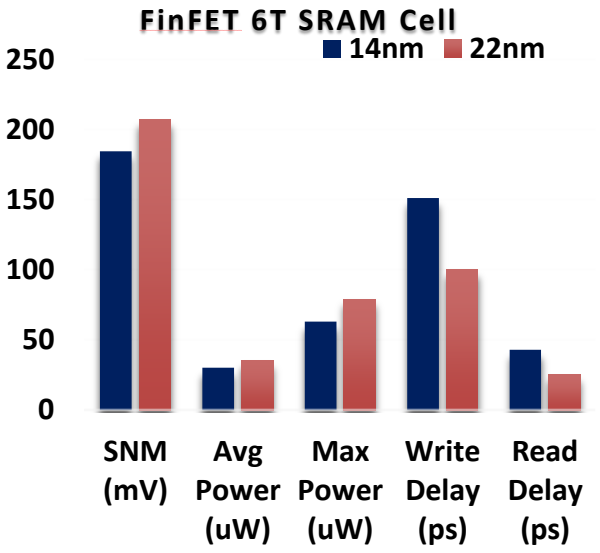

Fig.10 Graphical plot showing results of 6T SRAM cell at 22nm and 14nm

6. CONCLUSION

The FinFET based 6T SRAM cell at 22nm and 14nm are analyzed here. The obtained results for the SRAM spice models shows a promising solution for MOSFETs scaling issues. The static noise margin values obtained for the SRAM cell shows that the FinFET based SRAM cell is reliable at lower technology nodes and the tolerant capacity is better at the nanometer regime. The power consumption of the device has decreased significantly and this memory cell could be integrated with any such memory based devices needing less power consumption. The speed of the memory circuits are also studied in terms of the write and read delay which shows that the read and write speed has increased and the system trade-offs between power, area and delay is manageable where the delay has increased at 14nm model but the power and area has reduced significantly.

7. ACKNOWLEDGEMENTS

Author acknowledges the BMSIT for its infrastructure facility for carrying out the work.

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