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Design and Evaluation of High Efficiency Power Converters Using Wide-Bandgap Devices for PV Systems

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DESIGN AND EVALUATION OF HIGH EFFICIENCY POWER CONVERTERS USING WIDE-BANDGAP DEVICES FOR PV SYSTEMS

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Abstract

The shortage of fossil resources and the need for power generation options that produce little or no environmental pollution drives and motivates the research on renewable energy resources. Power electronics play an important role in maximizing the utilization of energy generation from renewable energy resources. One major renewable energy source is photovoltaics (PV), which comprises half of all recently installed renewable power generation in the world. For a grid-connected system, two power stages are needed to utilize the power generated from the PV source. In the first stage, a DC-DC converter is used to extract the maximum power from the PV panel and to boost the low output voltage generated to satisfy the inverter side requirements. In the second stage, a DC-AC inverter is used to convert and deliver power loads for grid-tied applications. In general, PV panels have low efficiency so high-performance power converters are required to ensure highly efficient PV systems.

The development of wide-bandgap (WBG) power switching devices, especially in the range of 650 V and 1200 V blocking class voltage, opens up the possibility of achieving a reliable and highly efficient grid-tied PV system. This work will study the benefits of utilizing WBG semiconductor switching devices in low power residential scale PV systems in terms of efficiency, power density, and thermal analysis.

The first part of this dissertation will examine the design of a high gain DC-DC converter. Also, a performance comparison will be conducted between the SiC and Si MOSFET switching devices at 650 V blocking voltage regarding switching waveform behavior, switching and conduction losses, and high switching frequency operation.

A major challenge in designing a transformerless inverter is the circulating of common mode leakage current in the absence of galvanic isolation. The value of the leakage current must be less than 300mA, per the DIN VDE 0126-1-1 standard. The second part of this work investigates a proposed high-efficiency transformerless inverter with low leakage current. Subsequently, the benefits of using SiC MOSFET are evaluated and compared to Si IGBT at 1200 V blocking voltage in terms of efficiency improvement, filter size reduction, and increasing power rating. Moreover, a comprehensive thermal model design is presented using COMSOL software to compare the heat sink requirements of both of the selected switching devices, SiC MOSFET and Si IGBT.

The benchmarking of switching devices shows that SiC MOSFET has superior switching and conduction characteristics that lead to small power losses. Also, increasing switching frequency has a small effect on switching losses with SiC MOSFET due to its excellent switching characteristics. Therefore, system performance is found to be enhanced with SiC MOSFET compared to that of Si MOSFET and Si IGBET under wide output loads and switching frequency situations. Due to the high penetration of PV inverters, it is necessary to provide advanced functions, such as reactive power generation to enable connectivity to the utility grid. Therefore, this research proposes a modified

modulation method to support the generation of reactive power. Additionally, a modified topology is proposed to eliminate leakage current.

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List of Terms

AC	Alternating Current
AlN	Aluminium Nitride
Al	Aluminium
CM	Common Mode
CEC	Californian Efficiency
Cu	Copper
C_{PV}	Parasitic Capacitance
DC	Direct Current
V_{DM}	Differential Mode Voltage
E_G	Material Bandgap
E_C	Critical Electrical Field
FEM	Finite Element Method
FEV	Finite Volume Method
FEA	Finite Element Analysis
GaN	Gallium Nitride
HERIC	Highly Efficient and Reliable Inverter Concept
HEMT	High Electron Mobility Transistor
IGBT	Insulated-gate Bipolar Transistor
I_L	Leakage Current
JFET	Junction Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPPT	Maximum Power Point Tracking
N_I	Intrinsic Carrier Concentration
PV	Photovoltaic
Q_{rr}	Reverse Recovery Charge
RERs	Renewable Energy Resources
Si	Silicon
SiC	Silicon Carbide
SPWM	Sinusoidal Pulse Width Modulation
THD	Total Harmonic Distortion
T_{rr}	Reverse Recovery Time
V_{CM}	Common Mode Voltage
V_{ECM}	Equivalent Common Mode Voltage
V_{BK}	Breakdown Voltage
V_{SAT}	Saturation Velocity
WBG	Wide-Bandgap
ε_r	Relative Permittivity
μ_n	Electron Mobility

Chapter 1. Introduction

Conventional sources of energy such as coal, oil, and natural gas are the major energy sources that have driven the industrial revolution for the past two hundred years. Unfortunately, these sources of energy are limited and non-renewable. Also, emission gases from these conventional energy sources cause air pollution, which contributes to global warming and climate change. Therefore, renewable energy resources such as solar, biomass, wind, and hydropower are the focus of much modern research literature because they are efficient, renewable, and create less pollution.

The expected total global energy generation from renewable sources by the end of 2018 is 2,017 GW [1]. One major renewable energy source is photovoltaics (PV), which comprises about 47% of recently installed renewable power generation [1]. The major drawback to renewable energy sources, including photovoltaics and wind power, is that they fluctuate and can be only intermittently reliable for energy generation because they rely on natural, not controllable factors such as the sun and wind. Therefore, an interface system between renewable energy sources and power grids is needed to meet the specifications of the given grid. A power electronic converter may play an important role in an interface system because it can maximize the utilization of renewable sources and contribute to high efficiency renewable energy systems. As a result, designing reliable

and highly efficient power converters is one of the most interesting topics in the field of renewable power generation.

Low power PV systems, such as those for residential scale, have been widely installed by municipal power grids financially supported by local authorities and governments. The high penetration of PV residential scale systems will reduce electrical energy consumption from the grid and possibly mean that surplus electricity will be generated that can be provided (or sold) to other users [2].

Power electronic converters are the key to providing a flexible and efficient connection between a residential PV system and the grid; and, they support many functions including: grid synchronization; boosting of input voltage; and, anti-islanding mode operation and detection. Therefore, the performance of the PV system is very dependent upon highly efficient and reliable power converters [3]. As a result, the development of high-efficiency systems has been the focus of much research on how to improve system performance, increase energy generation, and reduce costs of PV system power generation.

The development of high-efficiency power converters for residential PV systems can be achieved by introducing new and advanced converter topologies and by using wide-bandgap (WBG) power switching devices [3]. The use of the new generation of power devices, such as wide-bandgap switches, in PV converters is an important application in the field due to the superior performance of such devices versus that of the traditional, Si-based power switching devices. WBG power devices have the advantage of operating at high switching frequency with low switching and conduction loss

compared to those of conventional Si power switches, which as a result will enhance the performance of PV inverters [4], [5].

1.1 Research Objective

The objective of this thesis is to design high-efficiency power converters for a residential scale PV system and enhance system performance by utilizing WBG-based semiconductor power devices. Additionally, the impact of using WBG power devices will be investigated in terms of efficiency improvement, passive component volume reduction, and heat sink volume reduction. The following aspects are considered:

- A performance comparison between an SiC MOSFET switching device with 650 V blocking class and a standard Si MOSFET in terms of switching waveform behavior, switching and conduction losses, and high switching frequency operation in a proposed DC-DC converter.
- A performance comparison between an SiC MOSFET switching device with 1200 V blocking class and a standard Si IGBT in terms of switching waveform behavior, switching and conduction losses, and high switching frequency operation in a proposed DC-AC inverter.
- Modify the proposed DC-AC inverter to completely eliminate leakage current and be capable of generating reactive power to satisfy the future requirements of a PV grid-tied system.

1.2 Dissertation Outline

This dissertation is organized as follows. This first chapter will introduce the topic of the paper. In Chapter 2, the PV system architecture will be discussed. Also, PV grid integration configurations will be presented with multiple PV configurations depending upon the system application. After that, a high gain DC-DC converter is proposed to boost the low input voltage of the PV module. The chapter closes with simulation results showing the validity of the proposed high gain converter.

Chapter 3 discusses the impact of leakage current generation in transformerless inverters due to the absence of galvanic isolation. A common mode model is presented to follow the path of the leakage current. The leakage current is described by an equation of common mode voltage that includes the terminal voltages V_{AN} and V_{BN}. After that, two methods are introduced to solve the issue of the leakage current generation.

In Chapter 4, a review of transformerless inverters based on full bridge topology is presented. The review shows and discusses the common mode characteristics of each topology. After that, a proposed transformerless inverter is introduced. Then, a theoretical loss model is derived to evaluate the performance of the various transformerless inverters. The chapter concludes with comparisons between the various topologies and the proposed topology in terms of switching losses, conduction losses, and efficiency.

Chapter 5 will discuss the physical characteristics of the WBG materials and present their advantages in terms of low ON-state resistance, high switching speed, and temperature operation. Next, the static and dynamic characteristics of SiC MOSFET is compared to those of Si IGBT to evaluate their performance in terms of conduction and

switching losses. In Chapter 6, the benefits of WBG based power devices, such as SiC MOSFET, in the proposed converters are presented in terms of efficiency improvement, filter size reduction, power rating increase, and heat sink requirement. The simulation results show a significant impact through the adoption of WBG power devices in power converters in terms of enhancing system efficiency and reducing costs.

The seventh chapter presents a modified version of the proposed transformerless inverter to achieve two objectives for future PV grid tied system requirements. The first objective is to eliminate leakage current by combining the clamping method with the galvanic isolation method. The second objective is to modify the modulation technique to achieve reactive power generation. The study conclusions and a discussion thereof will be presented in the final chapter.

Chapter 2. PV System Architecture

2.1 Introduction

The total power capacity of solar photovoltaics (PV) installed around the world in 2014 was 187.24 GW and the new annually added power capacity of PV systems was 47.6 GW. By 2015, the new annually added power capacity of PV systems was 58.1 GW compared to 47.6 GW in 2014. There has recently been a rapid increase in the power generation of renewable energy sources such as PV as systems become less costly to build and the abundant resource of the sun is recognized as a viable and easy source to utilize. The annual energy growth of multiple energy sources around the world is presented in Figure. 2.1 [6].

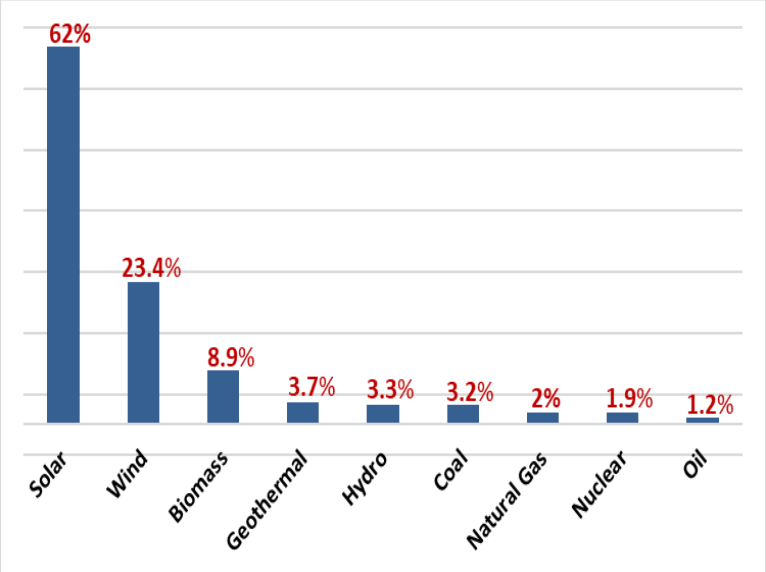


Figure 2. 1. Global annual growth of energy [6]

A major issue with grid-connected PV is the fluctuation and intermittent nature of PV sources with regard to output voltage and power due to weather conditions.

Additionally, the installation of PV systems is restricted by two main factors: low energy conversion and the high cost of manufacturing solar cells. The cost of PV arrays comprises the largest portion of the total cost of the system, approximately forty percent. Other costs include the power electronic components, energy storage, and the control circuit.

2.2 Configuration of PV Grid Integration

The configuration of PV is divided into four types, as shown in Figure 2.2: (a) central, (b) model, (c) string, and (d) multi-string. Each of these configurations can consist of parallel and/or series PV models, different arrangements of DC-DC converters, and/or DC-AC inverters, depending upon the system application.

2.2.1 Central Configuration

In this type of configuration, only one three-phase inverter is used to combine a large number of PV modules. Central inverters are utilized extensively in large scale PV systems because they are more cost efficient when there is only a single monitoring unit and control platform. On the other hand, this type of configuration has some disadvantages, including that there is only one maximum power point tracking (MPPT) utilized for the whole PV array so a high level of mismatch loss can occur between the PV modules.

2.2.2 Module Configuration

This type of configuration is used for low power (less than 500 W) and is known as micro inverter. With module inverter configuration, only one single phase inverter is

connected to one PV module so there is no mismatch loss between the PV modules. This configuration is also very flexible and installation and expansion are easily implemented.

2.2.3 String Configuration

In string configuration, one inverter is connected to a single PV string without using blocking diode. String inverter is an amplified version of module inverter configuration, where the power is increased by using single PV string that consists of multiple PV modules. In this type of configuration, the mismatch loss between PV modules is decreased by operating MPPT at string level. String configuration is designed for low power applications such as residential use.

2.2.4 Multi-String Configuration

Multi string configuration is the most commonly used configuration today as it combines the advantages of central and string configurations. In this type of configuration, multiple PV strings connected to separate DC-DC converters are attached to a single inverter. Multi string configuration can be used for medium power applications, such as commercial or residential.

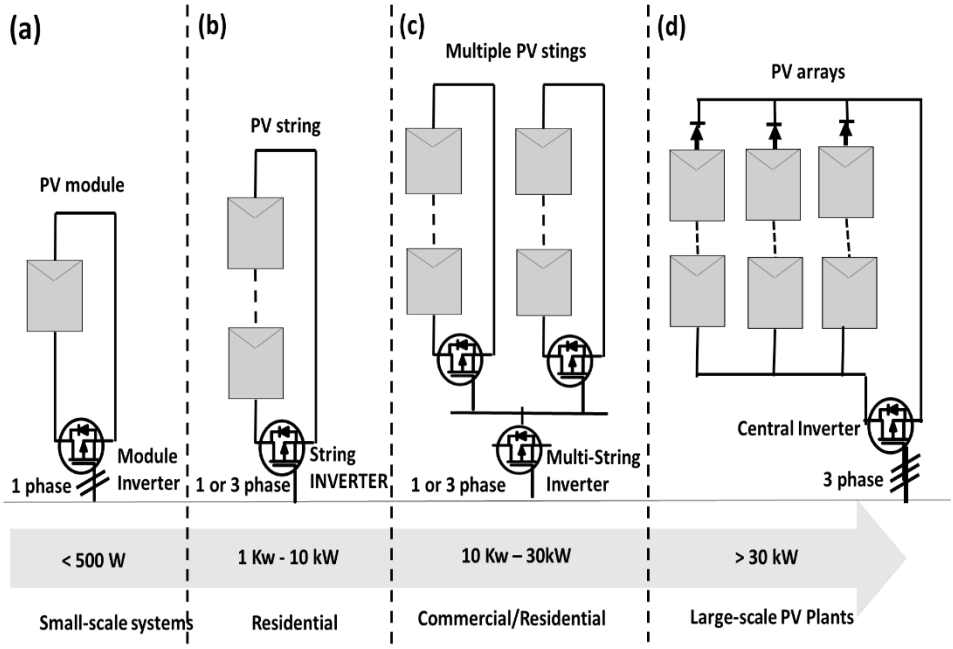


Figure 2. 2 PV system configurations: (a) module inverter; (b) string inverter; (c) multi-string inverter; and, (d) central inverter [7]

2.3 Modeling of Photovoltaic Module

A PV panel consists of a number of solar cells that operate differently under changing weather conditions. As a result, the maximum power point (MPP) of a PV panel will fluctuate [7], [8]. Therefore, a PV system requires that a DC-DC converter with MPPT control strategy be included in the design of the PV panel [9]. The characteristics of a PV panel, such as I-V and P-V, can be extracted from modelling the equivalent circuit of a PV cell so that its behavior can be predicted under different environmental conditions.

By representing a PV panel using a mathematical model, it's behavior can be simulated. A PV cell can be described by a current source and a diode connected in

parallel as shown in Figure 2.3. Two parameters can also be added to the model, the equivalent series resistance (R_s) and the equivalent parallel resistance (R_p). The values of R_s and R_P are unknown but can be calculated mathematically or by using curve-fitting approach [10].

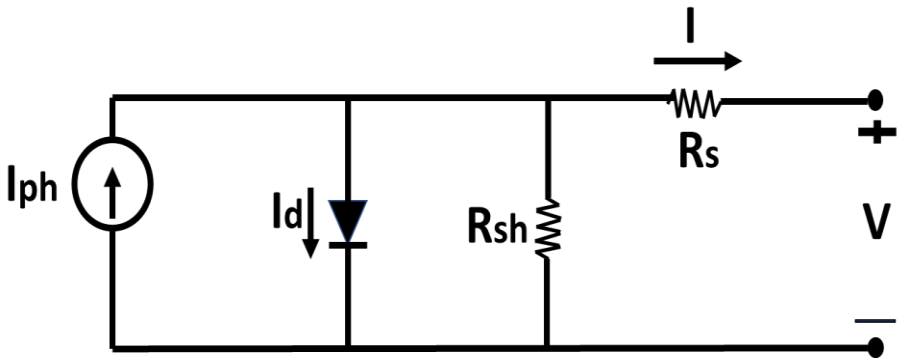


Figure 2. 3 PV cell equivalent circuit

The following equations are derived from the equivalent circuit to understand the fundamental characteristics of a PV panel such as I-V and P-V [11].

The input power is:

$$P_{in} = V_d \cdot I_{ph} \tag{2.1}$$

The diode current is calculated as follows:

$$I_d = I_{sat}\left[e^{\frac{V}{V_t}} - 1\right] \tag{2.2}$$

The output current is determined by:

$$I = I_{ph} - I_d - \frac{R_s \cdot I + V}{R_s} \tag{2.3}$$

The open circuit voltage is given by:

$$V_{oc} = V = \frac{nkT}{q} In\left[\frac{I_{ph}}{I_d} + 1\right] \tag{2.4}$$

The short circuit current is determined as:

$$I_{sc} = I_{ph}(V = 0) \tag{2.5}$$

The terms of the previous equations are defined as follows:

- I_{ph} denotes the generated current by the incident light;
- I_{sat} represents the saturated current;
- V_t is the solar cell's thermal voltage;
- n is the ideality factor of the diode;
- k is the Boltzmann's constant, which is equal to $1.3806503 \cdot 10^{-23} J/K$;
- T represents the operating temperature; and,
- q is the electron charge, which is equal to $1.60217646 \cdot 10^{-19} C$.

2.3.1. Design of a PV Module Using PSIM Simulation Environment

An accurate model of a PV panel can be designed using simulation software tools to analyze its performance. The PV module in PSIM is shown in Figure 2.4. Only the basic parameters of a solar cell, which can be extracted from its data sheet, are required to perform the simulation. For this study, PSIM simulation software offers a Physical Model that was used to design the PV module [12].

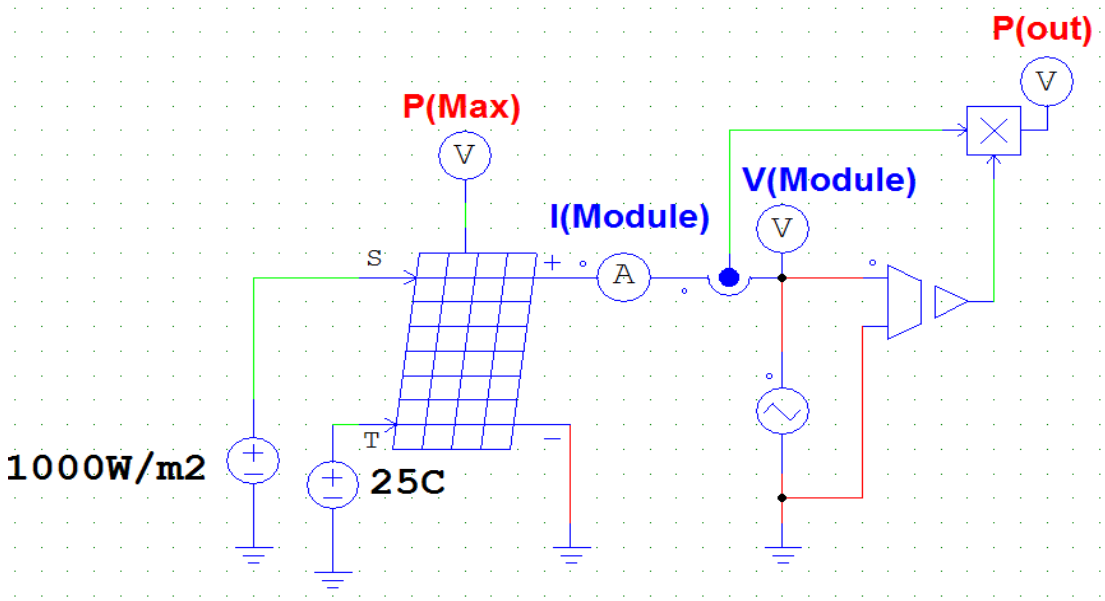


Figure 2. 4 PV module in PSIM

2.3.2. Physical Model of PV Panel in PSIM

PSIM simulation environment provides a physical model of a PV panel in its utility menu as presented in Figure 2.5. As this figure shows, many parameters are required to model a solar panel with the physical model feature provided by PSIM. Most of these parameters can be obtained from a PV panel's data sheet while other parameters such as shunt resistance (R_{sh}) and series resistance (R_s) can be calculated automatically in PSIM.

The fundamental parameters of simulating a PV panel are as follows:

- Maximum Power (P_{max})
- Voltage at P_{max} (V_{mp})
- Current at P_{max} (I_{mp})
- Open-circuit voltage (V_{oc})

- Short-circuit current (I_{sc})
- Light intensity (S_o)
- Temperature (T_{ref})

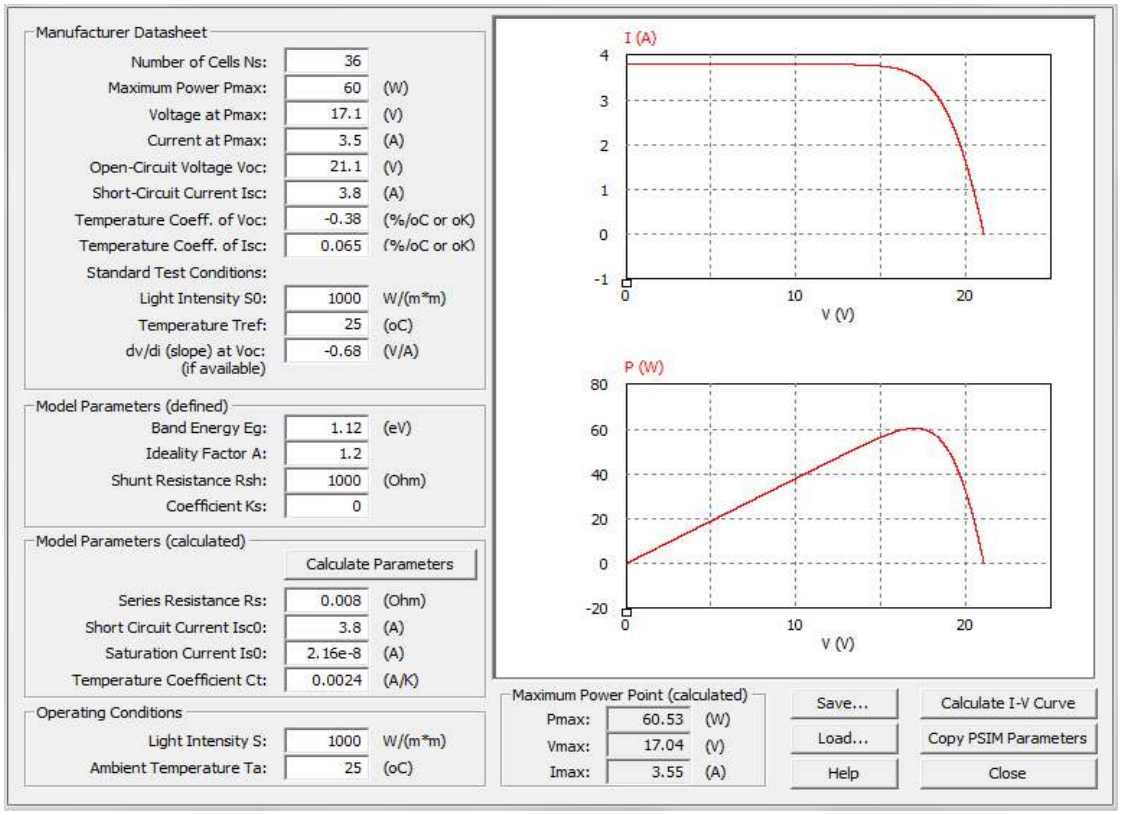


Figure 2. 5 Physical model simulator of a PV cell in PSIM

2.3.3. Design of a 3 kW PV Array

The output power of a PV system can be increased by connecting either solar modules in parallel or in series to form arrays. Series connection of PV modules will increase the output voltage, while parallel connection will increase the output current. MSX-60 PV module was chosen for this simulation model and its electrical specifications are provided in Table 2.1. The PV array is composed of five modules connected in series

and ten modules connected in parallel. The value of the output power is calculated as [5 × 10 × 60] which is equal to 3 kW. The PV characteristic of the array are given in Figure 2.6.

Table 2. 1 MSX-60 electrical specifications

Electrical Characteristics of Solar Module (MSX-60)	
Maximum Power (P_{max})	60 W
Voltage at P_{max}	17.1 V
Current at P_{max}	3.5 A
Open-Circuit Voltage (Voc)	21.1 V
Short-Circuit Current (Isc)	3.8 A

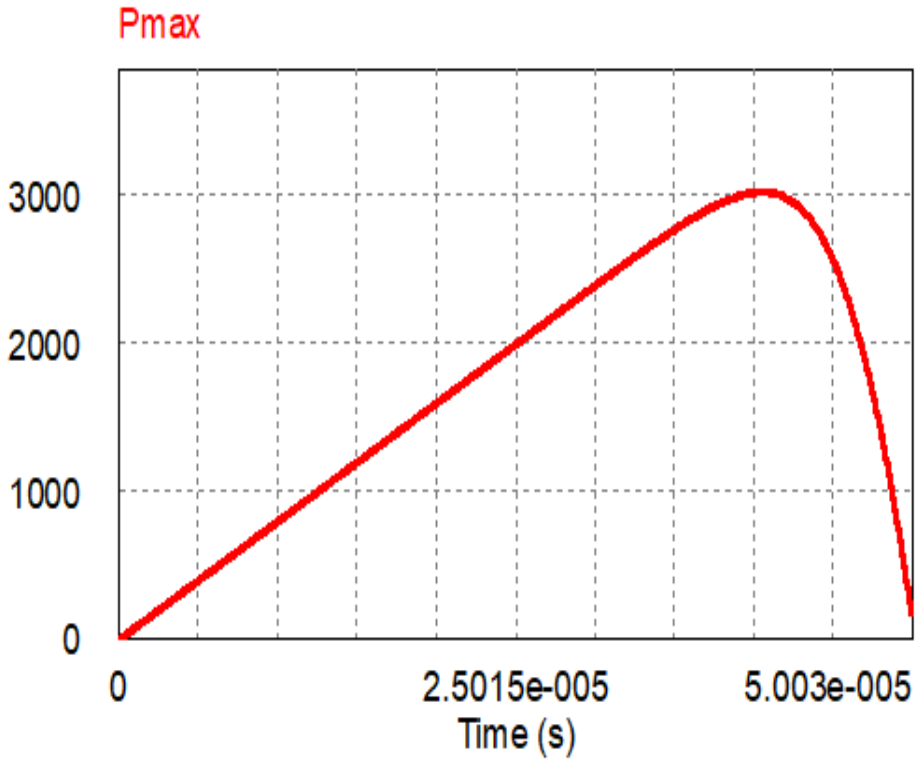


Figure 2. 6 PV characteristics of solar array

2.4 High Gain Boost Converter for PV Application

In PV systems, the voltage of the PV panels is low and needs to be increased to satisfy the inverter side requirements without increasing the cost by adding more PV panels. To achieve this goal, a high gain DC-DC converter must be inserted between the PV panel and inverter. A novel high gain boost converter is proposed to reach a high output voltage and overcome the associated drawbacks of a conventional converter such as high duty ratio and narrow turn-off interval. The proposed converter is composed of interleaved structure connected to the input voltage and voltage multiplier connected to the output voltage to achieve high gain ratio.

The emergence of renewable energy resources (RERs) has rapidly expanded over the last few years due to the finite nature of conventional energy sources, severe weather conditions, and environmental pollution. Photovoltaics are one of the major RERs expected to continue to be more and more popular and the generate an even higher percentage of total renewable energy generation [13]–[17].

2.4.1 Review of High Gain DC-DC Converter

Generating high output voltage from a PV module requires many solar cells connected in series. Using a high number of cells connected in series leads to mismatch between the cells, which will degrade the output voltage. Therefore, a high gain boost converter is needed to step up the output voltage for grid side applications [18]–[21].

The output voltage of a PV panel is usually in the range of 20 V to 80 V. Therefore, a DC-DC converter with high duty ratio is needed to generate high voltage for the inverter side. To achieve high output gain with a traditional boost converter, a large

duty ratio is needed that will cause high voltage stress, high ripple current, narrow turn-off interval, and high conduction losses [22], [23]. Accordingly, a high gain DC-DC converter is necessary for PV applications. The structure of the PV system is shown in Figure 2.7. Several high gain boost converters, such as interleaved structures, converter with coupled inductor, and switch capacitor converter, are broadly studied in [25]– [35].

A proposed high gain boost converter that combines the structure of the symmetrical interleaved converter and a voltage multiplier. The voltage multiplier consists of four capacitors and four diodes to achieve high output gain. A total of four stages is developed from the voltage multiplier that leads to a high gain of 10 with 50% duty cycle.

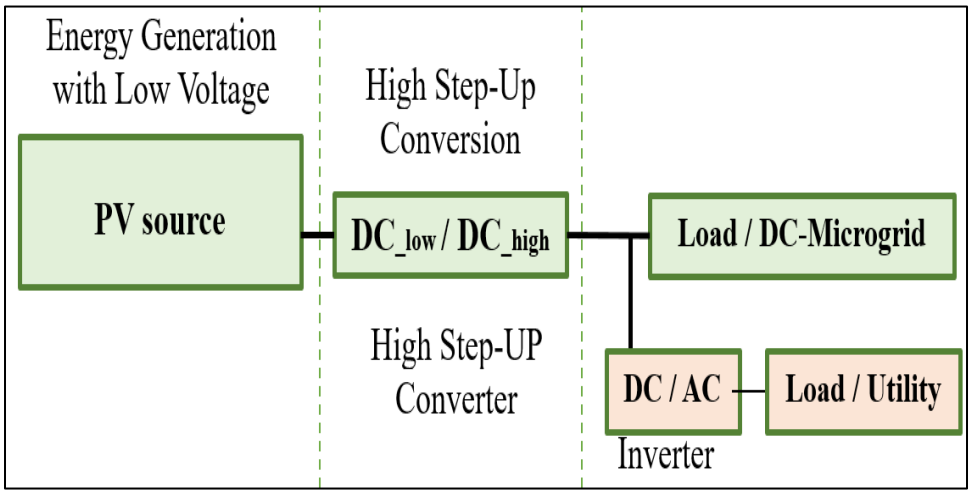


Figure 2. 7 Structure of PV system

2.4.2 Structure of Proposed DC-DC Converter

The structure of the proposed converter consists of two parts, an interleaved converter and voltage multiplier. The interleaved converter is connected to the input side and the voltage multiplier is connected to the output side, as shown in Figure 2.8. Four

diodes and four capacitors are used as the voltage multiplier to achieve a high gain ratio. A high gain ratio of 10 is achieved with a duty cycle of 50%, which means that the proposed DC-DC converter has a high output voltage equal to 10 times the input voltage.

2.4.2.1 Operating Principle

The duty ratio is selected to be equal to 50% of the total switching time; this means that half of the time the switches are ON and the other half of the time the switches are OFF. Therefore, there are two operational modes. The proposed converter has two switches and their corresponding switching signals are shown in Figure 2.9.

In mode I, S2 is ON and S1 is open (OFF) as presented in Figure 2.10(a). The inductor current I_{L1} flows through the voltage multiplier capacitors and charges C1, C3, and C_{out} and discharges C2 and C4. The output diode is conducting and the output capacitor is charged to feed the load.

In mode II, S1 is ON and S2 is open (OFF) as presented in Figure 2.10 (b). The inductor current I_{L2} passes through the voltage multiplier capacitors and charges C2, C4, and discharges C1 and C3. The output diode is reverse biased and the output capacitor feeds the load.

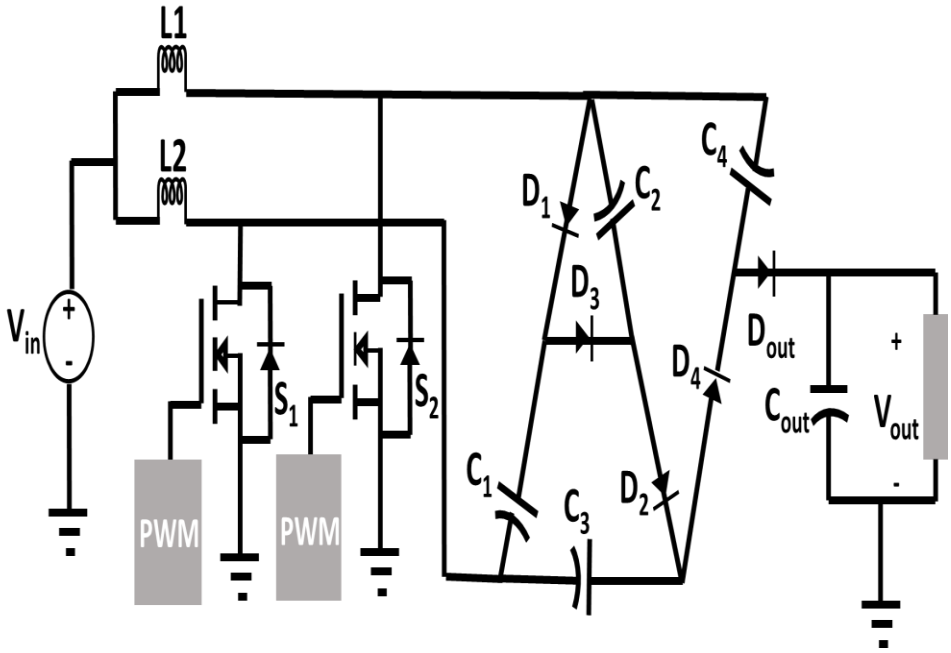


Figure 2. 8 Circuit structure of the proposed topology

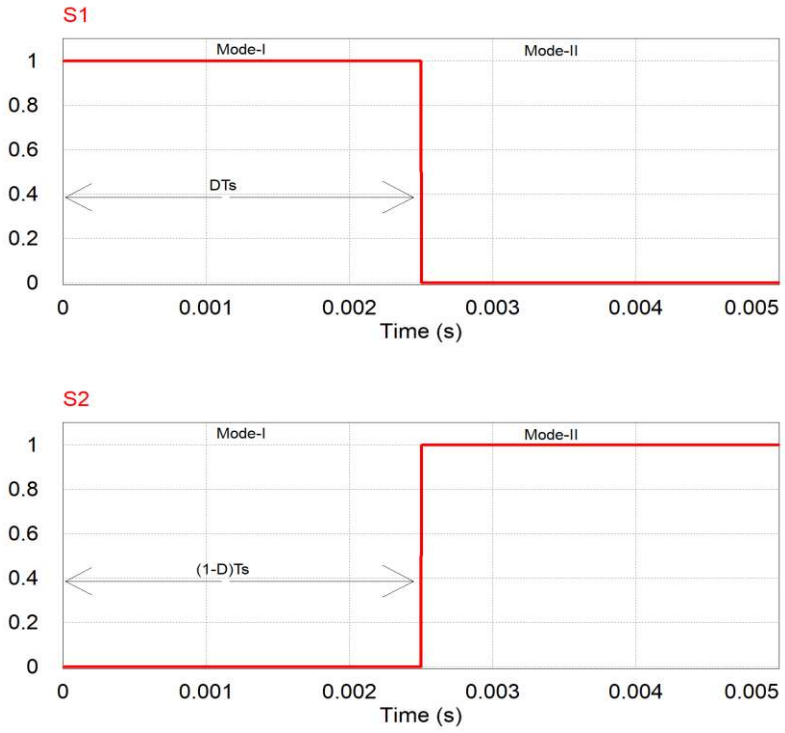
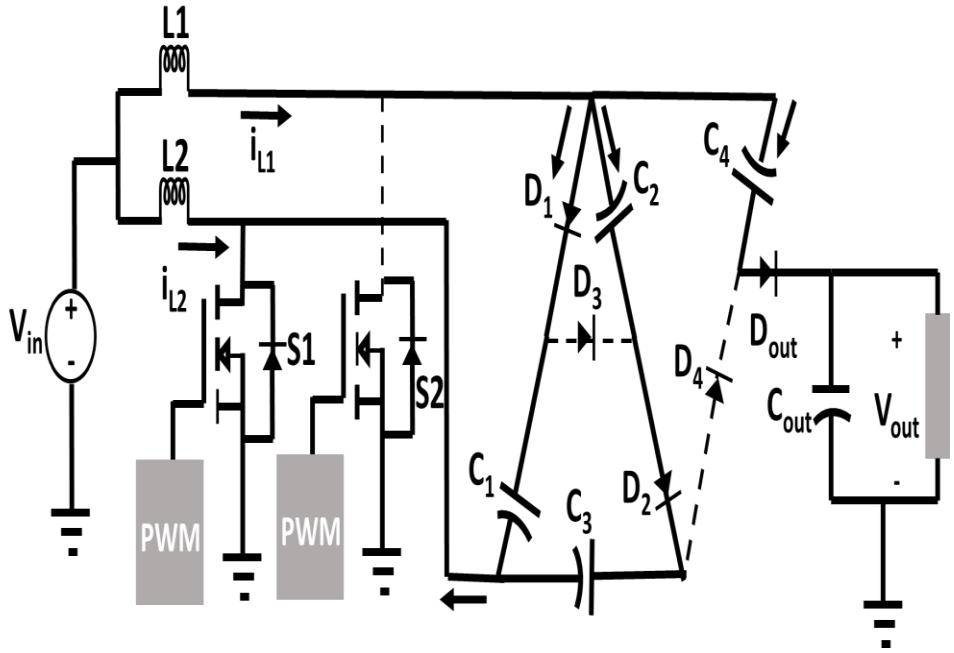
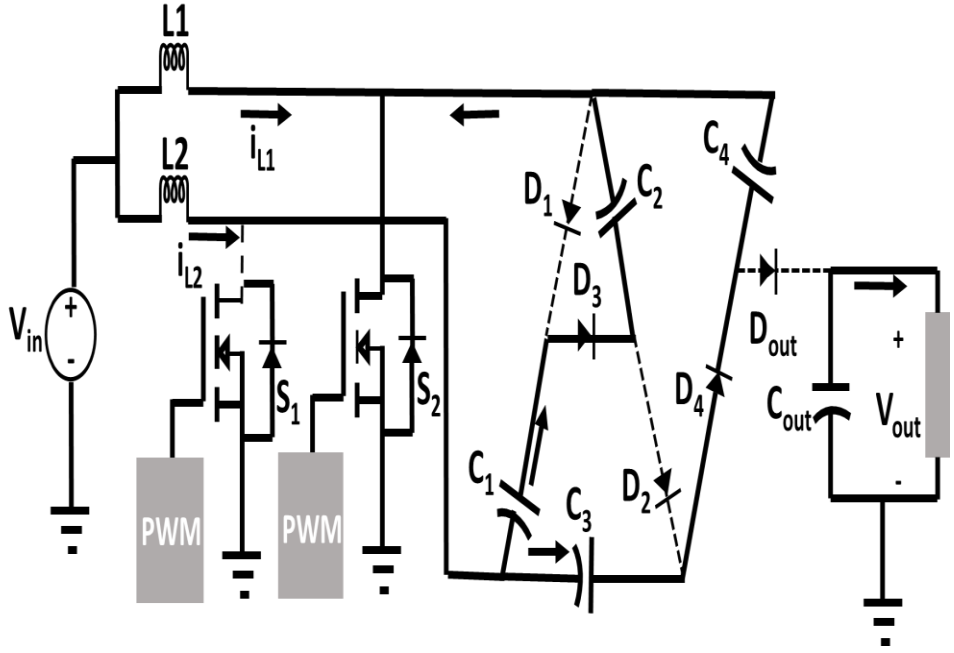


Figure 2. 9 Switching signals of proposed topology



(a)



(b)

Figure 2. 10 Operation modes. (a) Mode I; and, (b) Mode II.

2.4.2.2 Steady State Analysis

Assuming a periodic signal, the average voltage on the inductors is zero over the entire switching cycle.

$$\langle \mathrm{V_{L1}} \rangle = 0 \tag{2.6}$$

$$\mathrm{V_{L1}} = \mathrm{V_{in}} \tag{2.7}$$

$$\langle \mathrm{V_{L2}} \rangle = 0 \tag{2.8}$$

$$\mathrm{V_{L2}} = \mathrm{V_{in}} \tag{2.9}$$

From mode I, the following equations are derived:

$$V_{L1} = V_{in} - V_{C1} \tag{2.10}$$

$$V_{C1} = V_{C3} - V_{C2} = V_{out} - V_{C4} \tag{2.11}$$

From the volt-second balance:

$$V_{L1} = DTV_{in} + (1-D)T(V_{in} - V_{C1}) = 0 \tag{2.12}$$

$$V_{C1} = \frac{V_{in}}{(1-D)} \tag{2.13}$$

$$V_{C1} = V_{C3} - V_{C2} = V_{out} - V_{C4} = \frac{V_{in}}{(1-d)} \tag{2.14}$$

From mode II, the following equations are derived:

$$V_{L2} = V_{in} + V_{C1} - V_{C2} \tag{2.15}$$

$$V_{C2} - V_{C1} = V_{C4} - V_{C3} \tag{2.16}$$

From the volt-second balance:

$$V_{L2} = DTV_{in} + (1-D)T(V_{in} + V_{C1} - V_{C2}) = 0 \tag{2.17}$$

$$V_{C2} - V_{C1} = \frac{V_{in}}{(1-d)} \tag{2.18}$$

$$V_{C2} - V_{C1} = V_{C4} - V_{C3} = \frac{V_{in}}{(1-d)} \tag{2.19}$$

Solving for C_2, C_3, and C_4:

$$V_{C2} = V_{C1} + \frac{V_{in}}{(1-d)} = \frac{V_{in}}{(1-d)} + \frac{V_{in}}{(1-d)} = \frac{2V_{in}}{(1-d)} \tag{2.20}$$

$$V_{C3} = \frac{2V_{in}}{(1-d)} + \frac{V_{in}}{(1-d)} = \frac{3V_{in}}{(1-d)} \tag{2.21}$$

$$V_{C4} = \frac{3V_{in}}{(1-d)} + \frac{V_{in}}{(1-d)} = \frac{4V_{in}}{(1-d)} \tag{2.22}$$

Therefore, the output voltage is given as follows:

$$V_{out} = \frac{V_{in}}{(1-d)} + \frac{4V_{in}}{(1-d)} = \frac{5V_{in}}{(1-d)} \tag{2.23}$$

As shown in Equation (19), a high gain ratio of 10 is achieved with a duty cycle of fifty percent.

2.4.3 Component Selection

2.4.3.1 Inductor Selection

The inductor value is calculated based on the conventional boost converter and is shown by:

$$L_1 = \frac{V_{in}d}{\Delta I_{L1} f_{sw}} \tag{2.24}$$

$$L_2 = \frac{V_{in}d}{\Delta I_{L2} f_{sw}} \tag{2.25}$$

2.4.3.2 MOSFET Selection

The voltage stress on the switches is shown by:

$$V_{S1} = \frac{V_{in}}{(1-d)} \tag{2.26}$$

$$V_{S2} = \frac{V_{in}}{(1-d)} \tag{2.27}$$

2.4.3.3 Diode Selection

The voltage stress on the diode is determined by:

$$V_D = \frac{2V_{in}}{(1-d)} \tag{2.28}$$

$$V_{Dout} = \frac{V_{in}}{(1-d)} \tag{2.29}$$

2.5 Simulation Results and Discussion

A PSIM simulation software is used to simulate and analyze the proposed converter. The system parameters and device selections are shown in Tables 2.2 and 2.3.

Table 2. 2 Specifications of system design

Inverter Parameter	**Value**
Input Voltage	80 V
Output Voltage	800 V
Output Current	2.5 A
Switching Frequency	100 kHz, 200 kHz, 300 kHz
Capacitor	30 µF
Inductor	1.5 mH

Table 2. 3 Component selection

Item	Reference	Rating	Part No.
Si MOSFET	S_1, S_2	650V	Si MOSFET TK35A65W5
Diode	D_1, D_2, D_3, D_4, D_o	650V, 39A, V_D=1.45V	C3D30065D
Inductor	L_1, L_2	1mH, DCR=5mΩ	195C30-ND
Capacitor	C_1, C_2, C_3, C_4, C_o	30μF, 850V	399-14246-ND

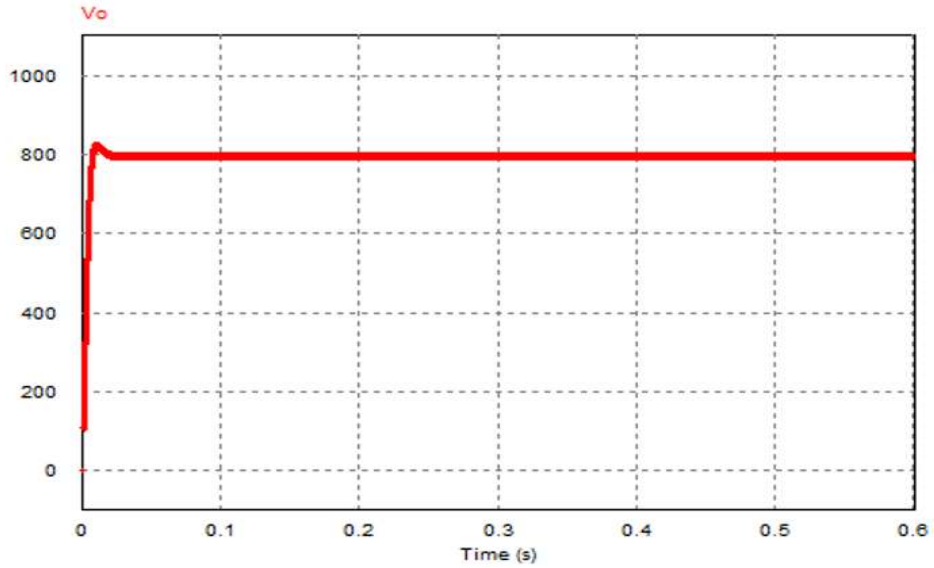


Figure 2. 11 The output voltage of the proposed converter [33]

Figure 2.11 presents the output voltage of the proposed converter, which succeeds in achieving a high gain ratio of 10 where the input voltage increased by a factor of ten. Conduction and switching losses of Si MOSFET at different switching frequencies and an output power load of 3 kW are presented in Figure 2.12.

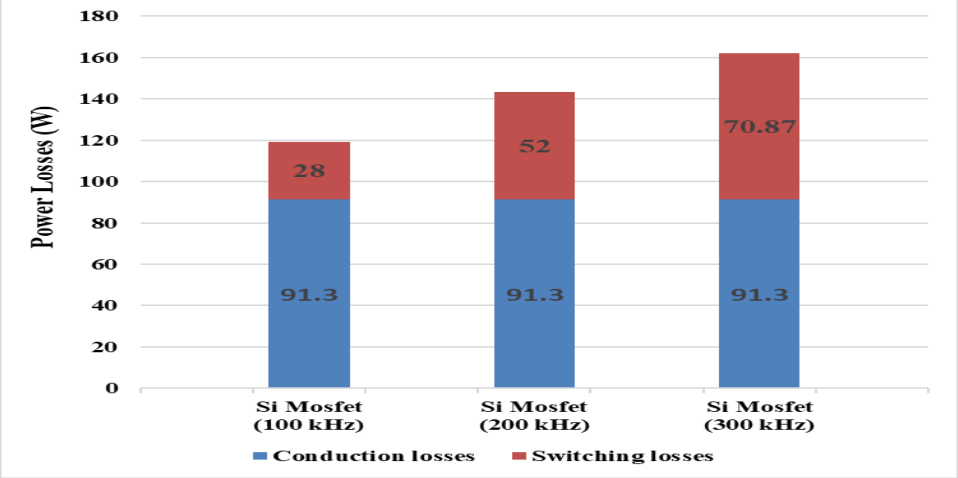


Figure 2. 12 Conduction and switching losses of Si and SiC MOSFET at different switching frequencies [33]

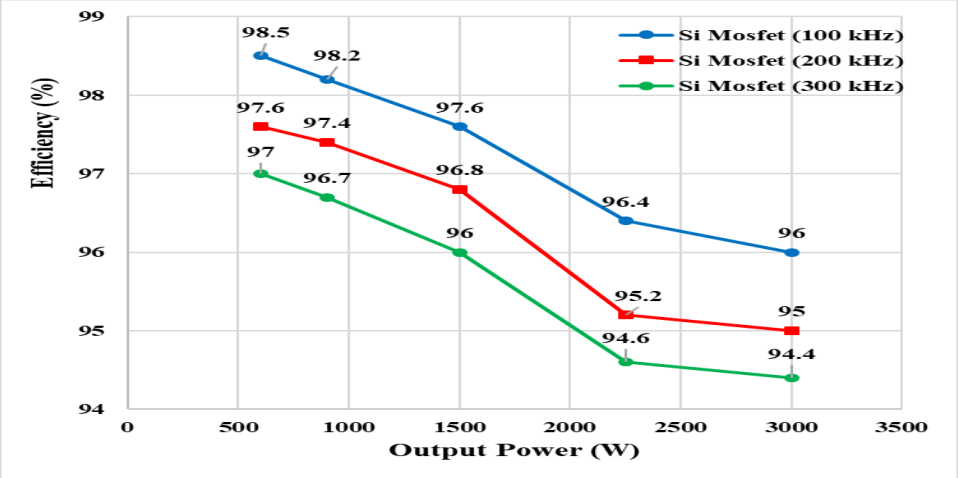


Figure 2. 13 Efficiency comparison of Si MOSFET at different switching frequencies with different output power loads [33]

Figure 2.13 demonstrates the efficiency of the system with different output power loads at different switching frequencies.

2.6 Conclusion

The PV structure and its integration configuration are explained in detail in this chapter. Also, the PV module was designed using the physical model simulator provided using the PSIM. A 3 kW PV array is designed using a combination of PV module

connected in parallel and series to achieve high voltage and high current. Moreover, a high gain boost converter is proposed for PV applications. The proposed converter is a combination of an interleaved structure and a voltage multiplier to obtain a high output gain. The proposed converter can achieve a high gain ratio of 10 with a duty cycle of fifty percent.

Chapter 3. Common-Mode Behavior

3.1 Introduction

PV systems have been broadly installed in domestic grid-connected such as low power residential sites [34]–[36]. Single and three-phase PV inverters are generally used in residential areas. These inverters can be implemented with or without line transformers. Using an inverter without a transformer (transformerless inverter) has the advantage of high power density, high efficiency, and lower cost because of the absence of galvanic isolation. Therefore, for low power and low-cost PV application to be used in the residential sector, transformerless inverters become the best option due to their benefits.

On the other hand, there are some drawbacks to transformerless inverters because a direct connection is established between the PV arrays and the grid. As a result, a resonant circuit is formed that includes PV stray capacitors, grid impedance, and output filter inductances as shown in Figure 3.1. When operating at high switching frequency, the stray capacitors will be charged and discharged by the common mode voltage (V_{CM}). Therefore, the resonant circuit will be excited and the leakage current will flow through the parasitic capacitances between the PV panel and the ground [37]–[42]. There are many disadvantages associated with the circulating of leakage current in the system, such as increased system losses, total harmonic distortion (THD), and serious safety and radiated interference problems [43].

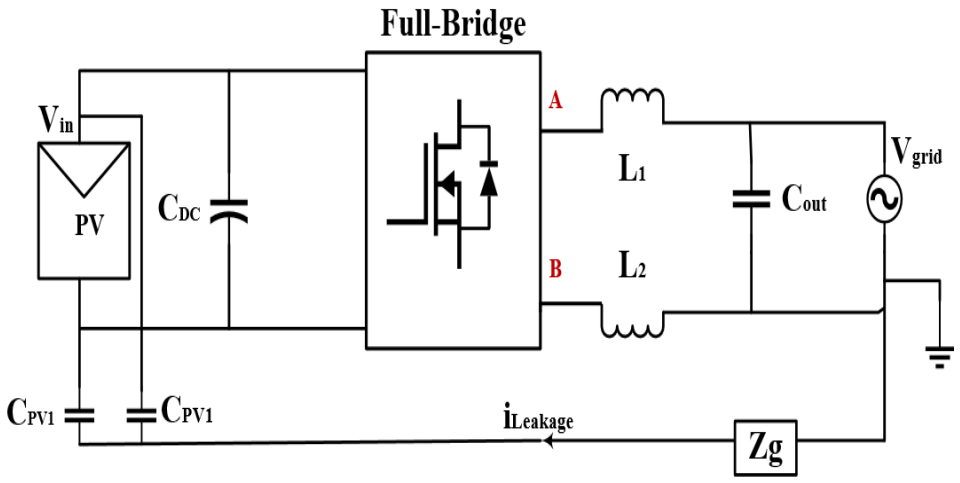


Figure 3. 1 Current leakage path in resonant circuit

Accordingly, the value of the leakage current must be minimized and restricted to an acceptable range [44]. The leakage current must be eliminated or minimized to a small value that does not affect the system. Therefore, to achieve a small value of leakage current, the common mode voltage must have a constant value or be varied at a low switching frequency (grid frequency) of 50Hz or 60Hz. In order to achieve this goal, traditional half bridge or full bridge inverters are employed and bipolar sinusoidal pulse width modulation (SPWM) is adopted [45], [46]. On the other hand, a half-bridge inverter utilizes half the DC voltage compared to the full-bridge inverter. For these purposes, high input DC voltage is required, which can be achieved by using a large number of PV panels connected in series or by using a high gain DC-DC converter placed between the PV panels and the inverter. As a result, using a half-bridge inverter leads to increased system cost and degrades system efficiency. Moreover, bipolar SPWM is a two-level modulation technique, meaning the voltage stress on the filter inductor is doubled. As a result, the efficiency of the system is decreased due to the high-power losses and high current ripples. This necessitates larger inductors, which in turn leads to

high cost and larger sized PV systems. Accordingly, numerous transformerless inverter topologies have been proposed as they have the benefits of low leakage current and high efficiency. Most proposed topologies are designed to provide galvanic isolation by disconnecting the AC or DC sides of the inverter during the freewheeling modes. Many topologies have been derived and developed based on this method, such as the highly efficient and reliable inverter concept (HERIC) [47], the H5 inverter [48], and the H6 topology [49].

3.2 Common Mode Model

The resonant circuit for a transformerless inverter is described previously in Figure 3.1. The major components of the resonant circuit are an inductor filter (L_1 and L_2), the parasitic capacitance (C_{PV}), the leakage current (I_L), and a power converter that can be represented by a number of different topologies. The positive and negative terminals are represented by P and N on the DC side respectively. On the AC side, the output of the power converter is represented by two terminals A and B that are attached to the AC single phase grid by the inductor filter. An equivalent circuit can be created from Figure 3.1, where the power converter can be represented by two voltage sources -- V_{AN} and V_{BN} as shown in Figure 3.2. Additionally, leakage current is a function of parasitic capacitance, inductor filters, V_{AN}, V_{BN}, and grid voltage.

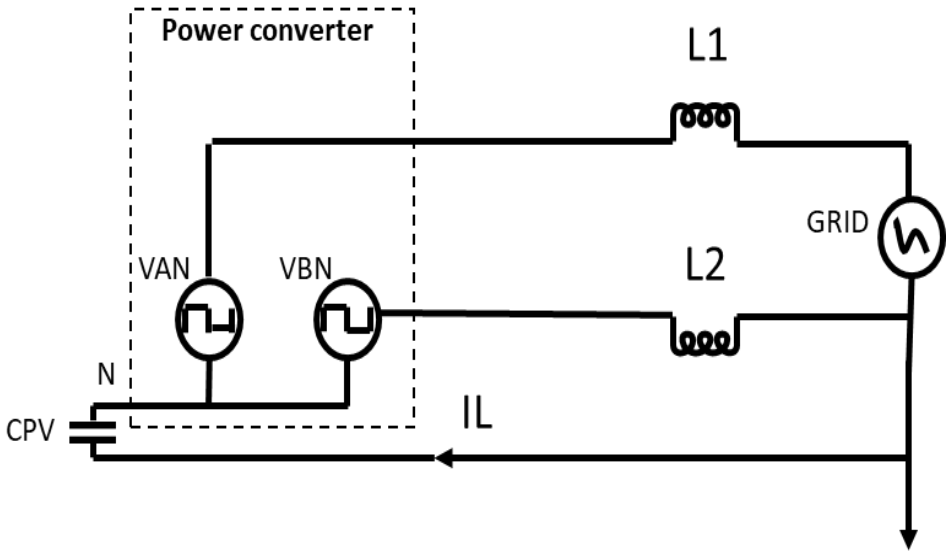


Figure 3. 2 Simplified path of leakage current in single phase inverter

The leakage current can be ignored at low switching frequencies. On the AC side, the grid frequency is low (50 to 60 Hz), so the common mode model will be ignored on this side. Therefore, the equivalent circuit can be simplified as shown in Figure 3.3, where V_{CM} and V_{DM} are represented by a combination of V_{AN} and V_{BN}. The common mode voltage (V_{CM}) and differential mode voltage (V_{DM}) are expressed as:

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} \tag{3.1}$$

$$V_{DM} = V_{AN} - V_{BN} \tag{3.2}$$

In Equations (3.1) and (3.2), V_{AN} and V_{BN} are expressed in terms of V_{CM} and V_{DM} as follows:

$$V_{AN} = V_{CM} + \frac{V_{DM}}{2} \tag{3.3}$$

$$V_{BN} = V_{CM} - \frac{V_{DM}}{2} \tag{3.4}$$

The common mode model can be simplified as shown in Figure 3.4 and the equivalent common mode voltage is given as:

$$V_{ECM} = V_{CM} + \frac{V_{DM}}{2}\left(\frac{L_2 - L_1}{L_1 + L_2}\right) \tag{3.5}$$

To prevent the impact of V_{DM}, the values of the filter inductors are set to be equal. As a result, the V_{ECM} will be equal to the V_{CM}, as expressed here:

$$V_{ECM} = V_{CM} = \frac{V_{AN} + V_{BN}}{2} \tag{3.6}$$

From the previous analysis, it is clear that the leakage current is extremely dependent upon the common mode voltage.

If the V_{CM} is fluctuating at high switching frequency, the parasitic capacitance will be charged and discharged, this will cause a generation of high leakage current. Therefore, a constant V_{CM} must be maintained to eliminate or minimize the value of the leakage current. To achieve a constant V_{CM}, the inverter structure and modulation techniques must be considered.

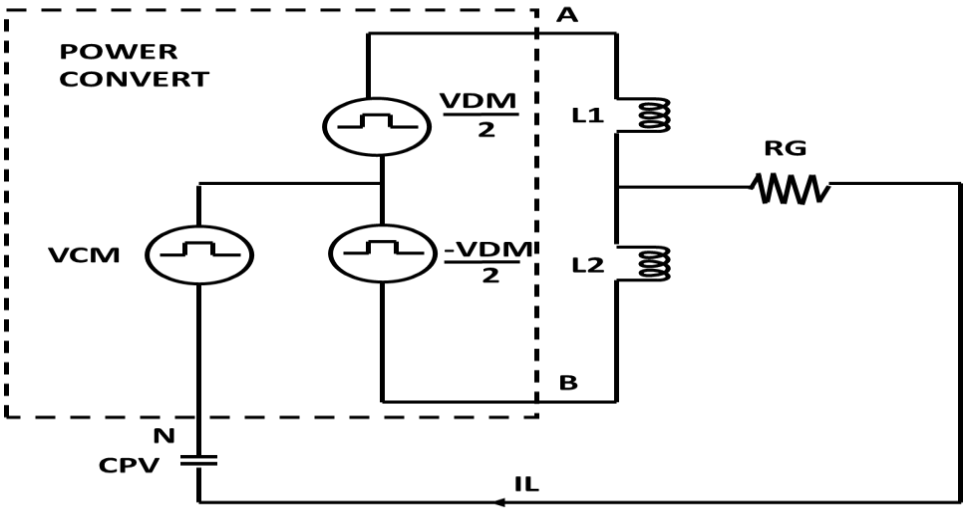


Figure 3. 3 The second simplified circuit of leakage current path

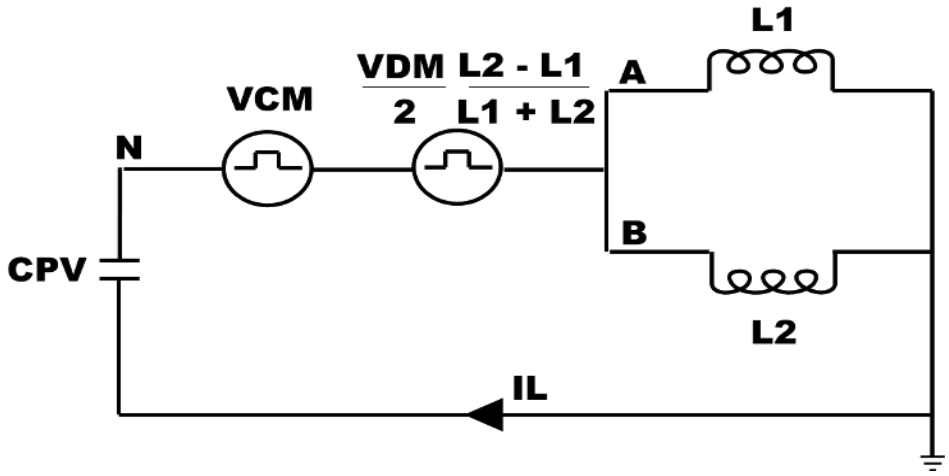


Figure 3. 4 The third and final simplified resonant circuit of leakage current path

3.3 Methods of Leakage Current Reduction

3.3.1 Galvanic Isolation

The greatest problem with transformerless inverters is that a galvanic connection is established that allows the flow of the leakage current between the PV arrays and the grid. Two methods can be applied to create galvanic isolation between the PV arrays and the grid: AC decoupling and DC decoupling. In DC decoupling methods, the disconnection between the PV and the grid during the freewheeling period is performed by attaching one or more bypass DC switches or diodes to the inverted DC side. Figure 3.5 presents the decoupling structure of both DC and AC techniques. Additionally, the number of conducting switches is increased when applying the DC decoupling method because it is inserted on the conduction route. Therefore, the total conduction loss is increased and the efficiency of the system is degraded by the DC decoupling method. On the other hand, when the AC decoupling method is applied on the AC side of the inverter and it can create galvanic isolation without affecting the total number of conducting

switches. As a result, higher efficiency can be achieved with the AC decoupling method in comparison to the DC decoupling method.

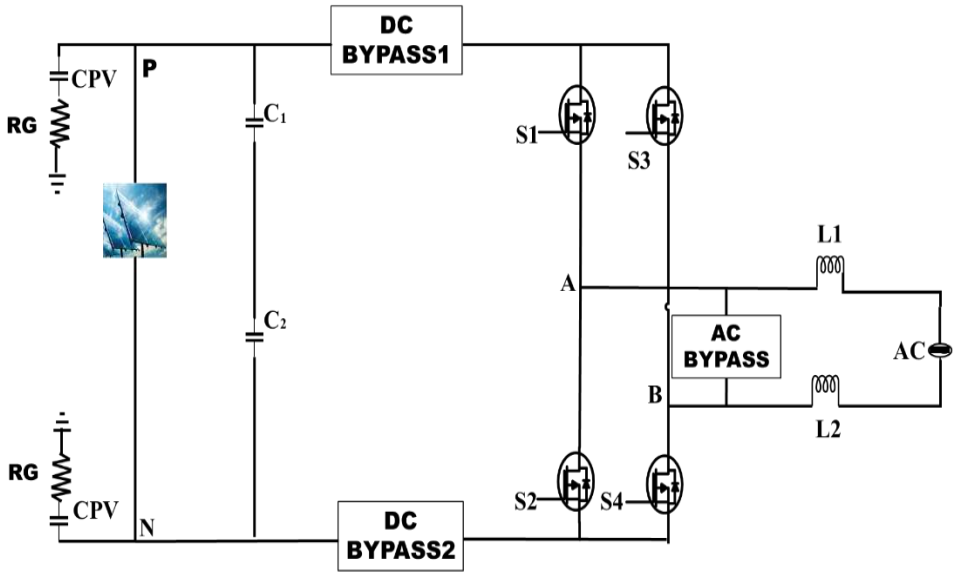


Figure 3. 5 Circuit structure of galvanic isolation with DC and AC decoupling method

The main issue with applying these methods for galvanic isolation is that it is impossible to control the V_{CM} during the freewheeling period using pulse width modulation. The active state of the positive half cycle of an inverter topology with DC decoupling is shown in Figure 3.6. In this mode, three switches are conducted -- the DC bypass switch, the S_1, and the S_4 -- to create the desired output voltage. The common mode voltage during this mode is given as:

$$V_{AN} = V_{DC} \tag{3.7}$$

$$V_{BN} = 0 \tag{1}$$

$$V_{CM} = \frac{1}{2}(V_{DC} + 0) = \frac{V_{DC}}{2} \tag{3.9}$$

The freewheeling mode during the positive half cycle is shown in Figure 3.7. In this mode, the DC link is disconnected from the grid to create galvanic isolation. It

should be noted that the terminal voltages V_A and V_B are detached from the DC link. Therefore, the terminal voltages are floating in regard to the DC link which means that the V_{CM} cannot be determined by the switching states. The value of the V_{CM} in this mode is fluctuating with amplitude and it depends on the parasitic capacitance and junction capacitances of the switches. As a result, the $V_{C'M}$ cannot be maintained at a constant during all the operation modes meaning that a considerable amount of leakage current can flow during the freewheeling period. The same situation can be found with the AC decoupling method. Therefore, it can be concluded that galvanic isolation technique is not sufficient to eliminate leakage current.

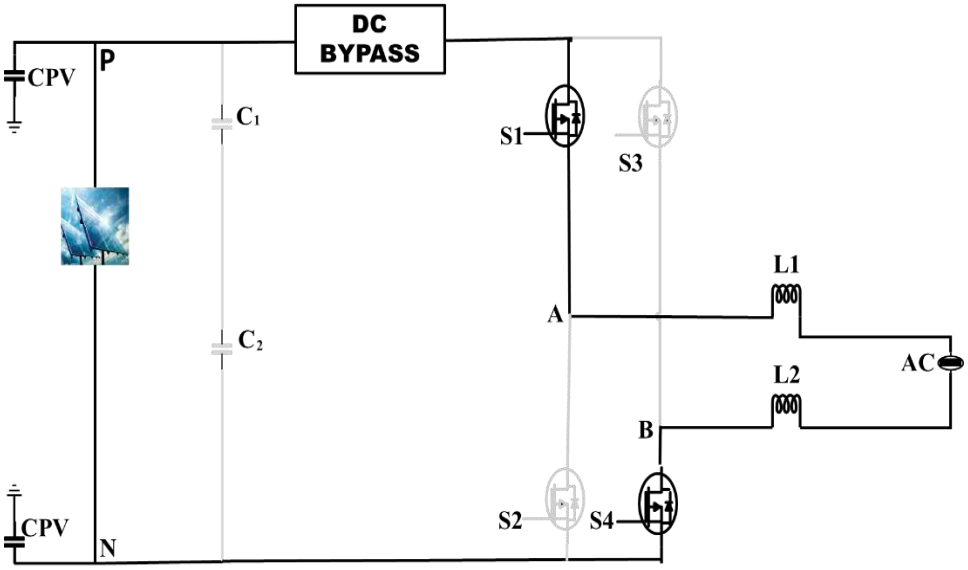


Figure 3. 6 Conduction mode during positive active state with DC decoupling

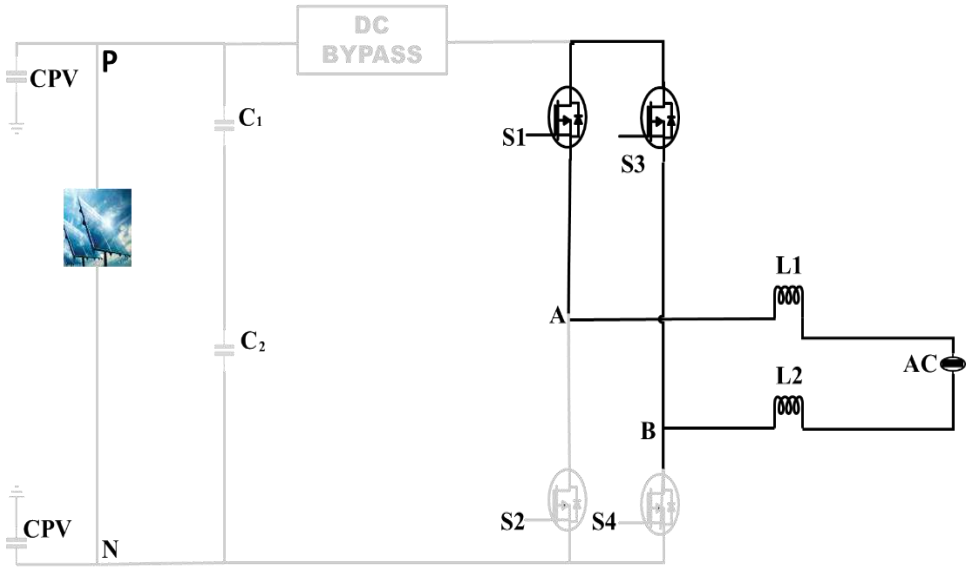


Figure 3. 7 Freewheeling mode with DC decoupling

3.3.2 CMV Clamping

A successful transformerless inverter topology must completely eliminate the leakage current. In the previous galvanic isolation technique, the V_{CM} during the freewheeling mode cannot be controlled by PWM because of parasitic elements in the circuit. Therefore, the value of the V_{CM} must be maintained as a constant to achieve zero (or minimal) leakage current. As a result, a clamping branch technique is proposed [50] to meet the requirement of eliminating the leakage current as shown in Figure 3.8. In this method, the clamping branch is represented with switches or diodes that clamp the output voltage during the freewheeling mode to halve the input voltage by using a capacitor divider. Thus, a suitable transformerless topology must consider combining the galvanic isolation method and the clamping method to satisfy the requirement of designing a transformerless inverter free of leakage current.

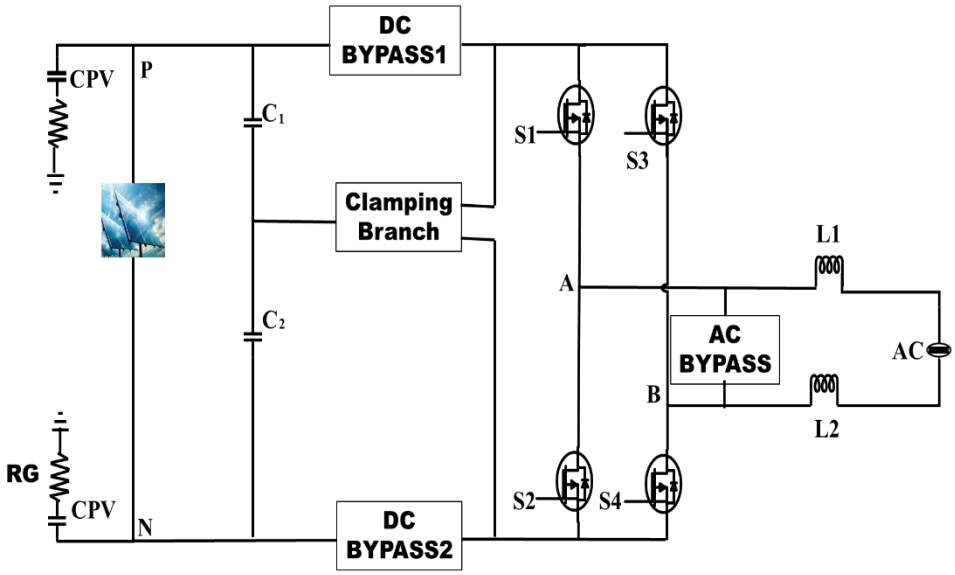


Figure 3. 8 Circuit structure with clamping method

An example of combining both techniques is shown in Figure 3.9. This figure shows the active mode during the positive half cycle. In this mode, S_1 and S_4 are conducting to produce the desired output voltage; the V_{CM} during this mode is given as:

$$V_{AN} = V_{DC} \tag{3.10}$$

$$V_{BN} = 0 \tag{3.11}$$

$$V_{CM} = \frac{1}{2}(V_{DC} + 0) = \frac{V_{DC}}{2} \tag{3.12}$$

In the freewheeling mode, the DC bypass switch disconnects the DC link from the grid. The freewheeling mode during the positive half cycle is shown in Figure 3.10. In this mode, the galvanic isolation is obtained by disconnecting the DC link from the grid using the DC bypass switch. Also, the terminal voltages A and B are clamped to halve the input voltage by turning ON the clamping branch (switches or diodes). The V_{CM} can be found as:

$$V_{AN} = \frac{V_{DC}}{2} \tag{3.13}$$

$$V_{BN} = \frac{V_{DC}}{2} \tag{3.14}$$

$$V_{CM} = \frac{1}{2}\left(\frac{V_{DC}}{2} + \frac{V_{DC}}{2}\right) = \frac{V_{DC}}{2} \tag{3.15}$$

Therefore, the problem of achieving a constant V_{CM} during the freewheeling mode is solved by using the clamping branch so that the leakage current can be successfully eliminated.

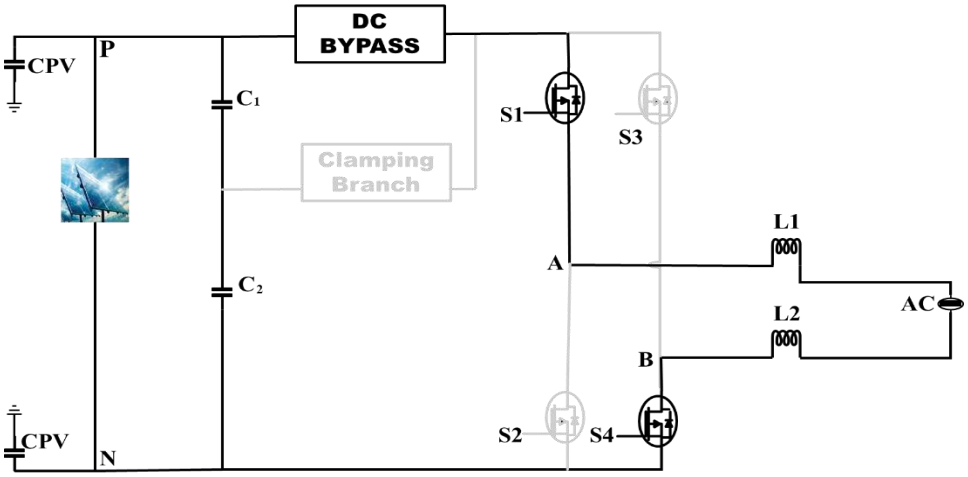


Figure 3. 9 Conduction mode during the positive active state with clamping method

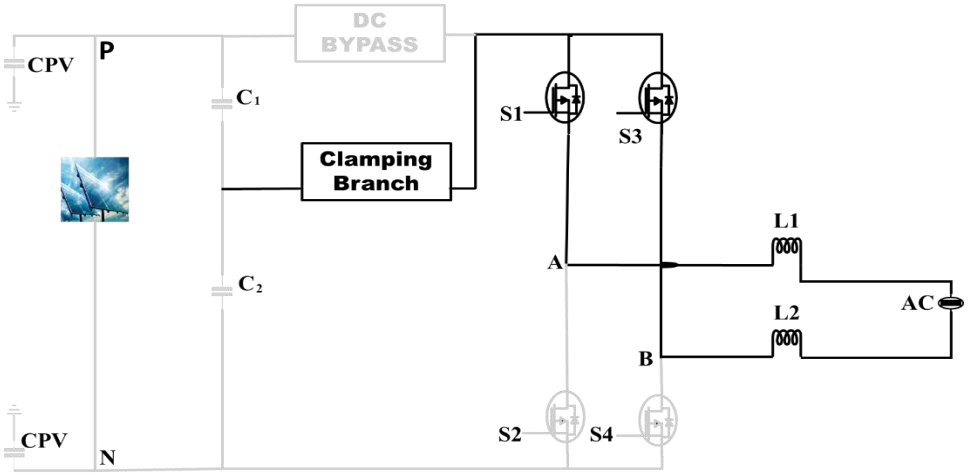


Figure 3. 10 Freewheeling mode with clamping method

3.4 Conclusion

This chapter presented a common mode model for an H-bridge inverter to solve the issue of leakage current generation. It is noted that to eliminate leakage current generation, the common mode voltage must be kept at a constant over the whole period. The literature proposes two methods to address this need. The first of these is galvanic isolation, where the DC side is disconnected from the AC side during the freewheeling period by inserting an extra switch on either the DC side or the AC side of the full bridge inverter. However, it was noted that the common mode voltage fluctuates during the freewheeling period and is not constant. As a result, leakage current generation is not eliminated. Conversely, this issue is addressed through the use of the clamping method, where the common mode voltage during the freewheeling period is clamped to the middle of the DC voltage.

Chapter 4. Review and Comparison of Single Phase Transformerless PV Inverter Topologies

4.1 Transformerless Inverter Based on Full Bridge Topology

Transformerless inverters can be constructed on full bridge or half bridge topologies. This section will discuss transformerless inverters based on full bridge topology. Inverters based full bridge topology are widely used in a number of different applications due to its simplicity and low cost.

4.1.1 Full-Bridge Topology

Four switches are used to form the structure of the full bridge topology presented in Figure 4.1. Two conventional modulation techniques – unipolar and bipolar - are generally used. The switching strategy of full bridge topology for the bipolar and unipolar SPWM modulation techniques is shown in Figure 4.2. Full bridge topology with bipolar modulation technique has two operational modes. In mode I, two switches are conducting during the positive half cycle: the S_1 and S_4. In mode II, S_2 and S_3 are conducting simultaneously during the negative half cycle. The simulated waveforms of common mode characteristics (CM) are shown in Figure 4.3. Full bridge topology with bipolar modulation technique can be used in transformerless inverters so constant common mode voltage and low leakage current are achieved. This modulation technique is known as a two-level modulation technique because two output voltages are generated, positive and negative V_{DC}. As a result, the voltage stress on the inductor filter is doubled

(twice the input voltage), leading to high current ripple and loss and high switching loss. These issues reduce the total efficiency of the system.

There are four possible modes with the unipolar modulation technique; this switching strategy is shown in Figure 4.4. In mode I, S_1 and S_4 are conducting to deliver the desired positive output voltage during the positive grid voltage. In mode II, the current freewheels through S_1 and the anti-parallel diode of S_3. In mode III, S_2 and S_3 are conducting to deliver the negative output voltage during the negative half-cycle. In mode IV, the current freewheels through S_3 and the anti-parallel diode of S_1. Three voltage levels are generated in unipolar modulation method $+V_{DC}$, 0, and $-V_{DC}$ across the inductor filters, which leads to lower core loss. The CM characteristics of a full bridge inverter with unipolar modulation method are presented in Figure 4.5. With this method, high leakage current is generated due to high frequency V_{CM}. The high frequency V_{CM} fluctuation occurs because there is no galvanic isolation between the PV arrays and the grid as one of the PV terminals is attached to the AC side during the freewheeling modes. As a result, the full bridge inverter with unipolar modulation method cannot be used in a transformerless inverter.

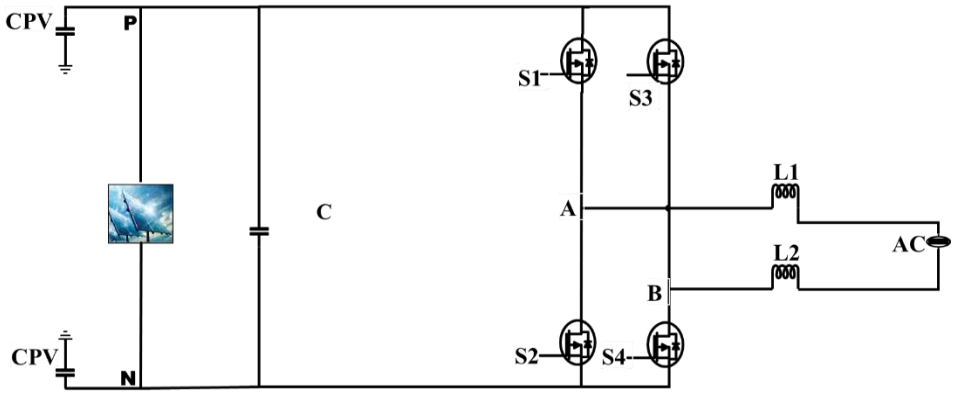


Figure 4. 1 Circuit diagram of full bridge topology

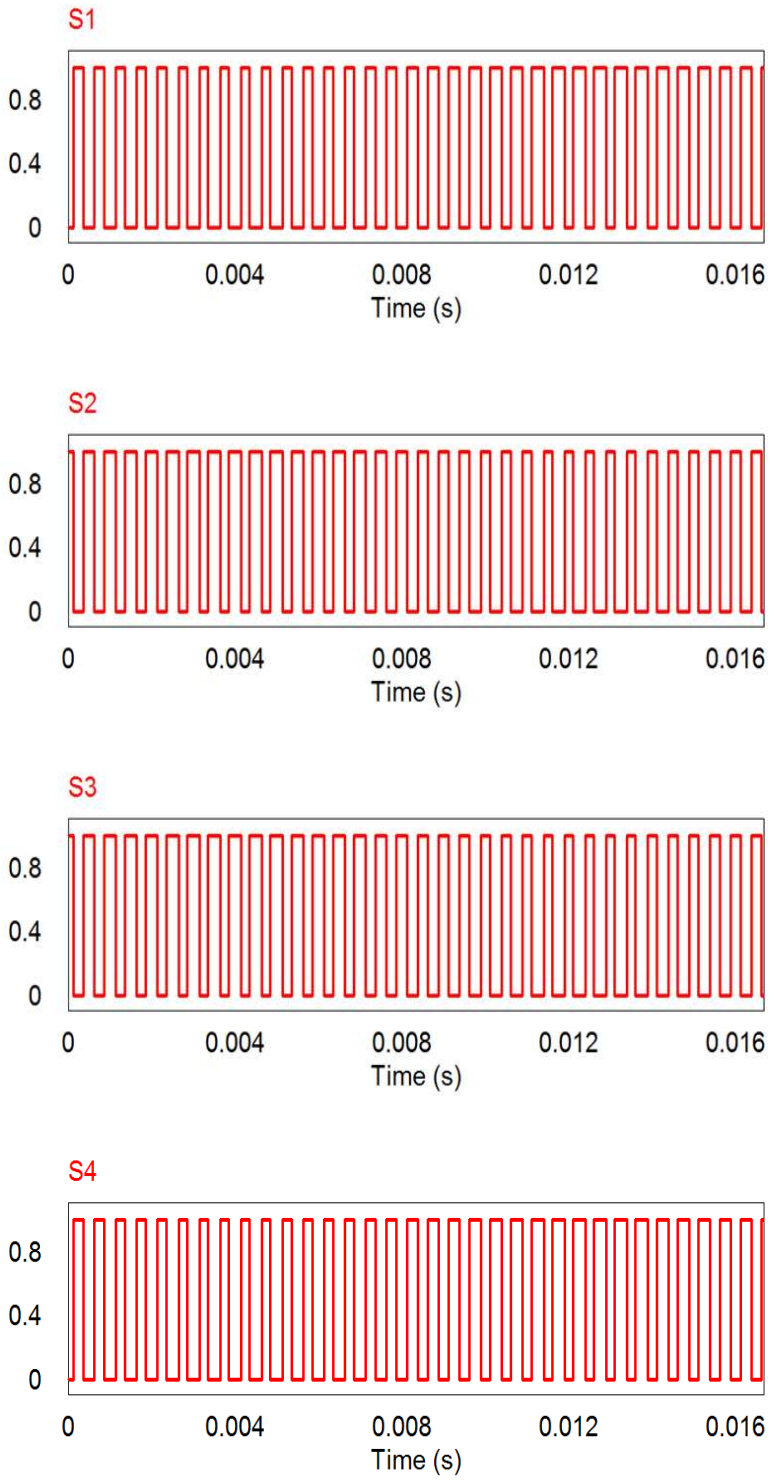


Figure 4. 2 Bipolar modulation strategy of H4 topology

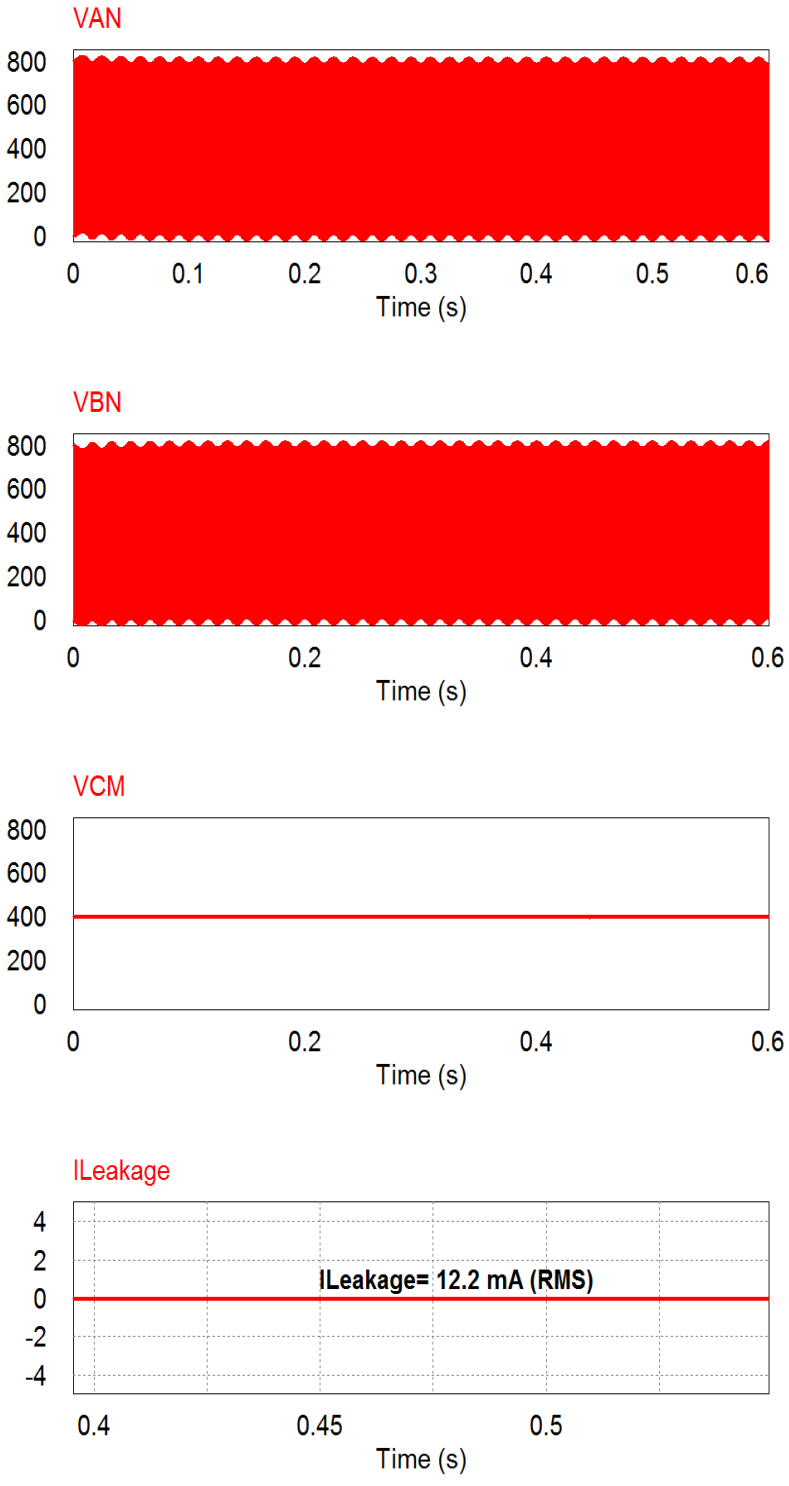


Figure 4. 3 Common mode characteristics of H4 topology with bipolar modulation

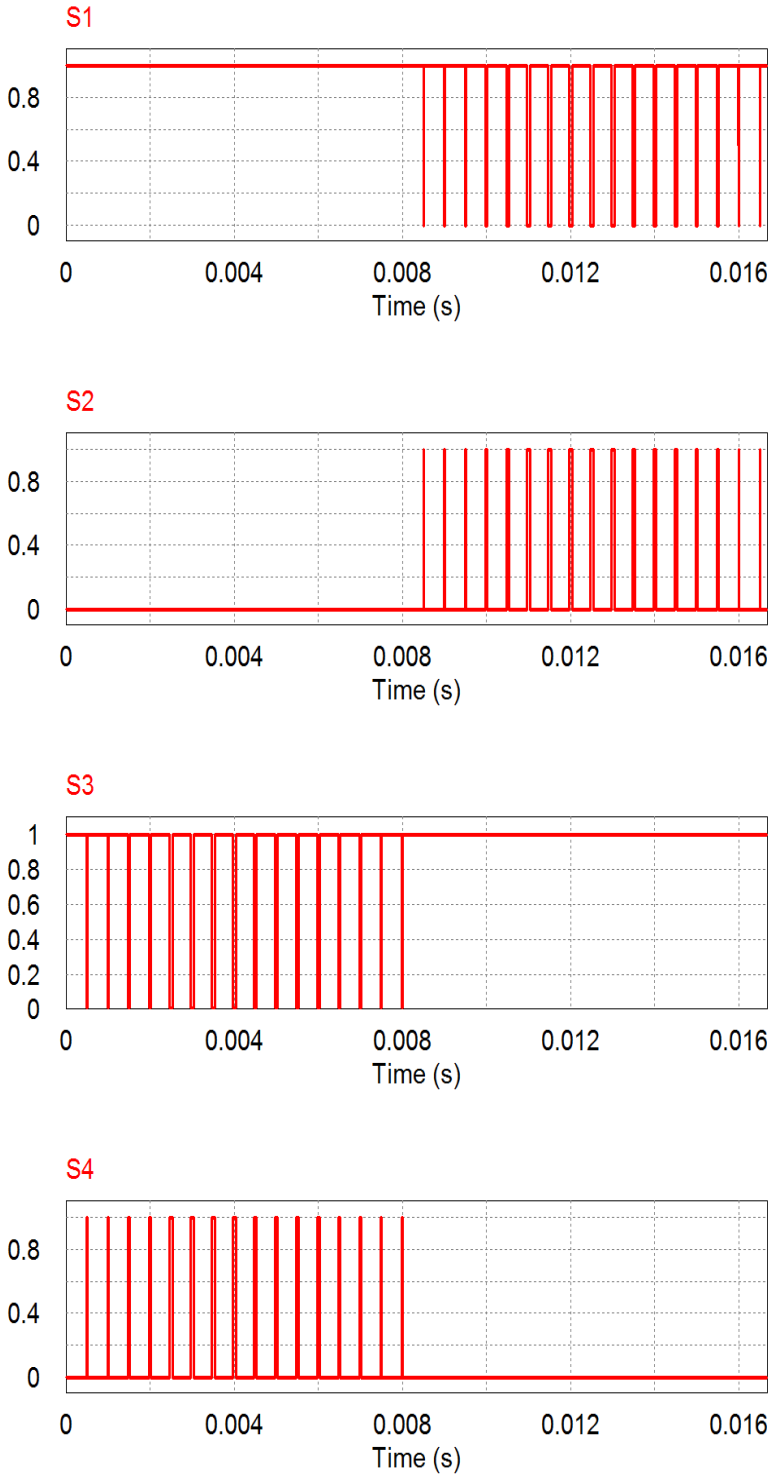


Figure 4. 4 Unipolar modulation strategy of H4 topology

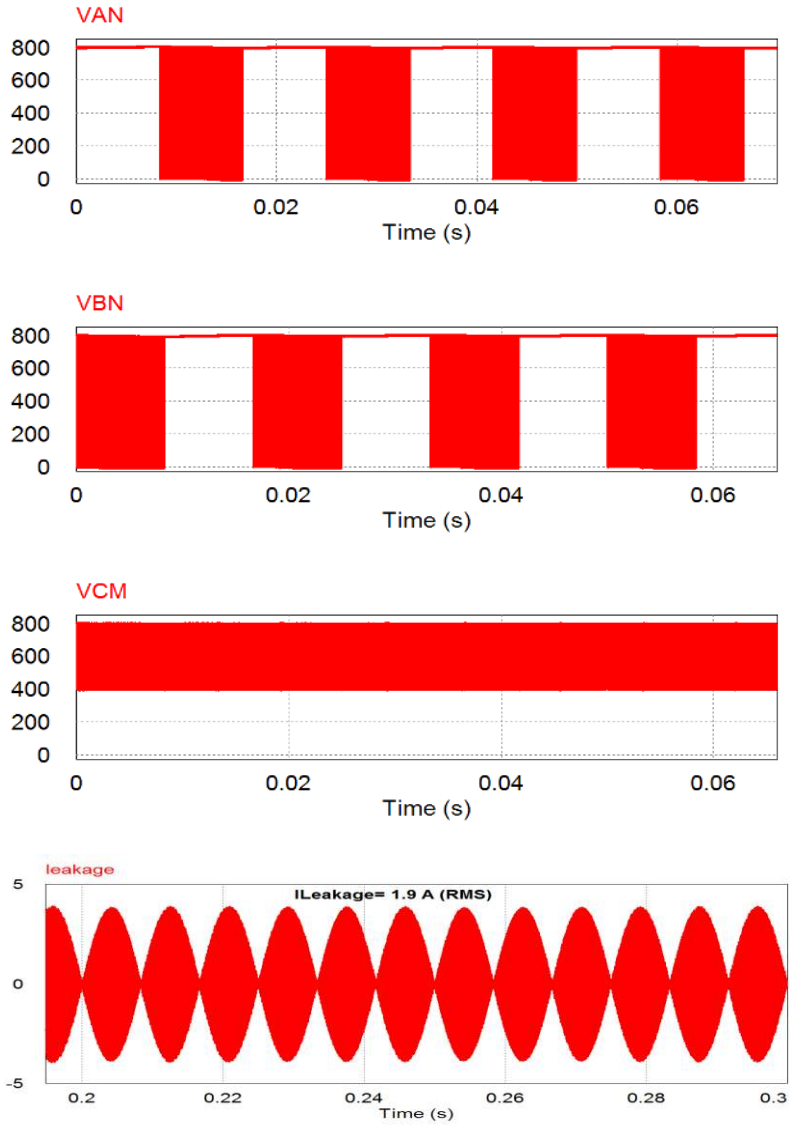


Figure 4. 5 Common mode characteristics of H4 topology

4.1.2 H5 Topology

H5 topology is derived from full bridge topology and consists of five switches [51]. In H5 topology, an additional switch (S_5) is used as a DC bypass switch for the purpose of galvanic isolation as shown in Figure 4.6. Two switches, S_1 and S_3, are used during the freewheeling period and are operated at the fundamental frequency (grid

frequency). There are four possible modes of H5 topology. In mode I, three switches (S_1, S_4 and S_5) are conducting during the positive half cycle. Mode II is the freewheeling mode during the positive half cycle where the current flows through S_1 and the anti-parallel diode of S_3. In mode III, S_2, S_3, and S_5 are conducting during the negative half cycle. Mode IV is the freewheeling mode during the negative half cycle where current flows through S_3 and the anti-parallel diode of S_1. A unipolar modulation technique is used meaning that three voltage levels are generated -- positive, negative, and zero -- as presented in Figure 4.7. Therefore, small current ripple and high efficiency are achieved compared to those of bipolar modulation. The CM characteristics of H5 topology are presented in Figure 4.8. It is observed that high fluctuation with a magnitude of up to 400 V occurred with V_{CM}. As a result, the V_{CM} is charging and discharging the stray capacitances which will lead to a flow of leakage current. The amount of leakage current is low, but it is not eliminated.

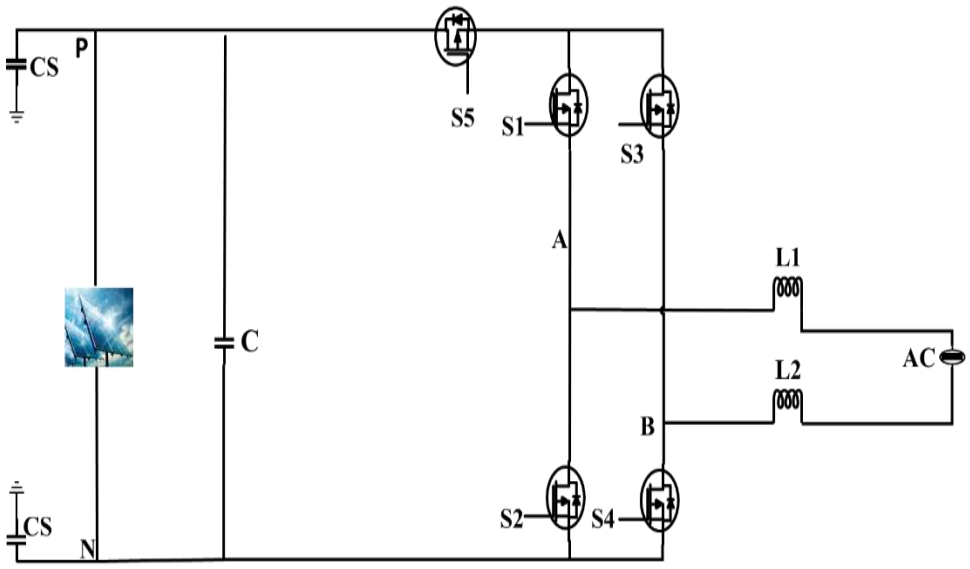


Figure 4. 6 Circuit structure of H5 topology

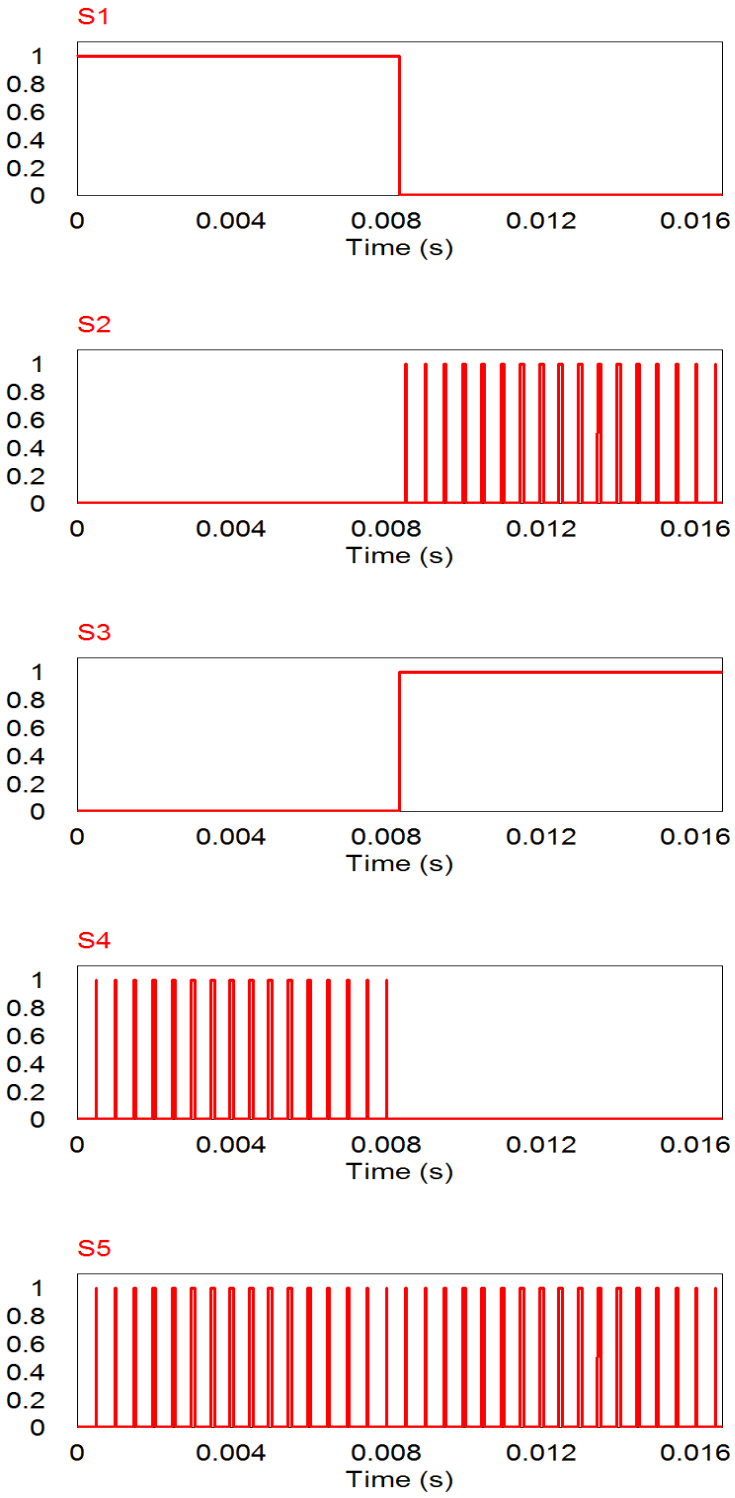


Figure 4. 7 Switching waveform of H5 topology

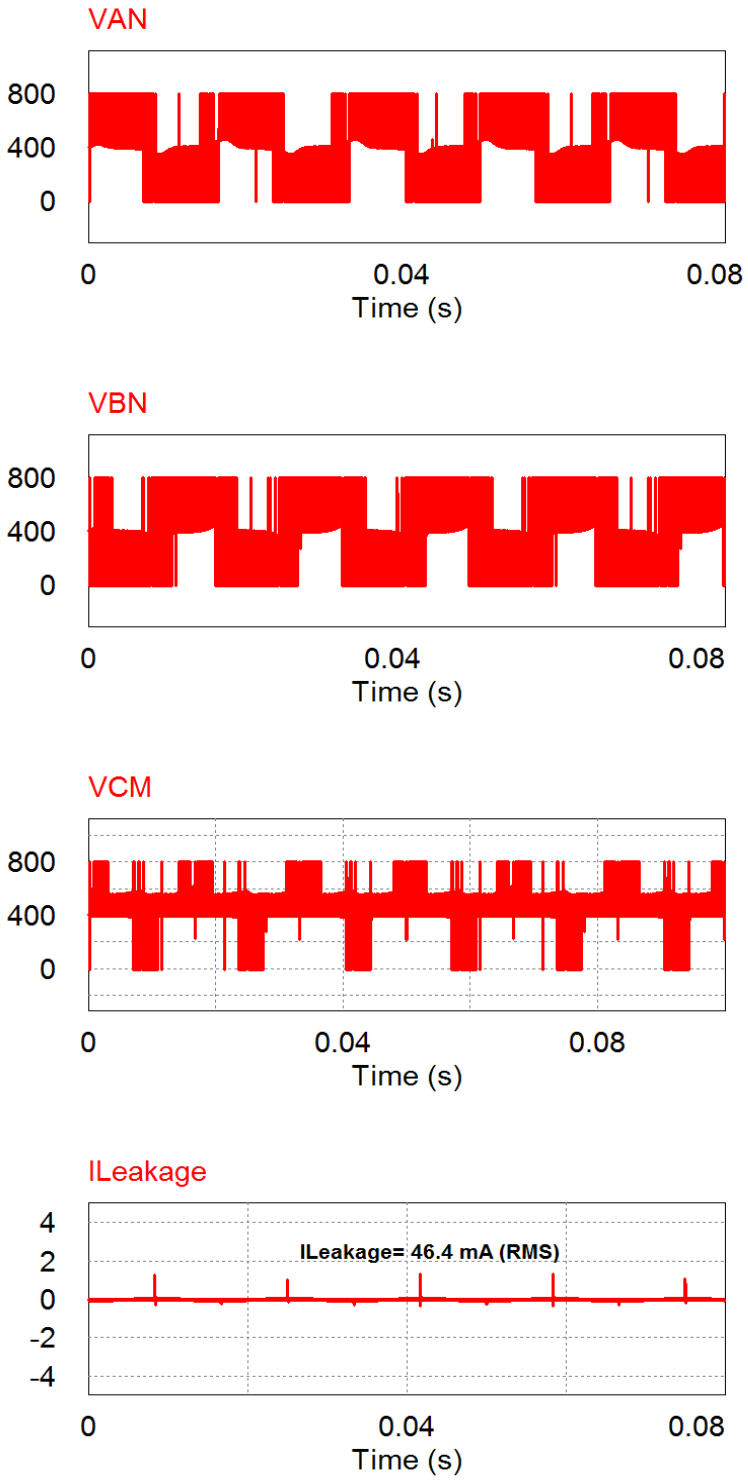


Figure 4. 8 Common mode characteristics of H5 topology

4.1.3 H6 Topology

H6 topology is proposed in [44] and is derived from H5 topology by inserting an additional active switch in the negative bus of the DC kink, as shown in Figure 4.9. There are then six switches forming the structure of the H6 topology that are controlled independently. A unipolar SPWM modulation technique is used, Figure 4.10 shows the driving signals. There are four possible operating modes. In mode I, there are four switches conducting during the positive half cycle, which are S_1, S_4, S_5, and S_6. Two switches (S_1, S_6) are switched at the fundamental frequency and the other two switches (S_4, S_5) are switched at high switching frequency. Mode II is the freewheeling mode in the positive half cycle where current flows through S_1 and the anti-parallel diode of S_3. In mode III, four switches (S_2, S_3, S_5, and S_6) are conducting during the negative half period. In this mode, S_2 and S_5 are switched at the fundamental frequency; S_3 and S_6 are switched at high frequency. Mode IV is the freewheeling mode during the negative half period where the current flows through S_3 and the antiparallel diode of S_1. The inverter output voltage, common mode voltage V_{CM}, and leakage current are presented in Figure 4.11.

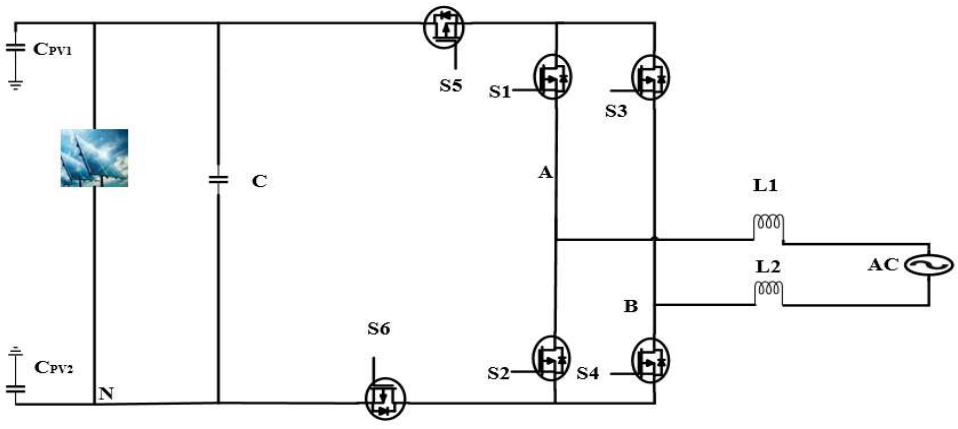


Figure 4. 9 Circuit diagram of H6 topology

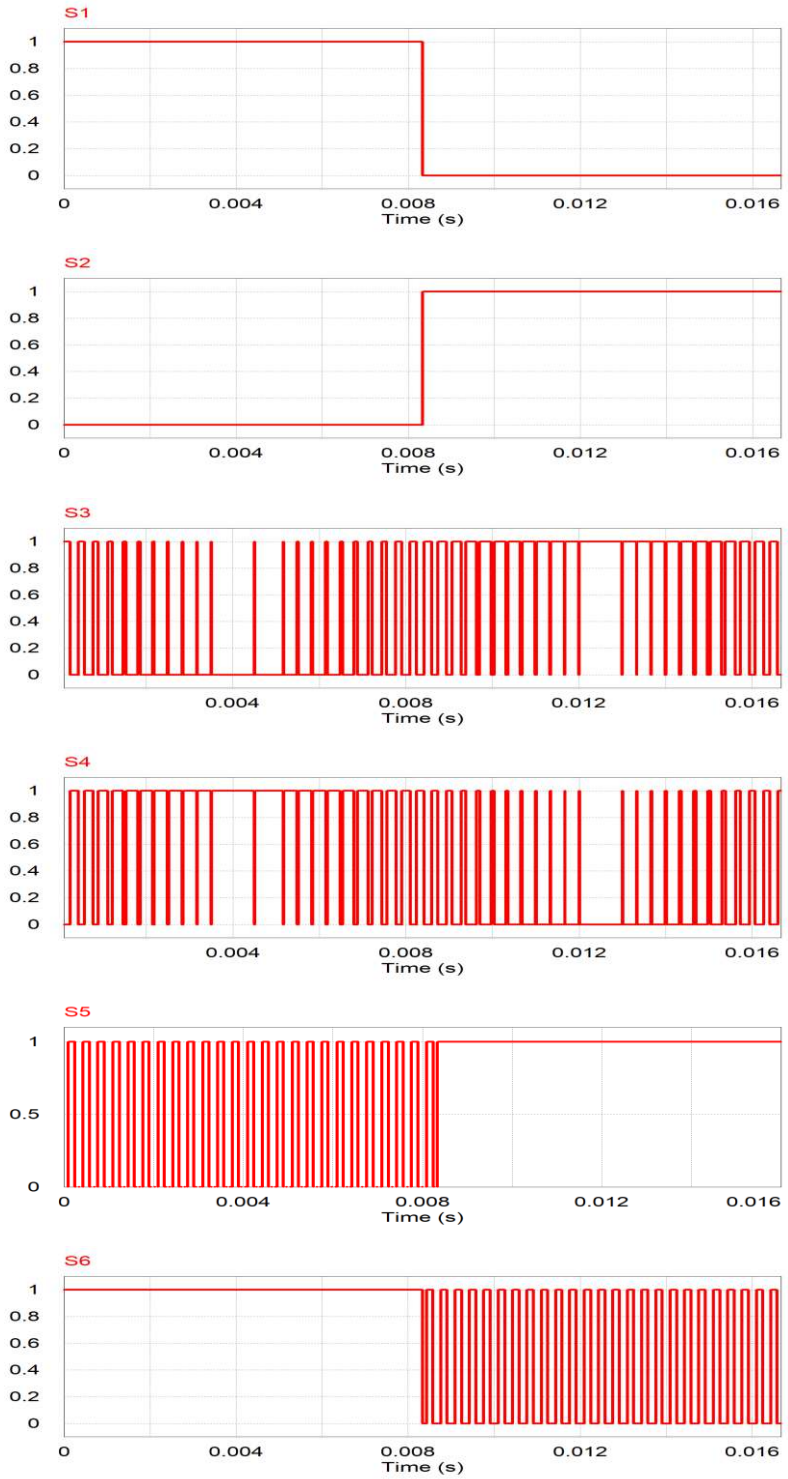


Figure 4. 10 Modulation strategy of H6 topology

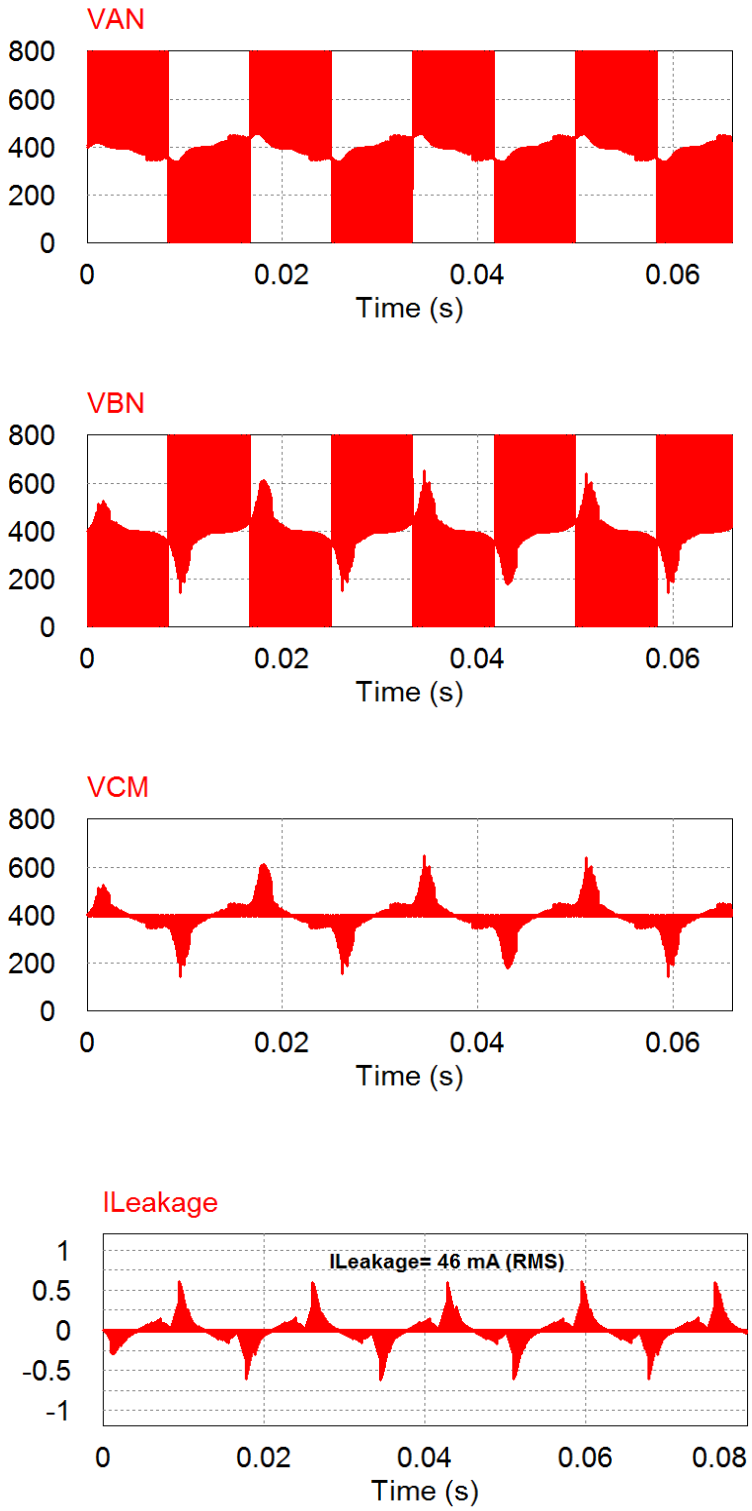


Figure 4. 11 Common mode characteristics of H6 topology

4.1.4 H6-I Topology

The H6-I topology is proposed in [49] and its structure and PWM strategy are presented in Figures 4.12 and 4.13. There are four possible operating modes. During the positive active state, S_1, S_5, and S_4 are conducting the positive output voltage. In the negative active state, switches S_3, S_6, and S_2 are conducting the negative voltage to the output. Thus, a total of six switches are conducting in the active states. In the freewheeling mode, the DC source is disconnected from the grid and the current passes through only S_5 and D_1 to achieve zero output voltage in the positive zero state. In the negative zero state, the current path is established by S_6 and D2 to obtain zero output voltage. The CM characteristics of the H6-I topology are shown in Figure 4.14. It should be noted that H6-I topology has the same levels of leakage current and common mode voltage as those of H5 and H6.

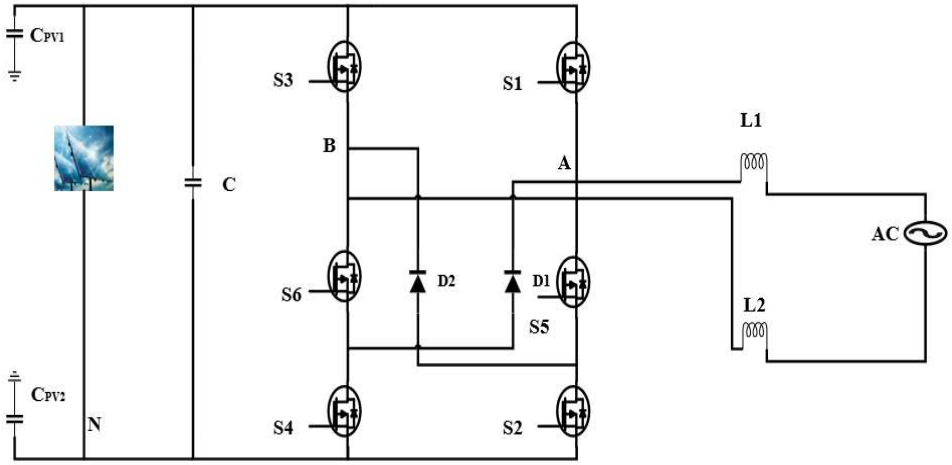


Figure 4. 12 Circuit structure of H6-I topology

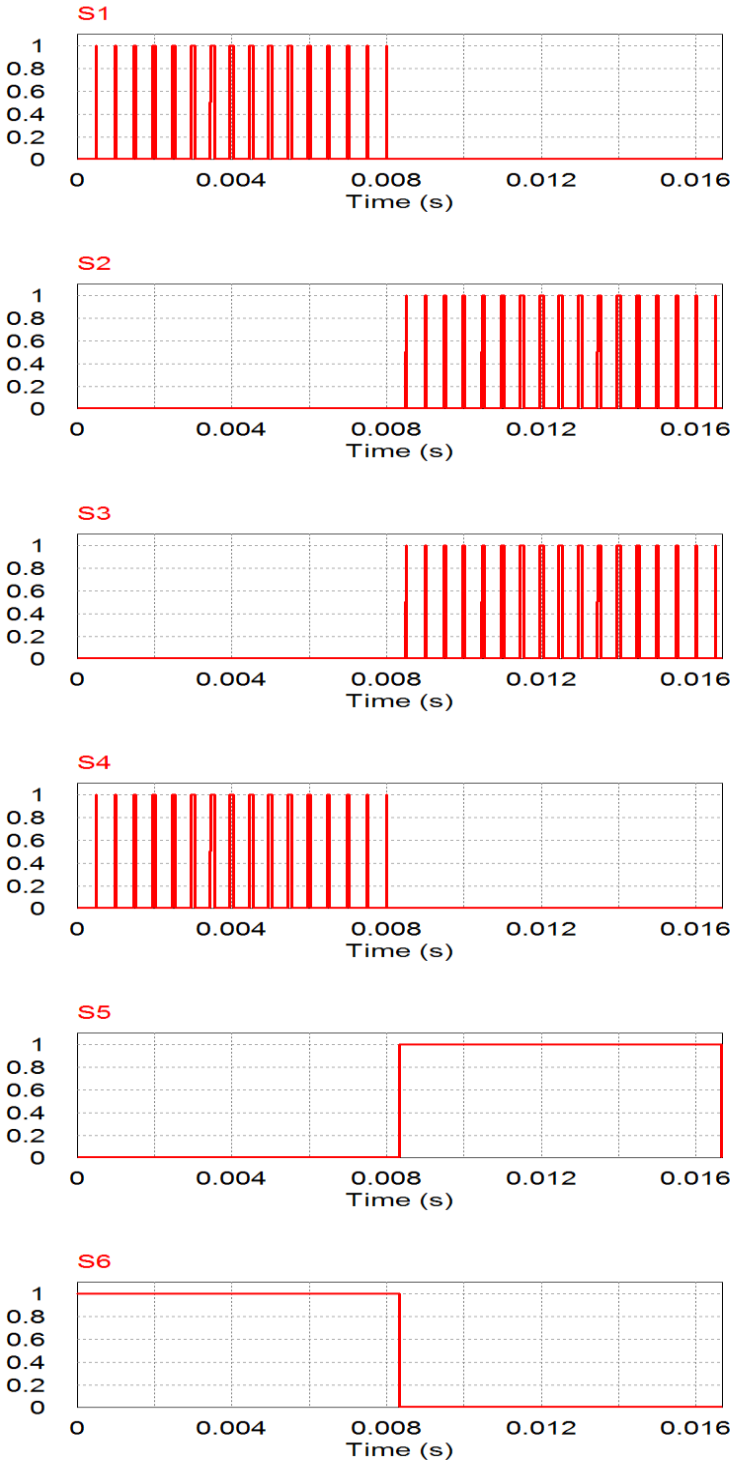


Figure 4. 13 Switching waveforms of H6-I topology

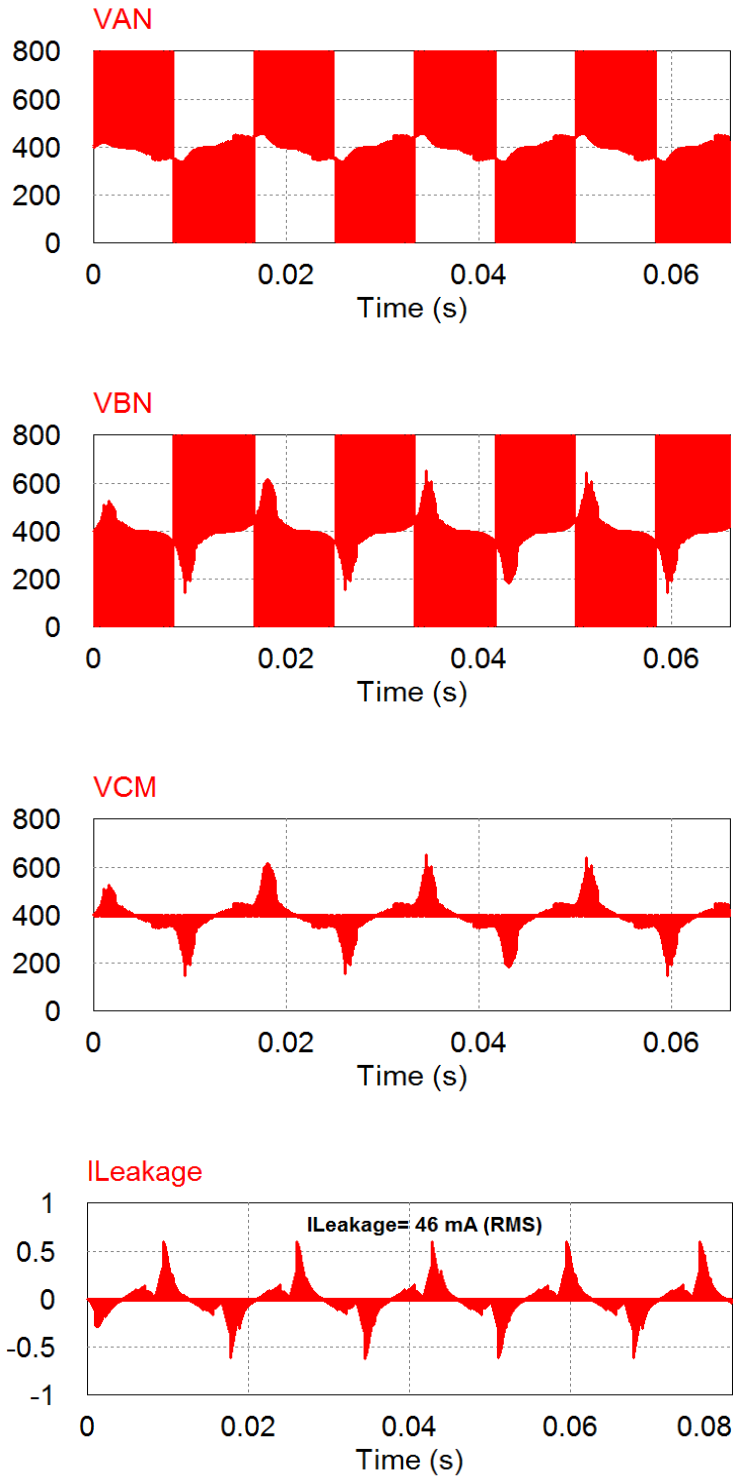


Figure 4. 14 Common mode characteristics of H6-I topology

4.1.5 Proposed Topology

The schematic diagram of the proposed topology is presented in Figure 4.15. The proposed H6 topology is a modified version of conventional H6 topology. For the proposed topology, there are two switches conducting in the positive half cycle instead of the three of conventional H6 topology. By reducing the total number of conducting switches from six to five, there is a reduction in total conduction losses.

There are four possible operating modes. The driving signals of the proposed topology are illustrated in Figure 4.17. During the positive active state, S_6 and S_4 are connected to deliver positive output voltage, as illustrated in Figure 4.16(a). In the negative active state, S_5, S_3, and S_2 are conducting, as presented in Figure 4.16(c). As noted, the total number of conducting switches during the active state is reduced from six to five switches. Consequently, the total conduction loss is reduced and system efficiency is improved. Figure 4.16(b) and Figure 4.16(d) show the freewheeling modes in the positive and negative half period during the zero state. In the positive zero state, the current passes through S_1 and the body diode of S_3 to achieve zero output voltage. In the negative zero state, current passes through S_3 and the body diode of S_1 to achieve zero output voltage.

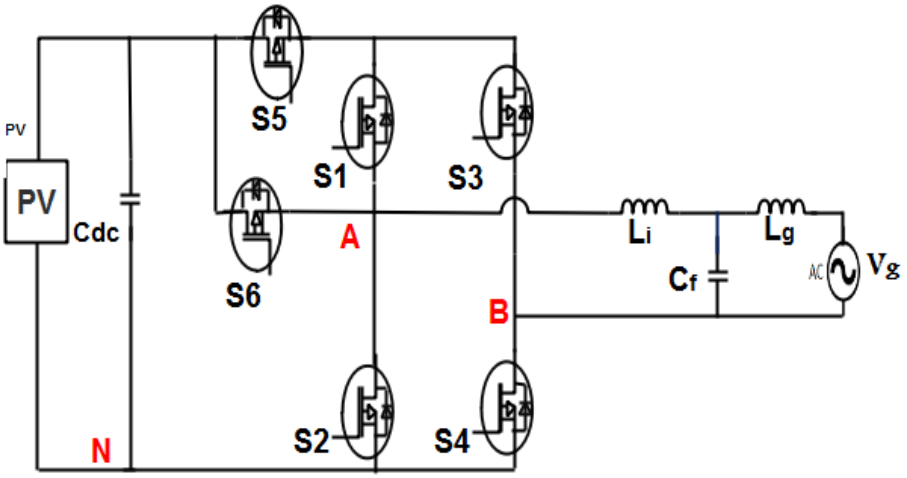


Figure 4. 15 Circuit structure of the proposed topology

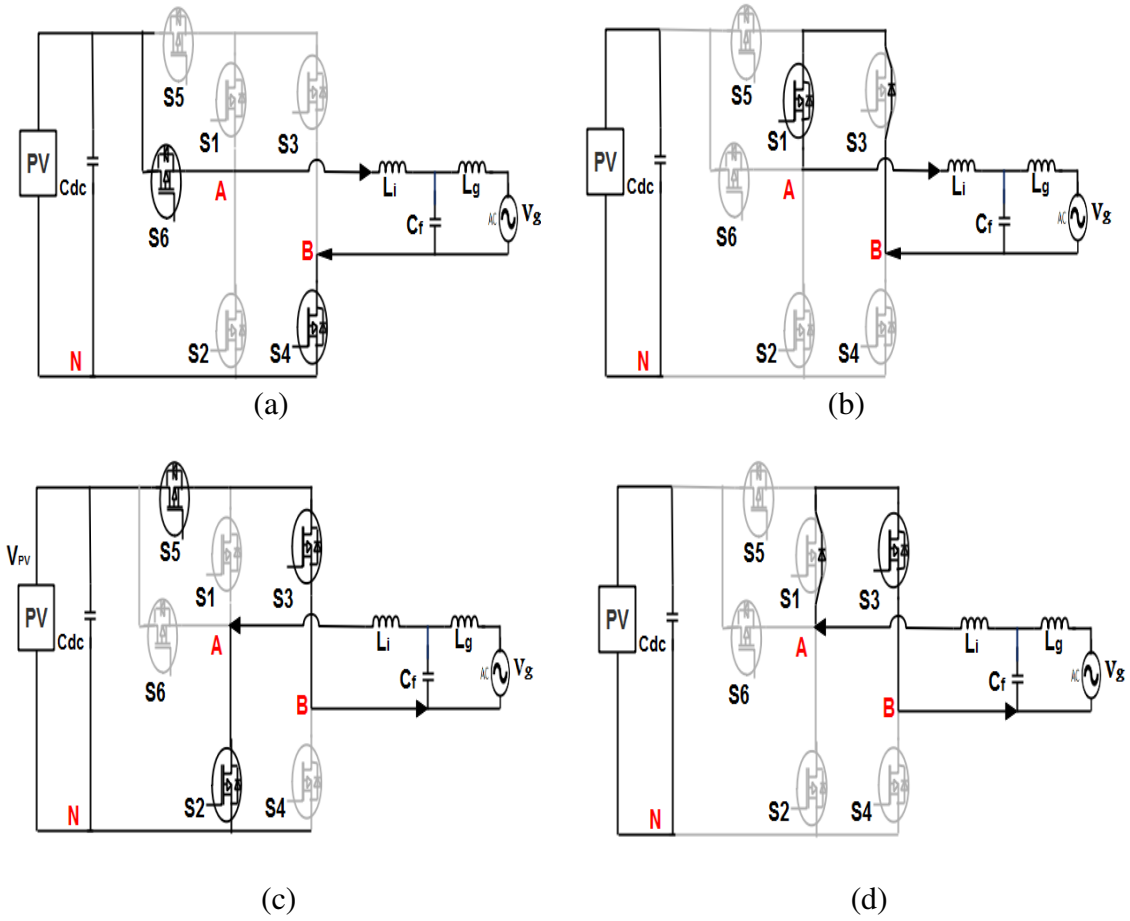


Figure 4. 16 Operation modes of the proposed topology. (a) The positive active state; (b) the zero state during the positive half period; (c) the negative active state; and, (d) the zero state during the negative half period

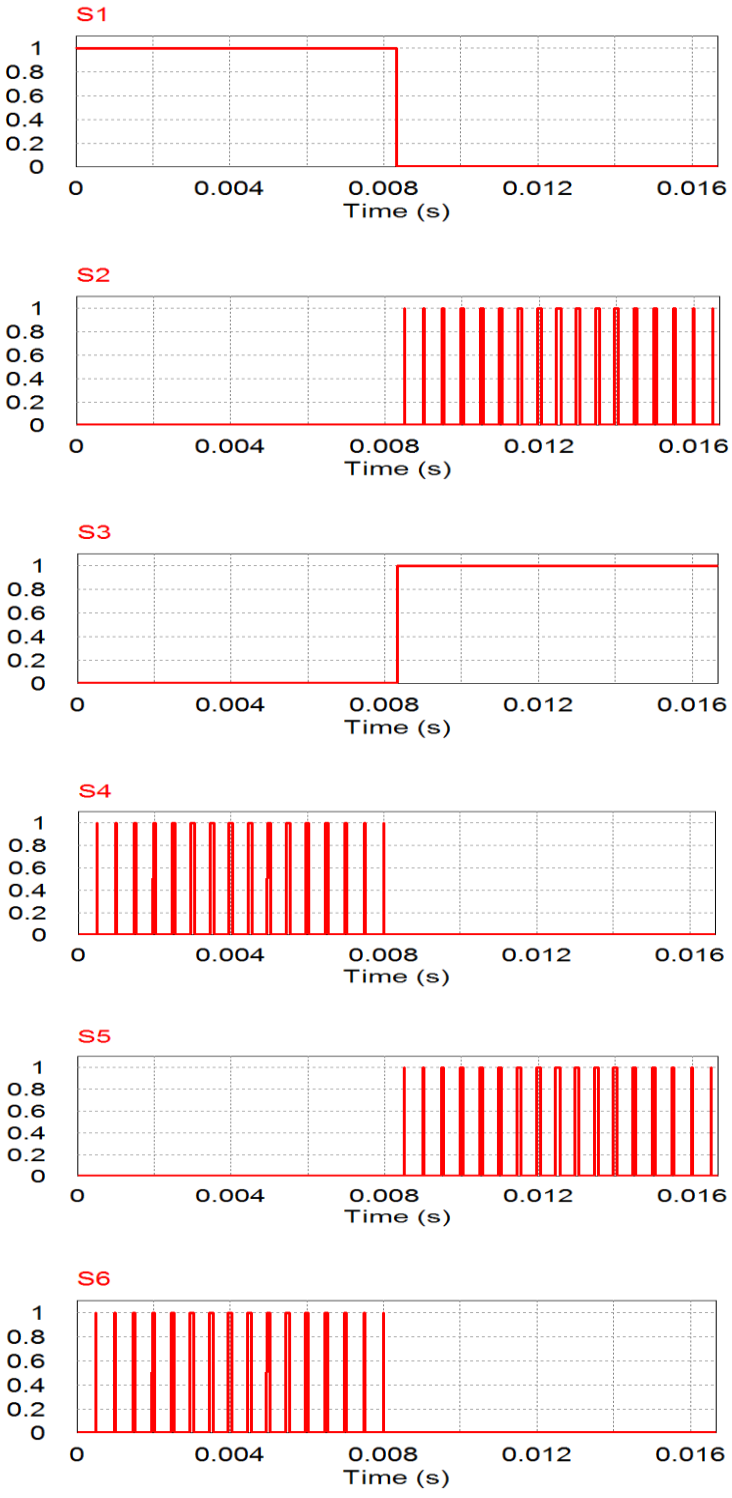


Figure 4. 17 PWM strategy of the proposed topology

The CM characteristics of the proposed topology are shown in Figure 4.18. It should be noted that the V_{CM} is oscillating from 200V to 600 V and is not fixed to $V_{DC}/2$. Also, the V_{AN} and V_{BN} are not flat at zero crossing because of the junction capacitances. Therefore, the leakage current is not completely eliminated. The simulated waveforms of grid current, grid voltage, and inverter output voltage are given in Figure 4.19.

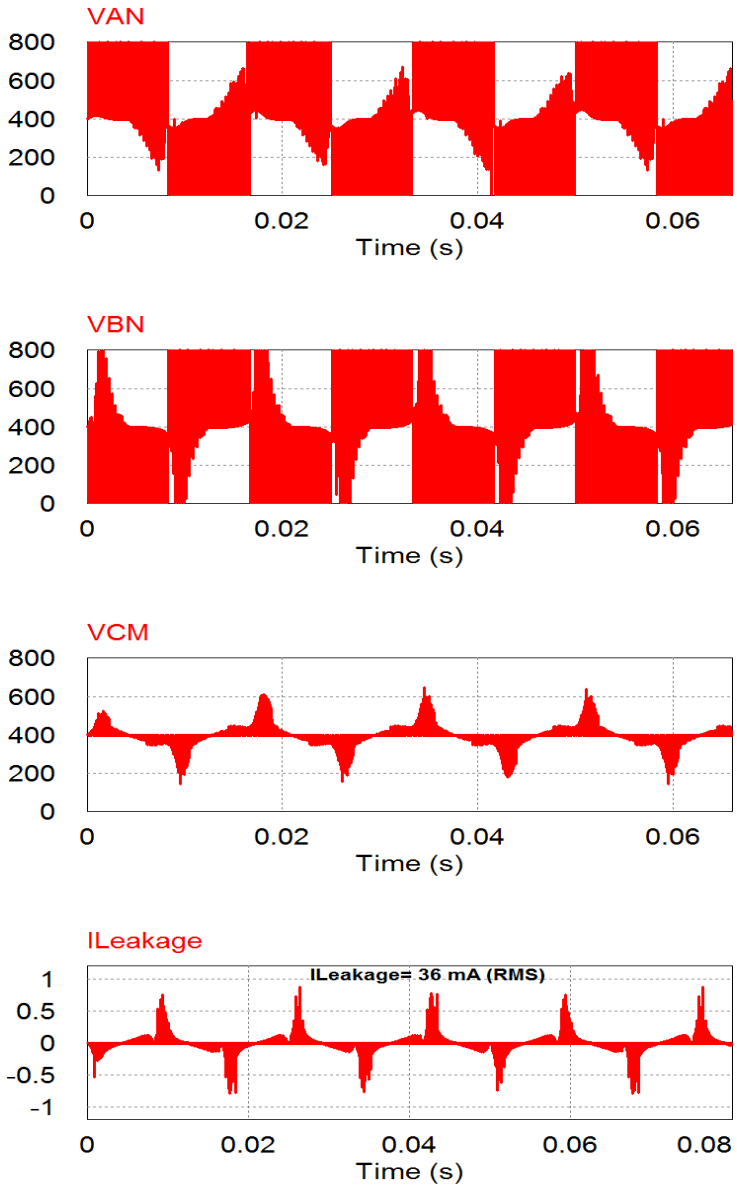
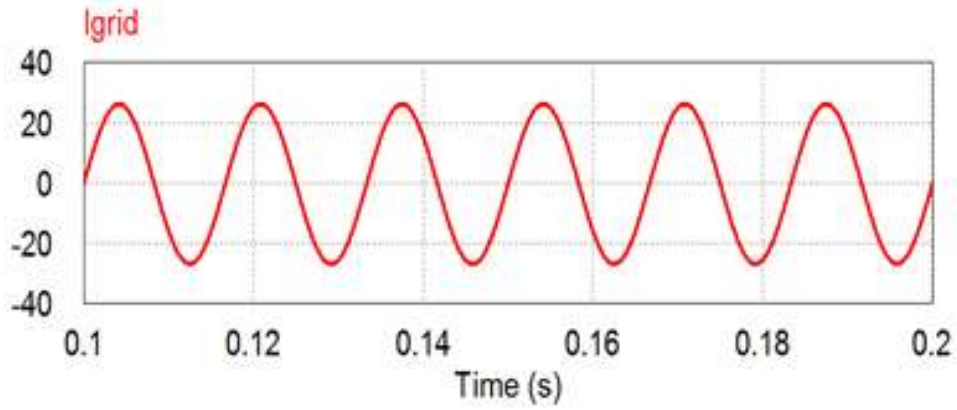
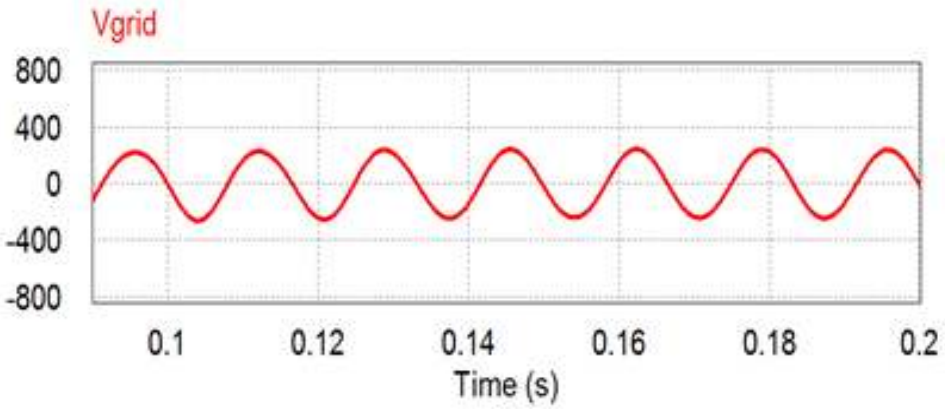


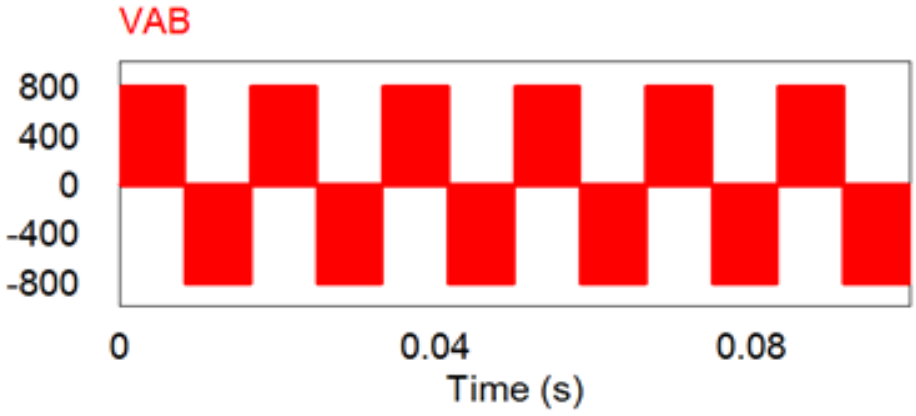
Figure 4. 18 Common mode characteristics of the proposed topology



(a)



(b)



(c)

Figure 4. 19 Output waveform. (a) Grid current; (b) grid voltage; and, (c) inverter output voltage

4.2 Power Loss Analysis

To evaluate the performance of PV transformerless inverters, it is important to measure the losses of the switching devices at different output loads. The losses in semiconductor power devices can be divided into two types: switching losses and conduction losses. A detailed power loss analysis of the semiconductor power devices and diode are given in [52]. To calculate the conduction losses, first the voltage drop across these devices must be identified as follows:

$$v_{DS}(MOSFET) = i(t) * R_{DS} \tag{4.1}$$

$$v_{CE}(IGBT) = V_t + i(t) * R_{CE} \tag{4.2}$$

$$v_{AK}(Diode) = V_f + i(t) * R_{AK} \tag{4.3}$$

Where V_{DS} represents a drain to a source voltage drop of the MOSFET, R_{DS} is the ON state resistance of the MOSFET, V_{CE} is the voltage between collector and emitter in IGBT, V_t indicates the corresponding voltage drop under zero-current condition, R_{CE} stands for the IGBT ON resistance, V_{AK} represents the voltage between the anode and cathode of the diode, V_f denotes the diode corresponding voltage drop under zero-current condition, R_{AK} is the ON resistance of the diode, and i(t) indicates the current passing through the device. The conduction losses can be calculated by the following equations:

$$P_{Con-act} = \frac{1}{2\pi}\int_0^{\pi} v_{cond} * i(t) * D_{act}(t) d(\omega t) \tag{4.4}$$

$$i(t) = I_m \sin(\omega t + \theta) \tag{4.5}$$

$$D_{act}(t) = M sin(\omega t) \tag{4.6}$$

Where I_m stands for the output current peak of the inverter, w represents the angular frequency, θ denotes the phase displacement between voltage and grid current, D_{act} represents the duty ratio during, the active state and M can take a value between 0 and 1. The conduction loss of a single switching device in the zero state is expressed as:

$$P_{cond-zero} = \frac{1}{2\pi}\int_0^{\pi} v_{con} * i(t) D_{zero}(t) d(\omega t) \tag{4.7}$$

$$D_{zero}(t) = 1 - Msin(\omega t) \tag{4.8}$$

Where D_{zero} represents the duty ratio during zero state. The second part of the power loss is the switching loss during turn-ON and turn-OFF time. The switching ON and OFF power losses are given as:

$$P_{ON} = \left(\frac{I_m \cdot V_{DC}}{2\pi}\right) \cdot f_{sw} \cdot \frac{E_{on}}{V_{test} \cdot I_{test}} \tag{4.9}$$

$$P_{OFF} = \left(\frac{I_m \cdot V_{DC}}{2\pi}\right) \cdot f_{sw} \cdot \frac{E_{off}}{V_{test} \cdot I_{test}} \tag{4.10}$$

Where E_{on} and E_{off} are the turn-ON and turn-OFF energy losses. These energy losses are measured under accurate test conditions over different junction temperatures and reported in data sheets for given values of switching current and voltage. The switching-ON loss of a diode can be ignored because it is very small. The diode switching-OFF loss is calculated as follows:

$$P_{Diode-OFF} = \frac{1}{12} \cdot t_b \cdot I_{RRM} \cdot \frac{V_{DC}}{2} \cdot f_{sw} \tag{4.11}$$

Where IRRM denotes the reverse recovery current.

4.3 Total Losses and Performance Analysis

PSIM simulation software was used to design and simulate the discussed various topologies. The thermal model also generated by the simulation software was used to calculate the switching and conduction losses and evaluate the system performance for the various topologies. The specifications of the system design are shown on Table 4.1.

Table 4. 1 Specifications of the System Design

Parameter	**Value**
Input Voltage	800 V
Grid Voltage	120 V
Grid Frequency	60 Hz
Switching Frequency	16 kHz and 100 kHz
DC Bus Capacitor (C_{DC})	970 µF
Output Power	3 kW

The switching and conduction losses at the rated power for different transformerless inverter topologies are presented in Figure 4.20. It is noted that H6 has higher conduction loss and total losses because it has a total of four switches conducting during the positive and negative half cycle. The H4 with bipolar modulation has higher total losses than H5 and H6-I because there are four switches operating at the switching frequency during the positive and negative active states. The proposed topology has the lowest total losses compared to the other transformerless inverter topologies because the total number of conducting switches is reduced to five.

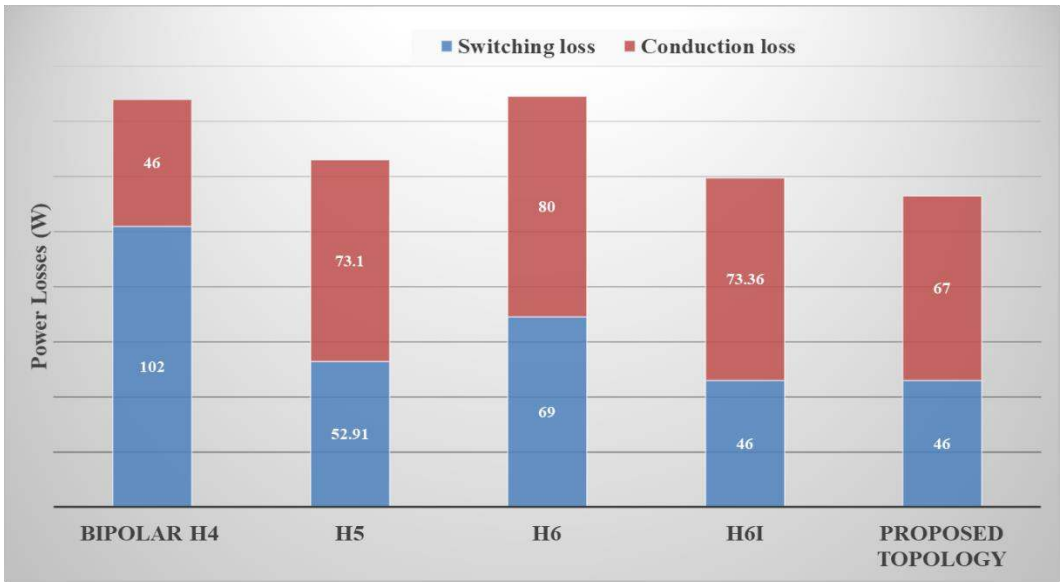


Figure 4. 20 Conduction and switching losses of various transformerless inverters at 16 kHz [53]

The efficiency of the various topologies is determined using the California Energy Commission (CEC) for different output power loads and is presented in Figure 4.21. The efficiency is calculated according to the following:

$$\eta_{CEC} = 0.04\eta_{10\%} + 0.05\eta_{20\%} + 0.12\eta_{30\%} + 0.21\eta_{50\%} + 0.53\eta_{75\%} + 0.05\eta_{100\%} \quad (4.12)$$

The calculated CEC for the bipolar H4, H5, H6, and H6-I and for the proposed topology are shown on Table 4.2.

Table 4. 2 CEC Efficiency of Various Transformerless Inverters At 16 kHz [53]

Output Power (W)	300	600	900	1500	2250	3000	CEC
Bipolar H4	86.55%	92.5%	93.8%	94.7%	95%	95%	94.33%
H5	94.8%	95.7%	95.9%	96%	95.9%	95.8%	95.862
H6	94%	94.4%	94.8%	95.3%	95.1%	94.7%	95%
H6I	95.6%	96.2%	96.47%	96.34%	96.2%	96%	96.2%
Proposed Topology	95.8%	96.4%	96.8%	96.5%	96.4%	96.2%	96.4%

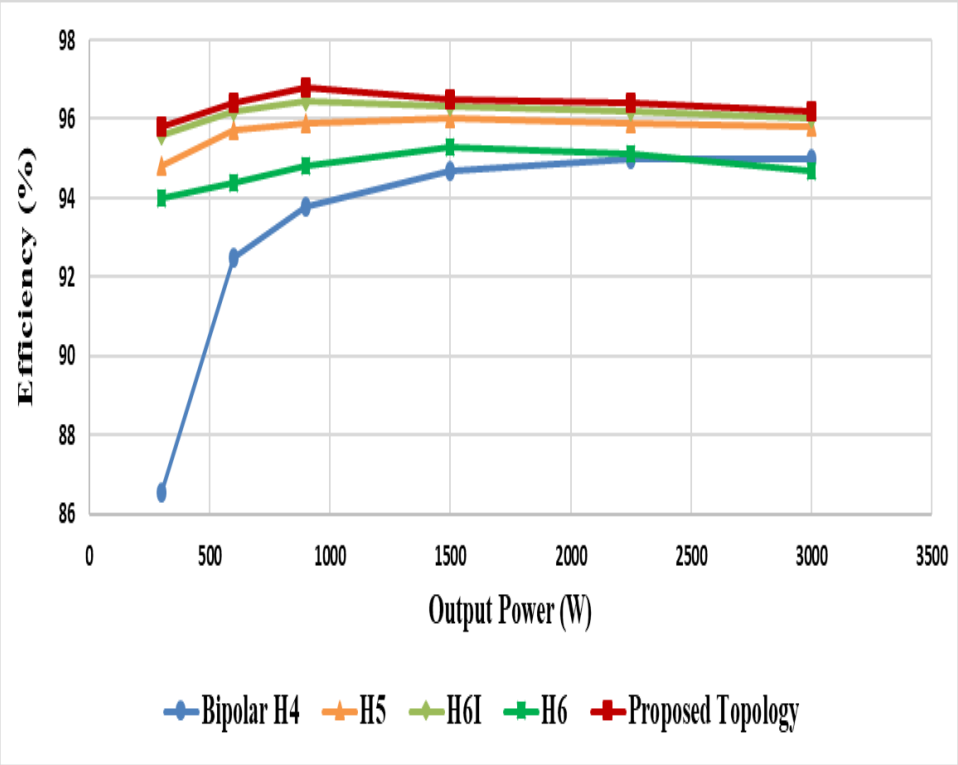


Figure 4. 21 Efficiency comparison of various transformerless inverter topologies with different output power loads [53]

4.4 Conclusion

This chapter presented a review of some of the recent advances in transformerless inverter topologies, such as H5, H6, and H6-I. All these topologies are modulated with unipolar SPWM to enhance system efficiency. Galvanic method isolation is used in these

topologies to solve the issue of leakage current. It is noted that leakage current is not completely eliminated because the common mode voltage is floating during the freewheeling period. A proposed transformerless inverter is introduced to increase system efficiency and reduce or eliminate leakage current. The number of conducting switches in the proposed topology is reduced from six to five switches. As a result, the total losses are reduced; the proposed topology also has the highest efficiency compared with the other reviewed topologies.

Chapter 5. Wide-Bandgap (WBG) Power Devices

5.1 Introduction

Wide-bandgap (WBG) materials, such as silicon carbide (SiC), gallium nitride (GaN), and diamond can be excellent alternatives for Si material due to their superior properties, such as low ON state resistance, high switching speed, and high operating temperature. The first of the SiC-based devices to be launched was the SiC Schottky barrier diode; subsequently, this was followed by the introduction of fully controlled power semiconductor devices, such as the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) and the Junction Field Effect Transistor (JFET) with a 600 V blocking voltage range. WBG power devices utilizing SiC and GaN offer superior conduction and switching performance compared to Si-based devices over a wide range of temperatures. Consequently, such WBG switching devices can be used to achieve high system efficiency and be promising solutions for highly efficient transformerless inverters.

5.2 Physical Characteristics of WBG Materials

The main physical characteristics of the newer WBG device materials, such as SiC and GaN, and those of traditionally used Si material are presented on Table 5.1 [53]–[64].

Table 5. 1 Comparison of Physical Characteristics of Si, SiC, and GaN

Material	E_G (eV)	N_I (cm^{-3}) at 27 °C	Dielectric constant (ε_r)	E_C (MV/cm)	V_{SAT} (10^7 cm/s)
Si	1.12	1.5×10^{10}	11.8	0.23	1.0
4H-SiC	3.26	8.2×10^{-9}	9.7	2.2	2.0
GaN	3.39	1.9×10^{-10}	9.0	3.3	2.5

Where E_G denotes the material bandgap, N_I represents the intrinsic carrier concentration, ε_r is the relative permittivity, E_C indicates the critical electrical field, and V_{SAT} stands for the saturation velocity. The physical characteristics of WBG materials are analyzed and compared with the material traditionally used, silicon, to explain the superior performance of WBG-based power semiconductor devices in terms of: (a) high operating temperature, (b) lower ON-state resistance, and (c) higher switching speed.

5.2.1 Higher Operating Temperature

Two physical characteristics are related to this feature: the lower intrinsic carrier concentration and the wider bandgap [66]. WBG materials have wider bandgap which means it needs high thermal energy to move the electron from the valence band to the conduction band. As a result, a higher temperature is required to trigger the electrons, a higher temperature which might lead to power device failure in devices made with silicon. In addition, WBG materials have a small value of intrinsic carrier concentration, which results in lower leakage current compared to Si-based devices at the same temperature.

5.2.2 Low ON-State Resistance

The critical electrical field (E_C) of WBG materials is almost more than 10 times higher than the E_C of devices constructed with silicon material. Therefore, WBG-based power devices have lower ON-state resistance, according to the following equation [67]:

$$R_{ON,SP} = \frac{4V_{BK}^2}{\varepsilon_r \mu_n E_C^3} \tag{5.1}$$

Above, V_{BK} denotes the device breakdown voltage, εs represents the relative permittivity, μ_n stands for the electron mobility, and E_C is the critical electrical field. Clearly, there is an inverse relationship between the ON-resistance and the E_C. Therefore, WBG-based power devices have much smaller ON-state resistance compared to Si-based devices. As a result, lower conduction losses are associated with WBG-based power devices due to this feature.

5.2.3 Higher Switching Speed

Switching speed is related to two physical characteristics: saturation velocity (V_{SAT}) and relative permittivity (ε_r). The V_{SAT} of SiC and GaN is almost double the V_{SAT} of silicon. Therefore, the electrons' movement in WBG-based power devices is much faster than in Si-based power devices. In addition, WBG materials have lower relative permittivity compared to Si material. As a result, the parasitic capacitances of WBG-based power devices are smaller than those of Si-based power devices, leading to higher switching speed and transitions.

5.3 Loss Evaluation of Si IGBT and SiC MOSFET Power Devices

The total power loss of a switching device can be classified in two ways, as a switching or a conduction loss. An accurate evaluation of conduction losses requires

specific performance data obtained from a datasheet, such as the ON-state resistance of MOSFET, saturation voltages of IGBT, and forward voltage of body diode [68], [69]. Different parameters must be established for the evaluation of switching energy losses such as gate drive voltage, gate resistance, and junction temperature. A double pulse test circuit was designed using LTSpice for both switching devices to create an accurate comparison of switching energy losses as shown in Figure 5.1.

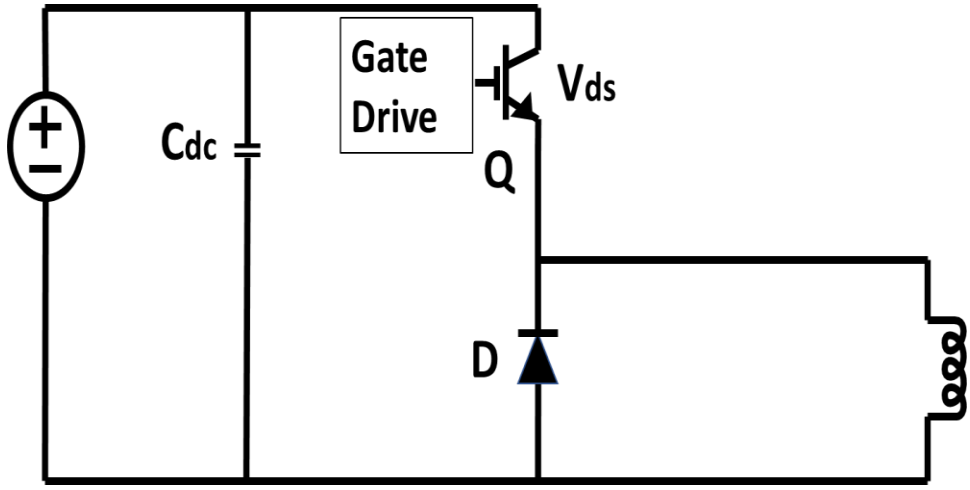
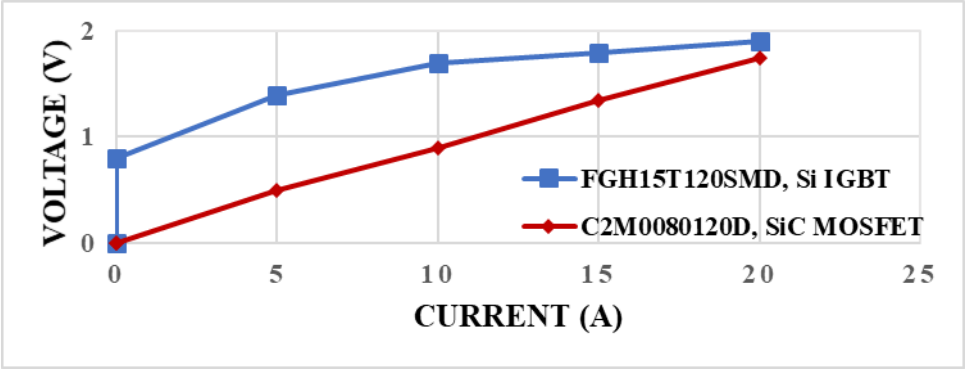


Figure 5. 1 Double Pulse Test Circuit

5.3.1 Evaluation of Conduction Losses

Conduction losses can be determined by multiplying the voltage drop across the switch when it is ON with current flowing through. Conduction losses represent a major portion of total overall semiconductor losses. The stated forward voltages of the selected switching power devices over different current values are given in Figure 5.1(a) and Figure 5.1(b). It was noted that the SiC MOSFET has a small voltage drop as compared to that of the Si IGBT due to the resistive output characteristics of the SiC MOSFET, which leads to a reduction in conduction losses.



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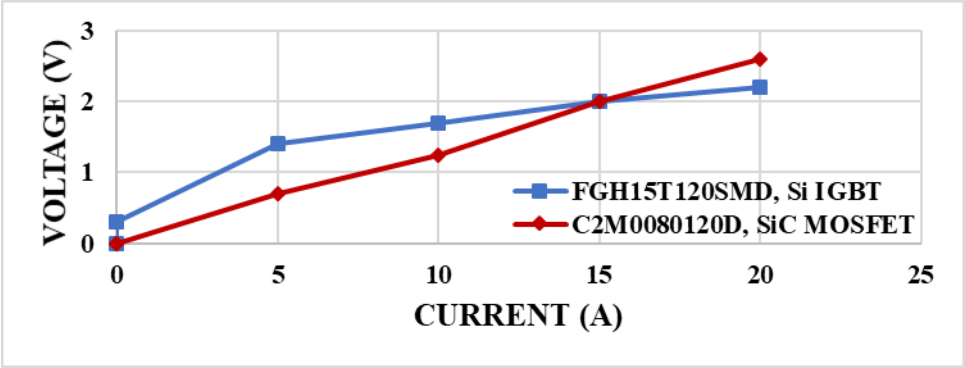
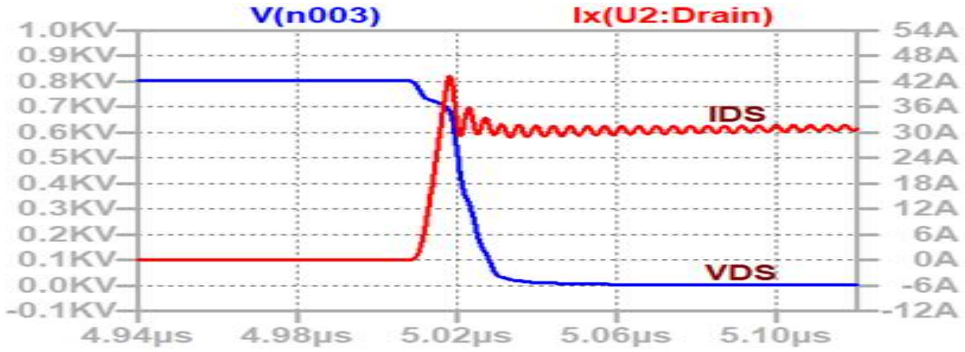


(b)

Figure 5. 2 (a) Forward voltages of SiC MOSFET and Si IGBT at 25 ℃; and, (b) forward voltages of SiC MOSFET and Si IGBT at 175 ℃

5.3.2 Evaluation of Switching Losses

LTspice software was used to study the switching waveform characteristics of the selected switching power devices. The models used with the software were provided by the manufacturers of the devices. The turn-ON and turn-OFF switching waveforms at 800 V and 30 A for SiC MOSFET and Si IGBT are shown in Figure 5.2. Clearly, the SiC MOSFET has better switching characteristics in terms of dv/dt and di/dt. At the turn-OFF transition, the dv/dt is measured for both switching devices. It was also found that SiC MOSFET switches at the much higher 19.8 kV/ms while the Si IGBT switches at 3.9 kV/ms. Table 5.2 presents the turn-ON and turn-OFF transition states for both switching devices.



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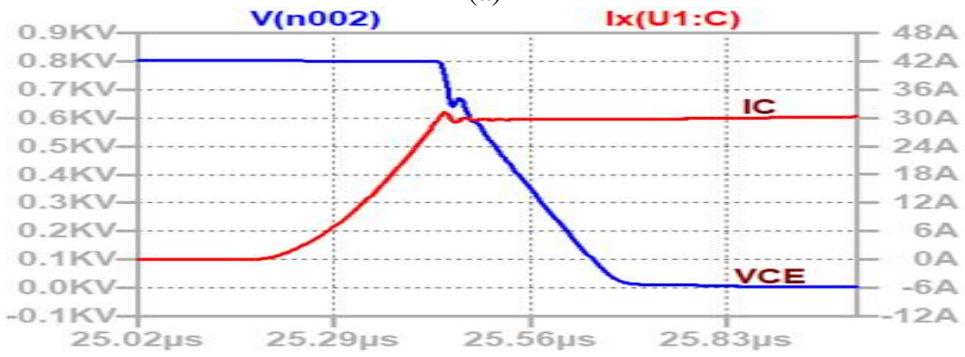

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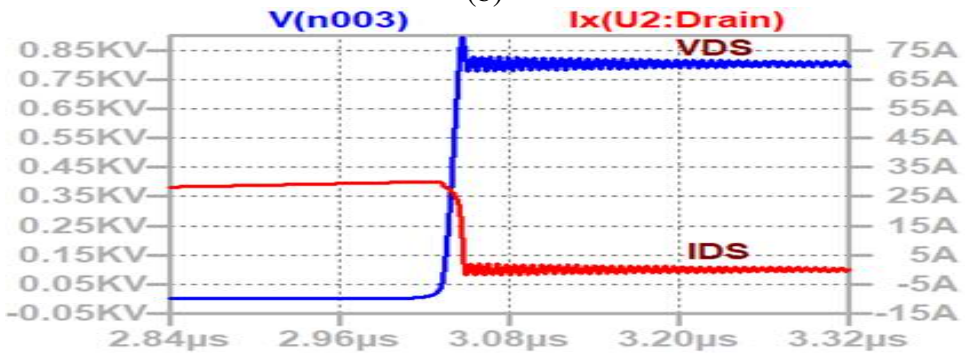

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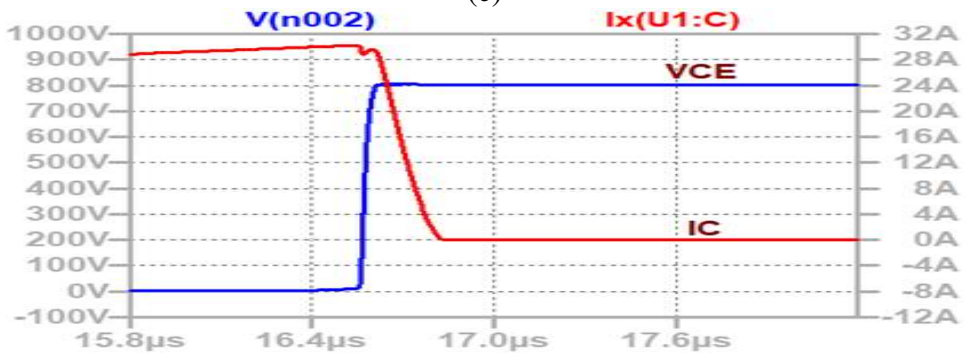


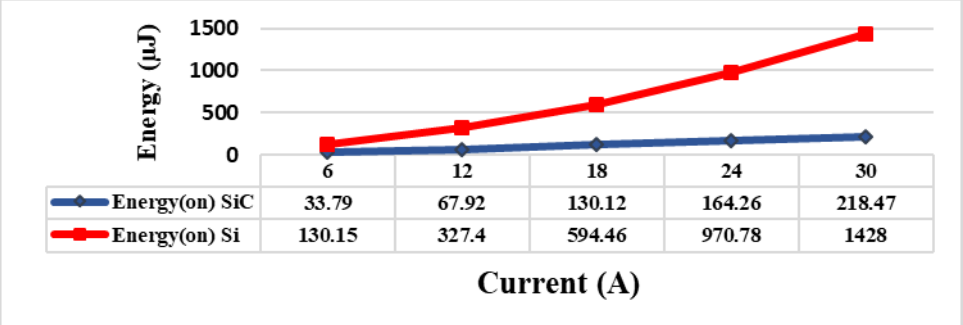
(d)

Figure 5. 3 Switching transitions of switching devices for a voltage of 800 V and 30 A. (a) Turn-ON SiC MOSFET; (b) turn-ON Si IGBT; (c) turn-OFF SiC MOSFET; and, (d) turn-OFF Si IGBT

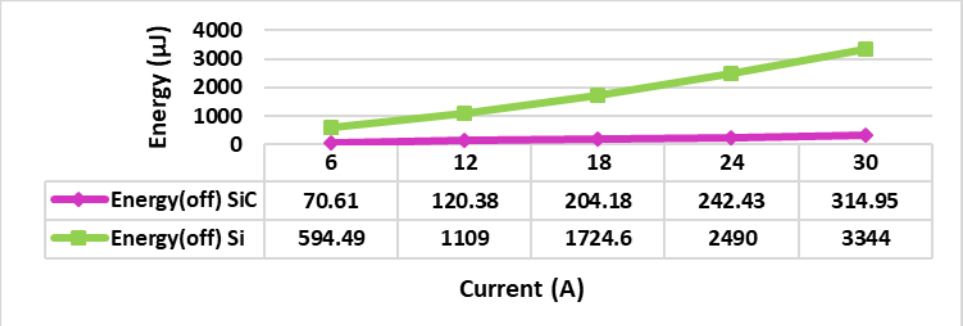
Table 5. 2 Turn-ON and turn-OFF switching transition

	Turn-on		Turn-off	
	Si IGBT	SiC MOSFET	Si IGBT	SiC MOSFET
$\frac{dv}{dt}\left(\frac{kV}{\mu s}\right)$	5	23	3.9	19.8
$\frac{di}{dt}\left(\frac{kA}{\mu s}\right)$	0.35	1.4	0.12	2

The switching energies can be calculated by taking the integral of the product of the voltage and current. By applying this method, the measured turn-ON and turn-OFF energies of both switching devices are given in Figure 5.3. The turn-ON switching energy losses are small compared to the turn-OFF switching energy losses for both switching devices. The study shows that at low current levels, the Si IGBT must dissipate more than three times the turn-ON energy of the SiC MOSFET. Therefore, the switching energy losses of Si IGBT are much greater and increase linearly with the current. However, SiC MOSFET has very low turn-OFF energy losses, which can be a major advantage compared to Si IGBT. Also, the total energy loss of SiC MOSFET increases slightly when the temperature is increased to 100℃. The turn-OFF energy losses of the Si IGBT are about eight times higher than SiC MOSFET at a current of 6 A and about 10 times higher at a current of 30 A, as shown in Figure 5.3(b). The drawback of Si IGBT is that it has large switching energy losses. As a result, SiC MOSFET is an attractive solution for high switching frequency application because of its superior switching characteristics.



(a)



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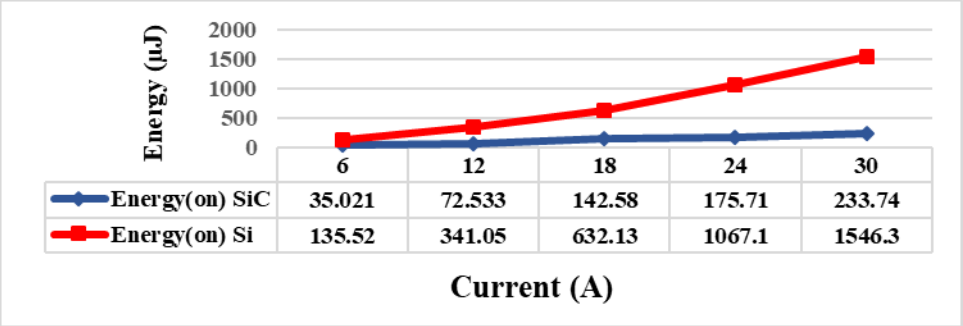

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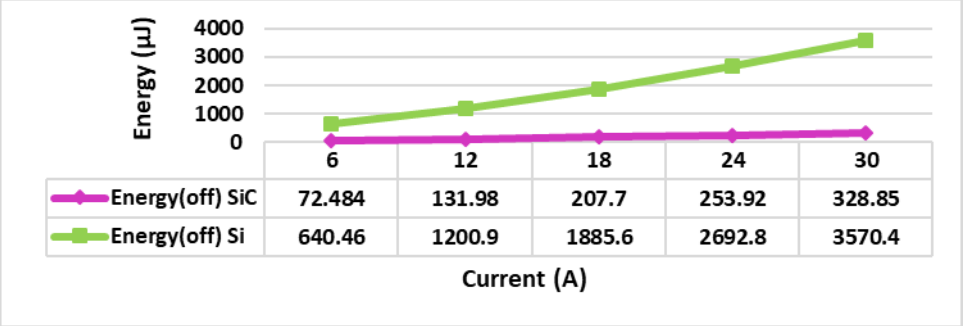


(d)

Figure 5. 4 Turn-ON and turn-OFF switching energy losses for 800 V and 30 A. (a) Turn-ON energies at 25℃; (b) turn-OFF energies at 25℃; (c) turn-ON energies at 100℃; and, (d) turn-OFF energies at 100℃

5.4 Conclusion

The physical properties of WBG materials such as SiC and GaN are described in this chapter. WBG materials have certain superior characteristics compared to those of Si material, such as wider bandgap, low intrinsic carrier concentration, and high saturation velocity. As a result, WBG-based semiconductor devices can operate at high temperature, have low ON-state resistance, and operate at high switching frequency. Moreover, a double pulse test circuit designed in LTspice to evaluate and simulate the dynamic and static characteristics of two switching devices, SiC MOSFET and Si IGBT, at 1200V blocking voltage found that SiC MOSFET also has low switching and conduction losses compared to those of Si IGBT.

Chapter 6. Benefits of SiC MOSFET in PV System

6.1 Introduction

The benefits of using WBG power devices, such as SiC MOSFET, are discussed in detail in this chapter. WBG power devices can operate at high switching frequencies and have low switching and conduction losses due to their material properties [70], [71]. Therefore, a high system efficiency and high-power density can be achieved with WBG power devices such as SiC MOSFET and GaN HEMT [72]–[76]. The benefits of utilizing SiC MOSFET instead of Si IGBT are studied and demonstrated in this section.

6.2 Performance Enhancement of the Proposed High Gain DC-DC Converter Using SiC MOSFET

The performance of the system is enhanced by using WBG power devices such as SiC MOSFET. Two types of switching power devices are used in this study, SiC and Si MOSFET, to compare their switching and conduction losses at high switching operating frequencies. The specifications of these two types of devices are shown in Table 6.1.

Table 6. 1 Specifications of the switching devices

Parameter	**Si MOSFET TK35A65W5**	**SiC MOSFET SCT3060AL**
Breakdown Voltage	650V	650V
Continuous Current	35A	39A
R_{DS-ON}	80mΩ	60mΩ
Q_{rr}	780nC	55nC
T_{rr}	130ns	15ns

Conduction and switching losses of Si and SiC MOSFET at different switching frequencies and output power of 2 kW are presented in Figure 6.1. The results show that the conduction losses of the proposed converter were reduced by 65% with SiC MOSFET. This reduction in conduction losses is due to the smaller ON state resistance of SiC MOSFET. Also, switching losses at 100 kHz were reduced by about 90% with SiC MOSFET. The reverse recovery charge of Si MOSFET is about 14 times greater than that of SiC MOSFET. Moreover, the reverse recovery time of Si MOSFET is approximately nine times greater than SiC MOSFET. This explains the large switching losses of Si compared to those of SiC MOSFET.

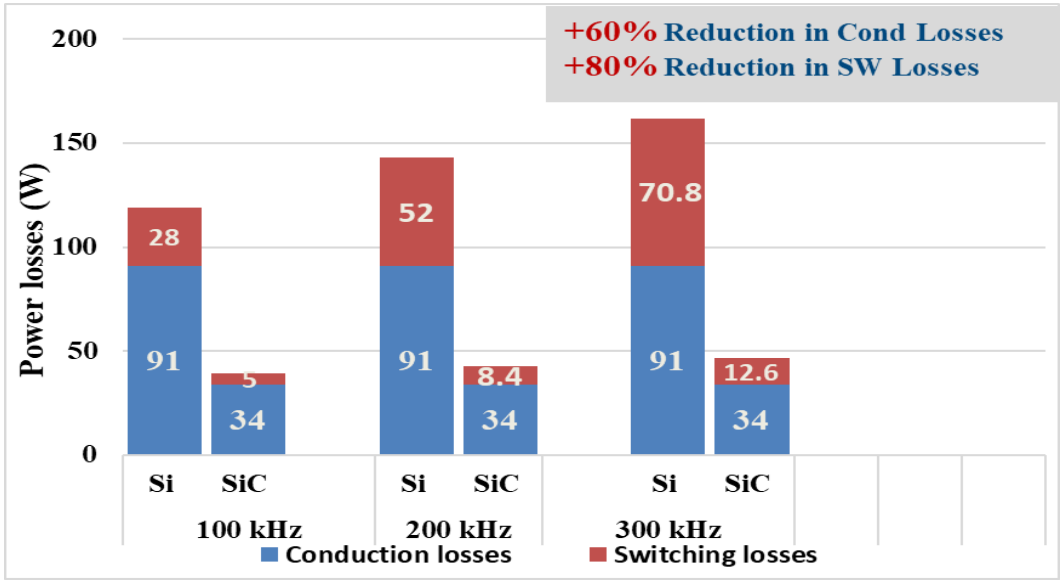


Figure 6. 1 Conduction and switching losses of Si and SiC MOSFET at different switching frequencies [33]

Switching losses of the system at 200 kHz are reduced by around 90% with SiC MOSFET, which is a significant reduction in switching losses. Compared with switching losses at 100 kHz, switching losses of SiC MOSFET is increased by only 3.5 W while the switching losses of Si MOSFET increased by 30.5 W.

Figures 6.2, 6.3, and 6.4, demonstrate the efficiency of the system with different output power loads at different switching frequencies. At 100 kHz, the efficiency of the system improved by two percent. Moreover, the efficiency increased by 3% when the switching frequency increased to 200 kHz. The advantages to using SiC MOSFET became even more obvious at a higher switching frequency where the efficiency increased by 4% at 300 kHz. Furthermore, it was observed that the power rating of the system can be increased from 200 W to 2000 kW for the same total losses at a switching frequency of 100 kHz.

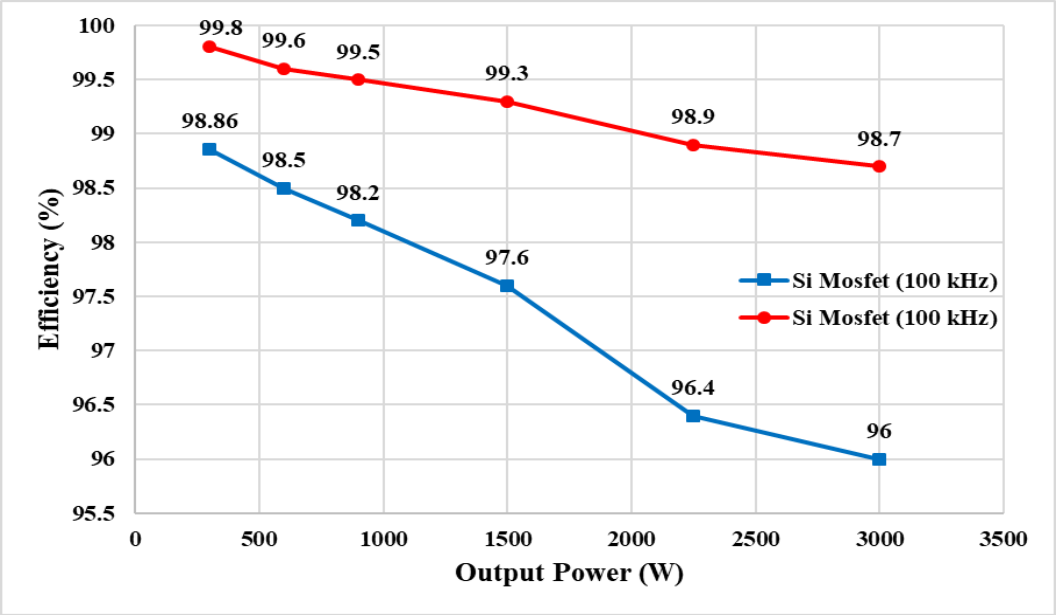


Figure 6. 2 Efficiency comparison of Si and SiC MOSFET at 100 kHz with different output power loads [33]

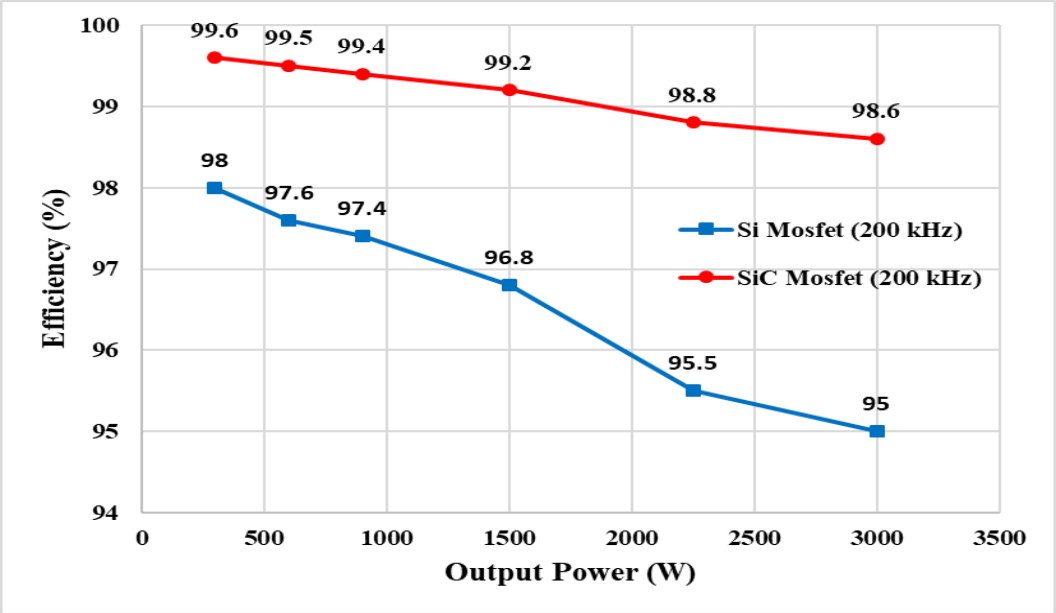


Figure 6. 3 Efficiency comparison of Si and SiC MOSFET at 200 kHz with different output power loads [33]

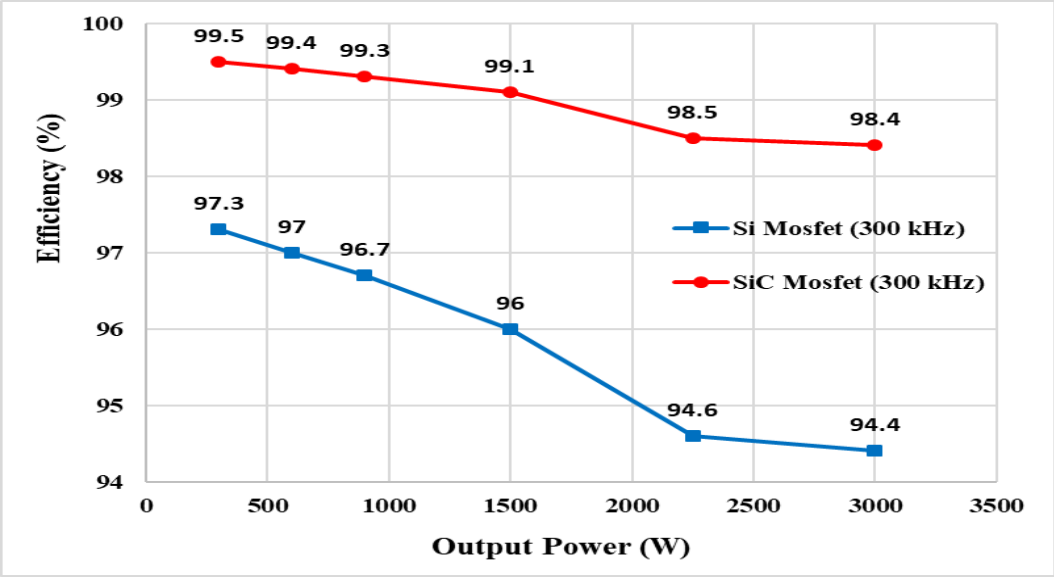


Figure 6. 4 Efficiency comparison of Si and SiC MOSFET at 300 kHz with different output power loads [33]

6.3 Benefits of SiC MOSFET in the Proposed Transformerless Inverter

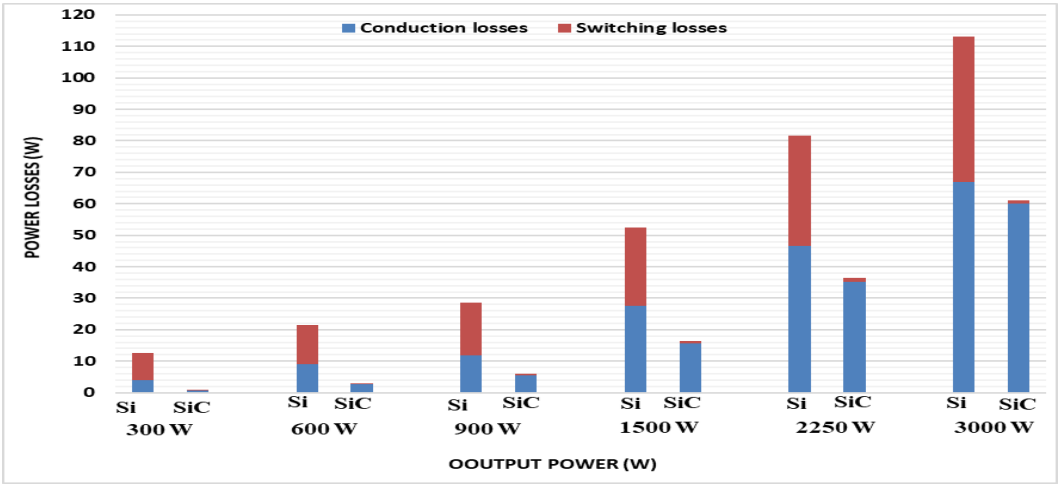
The benefits of implementing SiC MOSFET instead of Si IGBT are studied and demonstrated in this section. The parameters of the selected switching devices are given on Table 6.2.

Table 6. 2 Parameters of selected switching devices

Parameter	IGBT (FGH15T120SMD)	SiC (C2M0080120D)
Breakdown Voltage (V)	1200	1200
Continuous Current (A)	30	36
$R_{DS\text{-}ON}/R_{CE}$ (mΩ)	28	80
V_t (V)	0.75	-
V_f (V)	0.8	1.4
R_{AK} (mΩ)	183	80
I_{RRM} (A)	7.4	10
Q_{rr} (reverse recovery charge) (nC)	270	192
T_{rr} (reverse recovery time) (ns)	183	32

6.3.1 Efficiency Improvement

Semiconductor losses have a significant impact on inverter efficiency. The semiconductor losses for Si IGBT and SiC MOSFET over different output power loads at 16 kHz are presented in Figure 6.5(a). It is observed that SiC MOSFET has low conduction losses at light loads because of its resistive output characteristics. Moreover, at a full output power load of 3 kW, the conduction losses of the Si IGBT are almost the same as those of SiC MOSFET because Si IGBT has a constant voltage drop. On the other hand, the major benefit to using SiC MOSFET is its low switching losses due to the absence of tail current. The total losses are reduced by more than 50% with SiC MOSFET. The semiconductor losses with different output power loads at 100 kHz are given in Figure 6.5(b). The total power loss of the Si IGBT at 100 kHz is about four times greater than that at 16 kHz, which means that Si IGBT is not suitable for high switching frequency applications. On the other hand, the total power loss of SiC MOSFET is increased by only 12% at 100 kHz.



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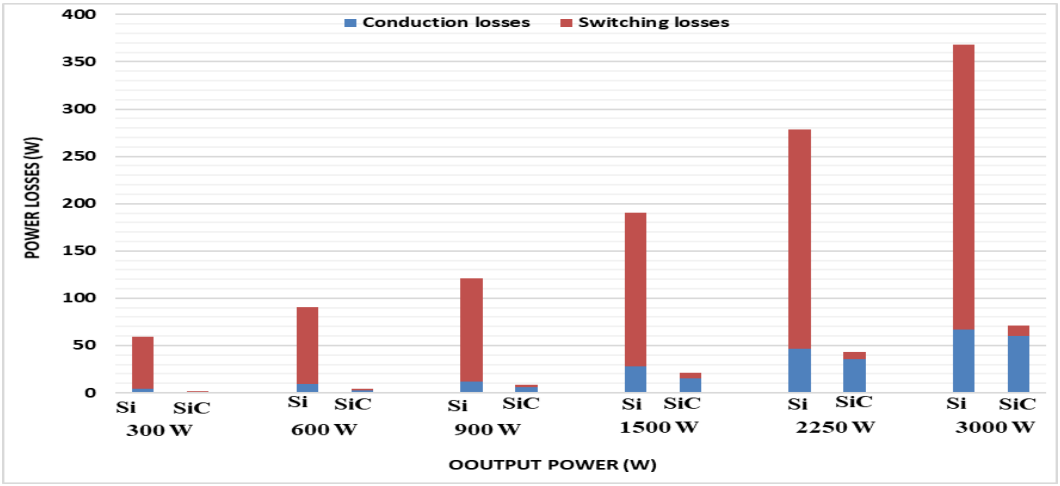


(b)

Figure 6. 5 Conduction and switching losses of Si IGBT and SiC MOSFET with different output power loads. (a) at 16 kHz; and, (b) at 100 kHz. [53]

The efficiency of the system with different output power loads at two different switching frequencies is illustrated in Figure 6.6. The efficiency of the system at 16 kHz is increased by 2% with SiC MOSFET. The benefits of using SiC MOSFET become more obvious at higher switching frequencies where the efficiency of the system increases by almost 14% at 100 kHz compared to the efficiency of Si IGBT at the same level.

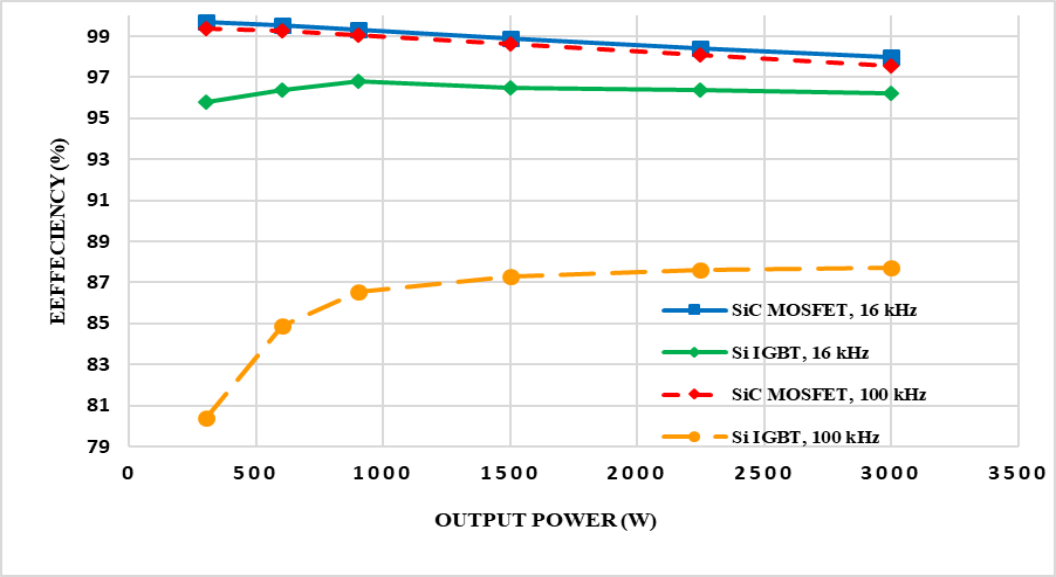


Figure 6. 6 Efficiency comparison between Si IGBT and SiC MOSFET with different output power loads and at two different switching frequencies [53]

6.3.2 Switching Frequency vs. Inductor Volume

The simulation results verified that SiC MOSFET can operate at high switching frequency while maintaining low power losses. The value of the inductor is inversely proportional to the switching frequency as shown in the following equation.

$$L = \frac{V_{DC}}{4 \cdot f_{sw} \cdot i_{max} \cdot \Delta i_{ripple}} \tag{6.1}$$

Where V_{DC} is the DC bus voltage, f_{sw} denotes the switching frequency, i_{max} is the peak current, and Δi_{ripple} is the current ripple and set as 20% of the peak current.

A significant reduction in the inductor volume can be achieved when the switching frequency increases to higher values. In this study, it was found to be possible to increase the switching frequency of the proposed SiC MOSFET system all the way to 200 kHz until the power losses matched those found in the Si IGBT system at only 16 kHz, as shown in Figure 6.7.

The inductor value at different switching frequencies is presented in Figure 6.8 where it is shown that it decreased from 1400 µH at 20 kHz to 140 µH at 200 kHz. The large reduction in the inductor value leads to small size and volume of inductor storage. The core material used in this study, for the sake of comparison, was a toroid core manufactured using Kool Mu material. The effect on the magnetic core volume of increasing the switching frequency is presented in Figure 6.9. This study shows that, as the switching frequency increases, the magnetic core volume decreases. The magnetic core volume decreased from 220 cm^3 at 20 kHz to 20.7 cm^3 at 200 kHz. Moreover, a smaller inductor volume leads to smaller inductor weight. The relationship between the switching frequency and the inductor weight is shown in Figure 6.10. The inductor weight is reduced from 1200 g at 20 kHz to 120 g at 200 kHz.

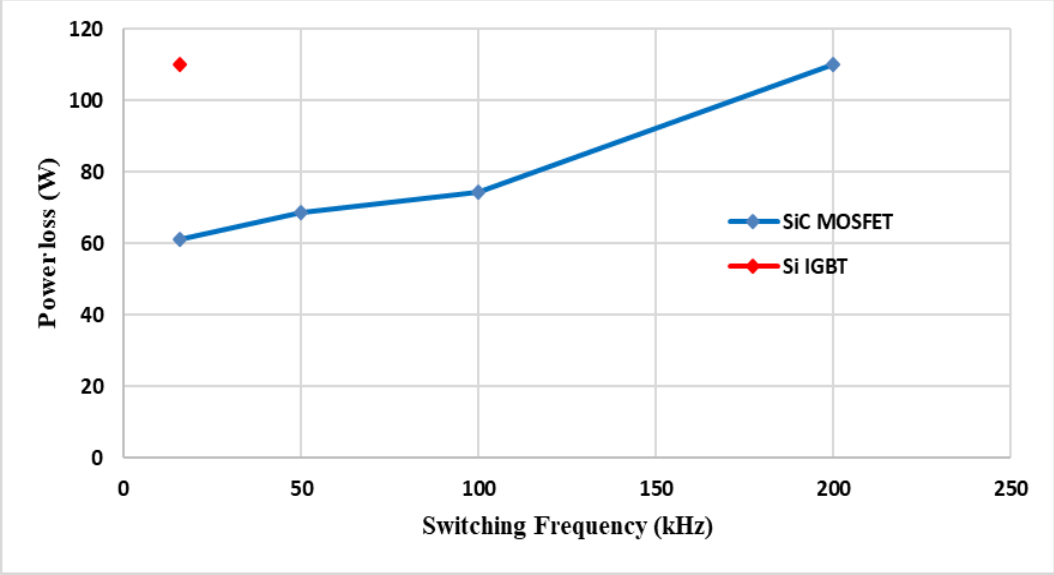


Figure 6. 7 Switching frequency vs. power losses for SiC MOSFET and Si IGBT [53]

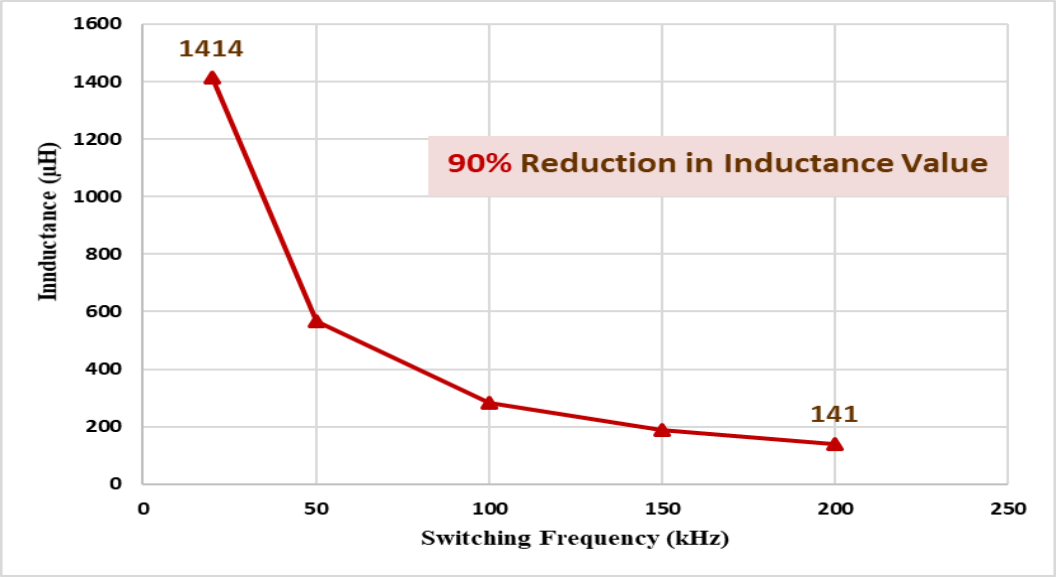


Figure 6. 8 Switching frequency vs. inductor values [53]

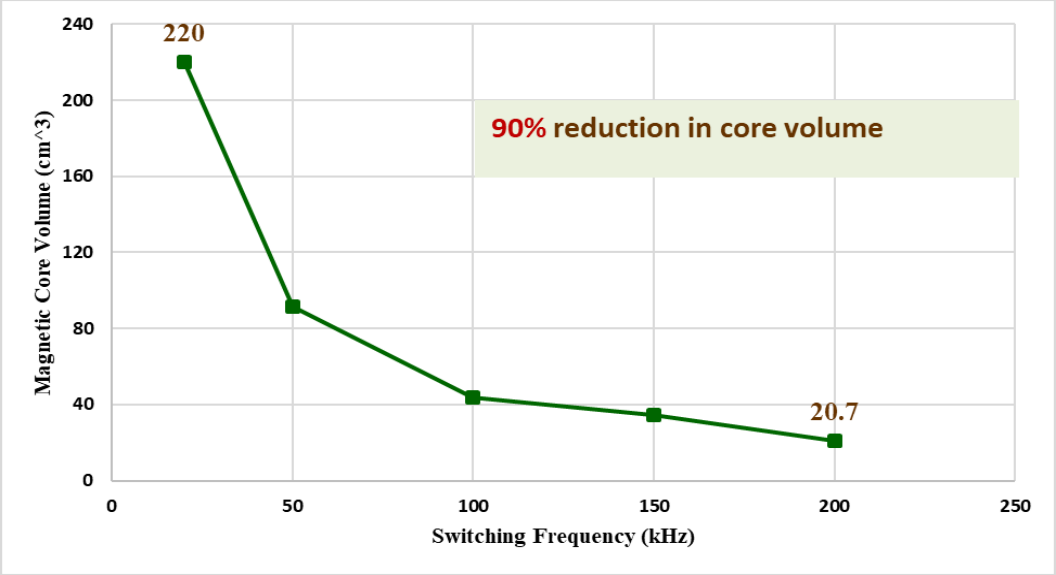


Figure 6. 9 Switching frequency vs. magnetic core volume [53]

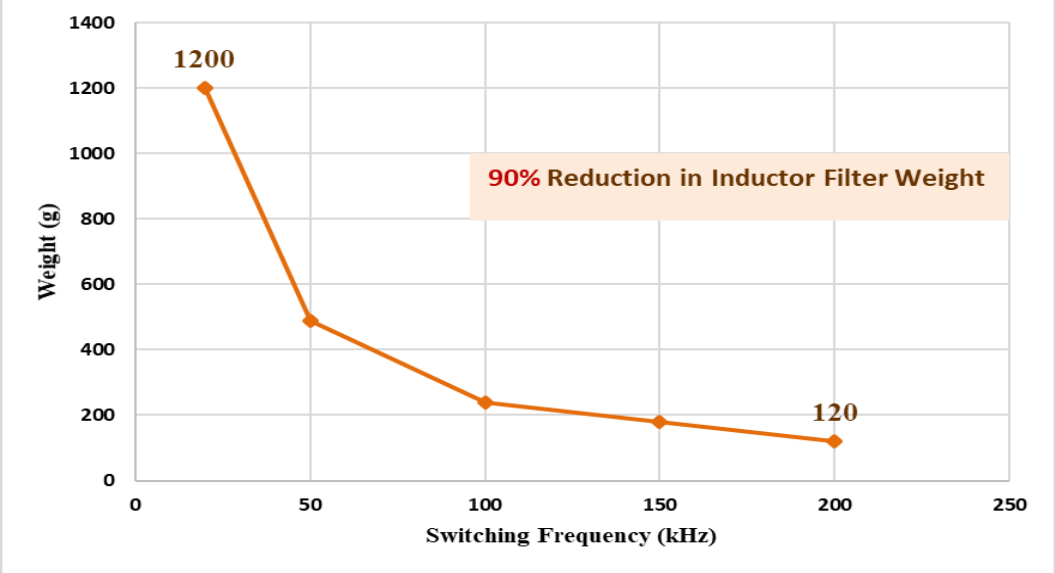


Figure 6. 10 Switching frequency vs. inductor weight [53]

6.3.3 Increasing Power Rating

As explained previously, using SiC MOSFET instead of Si IGBT leads to a significant reduction in total power losses. Therefore, the power rating of the inverter could be increased by adding more power to the load without modifying the size of the heat sink. The output of the inverter can be increased from 1.7 kW using Si IGBT to 3 kW using SiC MOSFET for the same total power semiconductor losses, as illustrated in Figure 6.11. In other words, the power rating of the system can be increased by more than 75% with SiC MOSFET.

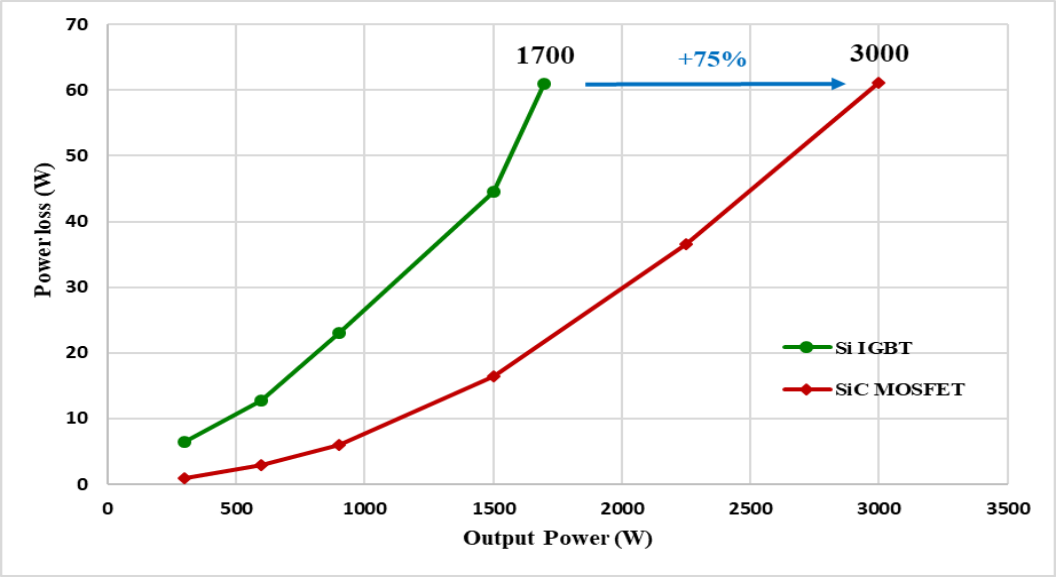


Figure 6. 11 Increased power rating with SiC MOSFET for the same power semiconductor losses [53]

6.4 Thermal Model Simulation and Heat Sink Design

The use of simulation software for modelling thermal performance of heat sinks is not a new practice and has been reported on in the literature [77]–[81]. Commercial software -- like COMSOL Multiphysics, FLUENT, ANSYS, Pro-MECHANICA, etc. -- are prime examples of simulation software that use numerical methods, Finite Element and Finite Volume Methods (FEM and FEV), along with Computer Aided Design (CAD) tools to model the thermal performance of heat sinks.

For the purposes of this paper, COMSOL Multiphysics was used to create two identical 3D models of a 6-pack MOSFET module with silicon (Si) and silicon carbide (SiC) as their respective semiconductor materials. Heat sinks were added to these MOSFET modules to reduce the structures' temperatures and to compare each semiconductor's thermal performance. COMSOL solved for the temperatures of the 3D structure using Finite Element Analysis (FEA). Boyd Corp's online tool, AAVID Genie,

was used to verify the results of the simulated structures with their commercially available heat sinks that were simulated in COMSOL. The Heat Transfer in Solids module of COMSOL simulated the thermal aspects of the models. The Joule heating generated by electric currents passing through each of the MOSFET modules were obtained from calculations made in PowerSim, which were used as the heat sources for the COMSOL calculations. A stationary study was created for each model to study the steady state effects of the Joule heating on the temperature of each structure. The physical dimensions of both MOSFET modules were kept the same and were obtained from the CREE 1200V, 50A 3-Ph SiC MOSFET module [81]. The dimensions of the heat sink for the SiC model were made smaller to demonstrate the superiority of the wide-bandgap (WBG) material SiC in terms of heat sink requirements for similar steady state temperatures. For the purposes of this paper, thermal stresses and physical deformation were not simulated.

6.4.1 Model Geometry

The internal structure the CREE 1200V, 50A 3-Ph SiC MOSFET module consists of multiple layers and components. The dimensions of this internal structure were obtained from [82] to create the 3D CAD model of the module in COMSOL. The module starts from the bottom to the top with a copper (Cu) Baseplate, a solder layer, a copper layer, an aluminium nitride (AlN) layer, and then another copper layer [82]. Six sets of MOSFETs and diodes are soldered on top of the final copper layer [82]. The dimensioned 3D view, the yz-plane view, and the xy-plane view of the MOSFET modules are shown in Figures 6.12, 6.13, and 6.14, respectively. Figure 6.13 is scaled so

that all the layers are viewable. The MOSFETs and diodes were set to be of the same semiconductor material, i.e., Si and SiC, for their respective models.

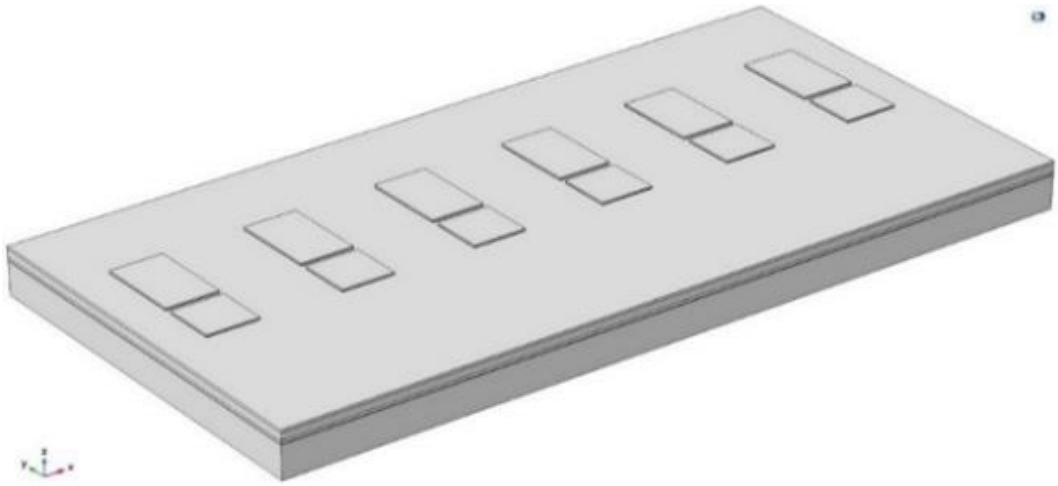


Figure 6. 12 3D View of MOSFET module

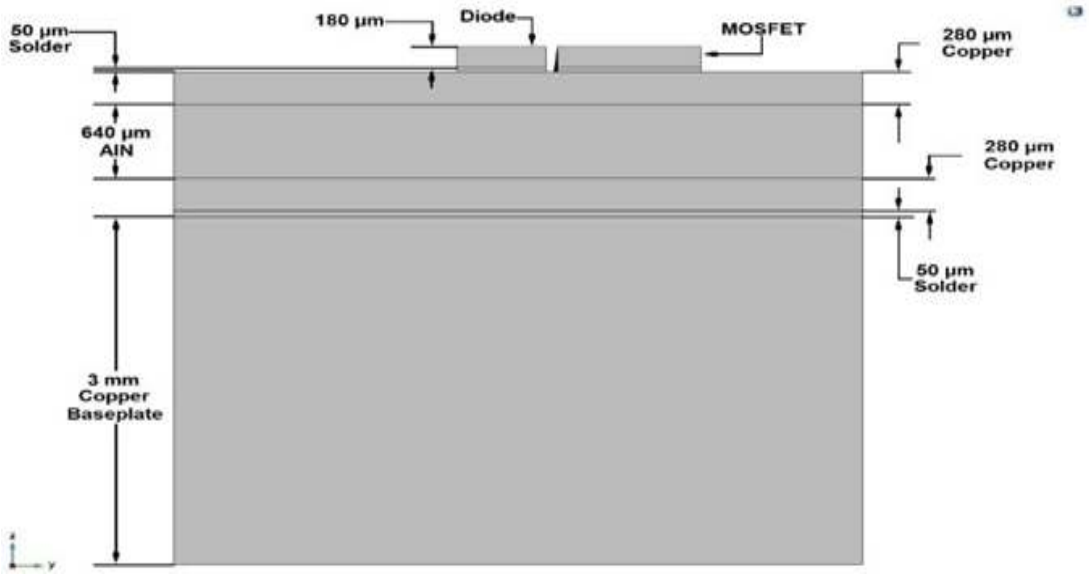


Figure 6. 13 yz-Plane view of the module

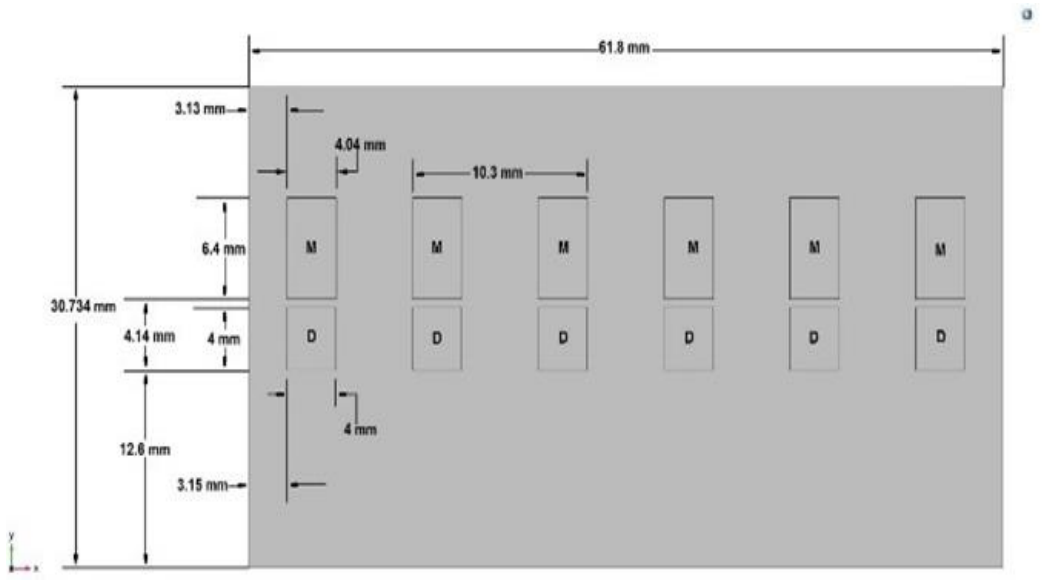
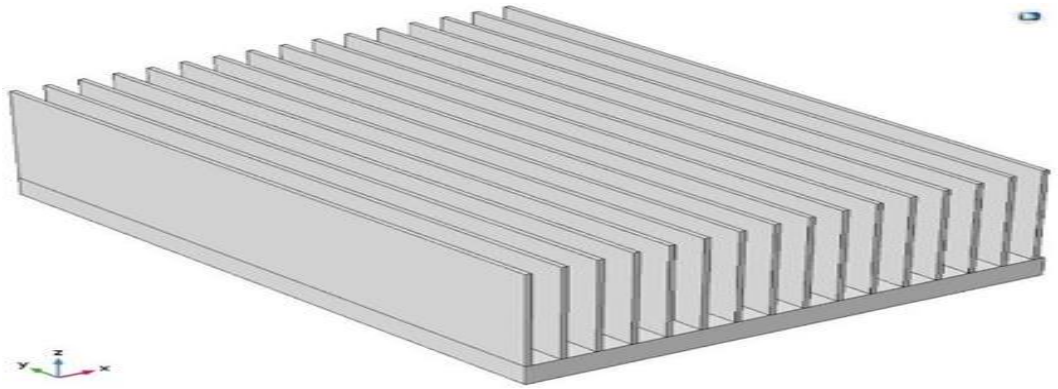
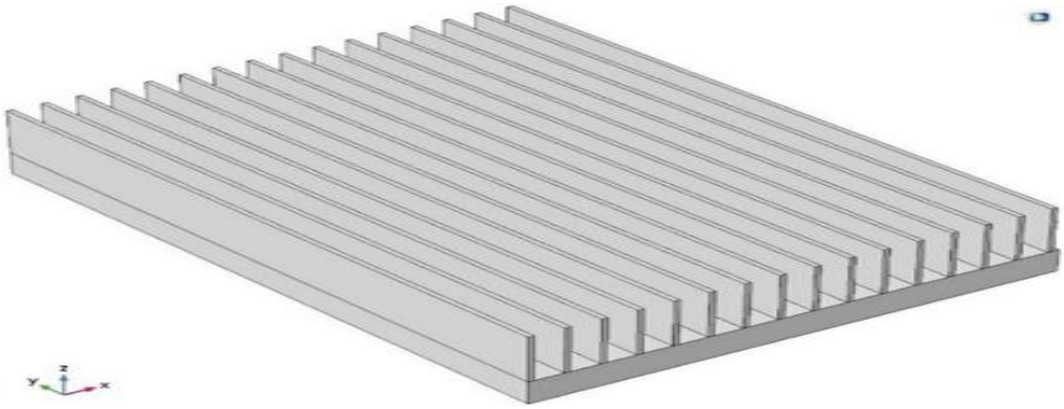


Figure 6. 14 xy-plane view of the module

The final layer of each model consists of an aluminium (Al) heat sink which rests on top of the MOSFET and diode layers. The dimensions of the heat sinks were obtained from Boyd Corporation's online tool, AAVID. These dimensions were based on real world heat sinks sold by Boyd Corp. that would make the maximum temperatures of the module-heat sink combinations below 100º C. The heat sinks used for the Si and SiC modules are shown in Figures 18(a) and 18(b), respectively. Each heat sink consists of a solid aluminium block with the dimensions: 141.8 mm × 104.3 mm. × 6.6 mm. A total of 16 aluminum fins (width of 1.134 mm) separated by 6.8 mm were added on top of this block with heights of 33.5 mm and 13.4 mm for the Si and SiC models, respectively.



(a)



(b)

Figure 6. 15 Heat sink structure. (a) Si model; and (b) SiC model

6.4.2 Material Properties

The physical material properties of both models were Density ρ, heat capacity at constant pressure (cp), and thermal conductivity (k). Only these three properties were used for the simulations because heat transfer in solids was the only physics being studied. The materials were assumed to be isotropic with every property considered to be constant in all three directions (xyz). The properties for all materials simulated in the models, except for the solder, were obtained from built-in libraries in COMSOL. SAC396 solder, an alloy of tin, silver and copper, was chosen for the models and its

properties were obtained from [83]. The material properties for all the materials used are given in Table 6.3.

Table 6. 3 Thermal properties of materials used

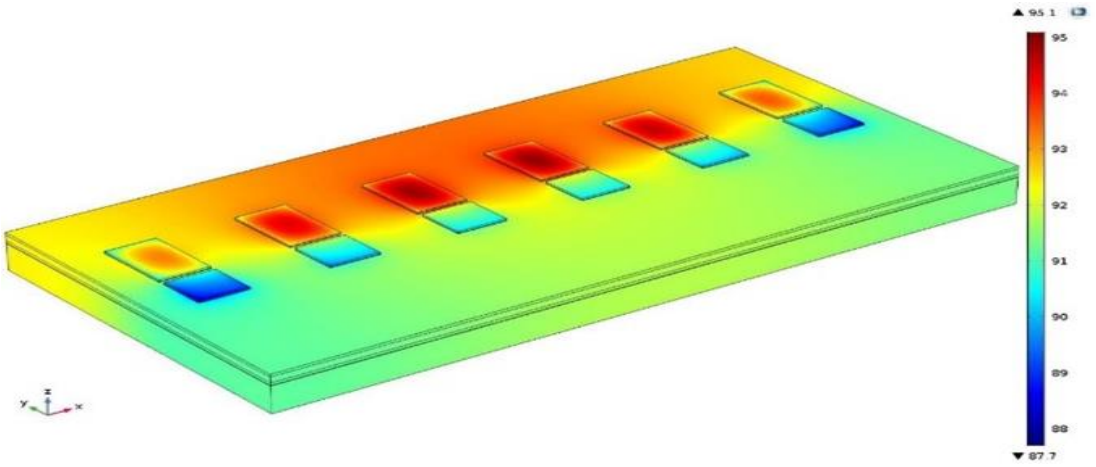
Property	Symbol	Unit	Cu	SA C396	AIN	Si	SiC	Al
Density	ρ	kg/m^3	8960	7400	3260	2329	3216	2700
Heat Capacity at Constant Pressure	C_p	J/(kg.K)	385	220	740	700	690	900
Thermal Conductivity	k	W/(m.K)	400	61.1	160	131	490	238

6.4.3 Heat Transfer Physics Modelling

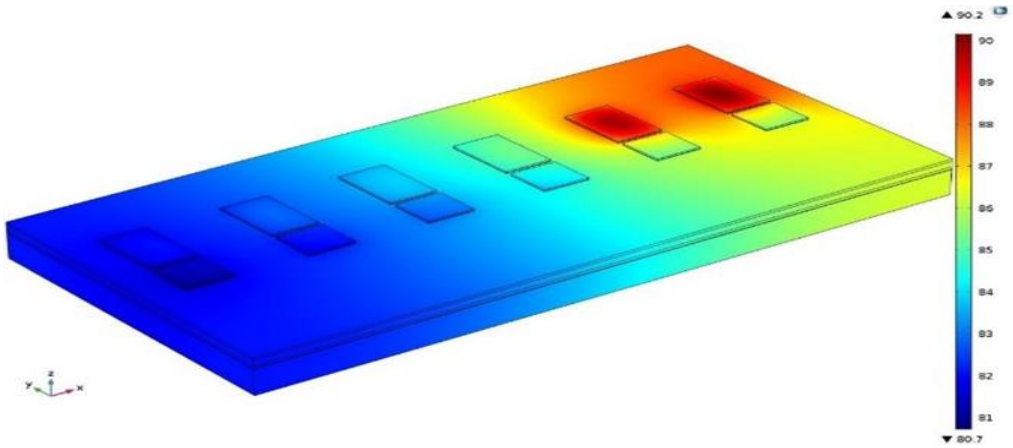
The heat transfer in the solids physics module of COMSOL was used to simulate the thermal performance of each MOSFET-heat sink structure. The heat losses calculated in PowerSim for each MOSFET in each semiconductor model were input as heat sources for the simulations. For the Si model, these losses, going from left to right were: 19.85 W, 19.85 W, 19.85 W, 19.85 W, 20.4 W, and 20.4 W; for the SiC, the losses were: 4.1 W, 4.1 W, 4.1 W, 4.1 W, 22.25 W, and 22.25 W, respectively. As the heat sinks dissipate, thermal energy from the heat generated by the MOSFETs to the surrounding air, a convective heat flux boundary condition for all heat sink surfaces in contact with that air was set up. The convective heat transfer coefficient was given a value of 10.45 $W/m^2.K$ to simulate non-forced free flowing air. The initial temperature of the structures and surrounding air was set to room temperature (i.e., 293.15 K or 20º C). Using these inputs and boundary conditions, COMSOL solved the heat equation in solids to obtain the temperature profiles of each model.

6.4.4 Model Simulation and Results

The temperature profile of the Si and SiC models with the heat sinks hidden are shown in Figure 6.16(a) and Figure 6.16(b). The temperature profiles for the Si and SiC models with the heat sinks visible are given in Figures 6.17 and 6.18. The temperatures displayed on the legends are in Celsius.



(a)



(b)

Figure 6. 16 Temperature profile of SiC model with heat sink not visible. (a) Si; and, (b) SiC. [53]

The temperature profiles for the Si and SiC models with the heat sink not visible show that the highest of temperatures are concentrated around the MOSFETs that have the highest heat losses. As the heat losses for all Si IGBTs are close to 20 W, the temperatures are fairly uniform throughout the Si MOSFET module structure whereas for the SiC model, the temperatures are higher at the right end near the MOSFETs with losses of 20.25 W losses while the left end with lower losses has lower temperatures.

The temperature profiles for the two models with the heat sink visible also show a similar distribution of temperatures. The Si model has higher temperatures on the heat sink that are fairly uniform around all the IGBTs, while the SiC model has higher temperatures more concentrated at the right end where the MOSFETs with higher losses are located.

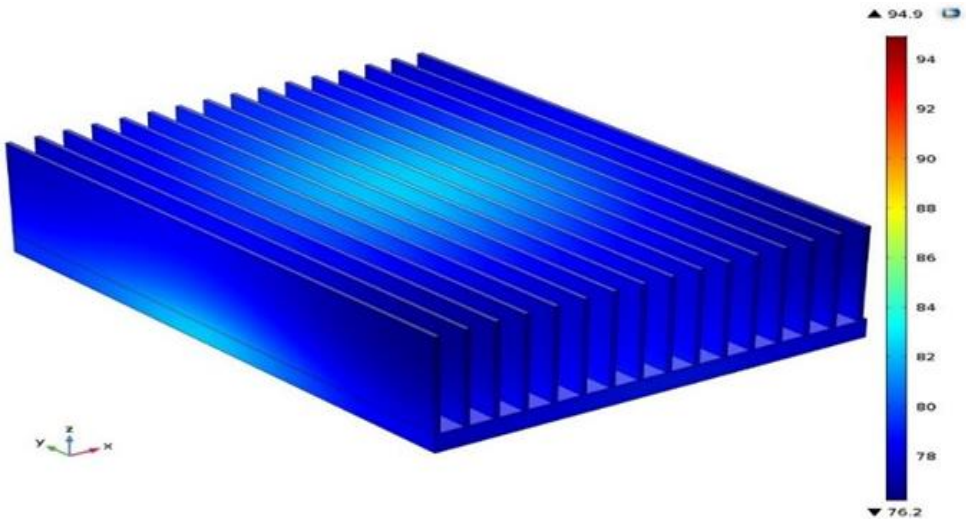


Figure 6. 17 Temperature profile of Si model with heat sink visible [53]

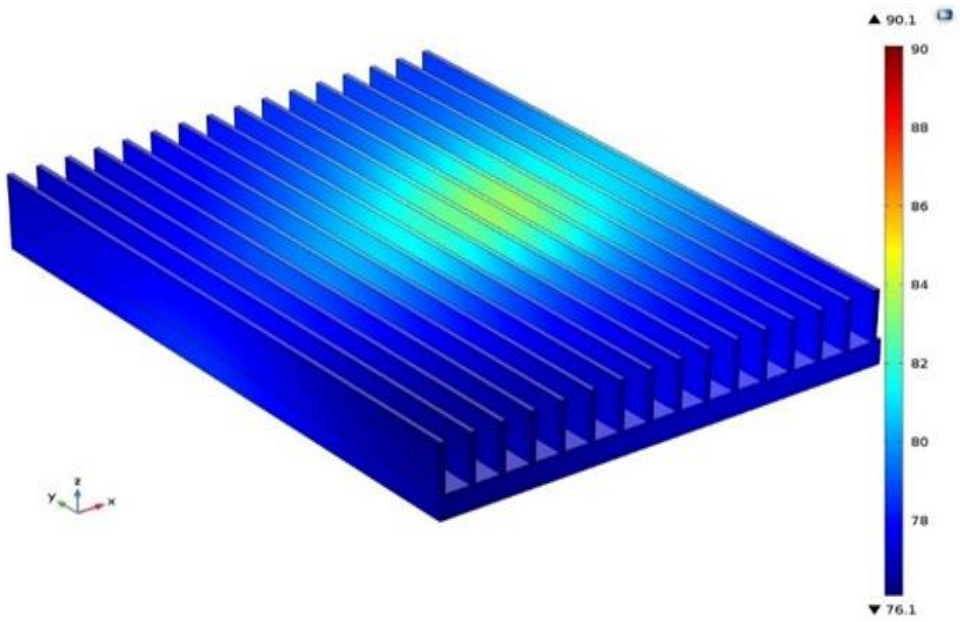


Figure 6. 18 Temperature profile of SiC model with heat sink visible [53]

The maximum temperatures for the Si and SiC models were found to be 95.15 ºC and 90.18 ºC respectively. The minimum temperatures were 76.23 ºC and 76.10 ºC for the Si and SiC models, respectively. The 3D model for the Si IGBTs had a volume of 183.8 cm^3 and surface area of 1,861 cm^2 for the heat sink. The SiC model had a volume of 132.1 cm^3 and surface area of 941.2 cm^2. From the simulations of the two models, it is clear that the SiC MOSFET module requires a smaller heat sink (by a factor of .505 – or approximately half - in terms of surface area) for similar maximum temperatures. High temperatures are more uniform in the Si model while only the areas with higher losses have areas of high temperature concentrations throughout the overall volume of the MOSFET module with SiC. The thermal modelling clearly demonstrates that the SiC module is more efficient in terms of heat sink size and overall heat dissipation.

6.5 Conclusion

The benefits of using WBG-based power devices, such as SiC MOSFET is investigated in this chapter. The benefits of using SiC MOSFET at 650 V blocking voltage is investigated in the proposed high gain boost converter and compared to those of Si MOSFET. The simulation results show that switching and conduction losses are reduced by more than 90% and 65%, respectively, with SiC MOSFET. Also, the efficiency of the system improved by more than 4% with SiC MOSFET at a high switching frequency of 300 kHz. Next, the benefits of using SiC MOSFET at 1200 V blocking voltage is studied in the proposed transformerless inverter and compared to those of using Si IGBT. The simulation results show that total switching and conduction losses are reduced by 50% at 16 kHz and the efficiency increased from 96% to 98% with SiC MOSFET. The benefits of using SiC devices become more obvious at a high switching frequency of 100 kHz where the efficiency increases by about 14%. The significant reduction of the total switching and conduction losses opens the possibility of increasing the inverter power rating level with SiC MOSFET. For example, the power rating of the inverter at 16 kHz with Si IGBT is increased by 75%, from 1.7 kW to 3 kW, with the same power losses when SiC MOSFET is used. Furthermore, SiC MOSFET has superior switching characteristics, which allow the system to increase its switching frequency by a factor of 15 while still having the same power semiconductor losses as an Si IGBT based inverter. By taking advantage of this fact, the volume and weight of the inductor filter may be reduced dramatically from 220 cm^3 to 20.7 cm^3 and from 1.2 kg to 120 g, respectively. Finally, thermal analysis shows that SiC MOSFET requires smaller

heat sink compared to Si IGBT under the same switching frequency and output power load. Accordingly, SiC devices are an attractive solution for residential PV applications that require high efficiency and small converter size.

Chapter 7. Improved Proposed Converter for Reactive Power Generation and Leakage Current Elimination

7.1 Introduction

Several transformerless inverter topologies have been presented and published [83]–[85]. One of the drawbacks of PV transformerless inverters is the generating of leakage current due to the absence of a transformer. High generation of leakage current increases system losses, THD, electromagnetic interference (EMI), and can cause personal safety issues [86]–[93]. The literature cites various modulation techniques that have been used to eliminate or minimize leakage current.

Many transformerless inverter topologies with unipolar modulation technique have been introduced to increase system efficiency and reduce the leakage current by disconnecting the AC and DC sides during the freewheeling modes, this is known as galvanic isolation. Many topologies have been derived and developed based on this method, including highly efficient and reliable inverter concept (HERIC), the H5 inverter, and the H6 topology [94], [95]. However, complete elimination of leakage current cannot be achieved with galvanic isolation method alone because common mode voltage (CMV) during freewheeling periods cannot be identified by the switching state, which means that it is not constant. Therefore, modulation strategies and converter structures must be modified so that CMV becomes constant during all inverter operating modes.

Most of the modulation techniques are designed for the application of a unity power factor. Indeed, next-generation PV inverters are required to support reactive power to allow for the high penetration of PV inverters to be connected to the utility grid [96]–[99]. Several international standards have been reviewed to achieve reactive power support. As reported by VDE-AR-N4105, PV grid connected inverters must have the ability to generate reactive power.

Considering all this, a traditional bipolar modulation technique is proposed as a possible candidate to be used in next-generation PV inverters, because it has the ability to generate reactive power and eliminate leakage current. Nevertheless, using bipolar modulation techniques to generate reactive power will increase switching losses and degrade system efficiency as it is a two-level modulation.

The Si MOSFET based transformerless inverter is highly efficient in generating reactive power, but the inverter design must be optimized to address the fact that the Si MOSFET's body diode has poor reverse recovery performance, which may lead to device failure [100]–[103]. These inverters are based on the idea of avoiding the conduction of an anti-parallel diode, which will result in a more complicated and complex inverter that in turn increases costs. On the other hand, the SiC MOSFET's body diode has superior reverse recovery performance because it has a shorter minority carrier lifetime [104]–[113]. Therefore, reactive power generation with SiC MOSFET can be achieved without any alteration to the converter structure or adding any additional freewheeling diodes (FWD).

7.2 Proposed Topology with Leakage Current Elimination and Reactive Power Generation

The proposed H6 topology is derived from conventional H6 topology where the sixth switch is repositioned and connected to the A terminal [114]–[115]. The proposed topology and its switching pattern are presented in Figures 7.1 and 7.2. The proposed topology has low conduction loss compared to traditional topologies, such as H5 and H6, because the number of conducting switches is reduced from six switches to five switches.

On the other hand, only using galvanic isolation will not maintain the desired constant CMV during the freewheeling period. Since the inverter output terminals A and B are floating during the freewheeling periods with respect to DC side, this means that CMV cannot be determined from the switching states. Accordingly, generation of leakage current cannot be fully controlled with the galvanic isolation method. Therefore, the proposed topology is improved by incorporating clamped method technique to eliminate the leakage current and achieve constant CMV during the freewheeling period, as shown in Figure 7.3. The dc link capacitor is divided into two series capacitors to achieve voltage divider. In the clamping method, an extra active switch is added to the proposed topology. This switch is known as a clamping switch and is placed between the midpoint of the freewheeling switches and the midpoint of the dc link capacitors.

The generation of reactive power cannot be accomplished in single phase transformerless inverter topologies because the existing modulation techniques are not adopted for a freewheeling path in the negative power region. To use unipolar PWM in the negative power region, the line to line voltage (V_{AB}) must have three values, + V_{DC}, -

V_{DC}, and zero. It is observed that zero voltage states cannot be achieved in the negative power regions because there is no current path established, as illustrated in Figure 7.4. The modulation method is modified to achieve leakage current elimination and reactive power generation, as shown in Figure 7.5.

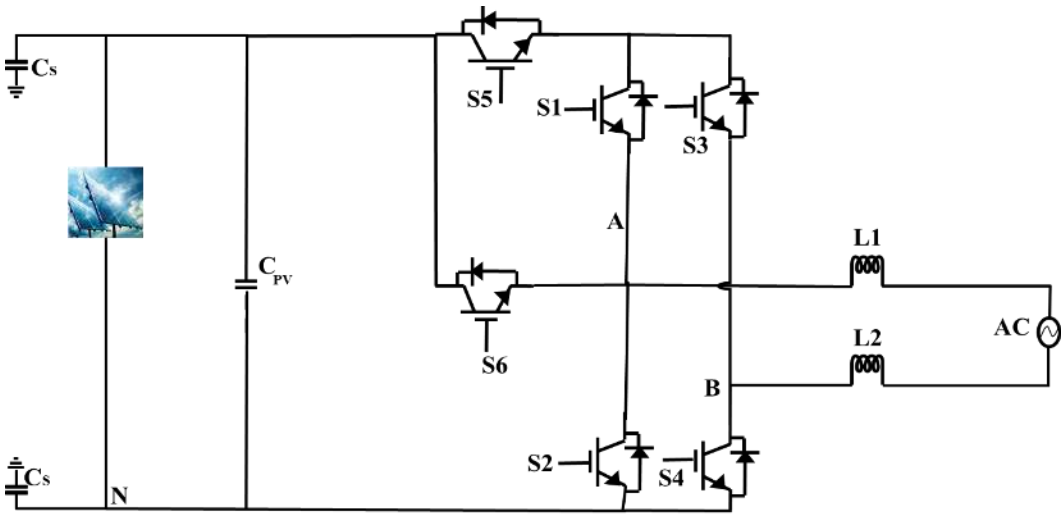


Figure 7. 1 Circuit diagram of proposed transformerless inverter topology

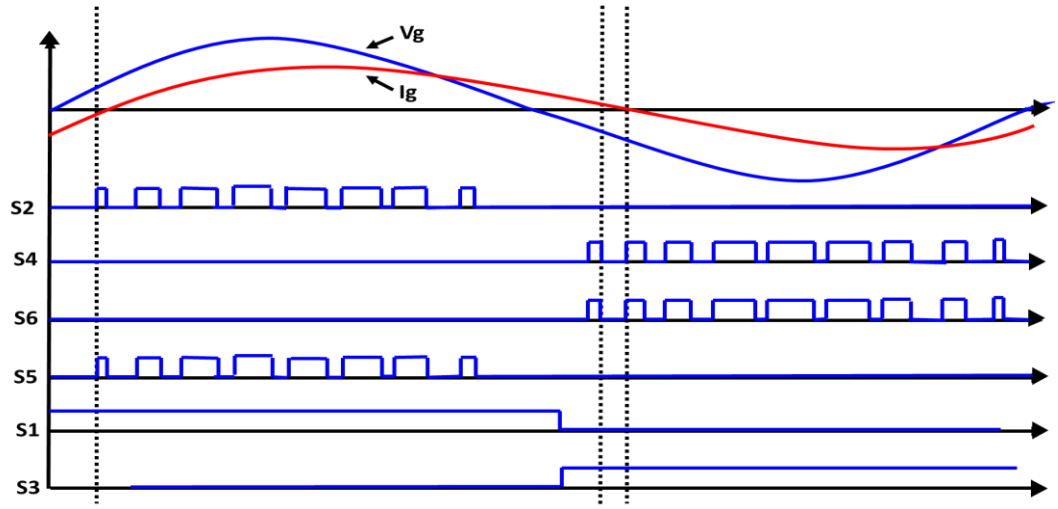


Figure 7. 2 Modulation strategy of the proposed transformerless inverter

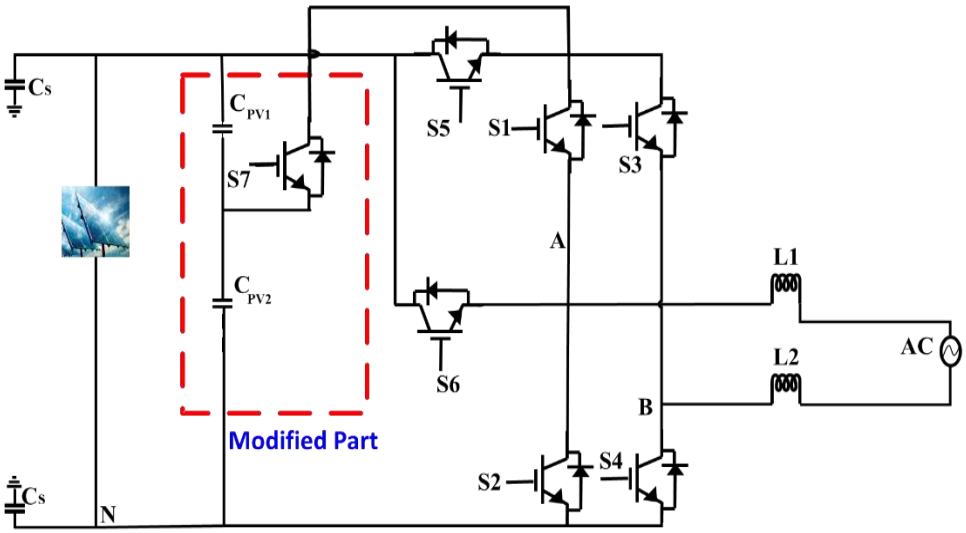
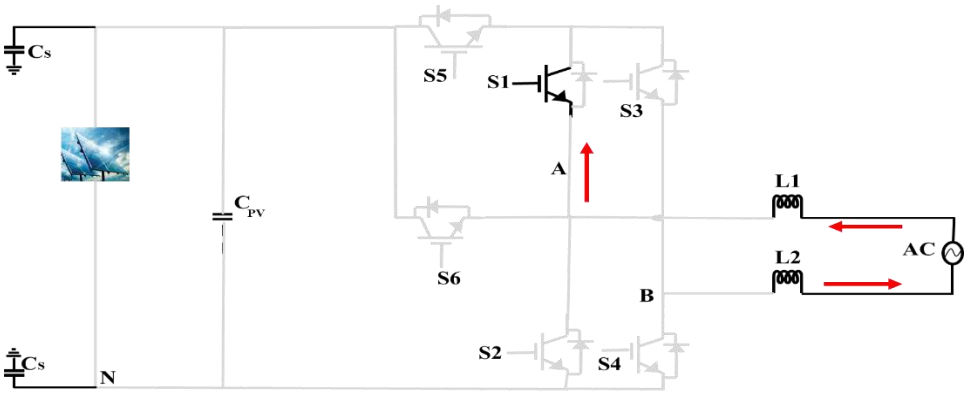
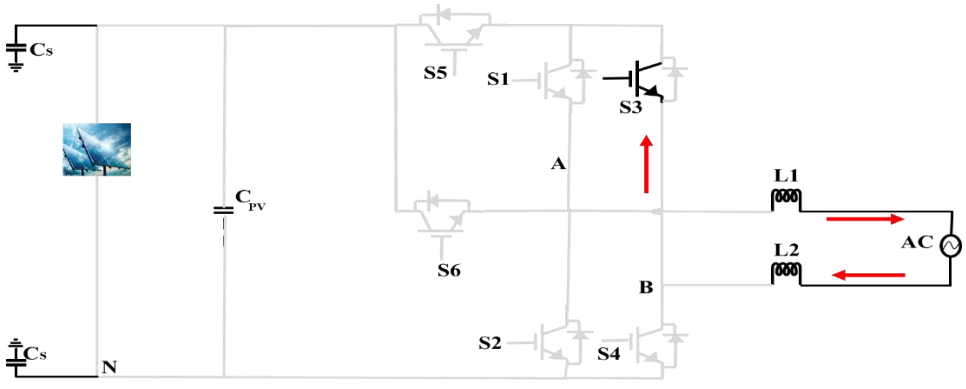


Figure 7. 3 Modified proposed transformerless inverter [116]



(a)



(b)

Figure 7. 4 Operation modes of the negative power region during freewheeling periods. (a) V_g is positive and I_g is negative; and, (b) V_g is negative and I_g is positive

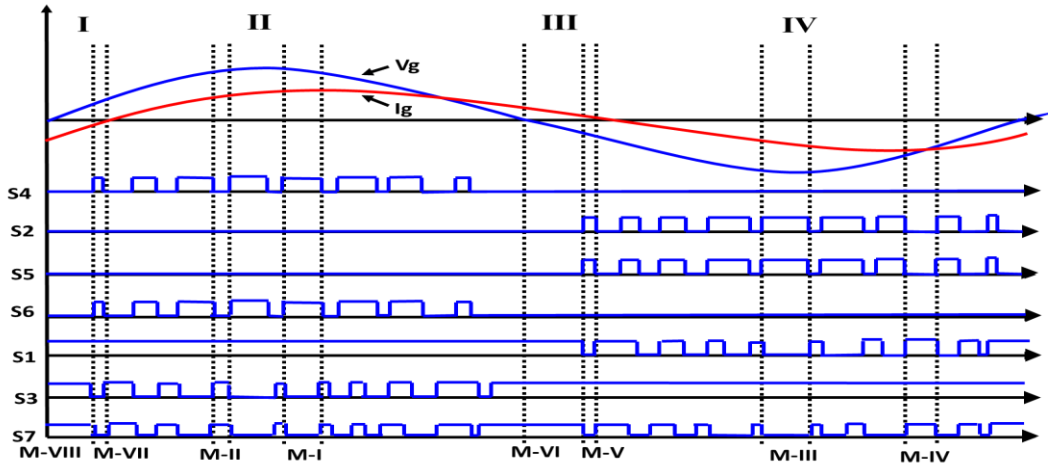


Figure 7. 3 Modified modulation strategy for leakage current elimination and reactive power generation

7.2 Modulation Technique for Reactive Power Generation

The proposed PWM modulation technique divided into four regions and eight modes, as shown in Figure 7.5. In regions II and IV, the power is positive where Ig and Vg have the same polarity. The power is negative in regions I and III where Ig and Vg have an opposite sign. The operation modes are described as follows.

Mode-I is the active mode in the positive power region (both I_g and V_g are positive). In this mode, S_1, S_6, and S_4 are turned ON, and the other switches are turned OFF, as shown in Figure 7.6(a). The inductor current is flowing through S_4 and S_6. The common mode voltage in Mode-I is calculated as follows:

$$v_{AN} = V_{PV} \tag{7.1}$$

$$v_{BN} = 0 \tag{7.2}$$

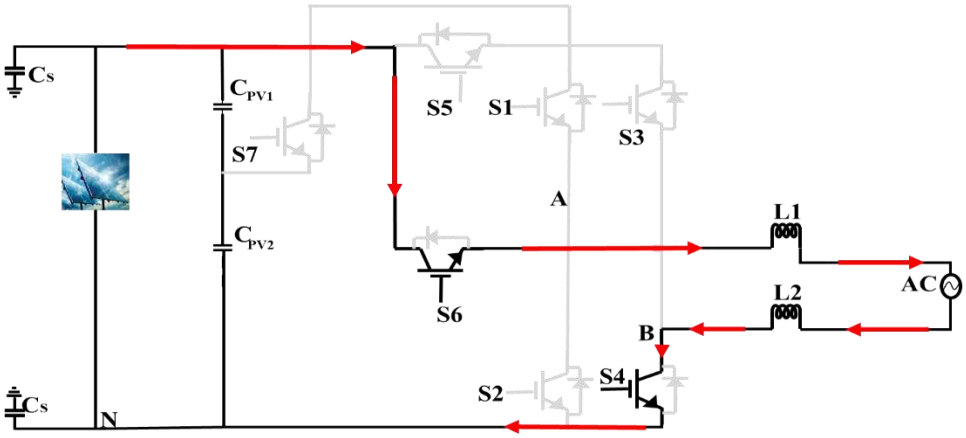
$$v_{CM} = \frac{v_{AN} + v_{BN}}{2} = 0.5V_{PV} \tag{7.3}$$

Mode-II is the freewheeling mode in the positive power region (both I_g and V_g are positive). In this mode, S_1, S_3, and S_7 are turned ON and the other switches are turned

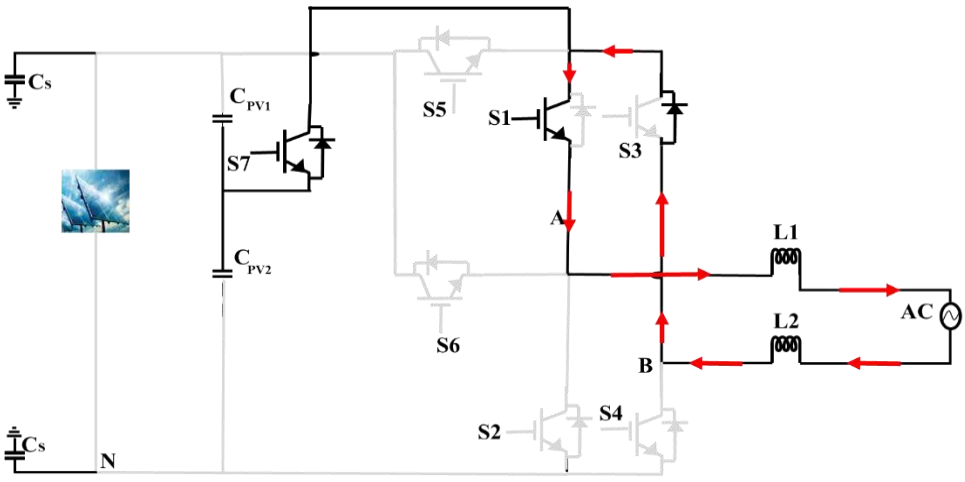
OFF, as shown in Figure 7.6(b). The inductor current is flowing through S_1 and the antiparallel diode of S_3. The common mode voltage in Mode-II is given as:

$$v_{AN} = v_{BN} = 0.5V_{PV} \tag{7.4}$$

$$v_{CM} = \frac{v_{AN} + v_{BN}}{2} = 0.5V_{PV} \tag{7.5}$$



(a)



(b)

Figure 7. 4 Operation modes of the proposed topology. (a) I_g and V_g are positive; and, (b) the zero state during this interval

Mode-III is the active mode in the positive power region (both I_g and V_g are negative). In this mode, S_5, S_3, and S_2 are turned ON and the other switches are turned OFF as shown in Figure 7.7(a).

The inductor current is flowing through S_2, S_3, and S_5. The common mode voltage in Mode-III is expressed as:

$$v_{AN} = 0 \tag{7.6}$$

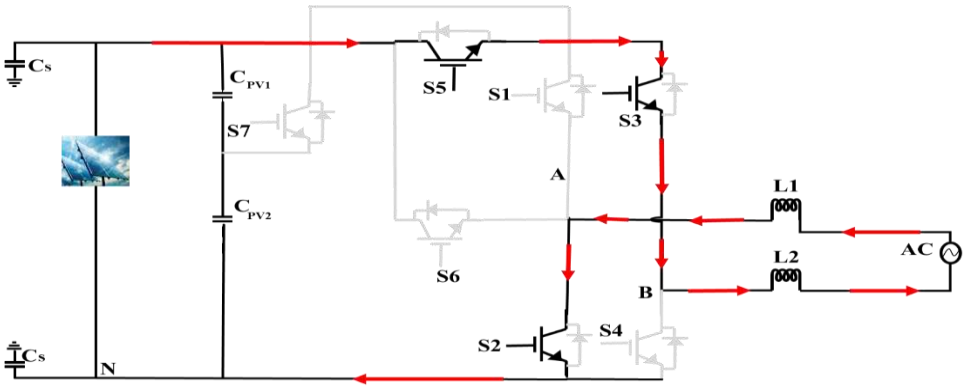
$$v_{BN} = V_{PV} \tag{7.7}$$

$$v_{CM} = \frac{v_{AN} + v_{BN}}{2} = 0.5V_{PV} \tag{7.8}$$

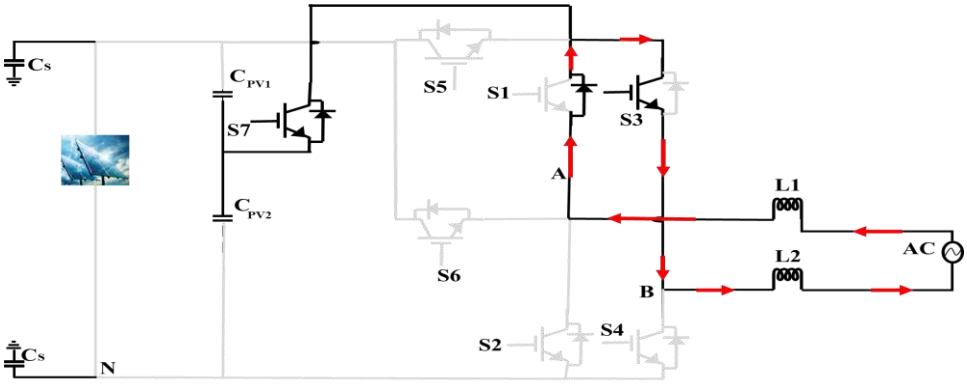
Mode-IV is the freewheeling mode in the positive power region (both I_g and V_g are negative). In this mode, S_1, S_3, and S_7 are turned ON and the other switches are turned OFF, as shown in Figure 7.7(b). The inductor current is flowing through S_3 and the antiparallel diode of S_1. The common mode voltage in Mode-IV is calculated as follows:

$$v_{AN} = v_{BN} = 0.5V_{PV} \tag{7.9}$$

$$v_{CM} = \frac{v_{AN} + v_{BN}}{2} = 0.5V_{PV} \tag{7.10}$$



(a)



(b)

Figure 7. 5 Operation modes of the proposed topology. (a) I_g and V_g are negative; and, (b) the zero state during this interval

Mode-V is the active mode in the negative power region (I_g is positive and V_g is negative). In this mode, S_4 and S_6 are OFF, while S_2, S_5, and S_3 are ON; thus, inductor current freewheels through the anti-parallel diodes of S_2, S_5, and S_3, as given in Figure 7.8(a). V_{CM} is determined as:

$$v_{AN} = 0 \tag{7.11}$$

$$v_{BN} = V_{PV} \tag{7.12}$$

$$v_{CM} = \frac{v_{AN} + v_{BN}}{2} = 0.5V_{PV} \tag{7.13}$$

Mode-VI is the freewheeling mode in the negative power region (I_g is positive and V_g is negative). In this mode, S_1 commutates complementary to S_2 and S_5 at the

switching frequency instead of being OFF for the whole negative period as in the conventional unipolar PWM modulation. In this arrangement, a new current path is created to generate zero-voltage by turning OFF S_2, S_4, S_5, and S_6 and turning ON S_1, S_3, and S_7. Thus, the inductor current passes over S_1 and the antiparallel diode of S_3 as depicted in Figure 7.8(b). V_{CM} is determined as:

$$v_{AN} = v_{BN} = 0.5V_{PV} \tag{7.14}$$

$$v_{CM} = \frac{v_{AN} + v_{BN}}{2} = 0.5V_{PV} \tag{7.15}$$

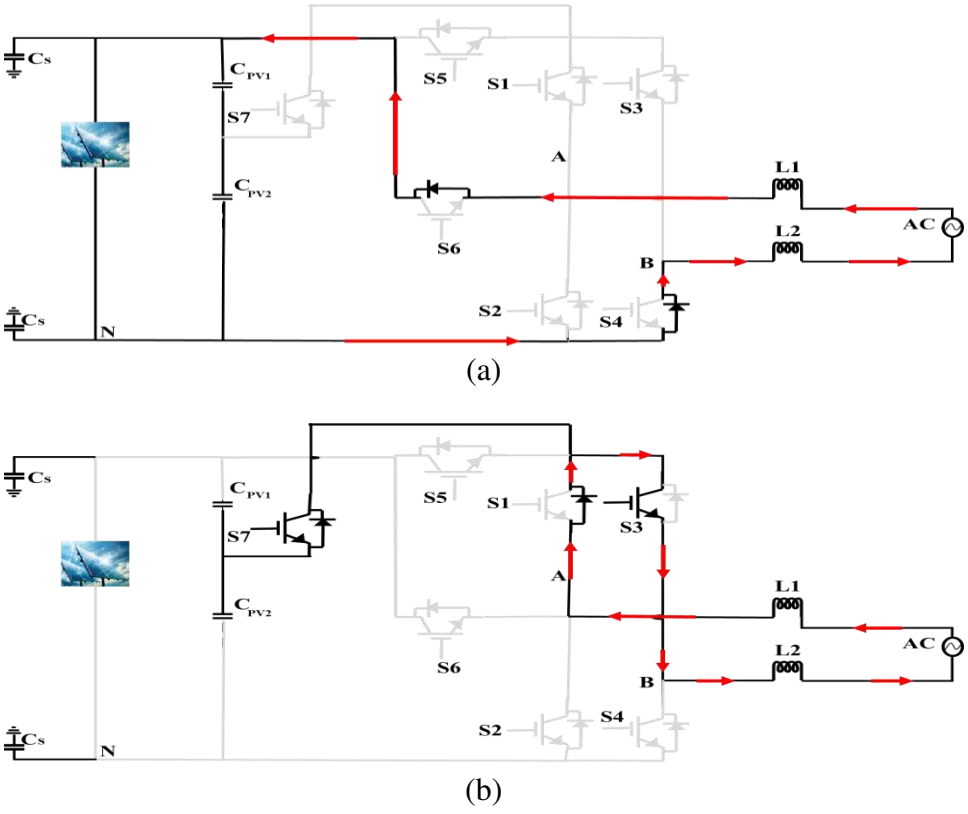


Figure 7. 6 Operation modes of the proposed topology. (a) V_g is positive and I_g is negative; and, (b) the zero state during this interval

Mode-VII is the active mode in the negative power region (I_g is negative and V_g is positive). In this mode, S_2, S_5, and S_3 are OFF while S_4, S_6, and S_1 are ON; thus, inductor current freewheels through the anti-parallel diodes of S_4 and S_6, as shown in Figure 7.9(a). V_{CM} is determined as:

$$v_{AN} = V_{PV} \tag{7.16}$$

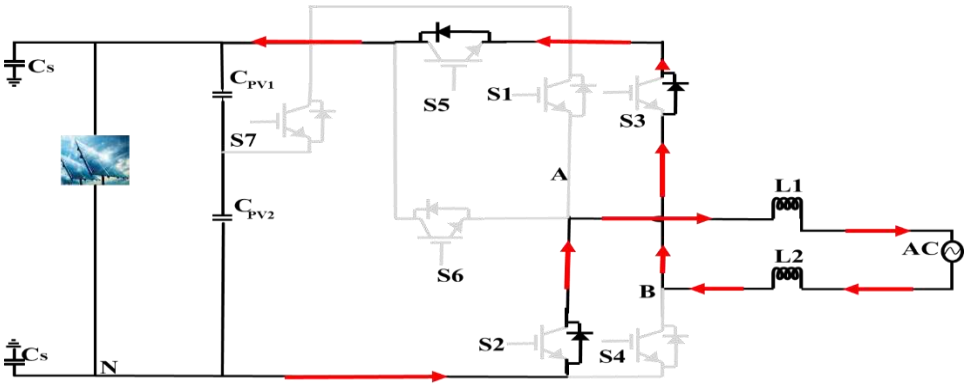
$$v_{BN} = 0 \tag{7.17}$$

$$v_{CM} = \frac{v_{AN} + v_{BN}}{2} = 0.5V_{PV} \tag{7.18}$$

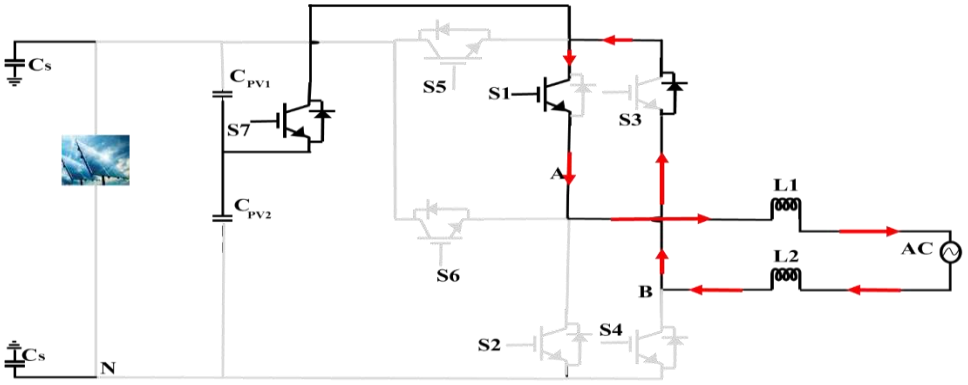
Mode VIII is the freewheeling mode in the negative power region (I_g is negative and V_g is positive). In this mode, S_3 commutates complementary to S_4 and S_6 at the switching frequency instead of being OFF for the whole positive period, as in the conventional unipolar PWM modulation. In this arrangement, a new current path is created to generate zero-voltage by turning OFF S_2, S_4, S_5, and S_6 and turning ON S_1, S_3, and S_7. Thus, the inductor current passes over S_3 and the antiparallel diode of S_1 as depicted in Figure 7.9(b). V_{CM} is determined as:

$$v_{AN} = v_{BN} = 0.5V_{PV} \tag{7.19}$$

$$v_{CM} = \frac{v_{AN} + v_{BN}}{2} = 0.5V_{PV} \tag{7.20}$$



(a)



(b)

Figure 7. 7 Operation modes of the proposed topology. (a) V_g is negative and I_g is positive; and, (b) the zero state during this interval

By implementing the proposed modulation, a new current path is created in region II and IV to achieve a zero-voltage state. Therefore, the three output voltages generated +VDC, 0, and -VDC, which satisfy the principle operation of unipolar PWM modulation technique. The main concept of the proposed modulation technique is to create a bidirectional current path of S1 and S3 during the negative power region. As a result, reactive power generation can be achieved with the proposed modulation technique. Moreover, the proposed modulation technique maintains a constant common mode voltage at VDC/2 over all the operation modes, which will result in eliminating leakage current. Consequently, the proposed H6 topology with the modified unipolar PWM

modulation technique is suitable for the next generation of PV transformerless inverter applications.

7.3 Simulation Results

PSIM and MATLAB/SIMULINK simulation software programs were used to design the proposed topology to evaluate its performance. The parameters of the system design are shown on Table 7.1. The simulation included two switching frequencies: 16 kHz and 100 kHz.

Table 7. 1 System Design Parameters

Parameter	Value
Input Voltage	800 V
Grid Voltage	120 V
Grid Frequency	60 Hz
Switching Frequency	16 kHz and 100 kHz
DC Bus Capacitor (C_{DC})	970 µF
Stray Parasitic Capacitance	300 nF
Output Power	3kW

The CM characteristics of the proposed topology, with only galvanic isolation, are given in Figure 7.10.

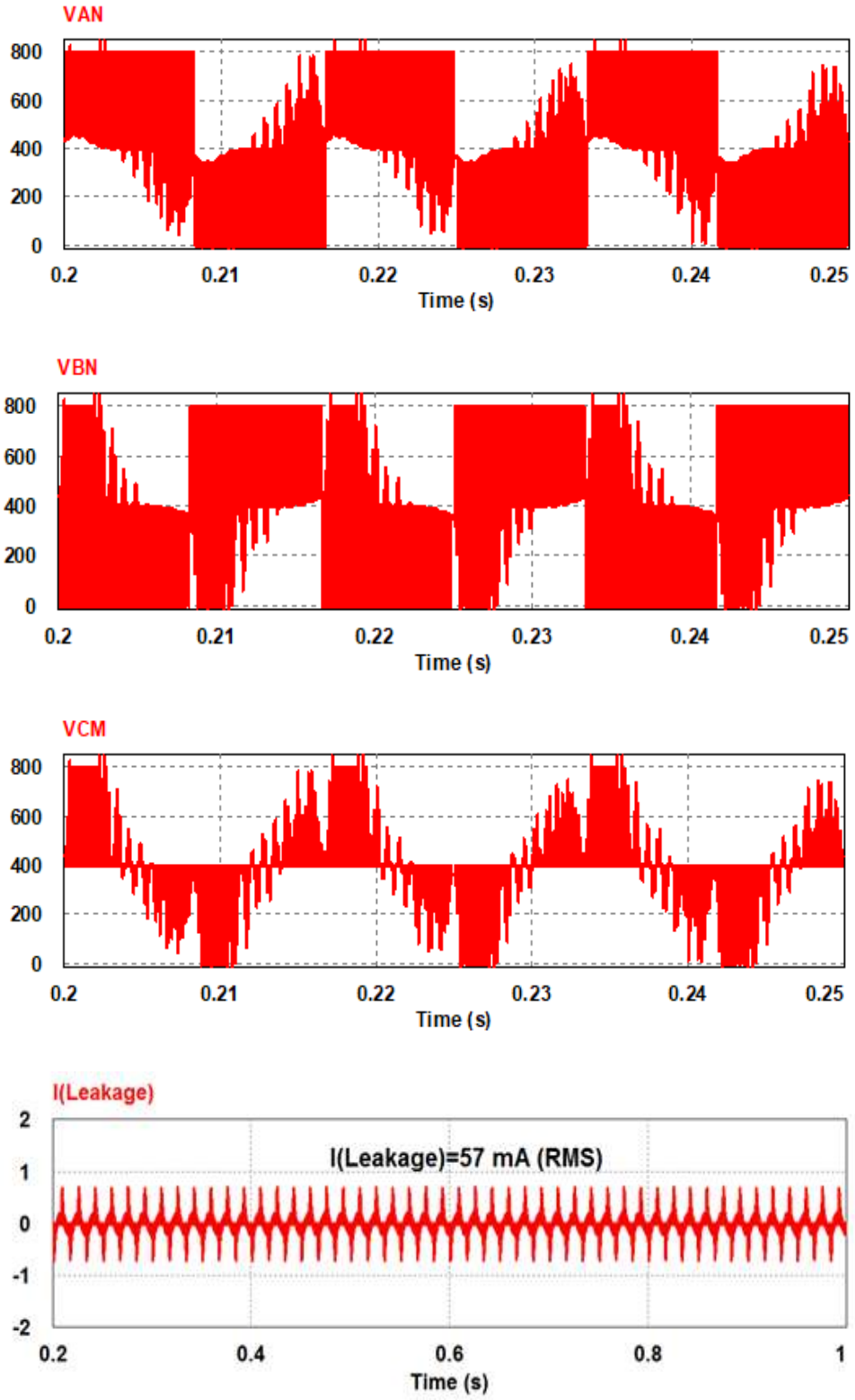


Figure 7. 8 CM characteristics of the proposed topology

It is observed that the voltage waveforms of V_{AN} and V_{BN} are oscillating. Also, the common mode voltage V_{CM} is oscillating and not constant at 400 V. Therefore, there is a flow of leakage current that cannot be eliminated. To resolve this problem, the proposed topology is modified with a clamping method and the CM characteristics, such as V_{AN}, V_{BN}, V_{CM} and $I_{Leakage}$, that are shown in Figure 7.11. It is also noted that the voltage waveforms of V_{AN} and V_{BN} are smooth and complementary to each other. As a result, the V_{CM} is totally clamped to 400 V over the whole period, which will lead to a total elimination of leakage current.

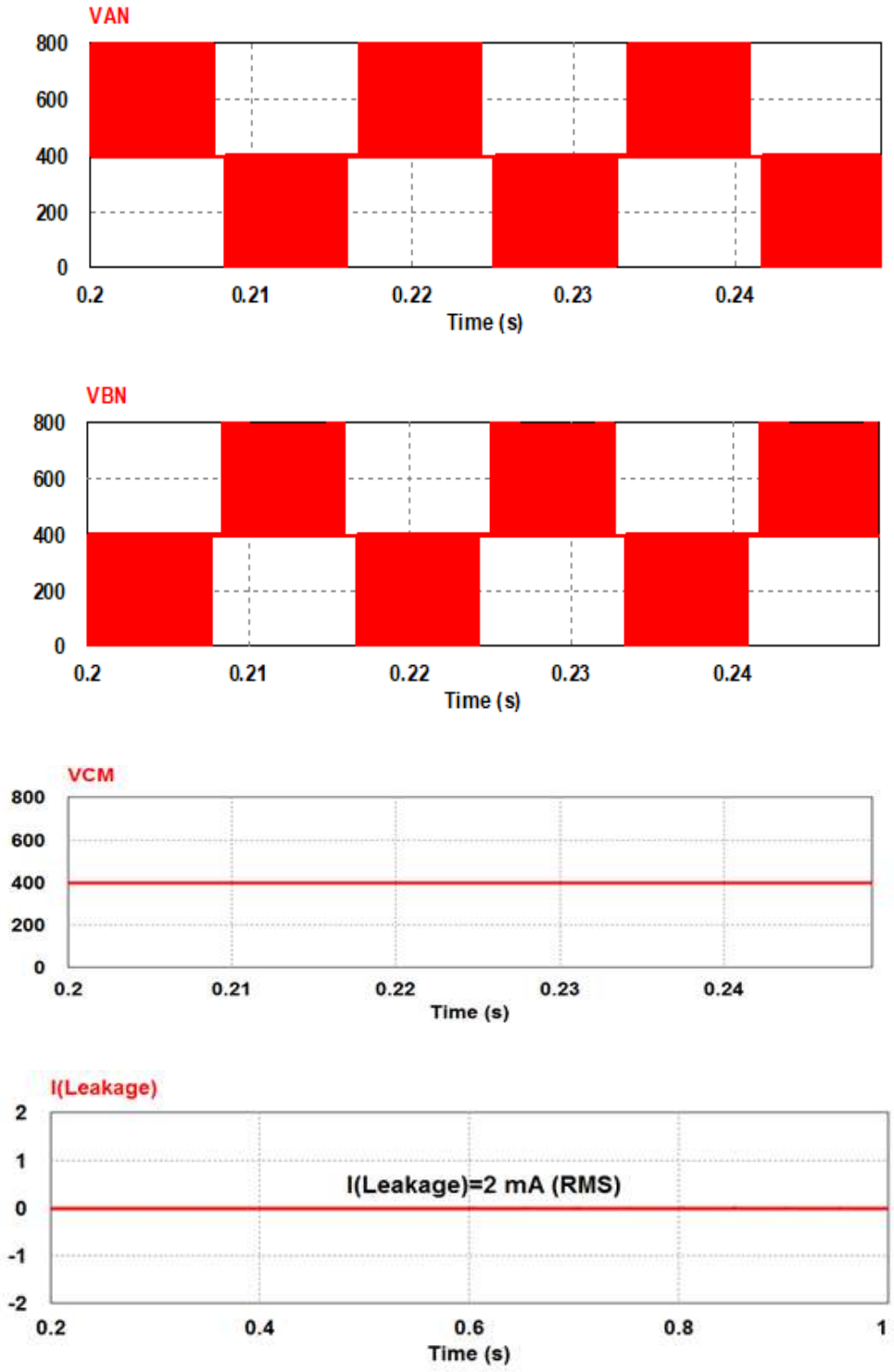
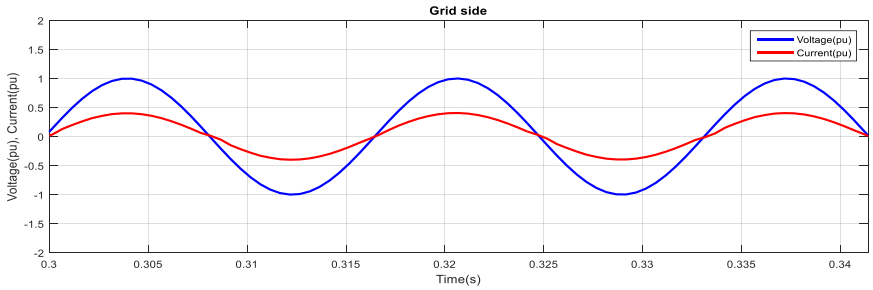


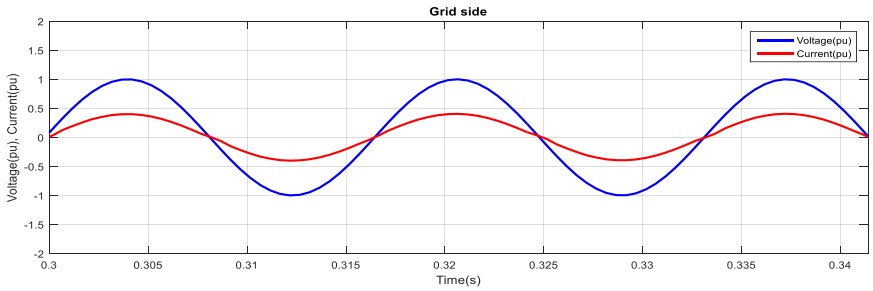
Figure 7. 9 CM characteristics of the modified proposed topology [116]

The simulated waveform of the proposed H6 inverter at unity power factor with traditional and proposed unipolar PWM modulation is presented in Figure 7.12. Both modulation techniques are expected to perform properly for purely active power of a unity power factor. On the other hand, with non-unity power factor (reactive power generation) the traditional unipolar PWM does not work correctly.

Figure 7.13 shows a current distortion in the negative power region because there is no current path to realize a zero-voltage through the negative power region. However, the issue of current distortion with conventional unipolar PWM can be resolved with the proposed unipolar PWM. The proposed modulation technique works optimally with lagging or leading power factor where the simulated waveform has free current distortion as depicted in Figure 7.14. Hence, the proposed modulation technique supports the proposed H6 inverter for reactive power generation.



(a)



(b)

Figure 7. 10 Vg and Ig for the proposed H6 inverter under unity power factor. (a) Traditional unipolar PWM; and, (b) proposed unipolar PWM [116]

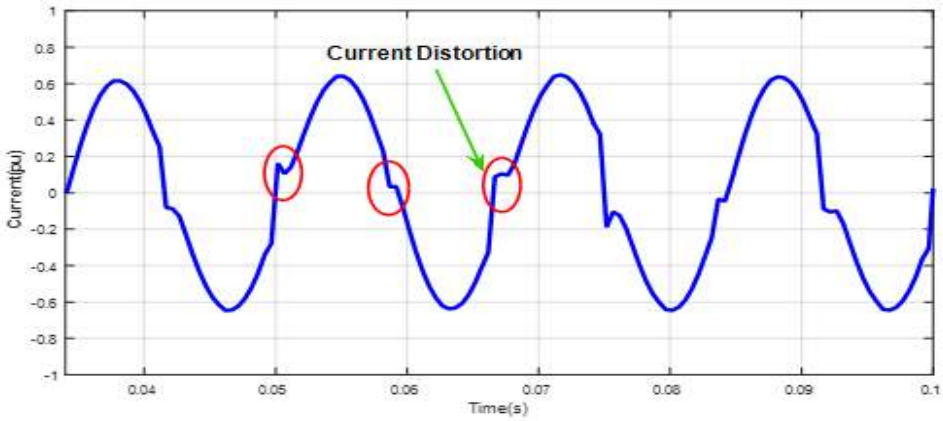


Figure 7. 11 Grid current for the proposed inverter under non-unity power factor with conventional unipolar PWM [116]

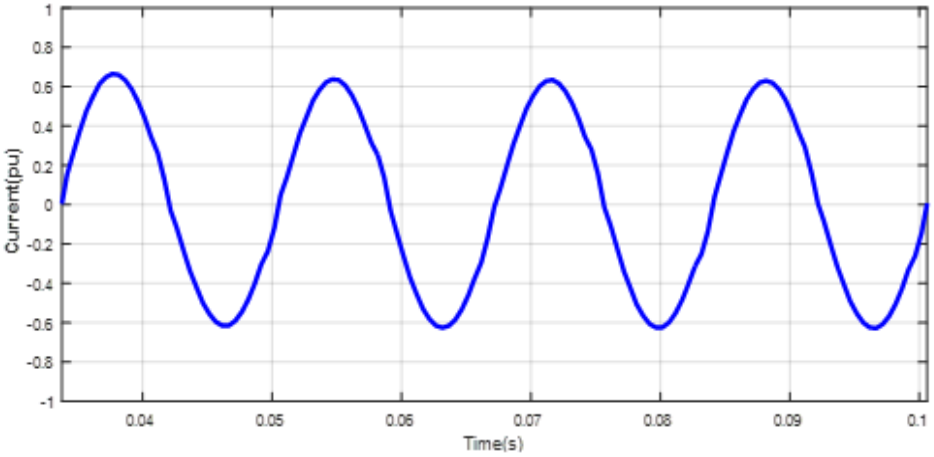


Figure 7. 12 Grid current for the proposed inverter under non-unity power factor with modified conventional unipolar PWM [116]

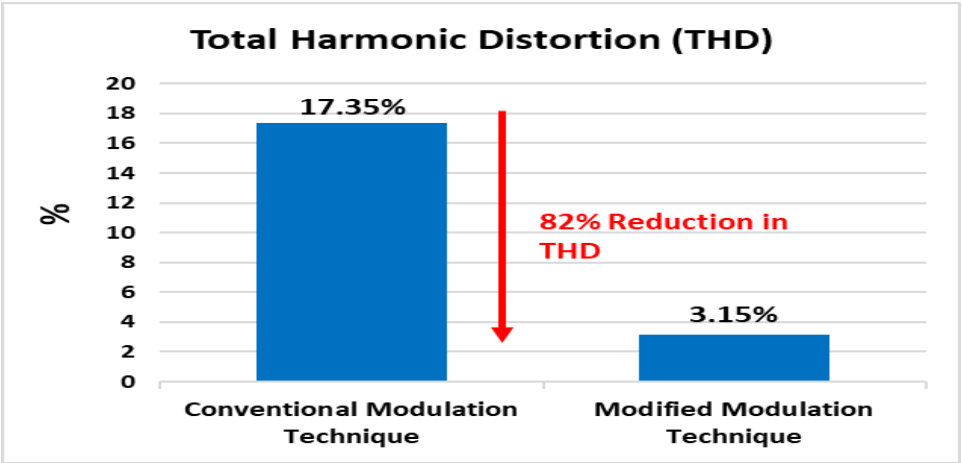


Figure 7. 13 Total harmonic distortion (THD) of the proposed topology with conventional and modified modulation technique [116]

It is noted that the proposed topology with modified modulation method succeeded in handling reactive power with 3.15% THD, as shown in Figure 7.15. However, the proposed topology incorporating the conventional modulation method generates high THD that does not comply with the IEEE 1547 Standard (THD < 5%) due to the absence of current path in the negative power region. The THD is reduced by 82% with the modified modulation. The efficiency of the proposed topology with and without reactive power capability is measured with SiC MOSFET switching devices. The efficiency is determined according to the California Energy Commission (CEC), as shown in the following:

$$\eta_{CEC} = 0.04\eta_{10\%} + 0.05\eta_{20\%} + 0.12\eta_{30\%} + 0.21\eta_{50\%} + 0.53\eta_{75\%} + 0.05\eta_{100\%} \quad (7.19)$$

Two switching frequencies using 16 kHz and 100 kHz and the calculated efficiency are given on Tables 7.2 and 7.3. The efficiency of the proposed inverter without reactive power capability at 16 kHz and 100 kHz is 98% and 97.6%, respectively. On the other hand, the efficiency of the proposed inverter with reactive power capability at 16 kHz and 100 kHz is 96.8% and 95.6%, respectively. These items are presented in Figures 7.16 and 7.17. Therefore, the cost of adding reactive power capability to the proposed inverter requires a reduction in system efficiency of about 1.2% and 2% for 16 kHz and 100 kHz, respectively. This reduction of system efficiency is due to the bidirectional flow of the current during reactive power generation, which leads to an increase in conduction loss.

Table 7. 2 CEC efficiency of proposed topology with SiC MOSFET at 16kHz

Output Power	300W	600W	900W	1500W	2250W	3000W	CEC
Proposed Topology (without reactive power capability)	99.7%	99.5%	99.3%	99%	98.4%	98%	98.7%
Proposed Topology (with reactive power capability)	99.2%	99%	98.6%	98.2%	97.5%	96.8%	97.7%

Table 7. 3 CEC efficiency of proposed topology with SiC MOSFET at 100kHz

Output Power	300W	600W	900W	1500W	2250W	3000W	CEC
Proposed Topology (without reactive power capability)	99.4%	99.3%	99%	98.6%	98.1%	97.6%	98.3%
Proposed Topology (with reactive power capability)	98%	97.8%	97.5%	96.9%	96.3%	95.6%	96.6%

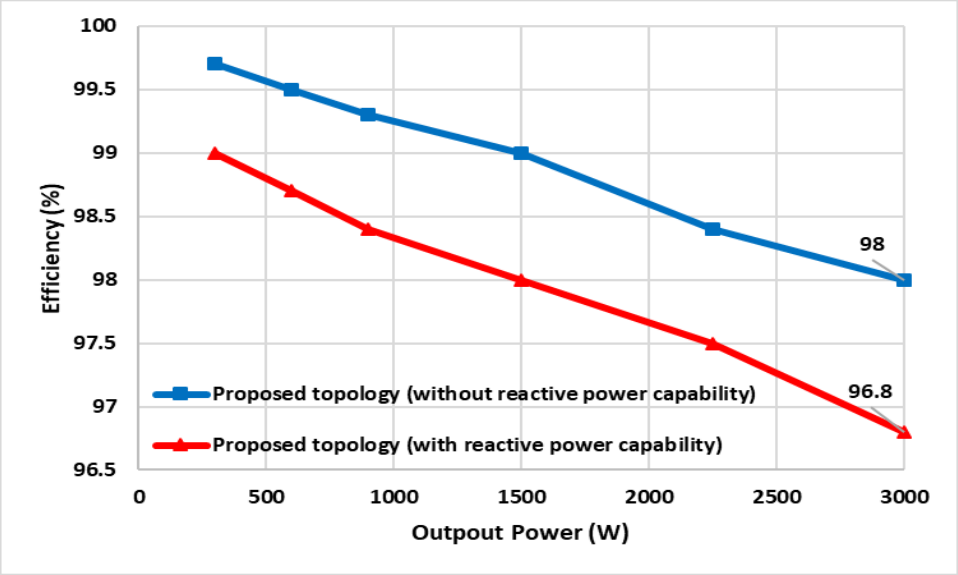


Figure 7. 14 Efficiency of the proposed topology with SiC MOSFET at 16kHz [116]

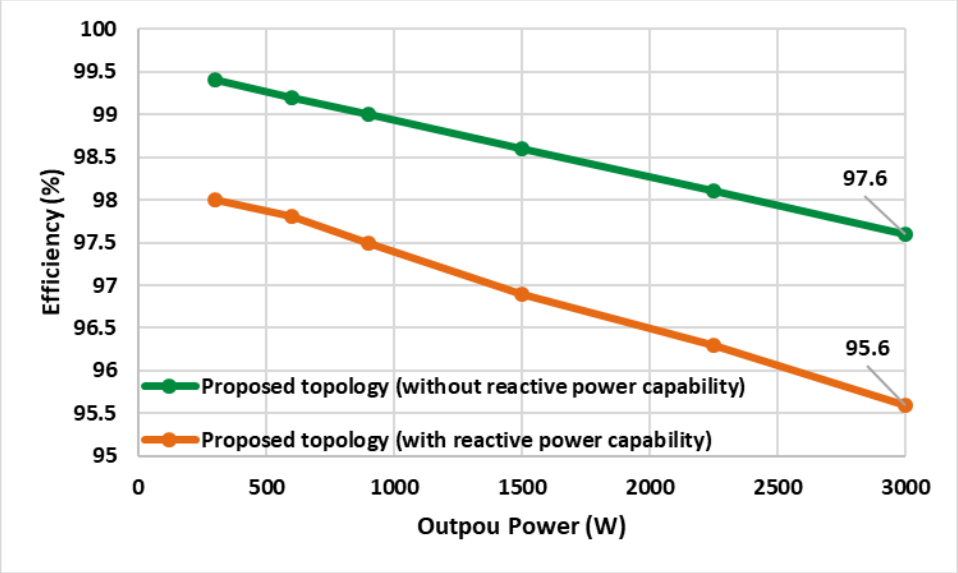


Figure 7. 15 Efficiency of the proposed topology with SiC MOSFET at 100kHz [116]

7.4 Conclusion

In this chapter, a proposed topology is modified with an extra switch to achieve constant common mode voltage and eliminating leakage current. Moreover, modulation method is modified so that reactive power generation can be achieved. Three voltages' states must be generated in the negative power region to satisfy the requirement of unipolar PWM. However, conventional unipolar PWM cannot generate a zero-voltage in the negative power region. The proposed modulation technique helps to create a new current path in the negative power region where a zero-voltage state can be achieved. To this end, the proposed modulation technique enables the proposed inverter with reactive power generation without any changes to the inverter structure. Moreover, the proposed modulation achieved a constant common mode voltage that leads to eliminating leakage current. The results show that common mode voltage is completely clamped at 400 V during the entire period and a complete elimination of leakage current is achieved.

Moreover, there is current distortion in the negative power region with conventional PWM modulation, while with the proposed modulation, a current path is created and the current distortion is eliminated. Furthermore, THD is reduced by 82% with modified modulation method. The efficiency of the system is measured with SiC MOSFET to enhance system performance, especially with reactive power generation. It is observed that system efficiency decreased by 2% at 100 kHz due to the reactive power capability, because the increase in conducting switches also increases loss. In brief, the proposed modulation technique satisfies the requirement for a next generation, single phase, PV grid tied inverter where reactive power control is required.

Chapter 8. Conclusion and Recommendations for Future Study

8.1 Conclusion

The need to reduce environmental pollution and the reality of limited nonrenewable energy sources, such as fossil fuels, motivates the research, including this investigation, on renewable energy technology. Advanced transformerless inverter topologies and the development of WBG power devices, particularly in the range of 650 V and 1200 V blocking voltage, open the possibility of achieving high-efficiency, reliable renewable energy systems. This study examines the most recent developments in transformerless inverter topologies and investigated the benefits of utilizing WBG power devices at 650 V and 1200 V blocking voltage for residential scale solar systems.

A review of PV system architecture and high gain DC-DC converters was presented in Chapter 2. The common mode behavior of a transformerless inverter was analyzed in Chapter 3. The next chapter was a review and comparison of advanced transformerless inverters with respect to their performance and leakage current generation. In the fifth chapter, the dynamic and static characterization of WBG power devices was evaluated. The benefits of using SiC MOSFETS at two different blocking voltages in PV systems with respect to system efficiency, power density, and heat sink requirements were presented in Chapter 6.

The benchmarking of WBG power devices demonstrates that SiC MOSFET has superior conduction and switching properties compared to Si-based devices. The

simulation results show that adopting SiC MOSFET in the proposed transformerless inverter enhance the system performance over Si-based power devices under high switching frequency operations and high temperature. Also, this work illustrated that a significant reduction in switching and conduction losses is achieved with SiC MOSFET in high switching frequency operations. Moreover, it is observed that using SiC MOSFET reduces the filter size by about 90%, without compromising system efficiency, when switching frequency is increased from 16 kHz to 200 kHz. In addition, the impact of using SiC MOSFET in reducing heat sink requirements was investigated and it was observed that heat sink volume and surface area were reduced by 28% and 50%, respectively.

Transformerless inverters suffer from leakage current generation due to the absence of galvanic isolation, which must be eliminated. Also, international standards require advanced control of PV systems such as reactive power generation due to the increased penetration of PV resources. The proposed topology and its unipolar modulation technique were modified to eliminate leakage current and can generate reactive power, as discussed in Chapter 7. The simulation results show that the leakage current is significantly reduced by more than 96%. In addition, reactive power generation is achieved with the modified modulation technique where the THD was reduced by about 82%.

8.2 Considerations for Future Research

There are some additional areas that need to be investigated that are not covered in this dissertation.

- The impact of high switching frequency on EMI filter design can be investigated because the volume of the EMI filter can occupy a large portion of the total inverter volume. Therefore, a significant reduction in the total inverter volume can be achieved by considering EMI filter design.
- WBG power devices can operate at high switching frequency, which leads to very fast switching transients and a high slew rate (dv/dt and di/dt). As a result, the effects of parasitic capacitance and inductance are amplified and may lead to spuriously turned-ON the switching device. Therefore, WBG power devices require a special design of gate drivers to maximize the performance of the switching devices and solve the drawbacks of the high slew rate.
- The advantages of higher switching frequency in control loop design of interface converters for grid integration renewable energy system should be investigated. For example, the delay time in the control loop can be significantly reduced when operating at a higher switching frequency, which will lead to large control bandwidth.

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