Design and Experimental Validation of a Wire-bond-less 10 kV SiC MOSFET Power Module

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Abstract— **Wide-bandgap power devices with voltage ratings exceeding 10 kV have the potential to revolutionize medium- and high-voltage systems due to their high-speed switching and lower on-state losses. However, present power module packages are limiting the performance of these unique switches. The objective of this work is to push the boundaries of high-density, high-speed, 10 kV power module packaging. The proposed package addresses the well-known electromagnetic and thermal challenges, as well as the more recent and prominent electrostatic and electromagnetic interference issues associated with high-speed, 10 kV devices. The module achieves low and balanced parasitic inductances, resulting in a record switching speed of 250 V/ns with negligible ringing and voltage overshoot. An integrated screen reduces the common-mode current that is generated by these fast voltage transients by ten times. This screen connection simultaneously increases the partial discharge inception voltage by more than 50 %. A compact, medium-voltage termination and system interface design is also proposed in this work. With the integrated jet-impingement cooler, the power module prototype achieves a power density of 4 W/mm³. This paper presents the design, prototyping, and testing of this optimized package for 10 kV SiC MOSFETs.**

Index Terms—**Electromagnetic interference, high-voltage techniques, packaging, silicon carbide**

I. INTRODUCTION

FOR several decades, silicon has been the primary semiconductor choice for power electronics applications [1]. However, silicon is quickly approaching its limits in power conversion [2],[3]. Wide-bandgap (WBG) semiconductors have demonstrated improved efficiency, reduced size and weight, and lower system cost [2],[3],[4],[5],[6]. Of the various WBG semiconductors, silicon carbide (SiC) is currently one of the most promising for medium- and high-voltage applications [2],[3],[7]. Today, medium- and high-voltage systems use silicon insulated gate bipolar junction transistors (IGBT), integrated gate-commutated thyristors (IGCT), or gate turn-off thyristors (GTO). While these devices have proven reliability and ruggedness, they have limited voltage ratings (typically 6.5 kV or less), requiring the series connection of devices or

multilevel converter topologies [8]. The series connection of devices raises the issue of voltage imbalance, and multilevel converters require additional components and complex control [8]. Moreover, these bipolar silicon devices have limited switching speed, which constrains the efficiency and switching frequency of the power converter [9],[10].

SiC power semiconductors are advantageous in these respects. Thus far, medium-voltage SiC MOSFETs [11],[12],[13], junction field effect transistors (JFET) [14],[15], bipolar junction transistors (BJT) [16], IGBTs [17],[18], GTOs [19], and emitter turn-off thyristors (ETO) [20],[21] have been demonstrated. Of these devices, the 10 kV SiC MOSFETs are of great interest due to their high blocking voltage, fast switching speed, simple drivability, reverse conduction capability, and moderate on-state losses. These features can increase the efficiency, reliability, and switching frequency, and reduce the complexity, size, and weight of medium- and high-voltage power conversion systems [18],[22]. Applications for 10 kV SiC devices include electric ships [23], traction [10],[24], data center distribution, direct renewables integration to a medium-voltage (13.8 kV) grid [17], fast charging stations [25], HVDC [26], flexible ac transmission systems (FACTS) [27],[28], and transformer-less intelligent power substations [17],[22],[29],[30],[31].

Due to the vast possibilities for ≥10 kV SiC devices, many resources have been devoted to their development. To date, the majority of the reports on these devices have been focused on the characterization [7],[13],[22],[29],[32],[33], gate driver design [34],[35],[36],[37], and converter evaluation [22],[33],[38]. However, the packaging of the semiconductor die has a significant impact on the performance, and is currently limiting their full potential; namely, their switching speed, voltage and current ratings, and operating temperature. Accordingly, the development of a suitable package will be critical for the adoption of high-voltage SiC devices.

However, the packaging of high-voltage SiC power semiconductors is nontrivial. The key benefits of these devices are also the primary challenges; specifically, the high-speed switching and the high voltage rating. A background of these

challenges, review of solutions proposed in the literature, and the unique solutions proposed in this work are described in the remainder of this section.

Due to their faster switching capability, SiC devices are more sensitive to parasitic elements in the module package, as well as in the bus bar and gate driver circuitry, than silicon. In particular, parasitic inductances can resonate with the device parasitic capacitances, causing undesirable ringing that increases electromagnetic interference (EMI) [39]. Also, during high speed current transients (di/dt), these parasitic inductances can cause disastrous overvoltage across the drain-source of the device. This is particularly a concern in the event of a short-circuit fault since the di/dt values can far exceed those seen during normal operating conditions.

Moreover, in order to increase the module current rating, several die are connected in parallel. If there exists a wide variation in the parasitic inductances for each of the paralleled die, then current imbalance can occur during the switching transients. It has been shown for a commercial silicon IGBT module that the current overshoots for each of the paralleled die can vary by more than two times [40],[41]. The die that experience the higher current overshoots will have larger switching losses [40],[41], and thus higher junction temperatures [41], which can reduce the overall lifetime of the module. Since SiC transistors are faster than silicon IGBTs, this problem is intensified.

To mitigate these issues of voltage overshoot, ringing, and dynamic current imbalance, it has become common practice for module manufacturers to integrate resistors into the power module, and users to add external gate resistors to slow down the switching speed. Adding resistance is not an ideal solution since it increases the switching times and losses, thereby diminishing the high-speed, high-efficiency advantages of SiC devices.

Instead, it is preferable to develop a module package with lower parasitic inductances. Several research groups and manufacturers have proposed to reduce the package inductance by replacing the traditional wire bond interconnections with ribbon [42],[43]; flexible PCB [44],[45],[46],[47],[48], solid posts, shims, or bumps [49],[50],[51]; solder balls [52]; direct-bonded solder [53]; or vias in PCB or ceramic substrates [54],[55],[56],[57]. Several packages also include integrated decoupling capacitors to mitigate the impact of stray inductances [55],[58],[59],[60],[61].

These embedded capacitors can also be used to create a symmetric layout for the die, as proposed in [58],[60]. However, since the modules in [58],[60] use wire bonds for the interconnection, the capacitors must be placed beside the die, thereby increasing the footprint of the module. Instead, in [55], the capacitors are placed above the semiconductor devices, creating a vertical high-frequency power loop that does not increase the module footprint, as it takes advantage of the third dimension.

To date, the majority of these low-inductance packages have been developed for silicon and SiC devices with voltage ratings of 1.2 kV or less, though some packages for higher-voltage devices have been reported. In [50], a flip-chip sandwich structure was applied for 3.3 kV silicon IGBTs. However, no electric field analysis or partial discharge (PD) tests were performed to ensure the package could reliably operate at the rated voltage. In [53], a sandwich structure with ceramic substrates on the top and bottom was used for a 6.5 kV silicon super GTO (SGTO). Electric field simulations showed that increasing the solder bondline thickness between the die and the top substrate could reduce the electric field in that region [53]. However, increasing the solder thickness increases the device junction temperature [53]. Benzocyclobutene (BCB) and underfill were also used for further insulation [53]. Leakage current tests at the rated device voltage of 6.5 kV were performed on the module [53]; however, this does not test the ability of the module to operate at the rated voltage for extended periods of time.

In addition to the parasitic inductances, parasitic capacitances within the power module are also a concern with high-speed devices, as they can become a path for common-mode (CM) current. In traditional power modules, there exists a parasitic capacitance across the insulating ceramic substrate (e.g., DBC). Since the cooling system (e.g., heatsink or coldplate) is generally grounded for safety, under high-speed voltage transients (dv/dt), this parasitic capacitance becomes a path for common-mode (CM) current to flow through the system ground [60]. This problem is especially critical for the fast-switching SiC devices, which have higher dv/dt transients than silicon IGBTs. Typically, filters and/or chokes are added to help reduce the EMI; however, these add cost, size, and complexity to the power conversion system. A simpler solution that requires fewer additional components is the implementation of a screen layer that returns the CM current back to the dc bus [62],[63],[64]. This can be realized with multilayer ceramic substrates, and has been shown to reduce the high-frequency noise [63],[64].

The high voltage rating of these SiC devices also poses a challenge for the packaging. To minimize the parasitic inductances and increase power density, it is desirable to have a compact power module; however, the high-voltage rating means the electric field strength within the package will be greater. If the electric field strength exceeds the electrical breakdown strength of the dielectric materials, then PD can occur, potentially causing permanent damage to the insulating materials, such as the insulating ceramic substrate [65]. Accordingly, the electric fields, both within the power module and at the external terminations to the rest of the power conversion system, must be carefully controlled. Recently, there has been focus on reducing the electric field strength near the insulating substrate, as this is typically where the PD occurs inside the power module [65],[66],[67].

Proposed solutions to reduce the electric field strength at this critical location include: increasing the ceramic thickness [65] and the permittivity of the encapsulation material [68]; adding a dielectric coating with high permittivity [69] or high breakdown field strength [70]; applying a high resistivity coating along the ceramic surface [70],[71]; using high permittivity non-linear dielectrics [72] or nonlinear resistive gel [73]; stacking multiple substrates [74]; and varying the metal-

ceramic interface geometry [70],[75]. Of these methods, those that are simple to implement have limited improvement on the PD inception voltage (PDIV), and those that have the highest improvement are complicated to fabricate or have questionable reliability. Furthermore, none of these methods have been implemented and tested in an actual power module. The primary challenges with using traditional power modules for packaging high-speed, high-voltage WBG devices are summarized in Fig. 1.

The objective of this work is to push the boundaries of high-density, high-speed, 10 kV power module packaging. The proposed 10 kV power module package enables the SiC devices to switch thousands of voltages in tens of nanoseconds with negligible voltage overshoot and ringing, while having low EMI, a small footprint, and high PDIV. The sandwich structures presented in [49] and [50] and the vertical-capacitor-loop reported in [55] are modified to create a low-inductance, symmetrical power module that is suitable for 10 kV SiC MOSFETs. The resulting module has a power-loop inductance of 4.4 nH, per MOSFET switch pair [76]. This is the lowest reported parasitic inductance for 10 kV power modules to date. Additionally, each MOSFET has its own gate and Kelvin source connection to the external gate driver, yielding symmetrical gate-loop inductances of 3.8 nH for each, thereby further improving the dynamic current sharing [76].

To reduce the EMI generated by this high-speed switching, a CM current screen that is fully integrated into the power module is proposed in this work. The proposed screen can reduce the ground current by 10 times [77]. This screening layer simultaneously increases the PDIV of the power module by 53 % [77]. To maintain low electric field strength in the air surrounding the power module, while also minimizing size and inductance, a unique housing and bus bar interfacing scheme is proposed. The bus bar compresses the spring terminals of the power module, creating a sealed connection so that there are no exposed conductors. In this way, creepage and clearance distances can be disregarded. Field-grading plates are included inside the bus bar to shift the peak electric field from the surrounding air to inside the solid dielectric. This is the first work reported in the literature to proposed electric field reduction methods both internal and external to the package of a high-density 10 kV SiC MOSFET power module.

In this paper, the detailed design of a high-power-density, high-speed, half-bridge power module package for 10 kV, 350 mΩ SiC MOSFET die [13] will be presented. The fabrication procedures for the 10 kV module prototypes will then be discussed, followed by the dynamic characterization and PD testing results of the power modules.
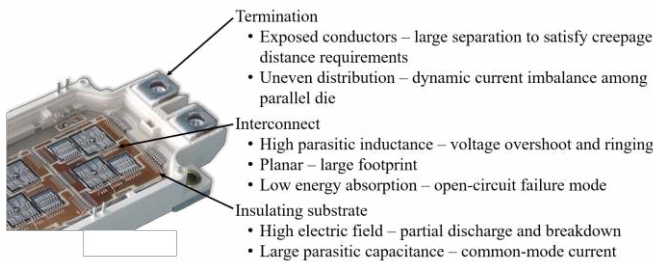

Fig. 1. Challenges with traditional power modules.

II. MODULE DESIGN

A. Module Overview

Fig. 2 shows the schematic and 3D model of the designed half-bridge power module. The colors of the metal pads in the 3D model (Fig. 2(b)–Fig. 2(f)) correspond to the node in the schematic (Fig. 2(a)) with the same color. The half-bridge module has three 10 kV, 350 mΩ, 8.1 mm × 8.1 mm die in parallel per switch position. To increase the power density and reduce the cost, no external antiparallel diodes will be used in the module; instead, the reverse current will flow through the MOSFET channel, and the body diode will only conduct during the dead time. This synchronous operation is made possible by the symmetrical reverse conduction and superior internal body diode of SiC MOSFETs, which have lower reverse recovery and thus lower losses than silicon MOSFET body diodes [78],[79]. In the past, conduction of the body diode of high-voltage SiC MOSFETs was avoided because it led to the propagation of stacking faults, which degraded the device performance [80],[81]. However, it was shown that the body diode of recent high-voltage SiC MOSFETs is stable [13],[82],[83]. As a result, Wolfspeed's latest 10 kV, 240 A module, does not include external antiparallel diodes [84].

The proposed module in this work has a planar, sandwich structure, using molybdenum (Mo) posts and direct-bonded-aluminum (DBA) substrates as the die interconnection instead of wire bonds. This type of structure allows for increased power density, and reduces the parasitic inductances and capacitances in the module, thereby improving the transient performance. Furthermore, by eliminating the wire bonds, the energy absorption capability during faults is increased, as shown in [85]. This structure also allows decoupling capacitors to be embedded within the module to further improve the dynamic performance without increasing the module footprint.

In total, four substrates are used in the power module: two beneath the die (DBA1 and DBA2) and two on the top (DBA3 and DBA4). The Mo posts act as standoffs that reduce the
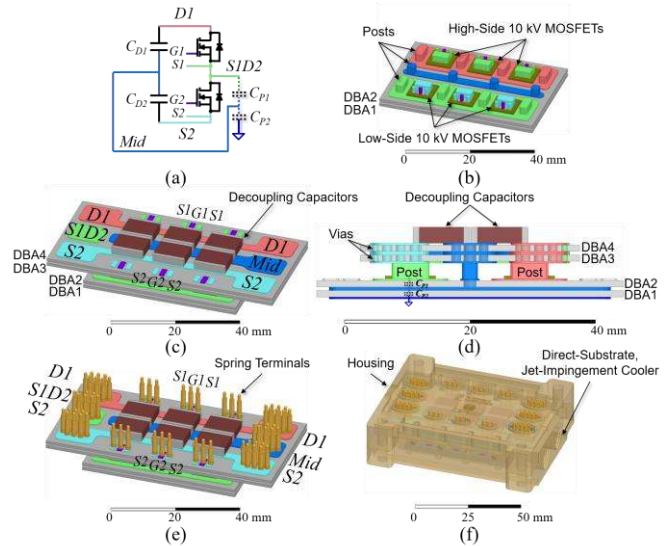

Fig. 2.   (a) Schematic, (b) bottom stacked substrates with six 10 kV SiC MOSFET die and posts, (c) top substrates stack and embedded decoupling capacitors, (d) side view with the vias shown, (e) module with spring terminals, and (f) housing with integrated direct-substrate cooler.

electric field strength between the die and the top DBA substrate. Mo was chosen as the post material because it has a coefficient of thermal expansion (CTE) of 4.9, which is closer to that of SiC (3.7) than Cu (17), and thus will result in lower thermomechanical stresses at the post–die interface [86].

The total module footprint is 74 mm × 49 mm × 11 mm without the housing. This gives a power density of 13 W/mm3. With the housing and integrated cooler, the dimensions become 83 mm × 68 mm × 25 mm, which results in a power density of 4 W/mm3. For reference, the power density of Wolfspeed's 10 kV, 240 A SiC MOSFET module is 4 W/mm3 without the cooling system [84]. Details of the module design will be discussed in the following subsections.

B. Electric Field Reduction

To address the enhanced electric field associated with a high-voltage, high-density package, the ceramic substrate must be thoughtfully designed and evaluated. In power modules, the electric field concentrates at the intersection of the ceramic, metal, and encapsulation [65],[66],[87],[88]. This is known as the triple point. If this electric field exceeds the breakdown field strength of the insulation materials, such as the ceramic or encapsulation, then PD can occur. Repetitive PD events can ultimately result in insulation failure, such as cracking of the ceramic substrate, as shown in [65].

According to the literature, the PDIV for standard 1-mm-thick aluminum nitride (AlN) DBC substrates is less than 10 kV rms [65], and can be as low as 5 kV rms [74]. To achieve sufficient margin for 10 kV SiC MOSFETs, methods for reducing the peak electric field within the power module must be employed. The method proposed in this work, is an adaptation of the stacked-substrate approach presented in [74], which effectively increases the PDIV, and is simple to implement.

In [74], it was shown that stacking DBC substrates reduces the electric field strength within the bulk ceramic and at the critical triple points. The PD tests revealed that the PDIV could be increased by 94 % by stacking two 0.32-mm Al2O3 substrates compared to having a single 0.63-mm substrate [74]. However, the practical implementation of this method was not explored. In a power module, the top and bottom metal layers are not symmetrical; the top metal is patterned to create the circuit, and the traces are at different potentials during the module operation. As a result, it is not clear what potential should be applied to the middle metal layer to achieve a meaningful reduction in the electric field strength. This key factor in the realization of this method is explored in this work.

Fig. 3 shows the simulated 2D electric field distribution for the case when the top metal is patterned and has two different potentials. One of the potentials represents the drain of the high-side switch, and the other represents the drain of the low-side switch. The former is consistently at the positive dc bus potential while the latter switches between the positive and negative dc bus potentials. The worst-case scenario is when the low-side switch is conducting and its drain is at the negative dc bus potential. This worst-case was simulated. The positive dc bus is set to 10 kV, and the negative is set to 0 V. The bottom-most metal is at the same potential as the cooling system, which

is grounded (0 V).

Fig. 3(a) shows the simulated electric field plot for a single DBA substrate. It can be seen that the electric field distribution is non-uniform within the bulk of the ceramic, and that the peak electric field occurs at the triple points. This peak electric field exceeds the typical dielectric strength for ceramic substrates (20 kV/mm).

Fig. 3(b) shows the simulated electric field plot for two stacked DBA substrates with the middle metal layer connected to the negative dc bus (0 V). Comparing Fig. 3(a) and Fig. 3(b), it can be seen that connecting the middle metal to the negative dc bus does not reduce the peak electric field at the triple point, nor does it improve the distribution within the bulk ceramic, compared to the single substrate case. This is because the bottom substrate has 0 V across it, while the top substrate has 10 kV. In this configuration, the bottom substrate does not help to support the voltage.

If the middle metal is connected to the positive dc bus, then the triple points at which the peak electric field occur will change, and the electric field distribution within the bulk ceramic will shift. This is shown in Fig. 3(c). However, the peak electric field, and therefore the PDIV, are similar to the case with a single substrate. This is because both the top and bottom substrates have 10 kV across them.

If the middle metal is connected to half of the bus voltage, then both the top and bottom substrates have a potential of 5 kV
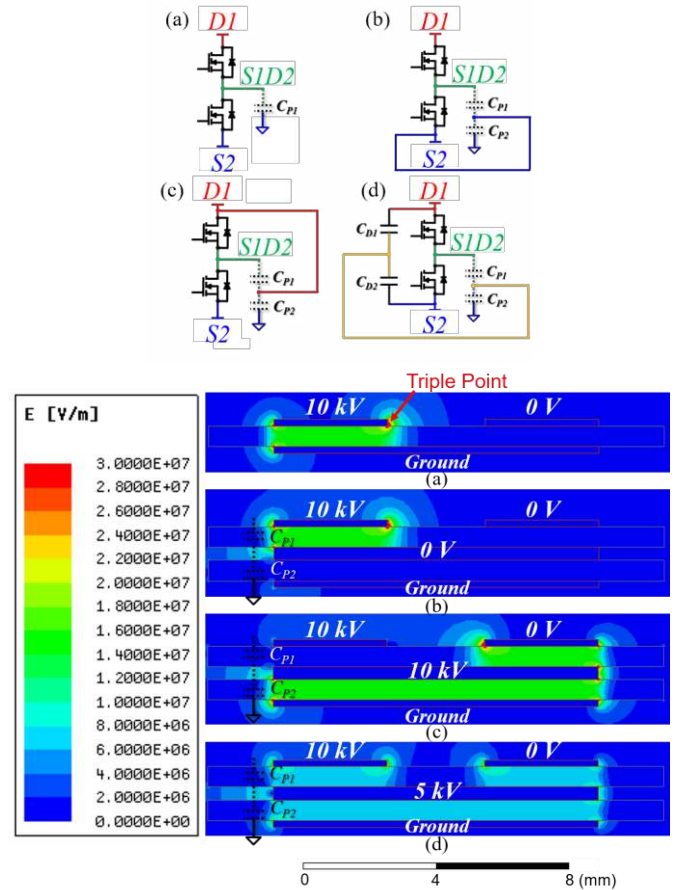

Fig. 3. Simulated 2D electric field distribution for (a) a single substrate, and two stacked substrates with the middle metal at the (b) negative dc bus, (c) positive dc bus, and (d) dc bus midpoint.

across them. The simulated electric field distribution for this case is shown in Fig. 3(d). The peak electric field is reduced by 58 % compared to the single-substrate case (Fig. 3(a)), and the electric field in the bulk ceramic is uniformly distributed in the two substrates. Therefore, in this work, the middle metal layer of the DBA stack is connected to half of the bus voltage. This connection can be realized with the embedded decoupling capacitors. Each set of decoupling capacitors shown in Fig. 2(c) consists of two, 5-kV ceramic capacitors placed in series. It is proposed in this work to connect the midpoint of the capacitors to the middle metal layer of the bottom DBA stack through vias and metal posts, as shown in Fig. 1(d). This compact, integrated connection method is made possible by the sandwich structure.

The metal post between the die and the top substrate acts as a standoff to reduce the electric field and improve the voltage isolation. The optimal post height is a tradeoff between the electromagnetic and electrostatic performances; a shorter post height will reduce the parasitic inductances and resistances, but will increase the electric field strength. In [89], the influence of the post height on the electric field strength was evaluated. In this work, the electric field distribution of the module cross-section was simulated to determine the optimal height of the posts (Fig. 4). In this simulation, the voltage distribution was graded along the top surface of the 10 kV SiC MOSFET to mimic the guard rings of the MOSFET die, as was done in [89]. It can be seen from Fig. 4 that the electric field strength between the die and the top DBA reduces when the post height is increased from 1 mm to 2 mm. If the electric field between the die and the top DBA exceeds the breakdown field strength of the encapsulation material, then PD or breakdown could occur. Based on these results, a post height of 2 mm was selected for this work.

C. EMI Reduction

For the 10 kV SiC MOSFETs to switch at high speeds, the negative effects of the high dv/dt must be addressed. One such effect is the conducted EMI that flows through parasitic capacitances. The primary capacitance of concern is the one that exists across the ceramic substrate between the S1D2 terminal and the cooling system. The S1D2 node experiences high dv/dt as it switches between D1 and S2. Since the cooling system is often grounded, this capacitance becomes a path for current to flow through the system ground.

To resolve this issue, [62] proposed a method for diverting the current back to the dc bus by using two stacked direct-bonded-copper (DBC) substrates, where the intermediate metal layer is connected to either the positive or negative bus. The amount of current that is diverted will strongly depend on the high-frequency impedance of the connection back to the dc bus, so the implementation of this screen is critical. In [62], wire bonds are used for the interconnections, and "lugs" are used for the terminals. These connection types have large parasitic inductance, which will increase the high-frequency impedance, thereby reducing the effectiveness of the screen.

In [63], a similar screen is proposed. For this implementation, a multilayer DBC substrate, and integrated dc-link capacitors are used to create a low-inductance connection between the
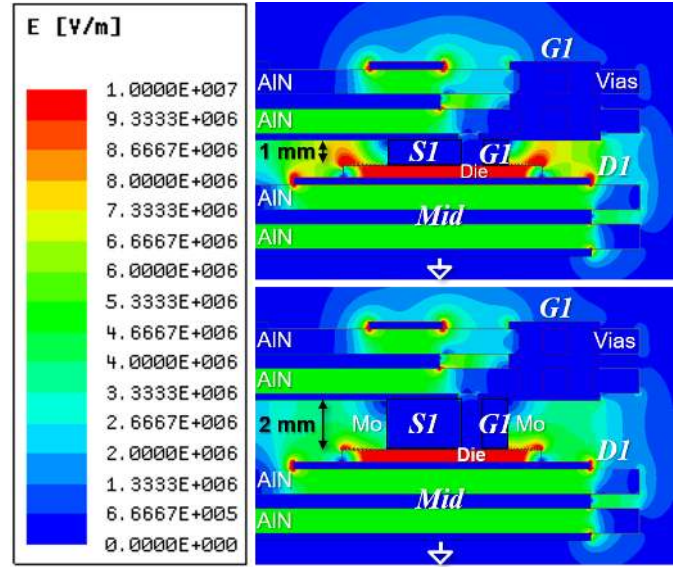

Fig. 4. Simulated electric field distributions for 1-mm post height (top) and 2-mm post height (bottom).

middle metal layer and the negative dc bus [63]. This method resulted in a 14-dB reduction compared to the reference module [63],[64]. However, by connecting the middle metal to the negative dc bus, the top ceramic is providing all the voltage isolation, as shown by Fig. 3(b). Additionally, placing the capacitors on the same plane as the MOSFETs, as is done in [63], increases the footprint of the module.

To mitigate the conducted EMI for a compact, high-voltage design, this work connects the middle metal layer to the midpoint of the embedded decoupling capacitors, which are arranged above each MOSFET switch pair. This implementation results in a low-inductance path for the CM current to flow, balances and reduces the power-loop inductances for the MOSFET switch pairs, and reduces the peak electric field at the critical triple points without increasing the module footprint.

D. System Integration

The module housing has a significant impact on the overall size, thermal resistance (current capacity), and voltage rating. To safely and reliably utilize the module at the rated voltage, creepage and clearance requirements [90], and PD and breakdown standards, should be considered. At 10 kV operating voltage, the minimum creepage distance is 100 mm for material group IIIa,b and pollution degree 2 [90]. This will significantly limit the minimum size of the power module. No previous literature was found on the development or investigation of high-density power module connectors for medium-voltage applications. Accordingly, a new connection scheme is proposed in this work.

First, to circumvent the creepage and clearance requirements, a sealed connection is designed. The housing design and system interface scheme that was developed for this 10-kV power module is shown in Fig. 5. The external bus bar is mounted on top of the power module. Pressure is applied to the top of the bus bar through mounting screws. This pressure compresses the springs until the bus bar contacts the protrusions in the housing
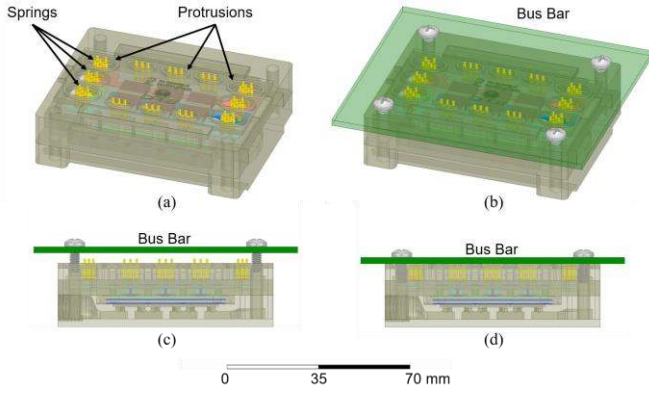
Fig. 5. 3D model of the (a) module with the housing and lid, (b) module with the bus bar, (c) side view of the module, and (d) side view of the module with the bus bar compressing the spring terminals.
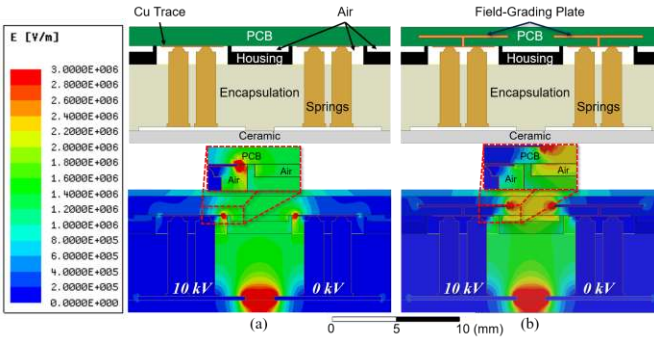

Fig. 6. Simulated electric field distribution (a) without and (b) with field-grading plates in the PCB.

lid. In this way, the springs are not exposed, and thus creepage and clearance restrictions do not apply.

Next, electric field strength for this connection scheme must be checked to ensure there will be sufficient PDIV and breakdown voltage. The electric field concentration in the air is critical due to the low dielectric strength of air (3 kV/mm). For this reason, protrusions were added to the housing lid (Fig. 4(a)). Without these protrusions, small air gaps could exist between the bus bar and the module lid; the smaller the air gap, the larger the electric field strength, and thus the lower the PDIV and breakdown voltage. Accordingly, increasing the height of the protrusions will increase the PDIV. However, increasing the height of the protrusions will also increase the inductance and resistance of the gate and power terminals. Given these considerations, a protrusion height of 1 mm was selected, though this air gap alone is not sufficient.

Fig. 6 shows the simulated 2D electric field distribution for a cross-section of the module–bus bar interface. As shown by Fig. 6(a), even with the 1-mm air gap, the electric field strength in the air exceeds 3 kV/mm. To further reduce the electric field strength in the air gap, this work proposes to add field-control plates within the bus bar. Fig. 6(b) shows how the field-grading plates can be used to shift the peak electric field strength from the air to the solid insulation of the bus bar, which has a greater dielectric strength. The plates shown in this embodiment are at the same potential as the spring terminals.

E. Thermal Management

Traditional power modules have the substrates and housing mounted to a baseplate. The substrates are typically attached to

the baseplate with solder, which is susceptible to delamination and voiding, resulting in low reliability and high thermal resistance [91],[92]. Bending stresses caused by the baseplate can also cause cracking of the ceramic substrates and semiconductor die [91]. A thermal interface material is commonly used between the baseplate and the cooling system, which further increases the thermal resistance. Overall, the many layers used in this traditional stack-up result in high thermal resistance and low reliability.

Previous work has shown that the baseplate can be eliminated if the cooling system provides sufficiently high heat transfer [93],[94]. As shown in [93],[94], targeted jet-impingement cooling is able to satisfy this requirement. In this work, the baseplate and thermal grease are eliminated, and a targeted jet-impingement cooling system is integrated into the module housing. The bottom DBA is sealed to the housing, and the jets impinge the coolant directly onto the lower surface of the substrate. The impingement cells are located underneath each SiC MOSFET die for targeted, efficient cooling. Further details on the design, simulation, and testing of the cooling system used for the proposed power module can be found in [95]. The final power density of the designed module with the housing and jet-impingement cooler is 4 W/mm^3, which is similar to that of the 10 kV, 240 A SiC MOSFET module in [84] without the cooling system.

III. MODULE FABRICATION

Table I summarizes the materials evaluated for the prototyping of the designed 10 kV power module. For each module component, several processing methods and materials were evaluated. Ag sintering was chosen for the substrate-substrate, die, and post attach because it creates a bond with lower voiding content, higher thermal conductivity, and improved reliability compared to solder [96].

Fig. 7 shows one of the procedures used for prototyping the 10 kV SiC MOSFET power modules. In this procedure, pressure-less Ag sintering is used for the post and die attachments. Pressure-assisted sintering procedures were also evaluated (Table I). With proper equipment, it could be possible to sinter multiple components simultaneously, thereby reducing the number of steps and shortening the manufacturing time. The details of the fabrication steps will be discussed in the following subsections.

A. Substrate Stacking

As shown in the previous section, stacking two ceramic substrates can reduce the electric field strength and conducted EMI of the power module. While multilayer ceramic substrates, such as LTCC [97],[98] and ceramic PCBs [99], are commercially available, they are not suitable for high power applications due to limited via sizes and Cu thicknesses. The performance of these multilayer ceramics under medium-voltages has also not been reported. As a result, in this work, a bonding process for attaching two separate substrates to create the stack was developed [100],[101].

A pressure-assisted Ag-sintering process was developed for bonding the 50 mm × 50 mm bottom and the 35 mm × 75 mm

Component	Process	Material	Advantages
Substrate	Direct-bonded aluminum (DBA)	Ag-plated 1-mm AlN with vias	High thermal conductivity, voltage isolation, and reliability
	Direct-bonded copper (DBC)	Au-plated 1-mm AlN with vias	High thermal conductivity, voltage isolation
Substrate attach	Pressure-assisted sintering	Nano-Ag paste	Low voiding and high thermal conductivity
Die attach	Pressure-less sintering	Nano-Ag paste	Low voiding, and high temperature, thermal conductivity, and reliability
	Pressure-assisted sintering	Dried nano-Ag paste	Low voiding, and high temperature, thermal conductivity, and reliability
Interconnect	e-beam deposition of Ti, Ni, and Ag	Mo posts	Low inductance, low effective CTE
	N/A	Au-plated Cu-Mo-Cu posts	Compatible with soldering, no extra processing
Interconnect attach	Pressure-less sintering	Nano-Ag paste	Low voiding and high thermal conductivity
	Pressure-assisted sintering	Dried nano-Ag paste	Low voiding and high thermal conductivity
	Soldering	Sn96.3/Ag3.7 paste	Thick bondline, compliant
Terminals	Pressure contact	Au-plated springs	Round geometry, easy connection, good reliability
Terminal and capacitor attach	Soldering	Sn63/Pb37 paste	Thick bondline, compliant, low melting temperature
Encapsulation	Deareation in vacuum, cure in furnace	Silicone gel	Good dielectric strength, medium hardness

top stacked substrates. Ag sintering was chosen because of its lower voiding content and higher thermal conductivity and reliability compared to solder [96]. Furthermore, since the melting temperature after sintering (960 °C) is higher than the sintering temperature ($\leq$ 260 °C), the sample can undergo multiple sintering processes without affecting the previously-sintered joints. This allows the substrates, die, and posts to be easily attached in stages. Solder, on the other hand, will reflow

1. Sinter posts to dies

2. Print Ag paste onto bottom substrate stack

3. Place dies and posts on printed paste

4. Print solder paste

5. Align substrates with jig

6. Dispense solder paste, place springs and capacitors, and solder

7. Seal module to housing

8. Pour silicone gel, degas in vacuum, and cure

9. Final module with lid

Fig. 7. Module prototyping procedure with pressure-less sintering.

when its melting point is reached. Accordingly, different solder alloys with varying melting points would be needed, which would limit the maximum operating temperature of the module.

For the developed large-area sintering process, 200-µm of the X-series nano-Ag paste from NBE Tech was printed onto one of the two substrates to be bonded. The printed paste was then dried in an oven at 130 °C for 30 minutes. The two substrates were then aligned and stacked together. The stacked sample was put into a hydraulic press, and 1 MPa was slowly applied. The temperature was then increased to 260 °C and held for 30 minutes to perform the sintering. After the sintering, the hotplate was turned off and the sample cooled under pressure. This prevents the substrate from bending due to CTE mismatch between the Al and AlN and the differences in the metal patterns between the two substrates. It is important to have uniform pressure distribution during this sintering process. If the pressure is not uniform, then the force applied to the substrate will not be homogeneously distributed and could result in cracking of the ceramic or poor bonding quality.

X-ray computed tomography (XCT) scans were performed to check the quality of the bonding layer and condition of the ceramic. The XCT images do not show any significant cracks, voids, defects, or misalignment (Fig. 8). It is particularly important to have low voiding content in the areas below the SiC MOSFET die so the heat can be effectively removed. The approximate die locations are outlined in Fig. 8. No significant voiding is observed in these critical areas.

To further check the thermal characteristics of the sintered bottom substrates, thermal impedance tests were performed at six locations along the surface of the sample where the SiC die would be located [96]. Cumulative structure-function analysis was then used to find the thermal resistance of the bond-line at each location [100]. The measured thermal resistances were 0.11 K/W to 0.14 K/W, which indicate good uniformity of the bond, and confirms that no large voids or cracks exist in these
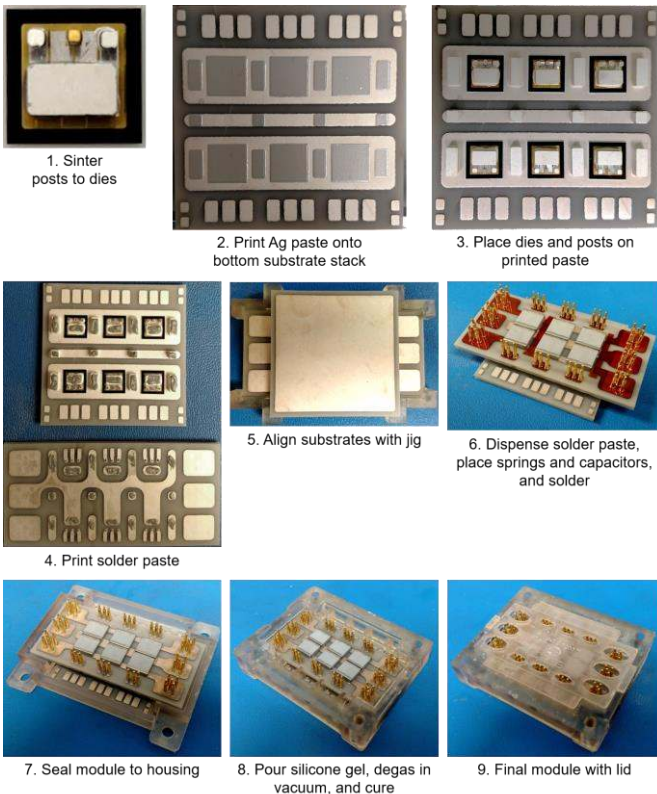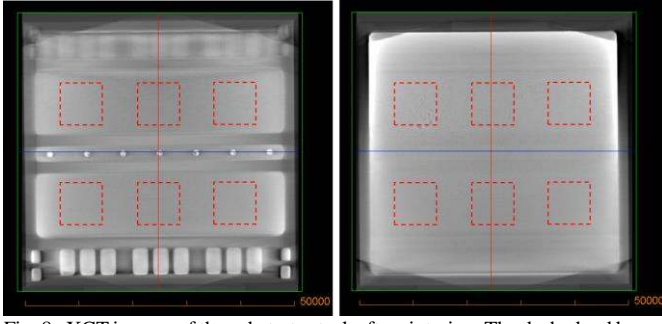
Fig. 8. XCT images of the substrate stack after sintering. The dashed red boxes indicate the approximate location of the 10 kV SiC MOSFET die.
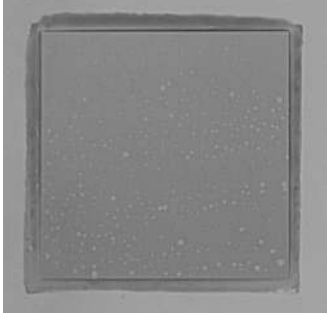

Fig. 9. X-ray image of the die attach layer for the 8.1 mm x 8.1 mm 10 kV die using the pressure-less sintering process.

locations.

B. Post Attachment

Mo posts are used to increase the distance and thereby reduce the electric field between the die and the top substrate. Mo was chosen because it has a low CTE, which reduces the thermomechanical stresses on the die. Pressure-less and pressure-assisted Ag sintering methods were evaluated for the post attachment. For the pressure-less sintering of the Mo post to the substrate, 50-µm-thick Ag paste was stenciled onto the substrate. The posts were then placed on top of the stenciled paste, and the sample was transferred to a hotplate and sintered. Bonding strengths between 31 MPa and 67 MPa (depending on the area of the post) were achieved when the posts were sintered to a Ag-plated substrate. The shear strength between the Mo posts and the MOSFET die using the same process were 47 MPa, on average, for the Kelvin source posts (1.0 mm × 1.0 mm) and 33 MPa for the power source posts (5.2 mm × 3 mm).

For the pressure-assisted process, Ag paste was dried and then the posts were stamped onto the dry film. This stamping transfers the Ag film to the post. The sample was then sintered under 10 MPa. This pressure-assisted sintering method yielded comparable bonding strength as the pressure-less process.

C. Semiconductor Die Attachment

As mentioned above, Ag sintering was chosen for the die attach because it has been shown to have lower thermal impedance and higher thermal cycling capability compared to solder [96]. Both pressure-less and pressure-assisted Ag sintering processes using different types of nano-Ag paste were evaluated. The 10 kV SiC MOSFET die are 8.1 mm × 8.1 mm × 0.5 mm and have Au backside metallization. Since Ag diffuses faster than Au, a sintering profile that limits the Ag diffusion is needed to prevent the formation of Kirkendall
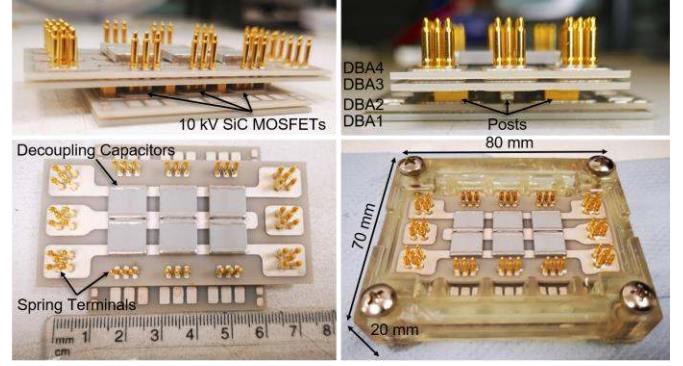

Fig. 10. 10 kV SiC MOSFET module prototype.

voids, which cause low shear strength [102],[103]. In this work, the sintering temperature was lowered to 230 °C and held for 90 minutes. This profile resulted in an average shear strength of 15 MPa, with a peak of 18 MPa. X-ray images of the sintered die attach layer shows low voiding content and defect density (Fig. 9).

Applying pressure during sintering can further improve the shear strength by creating a denser Ag layer [102]. However, pressure-assisted sintering can be more complex, especially when sintering multiple die simultaneously, since the pressure must be uniformly applied to all the die. For the pressure-assisted process, 100-µm-thick Ag paste was printed onto the substrate, and then dried in an oven at 130 °C for 10 minutes. Once the paste was dried, a 10-kV die was placed on top, and the sample was sintered in a hydraulic press at 250 °C and 10 MPa for 5 minutes. The die shear strength of the pressure-assisted Ag-sintered sample was 25 MPa.

D. Module Assembly

The top substrate stack is attached to the posts using solder paste. Solder is chosen for this bonding instead of sintering because it can create a thicker bondline to accommodate height tolerances and curvature of the substrates, and it is more compliant so it will enable some thermomechanical movement. The spring terminals and decoupling capacitors were also attached with solder. The springs used in this power module have a continuous current rating of 10 A [104]. The shear strength for the soldered springs, which have a diameter of 1.88 mm, is 64 MPa on average, with a maximum of 70 MPa.

The housing and integrated jet-impingement cooler were 3D printed out of high-temperature resin [105]. Silicone sealant was used to seal the bottom substrate stack to the housing. After curing, the module was encapsulated. Silicone gel was selected for the encapsulation because of its simple processing and good reliability and dielectric strength [69],[106]. Silicone gels with low viscosity were chosen so that the encapsulant can fill small gaps in the power module, leaving fewer air pockets. Fig. 10 shows the 10 kV SiC MOSFET module prototype. The testing of the module prototypes will be presented in the following section.

IV. MODULE TESTING

A. Dynamic Characterization

To evaluate the switching performance of the module,

double-pulse tests (DPT) were conducted. Fig. 11 shows the gate-source and drain-source voltage waveforms for the turn-on and turn-off transients for the DPTs performed on a scaled-down module prototype with two 10 kV SiC MOSFET die. The switching tests were performed at 5 kV and 20 A with turn-on and turn-off gate resistances of 0.33 Ω and 0.17 Ω, respectively. The drain current could not be measured due to the embedded decoupling capacitors and compact design. Table II lists the measured overshoot, undershoot, rise and fall times, and switching rates from the DPTs. During the turn-on transient, the fall time of the drain-source voltage was 16 ns (250 V/ns). At turn-off, the voltage rise time was 50 ns (80 V/ns). The voltage rise time is slower because it is controlled by the output capacitance and load current. Negligible voltage overshoot and ringing were measured, indicating low power- and gate-loop inductances. This is due to the low-inductance module design, as well as careful layout and connection of the gate driver, bus bar, external decoupling capacitors, and measurement probes.

To the best of the author's knowledge, these are the fastest switching speeds reported for similarly-rated SiC MOSFETs and IGBTs [33],[84],[107],[108],[109]. In [84], switching results for a module populated with a single die had turn-on and turn-off transition times of approximately 80 ns and 120 ns, respectively, giving switching speeds of 88 V/ns and 58 V/ns at a bus voltage of 7 kV, drain current of 15 A, and gate resistance of 21 Ω. The switching waveforms also showed a moderate voltage overshoot of approximately 300 V (4.3 %) [84].

B. Common-Mode Current Test

Further switching tests were performed to evaluate the impact of this high-speed switching on the conducted EMI. For these tests, the current through the ground path was measured
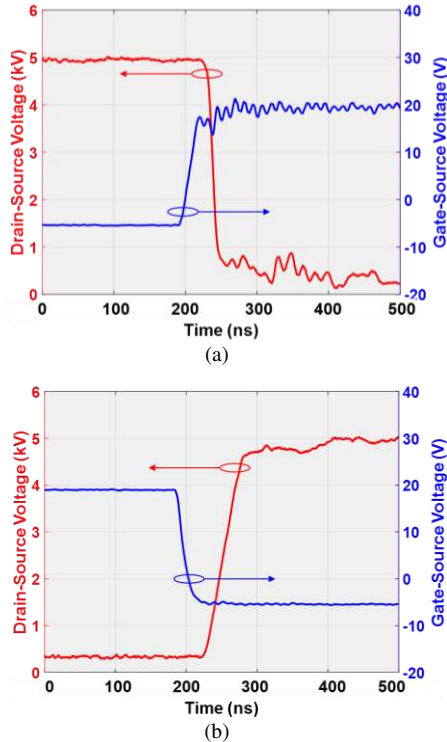
TABLE II
10 kV, 350 mΩ SiC MOSFET MODULE PROTOTYPE SWITCHING RESULTS

Parameter	Value	
	Gate-Source Voltage	*Drain-Source Voltage*
Overshoot	None	None
Undershoot	None	None
Rise time	24 ns	50 ns
Rise dv/dt	0.9 V/ns	80 V/ns
Fall time	26 ns	16 ns
Fall dv/dt	0.8 V/ns	250 V/ns

using an RF current transformer with a bandwidth of 200 MHz. Fig. 12 shows the turn-off drain-source voltage and ground current waveforms with and without the proposed CM screen. The dv/dt at this turn-off transient was 24 V/ns. This slower dv/dt is due to the lower bus voltage and larger device capacitance due to the three MOSFET die in parallel per switch position. A slower dv/dt was desired to improve the measurement accuracy.

For the case without the CM screen, the middle metal layer of the bottom substrate stack was left floating, and the measured peak current through the ground path during the turn-off transient was 2 A (Fig. 12). This peak current will increase as the dc bus voltage, and therefore the dv/dt, increases. When the middle metal layer of the bottom substrate stack was connected to the midpoint of two series decoupling capacitors, the peak current reduced to 0.2 A. This is an order of magnitude reduction, and validates the effectiveness of the proposed integrated CM screen.

C. Partial Discharge Test

PD tests were conducted to validate the electrostatic simulation results. The PD tests were performed using a 50 kV, 60-Hz ac excitation source, and a Doble PD Smart with the HFCT-300 sensor to detect the PD events [110]. PD tests were performed on a patterned, 1-mm-thick AlN-DBA substrate with 2-mm spacing between metal traces. Three cases were tested: 1) a single substrate, 2) two stacked substrates with the middle metal connected to the source ground, and 3) two stacked

Fig. 11. (a) Turn-on and (b) turn-off gate-source (blue, right axis) and drain-source (red, left axis) voltages.
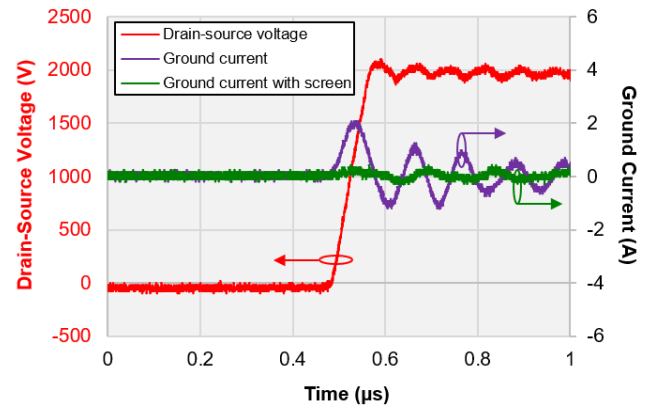

Fig. 12. Measured drain-source (red, left axis) and ground current (right axis) waveforms with (green) and without (purple) the CM screen at 2 kV and 20 A with no external gate resistance.

substrates with the middle metal connected to half of the applied excitation voltage. Each case was tested under the worst-case switching state, which is when the high-side switch is blocking and the low-side switch is conducting such that S1D2 is equal to S2.

First, the PD tests were performed with the samples in air in order to have a high signal-to-noise ratio. These tests revealed that, as was shown in the electrostatic simulations, the PD for the DBA substrates will occur at the triple points. Specifically, the PD will take place along the edge of the metal pad where the high potential is applied. The resulting PDIV for the cases when the samples are tested in air are listed in Table III. When the middle metal is connected to half of the applied voltage, the PDIV increases by 53 % compared to the single-substrate case. These results are in good agreement with the simulations.

Since the power module will be encapsulated, PD tests were also performed on a stacked substrate sample that was encapsulated with silicone gel. When the middle metal is connected to the source ground, the PDIV is 7.4 kV rms (10.5 kV peak). For this same case, breakdown occurred at 8.5 kV rms (12.0 kV peak). This means if the middle metal is connected to ground, or if a single substrate is used, then there is 20 % margin between the peak breakdown voltage and the voltage rating of the 10 kV SiC MOSFETs.

When the middle metal is connected to half of the applied voltage, no PD could be measured up to 10.5 kV rms (14.8 kV peak). The testing was stopped at 10.5 kV rms due to the reduced signal-to-noise ratio. This suggests that encapsulated stacked substrates with the middle metal connected to half of the applied voltage will have more than a 40 % higher PDIV compared to a single substrate or a stacked substrate with the middle metal connected to ground. Therefore, it is advantageous to use the stacked substrate structure with the middle metal connected to half the applied voltage in order to increase the high-voltage performance of the power module.

D. Thermal Characterization

To evaluate the performance of the integrated direct-substrate, jet-impingement cooler, thermal impedance measurements were carried out on a Mentor Graphics Power Tester [111]. The lowest junction-to-ambient specific thermal resistance of the module was measured to be 26 mm2·K/W (0.38 K/W) for a flowrate of 0.47 l/min. Further details on the thermal characterization of the cooling system developed for this power module can be found in [95].

V. Conclusion

This work proposed a high-density power module for 10 kV SiC MOSFETs with high-speed switching, improved high-voltage performance, and lower CM current. The optimal layout and system interface enabled the module to switch 5 kV in tens of nanoseconds with negligible ringing and voltage overshoot. This is the fastest switching speed reported to date for 10 kV SiC MOSFETs. The significantly reduced switching losses will enable medium-voltage converters to hard switch thousands of volts at tens of kilohertz while maintaining high efficiency. The increased switching frequency will dramatically

TABLE III
PARTIAL DISCHARGE TESTING SUMMARY

Sample	Voltage of Middle Metal	Surrounding Medium	PDIV (rms)
Single Substrate	N/A	Air	1.7 kV
Stacked Substrates	$1/2 \times V_{AC}$	Air	2.6 kV
Encapsulated Stacked Substrates	0 V	Silicone gel	7.4 kV
	$1/2 \times V_{AC}$	Silicone gel	>10.5 kV

reduce the size of the passive components, thereby further increasing the power density of the system.

However, this high-speed switching can reduce the PDIV and increase the conducted EMI. To increase the PDIV, it is proposed in this work to stack two substrates and connect the middle metal layer to the dc bus midpoint. This method was shown to increase the PDIV by 53 % compared to that for a single substrate. This connection also forms a low-impedance path at high frequency, diverting the current that would normally flow to the system ground to the bus through the embedded decoupling capacitors. Switching tests revealed a ten-time reduction in the ground current. This simple, integrated solution enables the 10 kV SiC MOSFETs to switch at high speeds without compromising the voltage isolation or system integrity. Moreover, the integrated screen reduces the need for external filters, thereby reducing the size and complexity of the power conversion system.

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