Design and Experimental Verification of a Third Harmonic Injection Rectifier Circuit Using a Flying Converter Cell

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***Abstract*—The proposed active three-phase rectifier circuit utilizing a Flying Converter Cell (FCC) based on the concept of third harmonic injection allows the extension of a passive three-phase diode bridge rectifier to a low-harmonic input stage ($\mathrm{THD_i} < 5\,\%$) for applications where dc-link voltage control is not required. In this work the design and experimental verification of a 10 kW laboratory prototype using the proposed concept is addressed. Based on the analysis of the rectifier system a control concept is developed which is implemented in a digital signal processor. It is shown that the proposed rectifier system shows several degrees of freedom which can be used for system optimization. Several implementation details are discussed and experimental results taken from the constructed 10 kW laboratory prototype demonstrate the good performance of the proposed rectifier system and verify the proper operation of the developed control concepts.**

I. Introduction

In recent years power quality and low harmonic distortion of the power supply grid are getting more and more important. Especially due to the smart grid vision, where many small power loads and generators are planned to be operating on the mains, power converter systems connected to the mains are facing advanced requirements in order not to distort the grid. Passive three-phase rectifier circuits, such as the standard B6 diode bridge with dc-side located smoothing inductor, are very robust, highly efficient and have therefore been widely used in industry. They can, however, not fulfill the more stringent requirements on input current quality ($\mathrm{THD_i} < 5\,\%$) anymore. Active rectifier systems such as the bidirectional six-switch rectifier circuit [1] are commonly used to improve the input current quality. An overview of active three-phase rectifier systems can be found in [2], [3]. The active current shaping of these topologies, however, results in a reduced efficiency compared to the B6 diode bridge rectifier. Existing passive diode rectifier systems can furthermore not be extended to these active rectifier circuits.

The idea of third harmonic injection improves the input current quality by injecting a current either into all three phases [4], [5] or into a single phase [6] of the diode bridge. It was first applied by the Minnesota Rectifier [4] which uses boost stages at the output of the diode bridge for current shaping and recently the Swiss rectifier [5] has been developed which uses buck stages for current shaping. The topologies show a $\mathrm{THD_i} < 5\,\%$ and offer a controlled dc-link voltage. A comprehensive overview on such three-phase rectifier topologies using the concept of third harmonic injection can be found in [7]. These topologies, however, also suffer from a reduced efficiency as the full power still has to be processed by the semiconductors used for current shaping and dc-link voltage control.

In many applications, e.g. ac drives, etc., a controlled dc-link voltage is not required and topologies based on the concept of third harmonic injection using either passive [8], [9] or active [10], [11] current shaping networks have been developed which do not offer a controlled dc-link voltage. These topologies typically require a constant power load at the output of the rectifier and cannot be used with a considerably large dc-link capacitors as often required in industrial applications.

In this work the design, implementation and control of a three-phase third harmonic injection rectifier circuit using a "Flying" converter cell (FCC) as proposed in [12] is discussed in detail (cf., **Fig. 1**). The FCC topology allows the extension of an existing passive B6 diode bridge rectifier with smoothing inductor and large dc-link capacitor to a low-harmonic rectifier system by application of an additional power electronic circuit called "Flying" converter cell.

II. Flying Converter Cell

The basic structure of the three-phase rectifier circuit using an FCC is shown in **Fig. 1**. The passive B6 diode bridge rectifier circuit with dc-side located smoothing inductor L_{DC} and considerably large output capacitor C_{o} is extended by the FCC and three bidirectional switches for current injection of the third harmonic current i_{h3} into a single phase. The basic idea is to inject current into the phase which would not conduct current in passive diode mode. In addition, currents i_{cp} and i_{cn} are injected into the positive and negative output of the diode bridge in order to achieve sinusoidal mains currents. The FCC basically consists of three converter stages: two half-bridges ($S_{\mathrm{cp}\pm}$, $S_{\mathrm{cn}\pm}$) and a three-level bridge leg ($D_{\mathrm{h3}\pm}$, S_{h3}). A unidirectional implementation of the three-level bridge-leg is used in this work, however, as discussed in [12] dependent on the operating mode of the FCC a bidirectional implementation of the three-level bridge leg may be required. As shown in

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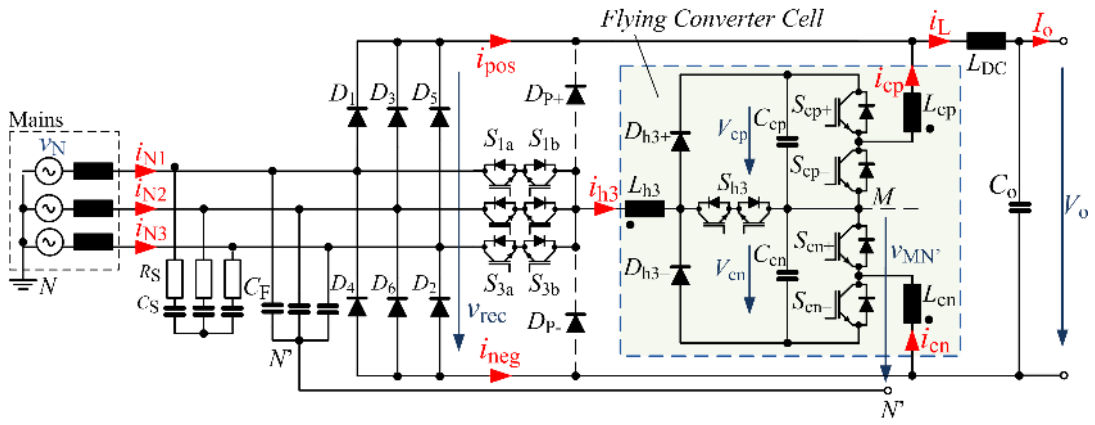


Fig. 1: Basic schematic of the proposed rectifier system employing a Flying Converter Cell.

Fig. 1 three inductors, L_{cp}, L_{cn} and L_{h3}, are required for proper operation of the FCC. According to Kirchhoff's law the three currents have to fulfill

$$i_{cp} = i_{cn} + i_{h3} \tag{1}$$

and therefore a coupled three-phase arrangement can be used advantageously for implementation of the chokes.

As discussed in [12] several operating modes of the FCC exist. The three converter systems are equal regarding control of the three currents and in this work the operating mode II, the two half-bridges are used to control the injected currents and the three-level bridge leg is used to control the average value (averaged over the switching frequency) of the midpoint voltage $v_{MN,avg}$, is used. The required FCC dc-link voltages V_{cp} and V_{cn} are related to the mains voltage and a modulation index

$$M = \frac{\hat{V}_N}{V_c} \tag{2}$$

is defined. The FCC dc-link voltage results in $V_c = 400\,V$ for a mains voltage of $V_{LL} = 400\,V$ and a modulation index of $M = 0.813$ and therefore semiconductors with a blocking voltage capability of 600 V can advantageously be applied for the half-bridges ($S_{cp\pm}$, $S_{cn\pm}$) and the switches of the three-level bridge-leg S_{h3}.

One remarkable advantage of the proposed topology is that the FCC only has to process a small amount of output power

$$P_{h3} = P_{cp} + P_{cn} = 5.8\,\%P_o\ . \tag{3}$$

Whereas the three-level bridge-leg processes only active power the two half-bridges used for injection of the currents i_{cp} and i_{cn} have to deal with reactive power of $Q_c = 16.7\,\%P_o$. As will be further discussed in section IV the total losses of the FCC are quite small which results in an excellent efficiency. The proposed rectifier also shows no high-frequency CM voltage at the rectifier output V_o, only the FCC shows a midpoint-voltage v_{MN} which is only present inside of the FCC.

In **Fig. 2** simulated current and voltage waveforms of the topology are shown for the parameters $P_o = 10\,kW$, $V_{LL} = 400\,V$ and $f_N = 50\,Hz$. The mains currents are in phase with the mains voltages and show sinusoidal shape with a THD_i of 2.7 %. The currents i_{cp} and i_{cn} injected into the positive/negative bus bar show 3^{rd} and 6^{th} harmonic components of the fundamental frequency. The current i_{h3} is composed of sections of the three mains currents and shows approximately triangular shape. In addition the high-frequency component of the midpoint voltage $v_{MN'}$ is shown in **Fig. 2** together with its averaged value $v_{MN',avg}$. More detailed information on the basic operation principle can be found in [12].

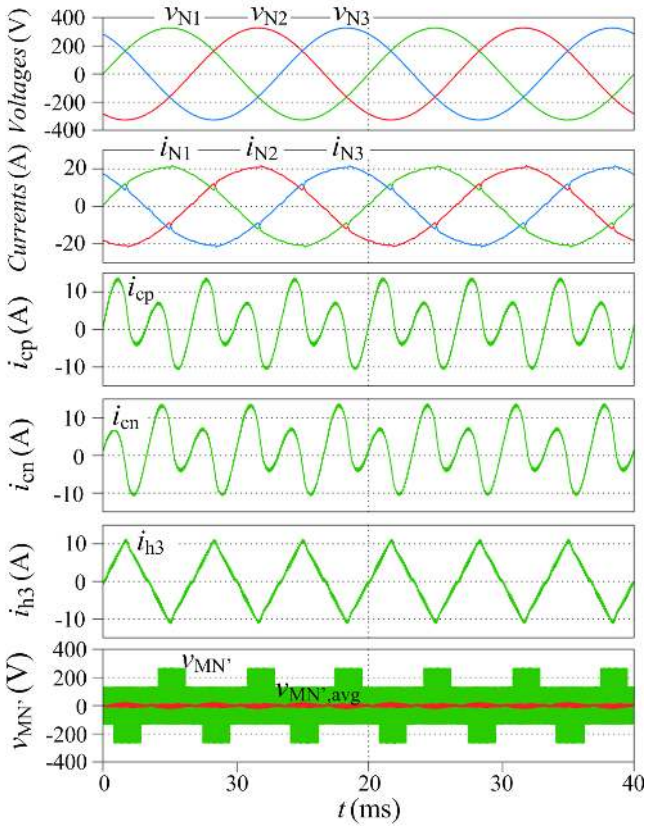


Fig. 2: Simulated current and voltage shapes of the proposed rectifier system for an output power of $P_o = 10\,kW$ and $V_{LL} = 400\,V$, $f_N = 50\,Hz$.

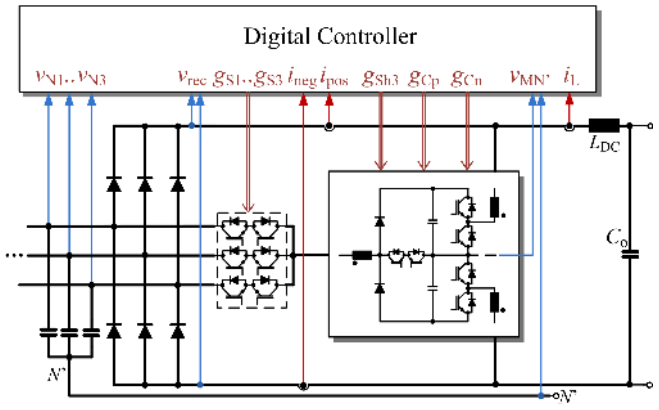


Fig. 3: Measured signals used for the digital control of the rectifier circuit.

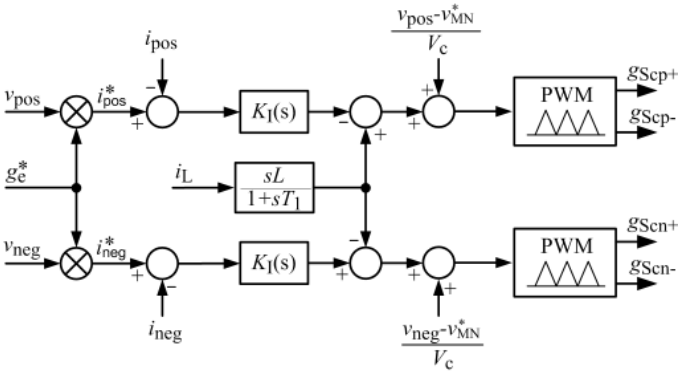


Fig. 4: Basic structure of the proposed current controller including pulse-width modulation.

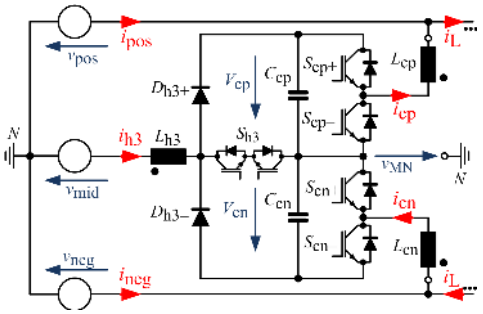


Fig. 5: Simplified circuit of the FCC used to derive the converter model for current control.

III. Control

Several controllers are required for proper operation of the new rectifier circuit. It is obvious that fast-acting current controllers are required to shape the mains currents, however, it is not clear in which way the reference currents must be generated. The reference current generation of topologies using the concept of third harmonic injection without output voltage control has insufficiently been discussed in literature up to now and a promising method is given below. Next to the current controller also controllers for the FCC dc-link voltages are required. In **Fig. 3** the measurement signals used for the digital control of the rectifier circuit are shown. Next to the mains voltages v_{Ni} also the currents i_{pos}, i_{neg} and i_L are measured as well as the rectifier output voltage v_{rec} and midpoint voltage $v_{MN'}$.

A. Current Control

The basic structure of the proposed current controller is shown in **Fig. 4**. In the following the concept of average mode current control is used. The basic idea is to control the output currents i_{pos} and i_{neg} of the diode bridge by injecting adequate currents i_{cp} and i_{cn} into the busbars as

$$i_{pos} = i_L - i_{cp} \qquad i_{neg} = i_{cn} - i_L \tag{4}$$

applies. The two half bridges are therefore used for current control whereat the three-level bridge-leg is used for balancing of the FCC dc-link voltages and to control the average value of the midpoint voltage $v_{MN,avg}$ to zero. Two independent current controllers are used for i_{pos} and i_{neg} and the current i_{h3} results due to (1).

In **Fig. 5** the simplified model of the FCC is shown. For $\varphi_N \in [0 \dots \frac{\pi}{6}]$ ($i_{N1}(\varphi_N) > 0$; $i_{N2}(\varphi_N), i_{N3}(\varphi_N) < 0$)

$$\begin{aligned} \delta_{cp} v_{cp} + v_{MN,avg} - v_{pos} &= L \frac{di_{cp}}{dt} \\ (1-\delta_{h3})(-v_{cn}) + v_{MN,avg} - v_{mid} &= -L \frac{di_{h3}}{dt} \\ (1-\delta_{cn})(-v_{cn}) + v_{MN,avg} - v_{neg} &= -L \frac{di_{cn}}{dt} \end{aligned} \tag{5}$$

can be calculated where equal inductors ($L = L_{cp} = L_{cn} = L_{h3}$) for the three converter stages are assumed. In the sector $\varphi_N \in [0 \dots \frac{\pi}{6}]$ $v_{pos} = v_{N1}$, $v_{mid} = v_{N2}$ and $v_{neg} = v_{N3}$ applies. The two dc-link voltages are controlled by the FCC dc-link voltage controller with reduced dynamic and equal (constant) voltages $V_{cp} = V_{cn} = V_c$ are assumed for the current controller. Also the average value of the midpoint voltage $v_{MN,avg}$ can be treated as constant as it shows much smaller dynamic. Based on this simplification Laplace Transformation can be applied which results in

$$\begin{aligned} \delta_{cp} V_c + V_{MN,avg} - v_{pos} &= sLi_{cp} \\ (1-\delta_{h3})(-V_c) + V_{MN,avg} - v_{mid} &= -sLi_{h3} \\ (1-\delta_{cn})(-V_c) + V_{MN,avg} - v_{neg} &= -sLi_{cn} \ . \end{aligned} \tag{6}$$

In the following only the equation for current i_{cp} is exemplary analyzed, similar considerations can, however, be done for the other currents. Using (4) for i_{cp} results in

$$sLi_{pos} = sLi_L - \delta_{cp} V_c - V_{MN,avg} + v_{pos} \ . \tag{7}$$

By inspecting (6) and **Fig. 5** it is obvious that the upper half bridge of the FCC must generate an average voltage which is equal to the voltage difference $v_{pos} - V_{MN,avg}$ which means that this voltage difference can advantageously be used as feed-forward signal. According to (4) the current i_L is a disturbance input of the current control loop and disturbance rejection can be applied using the measured current value i_L. Using the resulting feed-forward signal

$$\delta_{cp} = \tilde{\delta}_{cp} + \frac{v_{pos} - V_{MN,avg}}{V_c} + s\frac{Li_L}{V_c} \tag{8}$$

together with (7) results in the very simple model

$$G_{\mathrm{I}}(s) = \frac{i_{\mathrm{pos}}(s)}{\tilde{\delta}_{\mathrm{cp}}(s)} = -\frac{V_{\mathrm{c}}}{sL} \ . \tag{9}$$

The corresponding feed-forward terms are shown in **Fig. 4** where the required differentiator block for i_{L} is extended by a low-pass filter with higher cut-off frequency for noise suppression. The current controller $K_{\mathrm{I}}(s)$ can be a P-type or a PI-type controller.

B. Midpoint Voltage

According to **Fig. 1** the FCC is connected to the passive diode bridge using either three individual inductors or a coupled three-phase choke. Due to the switching actions of the FCC the midpoint voltage shows high-frequency voltage fluctuations (cf., **Fig. 2**) and its average value is only defined by the pre-control signals. An additional controller must be implemented to control the average value of the midpoint voltage to a dedicated value. The midpoint voltage $v_{\mathrm{MN'}}$ can be measured between the midpoint M of the FCC and the artificial star point N' built by the ac-side connected filter capacitors (see also **Fig. 1** and **Fig. 3**). The average value is determined by simply filtering the measured midpoint voltage which is not a challenge as the high-frequency components are at the switching frequency and harmonics of the switching frequency.

As the two half-bridges already shape the FCC currents the three-level bridge-leg can be used for control of the midpoint voltage (and for balancing of the FCC dc-link voltages). The reference value v^*_{MN} is thereto compared to the filtered voltage $v_{\mathrm{MN',avg}}$ and the deviation is the input of the midpoint voltage controller showing small dynamic. Similar to the current controller also here the voltage v_{h3} can be used as feed-forward term. The resulting controller is shown in **Fig. 7(b)**.

C. Generation of Reference Currents

In conventional active rectifier circuits [3], the reference currents are often generated by a superimposed voltage controller which indirectly determines the power demand by measuring the voltage of the dc-link capacitor. The output voltage of the proposed rectifier system is, however, not controlled, but is dependent on the mains and load situation and is even not measured. The power transferred from the mains to the output of the rectifier is not dependent on the current shape and can therefore be determined by measurement in both operating modes, operating in diode mode as well as for active current shaping using the FCC. The power demand can be determined using the mains voltages/currents

$$p(t) = v_{\mathrm{N1}}(t)i_{\mathrm{N1}}(t) + v_{\mathrm{N2}}(t)i_{\mathrm{N2}}(t) + v_{\mathrm{N3}}(t)i_{\mathrm{N3}}(t) \tag{10}$$

with subsequent low-pass filtering of the actual active power. This would, however, require three additional current sensors for mains current measurement. A more convenient way is to use v_{rec} and i_{L}

$$p(t) = v_{\mathrm{rec}}(t)i_{\mathrm{L}}(t) \ . \tag{11}$$

The voltage v_{rec} can either be calculated using the mains voltage measurement or measured using a dedicated voltage measurement circuit. Considering also the case where all diodes are in blocking mode measuring of the voltage v_{rec} is preferred. The equivalent conductance g^*_{e} can now be calculated by

$$g^*_{\mathrm{e}} = \frac{P_{\mathrm{in}}}{V^2_{\mathrm{N1,rms}} + V^2_{\mathrm{N2,rms}} + V^2_{\mathrm{N3,rms}}} \tag{12}$$

and finally multiplied with the (calculated) voltages u_{pos} and u_{neg} to derive the reference currents i^*_{pos} and i^*_{neg}.

D. Modulation

In this work pulse width modulation is used to generate the gate signals of the semiconductors. The triangular shaped carrier signals of the FCC's three converter stages can advantageously be synchronized and a possibility to optimize system behavior with respect to current ripple and midpoint voltage v_{MN} exists. **Fig. 6(a)** shows the PWM, the switching sequence and the resulting midpoint voltage v_{MN} at $\varphi_{\mathrm{N}} = 15\,^\circ$ if all three triangular shaped carrier signals are in phase and **Fig. 6(b)** depicts the situation where the carrier signal of S_{h3} is phase shifted by $180\,^\circ$. In order to analyze the behavior similar to [12] a switching state (s_{cp},s_{h3},s_{cn}) can be defined where e.g. $s_{\mathrm{cp}} = 1$ denotes the turn-on state of the switch $S_{\mathrm{cp+}}$ (switch $S_{\mathrm{cp-}}$ is turned off) and $s_{\mathrm{cp}} = 0$ denotes the turn-on state of the switch $S_{\mathrm{cp-}}$ (switch $S_{\mathrm{cp+}}$ is turned off).

As shown in **Fig. 6(a)** for $\varphi_{\mathrm{N}} = 15\,^\circ$ the midpoint voltage shows voltage levels of $\pm V_{\mathrm{c}}/3$, 0 and $\pm 2V_{\mathrm{C}}/3$ if symmetrical FCC dc-link voltages are assumed. As can be observed in **Fig. 6(b)** the midpoint voltage shows only voltage levels of $\pm V_{\mathrm{C}}/3$ and 0 if the carrier signal for the three-level bridge-leg is shifted by $180\,^\circ$. This allows to optimize the high-frequency midpoint voltage v_{MN}. On the other hand the current ripple of the injected currents increases considerably if the carrier signals are phase shifted by $180\,^\circ$ (not shown in **Fig. 6**). The maximum current ripples derived in [12] are only valid for carrier signals showing a phase shift of $180\,^\circ$ (cf., **Fig. 6(b)**). If synchronized carrier signals without phase shift shall be used the maximum current ripple calculates to

$$\begin{aligned} \Delta i_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}},\mathrm{pkpk}} &= \frac{V_{\mathrm{c}} M^2}{4 f_{\mathrm{s}} L} \\ \Delta i_{\mathrm{h3,pkpk}} &= \frac{V_{\mathrm{c}} \frac{M}{2} \left(1 - \frac{M}{2}\right)}{f_{\mathrm{s}} L} \end{aligned} \tag{13}$$

which are quite smaller than the current ripples given in [12]. The choice of phase shift between the carrier signals therefore allows to optimize the system behavior for minimal current ripple or for minimal midpoint voltage v_{MN}. As the current ripple is directly related to losses the operating mode with synchronized carrier signals in phase is used in this work.

E. FCC DC-Link Voltages

As already noted, the voltages of the FCC dc-link must be controlled. The total voltage is handled by a voltage controller and balancing of the two dc-link capacitors requires a dedicated controller. Control of the dc-link voltages must be done without disturbing the input currents. The structure of the voltage

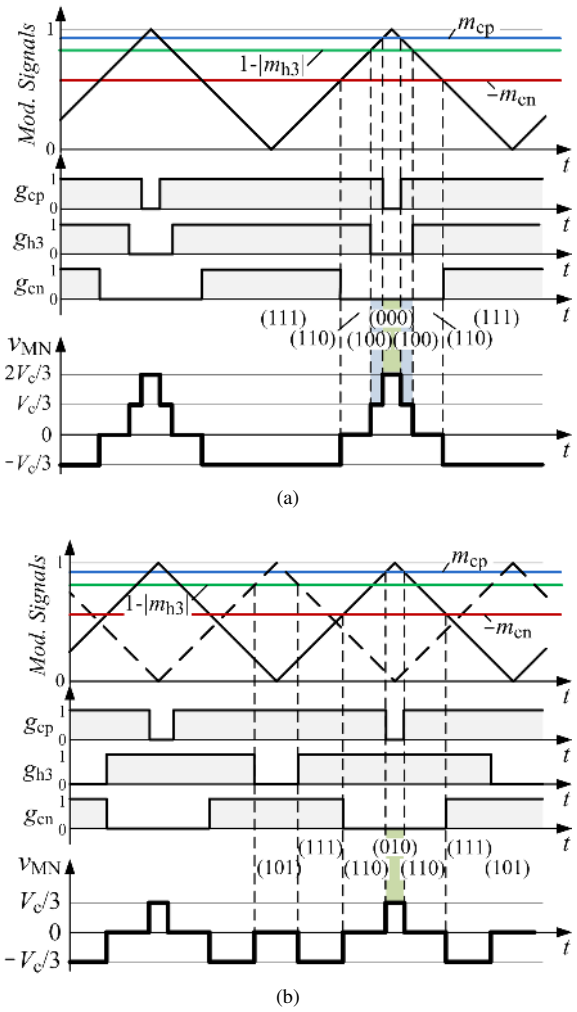


Fig. 6: Modulation of the three converter stages of the FCC using synchronized triangular shaped carrier signals at $\varphi_N = 15\,°$. (a) All three converter stages use carrier signals in phase and (b) the three-level bridge-leg uses a carrier signal with a phase shift of 180 deg.

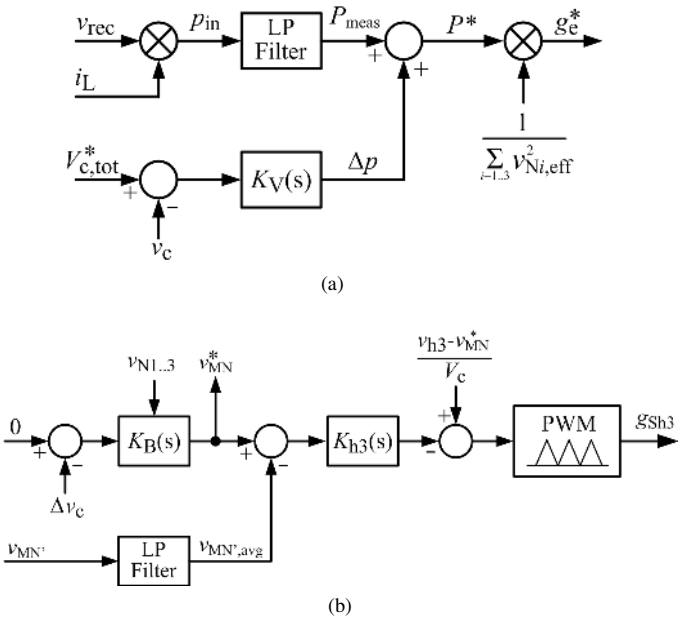


Fig. 7: (a) Structure of FCC dc-link voltage controller and reference current generation and (b) balancing of FCC dc-link voltages and control of average value of midpoint voltage $v_{MN'}$.

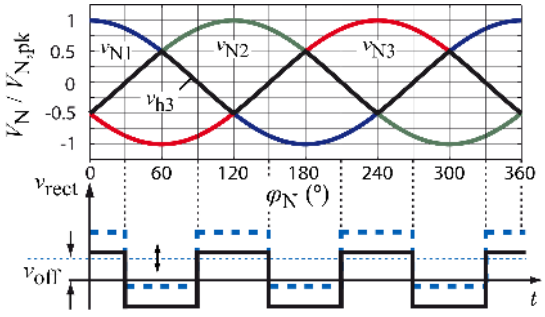


Fig. 8: Proposed midpoint voltage variations used for balancing of the two FCC dc-link voltages.

controller is shown in **Fig. 7(a)**. The output of the FCC dc-link voltage controller Δp is added to the measured power P_{meas} which yields the requested power P^*. The equivalent conductance g_e^* is finally calculated according to (12). Please note that the FCC dc-link voltage controller may include some nonlinear control behavior and that the power demand Δp required for control is typically only a small fraction of P^*.

A detailed analysis of the FCC showed that different midpoint voltages v_{MN} result in different currents in the two dc-link capacitors. This effect can be used for balancing of the FCC dc-link capacitor. The average value of the midpoint voltage must thereto be shaped as shown in **Fig. 8**. Dependent on the offset v_{off} of the rectangular waveform v_{rect} the capacitors are charged or discharged. The amplitude of the rectangular waveform is fixed to a small amount of V_c and the balancing controller only alters the offset. These details are not shown in **Fig. 7(b)** and the whole controller is simply represented by $K_B(s)$. The output of the balancing controller v_{MN}^* is the reference value for the midpoint controller.

IV. System Design

A 10 kW laboratory prototype according to the specifications given in TABLE I has been constructed. The built prototype is used to verify the basic operating principle of the FCC and is neither optimized for size nor for efficiency. It should furthermore act as a scaled demonstrator for higher power ratings (e.g. 200 kW) and therefore a rather small switching frequency of $f_s = 10\,\text{kHz}$ is chosen intentionally. Please note that MOSFETs could be applied advantageously due to the small voltage rating of the FCC switches which would allow to increase the switching frequency considerably and which would result in a considerably higher power density. In addition the switching frequency of 10 kHz is a challenge for control as the currents i_{cp} and i_{cn} show high harmonics (3^{rd} and 6^{th} harmonic) and the head room to the switching frequency is rather small. As shown below the constructed hardware demonstrates that a high current quality can be achieved using

TABLE I: Design Specifications of the Built Three-Phase Rectifier using a FCC.

Mains voltage:	$V_{\mathrm{LL}} = 400\,\mathrm{V_{rms}}$
Mains frequency:	$f_{\mathrm{N}} = 50\,\mathrm{Hz}$
Switching frequency:	$f_{\mathrm{s}} = 10\,\mathrm{kHz}$.
FCC dc-link voltage:	$V_{\mathrm{cp}} = V_{\mathrm{cn}} = 400\,\mathrm{V}$
Output power:	$P_{\mathrm{o}} = 10\,\mathrm{kW}$

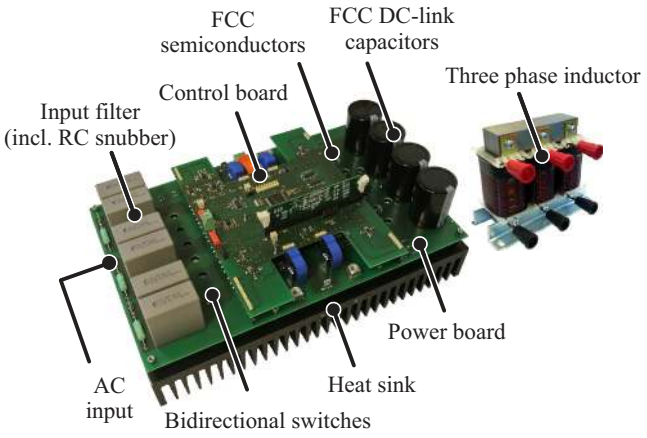


Fig. 9: Constructed 10 kW laboratory prototype of the FCC and used three-phase choke. Dimensions FCC: 300 mm x 200 mm x 97 mm and three-phase choke 120 mm x 50 mm x 100 mm.

the proposed topology even with the small switching frequency.

The constructed prototype is shown in **Fig. 9** together with the applied three-phase choke (the passive diode rectifier with dc-side located smoothing inductor is not shown in **Fig. 9**). The FCC consists of two boards, the power board containing all main power components such as semiconductors, FCC dc-link capacitors, input filter, etc., and the control board which basically includes the digital controller and analog measurement circuitry. The proposed control algorithm is implemented in a fixed point DSP (TI 320F2808) and a Lattice CPLD (Mach XO 2280) is used to implement the four step commutation sequence for the bidirectional switches.

The current stress formulas for semiconductors and passive components derived in [12] have been used to design the FCC and system losses are calculated. The applied components of the FCC are listed in TABLE II and the results of the loss calculation for an output power of $P_{\mathrm{o}} = 10\,\mathrm{kW}$ are given in **Fig. 10** where a calculated efficiency of 98.0 % is stated. The system elements with highest losses are, as expected, the diode bridge and the dc-side connected smoothing inductor of the passive rectifier circuit as 95 % of the output power is delivered by the diode bridge. The biggest loss part of the FCC is the coupled three-phase choke. The semiconductor losses of the FCC on the other hand are quite small and the losses of the three-level bridge leg are mainly caused by switching losses which could be reduced by application of SiC diodes. As discussed earlier also the losses of the bidirectional switches can be reduced by application of RB-IGBTs.

TABLE II: Power Devices Selected for Implementation of the FCC Prototype.

$S_{\mathrm{ia,b}}$	1200 V/40 A IGBT, IKW40T120, Infineon
$S_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}}\pm}$	600 V/20 A IGBT, IKW20N60H3, Infineon
$D_{\mathrm{h3}\pm}$	1200 V/15 A, STTH1512W, ST-Microelectronics
$C_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}}}$	470 μF/400 V, EPCOS B43501-type
L_{cp}=L_{cn}=L_{h3}	3.2 mH, Iron core 3UI60a, N = 123 turns
C_{F}, C_{S}	6.8 μF/275 $\mathrm{V_{AC}}$, MKP X2, Arcotronics
C_{o}	2.2 mF/400 V, Felsic CO 39 A728848
L_{DC}	2.25 mH, Iron core 2 x UI60a
$D_1 - D_6$	35 A/1600 V, 36MT160, Vishay

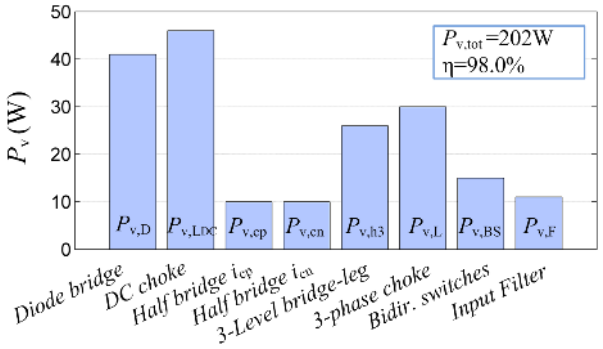


Fig. 10: Calculated power loss breakdown of the proposed rectifier system for an output power of 10 kW.

A. *Bidirectional switches* $S_{1\mathrm{a}} \ldots S_{3\mathrm{b}}$

The bidirectional switches ($S_{1\mathrm{a}} \ldots S_{3\mathrm{b}}$) used for current injection of the current i_{h3} into the mains are implemented using back-to-back connected 1200 V rated IGBTs (cf., **Fig. 1**). Alternatively to the two back-to-back connected IGBTs also parallel arranged Reverse Blocking IGBTs (RB-IGBTs) could be used which would allow a reduction of losses. In **Fig. 11** the required switching scheme of the switches $S_{1\mathrm{a}} \ldots S_{3\mathrm{b}}$ is shown. According to **Fig. 11** each IGBT is switched only twice a period and semiconductors with a large chip area and therefore small conduction losses can be applied as switching losses can be neglected due to the very few switching actions. A four step commutation sequence as known from Matrix converters [13] can be implemented advantageously to commutate the current i_{h3} from one phase to another phase. As can be seen in **Fig. 11** the commutation has to be done when the amplitude of i_{h3} reaches its maximum/minimum and the current direction in these points is clearly defined. The current dependent four step commutation sequence is therefore applied. In case of no-load or light-load situation the detection of the actual current direction might be incorrect and two additional diodes ($D_{\mathrm{P}+}$ and $D_{\mathrm{P}-}$) to the positive/negative output of the diode bridge as indicated in **Fig. 1** are proposed to prevent the bidirectional switches from damage.

A sector detection must be implemented to initiate the four step commutation sequence. The correct detection of the sectors is very important as slight deviations result in considerably large current distortions. Sector detection could be done by application of a PLL in the digital controller, however, the

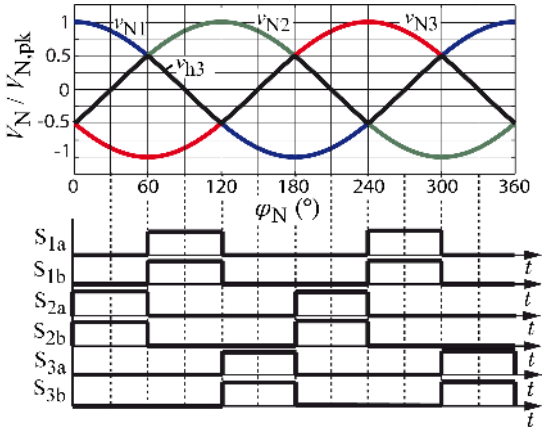


Fig. 11: Switching scheme of bidirectional switches $S_{1a} \dots S_{3b}$ used for current injection of i_{h3} into a single phase.

limited switching frequency of 10 kHz results in an update of every 50 μs if double edge sampling is used for PWM which would lead too large current distortions. Analogue comparators in combination with bandpass filters are hence used for sector detection and the commutation sequence is implemented using a Lattice CPLD (Mach XO 2280).

B. Input Filter

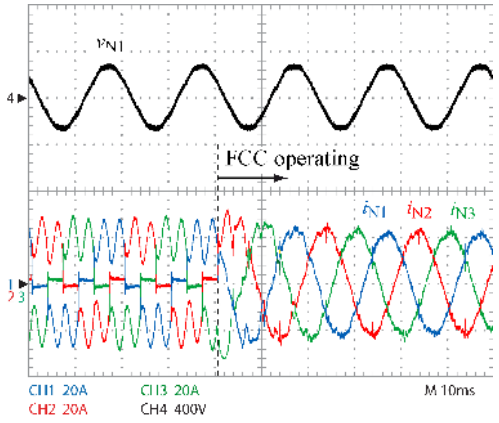
Filter capacitors at the ac-side of the rectifier are required due to the current ripple of the injected currents. These filter capacitors build an LC-tank together with the mains impedance which is excited at the end of every multi-device commutation process of rectifier diodes and bidirectional switches and must be damped. An RC snubber circuit (R_S, C_S) as shown in **Fig. 1** is used to damp this oscillation. The FCC may optionally be used to implement active damping of the input filter but this is subject of further research.

V. Experimental Results

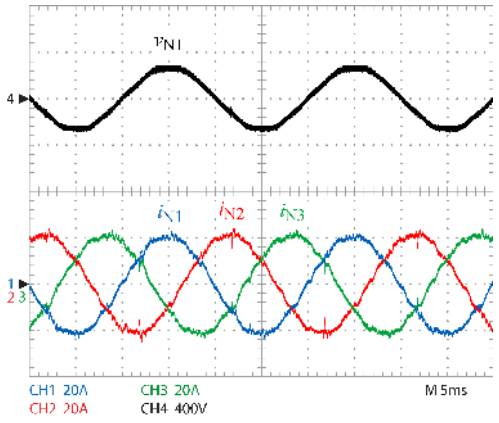
Measurement results of the constructed 10 kW laboratory prototype are given in **Fig. 12** and **Fig. 13**. **Fig. 12(a)** shows the transition from passive diode mode operation with poor input current quality ($\mathrm{THD_I} = 46.4\,\%$) to active current shaping using the proposed FCC for $P_o = 10\,\mathrm{kW}$. A smooth transition can be observed and the active current shaping results in sinusoidal mains currents with good input current quality.

The three mains currents i_{Ni} and phase voltage v_{N1} are shown in **Fig. 12(b)** for $P_o = 10\,\mathrm{kW}$. The currents show a $\mathrm{THD_I}$ of 2.3 % and a power factor of $\lambda = 0.99$ can be read. Please note that the mains voltage already shows a $\mathrm{THD_v}$ of 1.7 %. Adverse spikes of i_{N2} which can be observed in **Fig. 12(b)** originate from a non-optimal sector determination of phase i_{N3} caused by an inaccurate behavior of one channel of the analog measurement circuitry. It is expected that with an enhanced analog stage this spikes can be avoided leading also to a slight $\mathrm{THD_I}$ improvement.

Fig. 13(a) shows the measured currents i_{pos}, i_L and i_{cp} for an output power of $P_o = 10\,\mathrm{kW}$. The current i_L is defined by the voltage difference between the output of the diode bridge



(a)

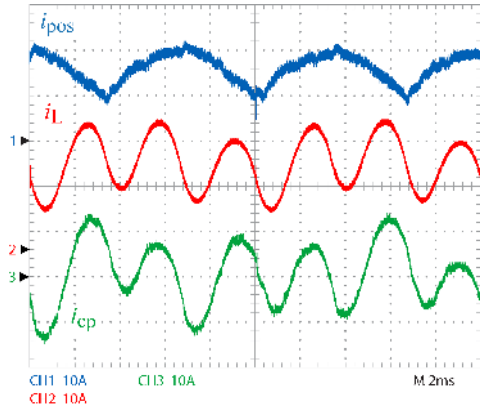


(b)

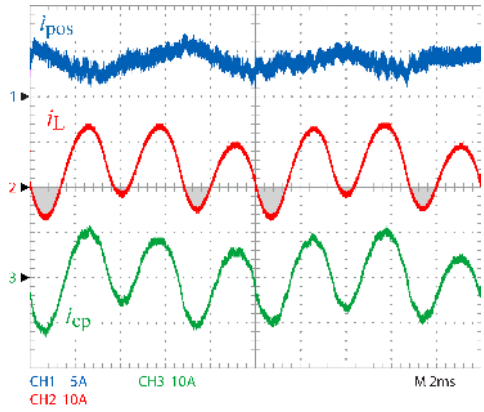
Fig. 12: Measurement results taken from the laboratory prototype an output power of 10 kW; (a) Transition from passive diode mode operation ($\mathrm{THD_I} = 46.4\,\%$, $\lambda = 0.905$) to active current shaping using the proposed FCC, (b) Steady state operation at $P_o = 10\,\mathrm{kW}$ ($\mathrm{THD_I} = 2.3\,\%$, $\lambda = 0.998$).

and the output voltage V_o and shows an average value of $I_{L,avg} = 18.5\,\mathrm{A}$ and a peak to peak ripple of $\hat{I}_{L,AC} = 15\,\mathrm{A}$ with characteristic 6^{th} harmonic. In addition to the expected 300 Hz ripple also a 150 Hz variation occurs. This is a result of asymmetrical voltages of the feeding mains and the injection currents i_{cp} and i_{cn} have to compensate this effect as shown in **Fig. 13(a)**. **Fig. 13(b)** shows the situation for $P_o = 2.6\,\mathrm{kW}$ where in passive operating mode a discontinuous current i_L would occur. Negative values of i_L can be read which is injected by the currents i_{cp} and i_{cn} - the ripple current results in a circulating current in L_{DC}, C_o and the two half-bridges which reduces the efficiency at light-load or no-load condition.

The measured efficiency rates η_{meas} of the total converter are shown in **Fig. 14(a)** as a function of output power P_o in comparison with the calculated efficiency η_{calc}. An excellent measured efficiency of 97.8 % can be read at $P_o = 10\,\mathrm{kW}$. The efficiency of the passive diode rectifier for the same load conditions has been obtained with 98.7 %. **Fig. 14(b)** depicts the measured input current quality $\mathrm{THD_I}$ and power factor λ as a function of output power P_o. The built rectifier system achieves a $\mathrm{THD_i}$ below 5 % down to $P_o \approx 3\,\mathrm{kW}$. Also a power factor above 0.95 is measured for an output power above



(a)



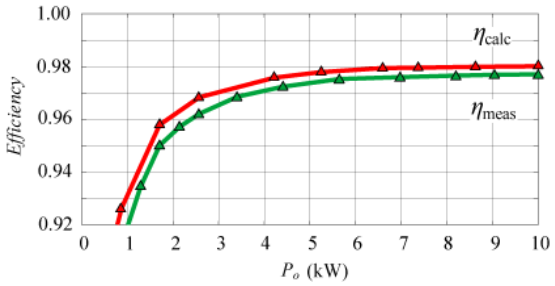
(b)

Fig. 13: Measured currents i_{pos}, i_{L} and i_{cp} for an output power of (a) $P_{\mathrm{o}} = 10\,\mathrm{kW}$ and (b) $P_{\mathrm{o}} = 2.6\,\mathrm{kW}$.

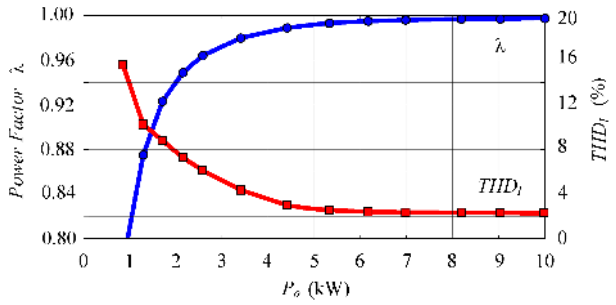
$P_{\mathrm{o}} \approx 2.2\,\mathrm{kW}$. The constructed FCC shows a good performance even for half load condition ($P_{\mathrm{o}} = 5\,\mathrm{kW}$) where a $\mathrm{THD_I}$ of $2.7\,\%$ and a power factor of $\lambda = 0.992$ can be measured at a good efficiency of $\eta_{\mathrm{meas}} = 97.5\,\%$. It has to be noted that the presented prototype converter neither has been optimized for power density nor for efficiency. A further improvement of the efficiency would be achievable based on an optimized design.

VI. Conclusion

The basic operating principle of the three-phase rectifier circuit using a FCC is verified by the constructed laboratory prototype with a power rating of 10 kW. Although the system is not optimized for efficiency and a rather small switching frequency of 10 kHz is used an efficiency of 97.8 % is achieved. The input currents show a $\mathrm{THD_I}$ of only 2.3 % and even at 30 % of output power a $\mathrm{THD_I}$ of $\approx 5\,\%$ is measured. The system shows several degrees of freedom which allow to optimize it in different directions. The topology allows the extension of an existing passive rectifier circuits with dc-side located smoothing inductor to a low-harmonic input stage but in contrast to standard active three-phase rectifier systems the rectifier output V_{o} shows no high-frequency CM voltage. Several controllers are required for the proper operation of the rectifier topology which are implemented in a single DSP.



(a)



(b)

Fig. 14: (a) Measured η_{meas} and calculated efficiency η_{calc} of the laboratory prototype for a mains voltage of $V_{\mathrm{LL}} = 400\,\mathrm{V}$. (b) Measured power factor λ and input current quality ($\mathrm{THD_I}$) as a function of output power.

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