Design and Fabrication of 50-nm Thin-Body p-MOSFETs With a SiGe Heterostructure Channel

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***Abstract*—Thin-body p-channel MOS transistors with a SiGe/Si heterostructure channel were fabricated on silicon-on-insulator (SOI) substrates. A novel lateral solid-phase epitaxy process was employed to form the thin-body for the suppression of short-channel effects. A selective silicon implant that breaks up the interfacial oxide was shown to facilitate unilateral crystallization to form a single crystalline channel. Negligible threshold voltage roll-off was observed down to a gate length of 50 nm. The incorporation of $Si_{0.7}Ge_{0.3}$ in the channel resulted in a 70% enhancement in the drive current. This is the smallest SiGe heterostructure-channel MOS transistor reported to date. This is also the first demonstration of a thin-body MOS transistor incorporating a SiGe heterostructure channel.**

***Index Terms*—Heterojunctions, MOSFETs, SiGe, strain, thin-body.**

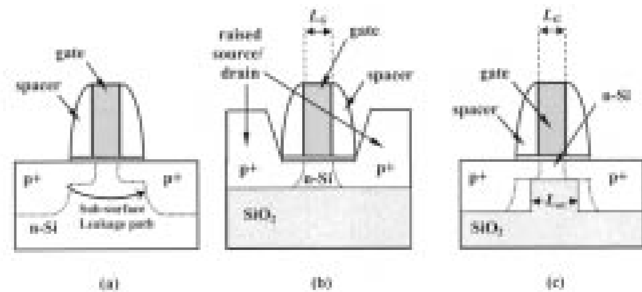

Fig. 1. Comparison of the device structures for (a) a conventional MOS transistor, (b) a raised source/drain thin-body transistor, and (c) a thin-body transistor with a buried oxide wall. The advantage of the thin-body device structure in suppressing subsurface leakage current is illustrated.

I. Introduction

As the gate length L_G of the MOSFET is scaled down into the sub-100-nm regime for improved performance and density, the requirements for body-doping concentration, gate oxide thickness, and source/drain (S/D) doping profiles to control short-channel effects become increasingly difficult to meet when conventional device structures based on bulk silicon (Si) substrates are employed. The heavy channel doping required to provide adequate suppression of short-channel effects results in degraded mobility and enhanced junction leakage. The aggressive reduction of the SiO_2 gate dielectric thickness for reduced short-channel effects and improved drive current leads to increased direct tunneling gate leakage current and standby power consumption, and also raises concerns regarding the gate oxide reliability. For device scaling well into the sub-100-nm regime, a promising approach to controlling short-channel effects is to use a thin Si film as the MOSFET channel so that sub-surface leakage paths are eliminated. A device structure that implements this concept is the thin-body MOSFET [1], [2]. In a thin-body MOSFET, the source-to-drain current is restricted to flow in a region close to the gate for superior gate control, as illustrated in Fig. 1. Since it does not rely on a heavily-doped channel for the suppression of short-channel effects, it avoids the problems of mobility degradation due to impurity scattering and threshold voltage (V_{TH}) fluctuation due to the random variation of the number of dopant atoms in the channel region of nanoscale transistors [3].

Another attractive approach to improving device performance exploits the strain- or band-structure-induced mobility enhancement to increase the drive current. One of the most notable effects is the enhanced hole mobility in silicon–germanium (SiGe) under biaxial compressive strain [4]–[7]. Recently, we have demonstrated enhanced performance for p-type SiGe-channel MOSFET on bulk Si substrate down to a channel length of 100 nm [8]. There is strong indication that compressively strained SiGe not only increases the hole mobility, but also enhances hole velocity overshoot and improves the effective saturation velocity. This is supported by a recent experimental investigation of the high-field hole transport in strained SiGe using thick-oxide MOSFETs [9]. Therefore, a device that combines the advantages of the SiGe/Si heterostructure and a thin-body could be the device structure of choice in the sub-100-nm regime [10].

In this work, we report the concept, design, and demonstration of 50-nm thin-body silicon-on-insulator (SOI) p-channel MOSFETs and show the enhancement in drive current due to the incorporation of SiGe in the channel. Section II explains the design considerations for the thin-body structure and the SiGe/Si heterostructure channel. Device fabrication is described in Section III. A discussion of the device characterization results is given in Section IV. Section V summarizes this work.

II. Device Design Considerations

Design considerations for the thin-body structure and the SiGe heterostructure layers are addressed in this section. In comparison to the vertical transistor [11] or the surround-gate structure [12], the thin-body structure is a more evolutionary

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improvement of the conventional transistor structure, and can be fabricated with less process complexity.

A. Thin-Body Structure

Two possible implementations of the thin-body concept are illustrated in Fig. 1(b) and (c). The first demonstrations of the device structures in Fig. 1(b) and (c) were reported in [2] and [10], respectively. Both device structures make use of a channel with a thickness of 20 nm or less to control short-channel effects.

The device shown in Fig. 1(b) has a thin-body on insulator structure [13], [14], and is essentially an extension of the fully depleted SOI transistor. Since a thin S/D region would contribute a high series resistance that degrades the drive current, a raised S/D is introduced to avoid the series resistance problem. There are a few ways of forming the raised S/D structure after the gate patterning step. Reference [14] demonstrated raised S/D formation by poly-Si deposition followed by an etch-back process. A more elegant approach was reported in [13] where the raised S/D structure was formed by the selective deposition of Germanium (Ge) onto the source and drain regions. Nevertheless, parasitic capacitances between the raised S/D and the gate are inherent in this device structure. This is expected to adversely impact the device speed and power consumption. An attempt to reduce the parasitic capacitance by increasing the distance between the raised S/D and the gate leads to an increase in series resistance. This tradeoff between series resistance and gate parasitic capacitances is not present in the planar thin-body structure as depicted in Fig. 1(c).

The planar thin-body structure resembles the conventional transistor structure, except that it has a buried oxide wall below the channel. This oxide wall effectively blocks subsurface leakage paths between the source and the drain. Since the S/D current must flow in the vicinity of the Si-SiO_2 interface, the gate exerts excellent control of the carrier density in the channel. It should also be noted that this concept is also compatible with bulk substrates and does not necessarily require an SOI substrate. The channel and S/D regions of the planar thin-body structure [Fig. 1(c)] can also be visualized as being transformed from the raised S/D structure [Fig. 1(b)] by a reflection about the Si surface (dashed line). This is the device structure that is investigated in this work.

Two-dimensional (2-D) process and device simulations were performed using *Silvaco Athena* and *Atlas*, respectively, to study the device design issues. Fig. 2 shows the simulated drain current $I_{\rm DS}$—gate voltage $V_{\rm GS}$ characteristics of a $L_G = 50$ nm p-MOS device. The thickness of the Si channel is 20 nm, and the gate oxide thickness is 2 nm. We have assumed a low and uniform body doping (10^{15} cm^{-3}) and simple Gaussian S/D doping profiles (peak concentration $= 10^{20}$ cm^{-3}, surface doping concentration under the gate edge $= 5 \times 10^{16}$ cm^{-3}). There is a trade-off between the drive current $I_{\rm Dsat}$ and the off-state leakage $I_{\rm off}$, as determined by $L_{\rm ox}$ [15]. A smaller $L_{\rm ox}$ leads to degraded short-channel immunity, e.g., high subthreshold swing and $I_{\rm off}$, but also leads to a smaller series resistance and therefore a higher drive current. For a device with $L_G = 50$ nm, choosing $L_{\rm ox} = 30$ nm gives a good subthreshold swing of $\approx$80 mV/decade without significant compromise on $I_{\rm Dsat}$. Fig. 3 shows the effect of a gate-to-oxide-wall misalignment on the threshold voltage. $V_{\rm TH}$ is defined as the $V_{\rm GS}$ at which $I_{\rm DS} = 1$ μA/μm at $V_{\rm DS} = 50$ mV. With increasing gate misalignment, the effective channel thickness is increased, and this results in higher subthreshold current and thus lower $|V_{\rm TH}|$. A larger $L_{\rm ox}$ improves immunity to the misalignment of the oxide wall and the associated $V_{\rm TH}$ variation. The simulation shows that for a 50-nm device with a $L_{\rm ox}$ of 30 nm, a misalignment of about $\pm$15 nm is tolerable given that $\Delta|V_{\rm TH}| < 50$ mV. The insensitivity of $V_{\rm TH}$ to the channel dopant concentration $N_{\rm sub}$ is shown in Fig. 4. $\Delta V_{\rm TH}$ is defined to be $[V_{\rm TH} - V_{\rm TH}(N_{\rm sub} = 1 \times 10^{16}\ {\rm cm}^{-3})]$. Since $V_{\rm TH}$ does not vary significantly for dopant concentrations up to at least 4×10^{17} cm^{-3}, this device design achieves a high tolerance to statistical fluctuation of the dopant density. By using a low-body dopant concentration, the body depletion charge has a negligible contribution to the threshold voltage, so that the threshold voltage variation due to random fluctuations in the dopant density and position can be greatly reduced. The

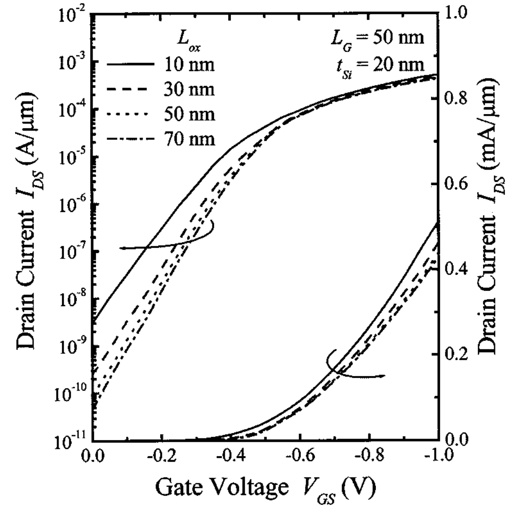

Fig. 2. Simulated $I_{\rm DS} - V_{\rm GS}$ of a $L_G = 50$ nm P-MOS device with a body thickness of 20 nm, illustrating the tradeoff between the drive current $I_{\rm Dsat}$ and the off-state leakage $I_{\rm off}$ as a function of $L_{\rm ox}$.

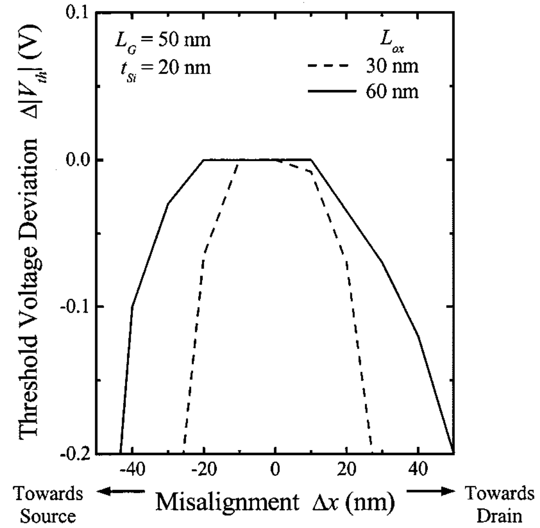

Fig. 3. Effect of the gate-to-oxide-wall misalignment on the threshold voltage $V_{\rm th}$. Misalignment toward drain is positive. The body thickness is 20 nm.

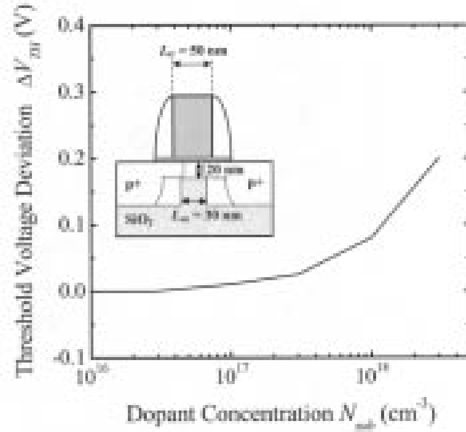

Fig. 4. Dependence of threshold voltage $V_{\rm TH}$ on the channel dopant concentration $N_{\rm sub}$. $\Delta V_{\rm TH}$ is defined to be $[V_{\rm TH} - V_{\rm TH}(N_{\rm sub} = 1 \times 10^{16}\ {\rm cm}^{-3})]$. The device dimensions are indicated in the inset.

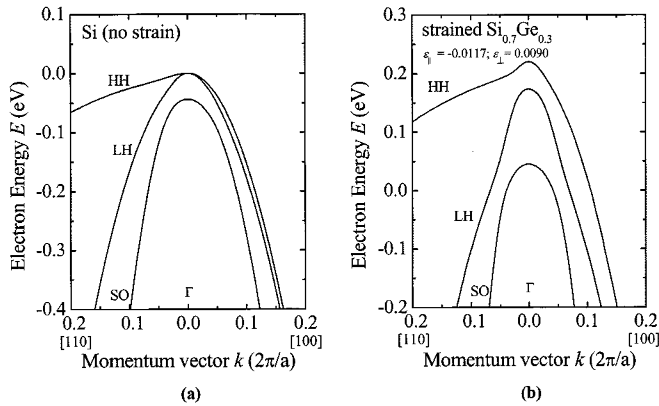

Fig. 5. Electronic band structures for (a) bulk Si and (b) strained-$\rm Si_{0.7}Ge_{0.3}$ along the [100] and [110] crystallographic directions in the vicinity of the Γ point. Biaxial compressive strain in $\rm Si_{0.7}Ge_{0.3}$ results in a lower effective mass in the top-most valence band.

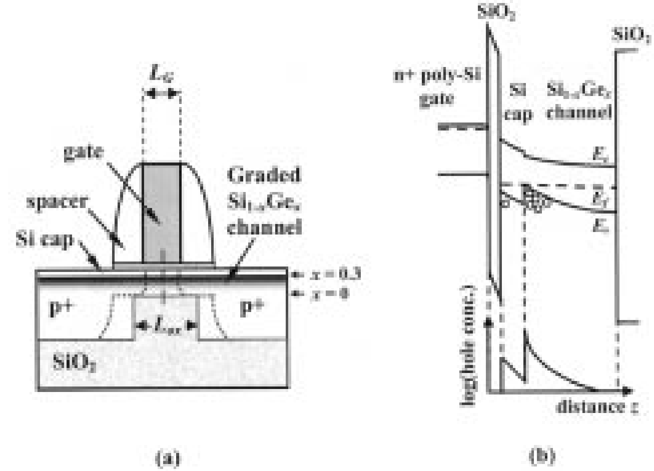

Fig. 6. (a) Cross section of a thin-body transistor with a SiGe heterostructure channel. The energy band diagram along the dashed line is shown in (b). Most of the holes in the inversion layer are found in the SiGe layer.

threshold voltage can be controlled by varying the workfunction of the gate through the use of SiGe or metal gates.

B. Silicon-Germanium (SiGe) Heterostructure

The performance of n- and p-MOS transistors are strongly asymmetric because the electron mobility is much higher than the hole mobility in silicon. To improve p-MOSFET performance and reduce this asymmetry, various heterostructure devices with SiGe-layers have been proposed to improve the hole mobility [16]. The most promising method for improving p-MOSFET performance is through the use of a strained SiGe-layer grown on relaxed or bulk Si because this does not require a thick relaxed SiGe buffer layer which is expensive and difficult to process.

It is imperative to review the effect of strain on the electronic band-structures of SiGe before we explore the design of the SiGe heterostructure. When a thin SiGe film is pseudomorphically grown on Si, it experiences biaxial compressive strain. In Fig. 5, we show the heavy-hole (HH), light-hole (LH), and spin-orbit split-off (SO) bands of bulk Si and bulk $\rm Si_{0.7}Ge_{0.3}$ under biaxial compressive strain. The band structures were calculated using the k.p. method, where the valence-band maximum in Si is taken as the reference energy level. Material parameters were taken from [17] and [18]. The HH and LH bands in strained-SiGe become nondegenerate at the Γ point. In addition, the existence of biaxial compressive strain in the $\rm Si_{0.7}Ge_{0.3}$ film couples the HH and LH bands and introduces band-mixing which reduces the effective mass in the top-most HH band. Consequently, the hole mobility in compressively strained SiGe is increased. By introducing 30% Ge in the pseudomorphic layer, the in-plane mobility is expected to be enhanced by more than 33% [19].

Fig. 6(a) shows our design of a thin-body transistor with a graded $\rm Si_{1-\it x}Ge_{\it x}$ heterostructure channel. The Ge mole fraction x is graded from 0 to 0.3 (bottom-to-top) in the 15-nm thick $\rm Si_{1-\it x}Ge_{\it x}$ layer. The energy-band diagram along the dashed line in the device cross section is shown in Fig. 6(b). The top Si cap layer has a thickness $t_{\rm Si\text{-}cap}$ of 4 nm and serves to provide a good Si/$\rm SiO_2$ interface quality. Nearly all of the band-gap difference between $\rm Si_{0.7}Ge_{0.3}$ and Si appears at the valence band. As a result, the majority of the holes are confined in the SiGe-channel where the mobility is enhanced [Fig. 6 (b)]. The carrier profile under a typical inversion bias is schematically shown below the energy band diagram.

By integrating the charge density over the regions of the Si-cap and the SiGe-channel, one can determine the ratio of the amount of charge in the SiGe-channel to that in the parasitic Si-channel (Si-cap). It is advantageous to ensure that this ratio is larger than unity in the operation regime of the transistor so that most of the holes are in the high-mobility SiGe layer. There is a gate voltage, $V_{G,\rm Si\text{-}cap}$, above which the parasitic surface Si-channel contains more carriers than the SiGe-channel. Thus, at $V_G = V_{G,\rm Si\text{-}cap}$, the total integrated charge density in the SiGe-channel $Q_{\rm SiGe}$ is equal to that in the Si-cap $Q_{\rm Si}$. Parameters which are critical in determining $V_{G,\rm Si\text{-}cap}$ include the relative thicknesses of the gate oxide thickness $t_{\rm ox}$ and $t_{\rm Si\text{-}cap}$, and the thickness and Ge mole fraction of the SiGe layer. A larger Ge mole fraction and band offset at the Si/SiGe interface results in better hole confinement, but strain relaxation issues set the upper limit on the mole fraction of Ge that can be incorporated. Using $t_{\rm ox} = 2.0$ nm, $t_{\rm Si\text{-}cap} = 4.0$ nm, and a graded

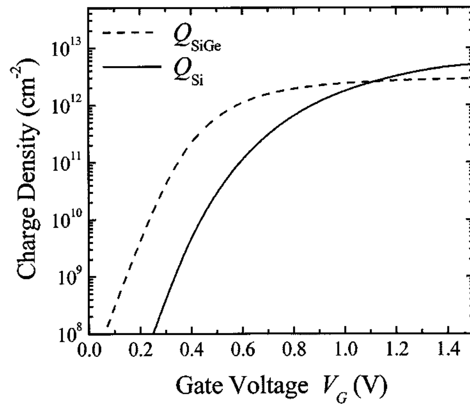

Fig. 7. The integrated charge densities in the Si and SiGe layers, $Q_{\rm Si}$ and $Q_{\rm SiGe}$, respectively, as a function of the gate voltage.

Ge mole fraction from 0 to 0.3 (bottom-to-top) over a 15-nm SiGe layer, our calculations indicated that $V_{G,\text{Si-cap}}$ is about 1.15 V (Fig. 7). The supply voltage $V_{\rm DD}$ for the technology node with $L_G = 50$ nm is 1 V [20]. Since $V_{G,\text{Si-cap}} > V_{\rm DD}$, most of the carriers are in the SiGe layer in the regime of device operation.

III. Device Fabrication

Since we want to achieve a thin-body thickness of less than two or even one hundred angstroms, etch-back or oxidation-thinning processes may be incapable of producing a uniform body thickness as this is limited by the thickness uniformity of the starting thick SOI layer, which is typically in the order of 5 nm. A deposited channel film is more desirable as it would provide a better thickness uniformity.

MOSFETs with gate length down to 50 nm were fabricated on SmartCut wafers which had a 50-nm thick SOI layer and a 400-nm buried oxide. The SOI layer was etched away completely except for regions which were to become the thick source and drain islands. The trench between the source and drain islands, which is about 20-nm shorter than the gate length, was filled with SiO_2 using low-pressure chemical-vapor deposition (LPCVD) and planarized to give the structure shown in Fig. 8(a). Then, 15 nm of undoped amorphous $Si_{1-x}Ge_x$ (graded from $x = 0$ to $x = 0.3$ from bottom to top) and 5 nm of undoped amorphous-Si (α-Si) were deposited at 425 °C using LPCVD to form a heterogeneous amorphous film connecting the source and drain islands. The precursor gases were germane GeH_4 and disilane Si_2H_6 and the pressure was 300 mtorr. On the control wafer, 20 nm of undoped α-Si was deposited instead of the SiGe/Si stack to obtain a pure-Si channel. The process conditions used are derived from Fig. 9. The transition temperature for deposition in the amorphous phase to deposition in the polycrystalline phase is lower for SiGe than for Si. Therefore, the depositions for the SiGe heterostructure channel and the Si control were done at lower temperatures than those that are typically used for Si films.

This was followed by a masked or unmasked 20 keV Si^+ implant with a dose of 7×10^{15} cm^{-2} to break up the interfacial oxide over the source island or over both the source and drain islands, respectively (Fig. 10). This interfacial native oxide is

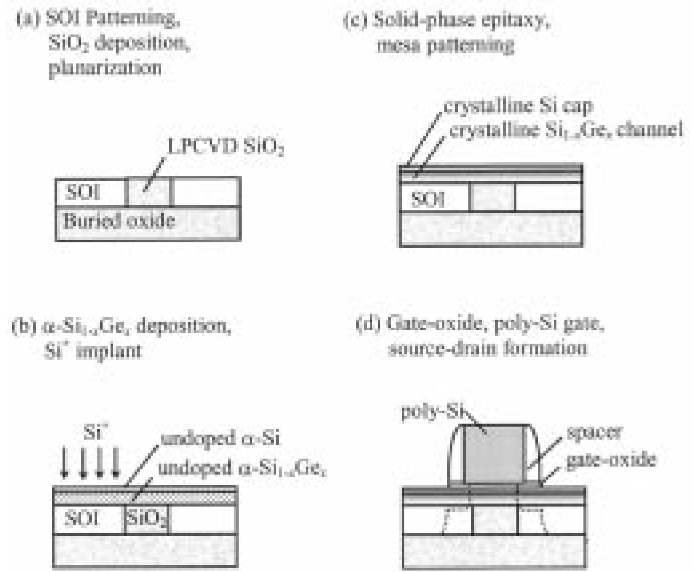

Fig. 8. Process flow for the SiGe-channel thin-body MOSFET. Mesa patterning is not shown.

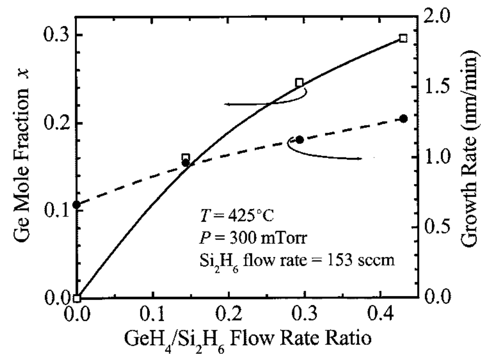

Fig. 9. Process conditions used for the deposition of amorphous $Si_{1-x}Ge_x$ for channel formation. The Ge mole fraction and growth rate are determined from the growth time and Rutherford back-scattering (RBS) analysis.

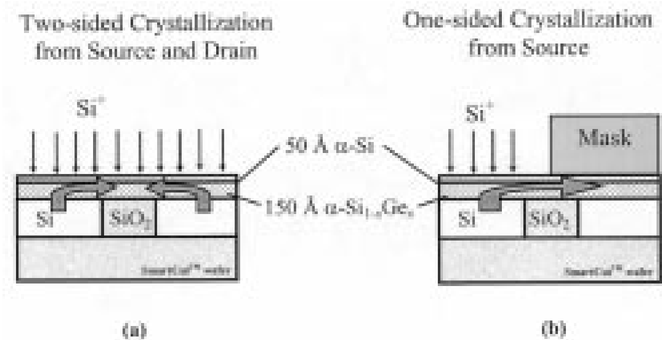

Fig. 10. Facilitation of directional crystallization. (a) With Si^+ implant on both the source and drain islands, SPE growth fronts meet near middle of channel to form a grain boundary. (b) With a masked Si^+ implant, SPE growth proceeds from one side to the other.

found to exist between the crystalline silicon and the deposited amorphous layer and acts as a barrier to solid-phase epitaxy (SPE). By breaking this interfacial oxide, the Si^+ implant effectively facilitates the crystallization of the amorphous film with the SOI island(s) as the seed. With an unmasked Si^+ implant, the

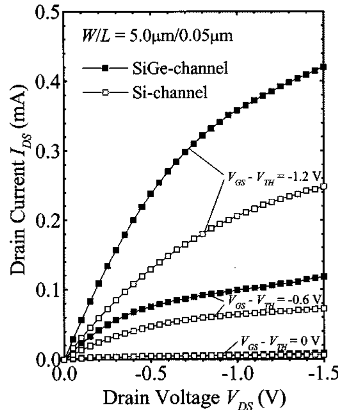

Fig. 11. Output characteristics of the SiGe-channel and the Si-channel thin-body MOSFETs. The higher hole mobility in the SiGe-channel results in a 70% improvement in the drain current at $V_{\rm DS} = -1.5$ V and $V_{\rm GS} - V_{\rm TH} = -1.2$ V.

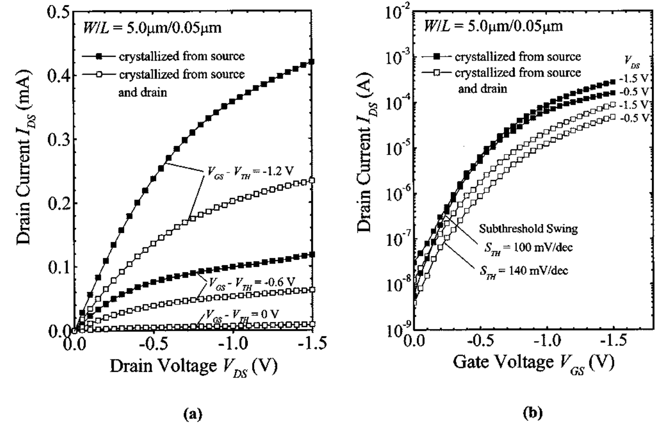

Fig. 12. (a) $I_{\rm DS}$ is 80% higher in the SiGe-channel thin-body MOSFETs with the channel laterally crystallized from the source than from both the source and drain. (b) SiGe-channel thin-body MOSFETs with SPE seeding at the source only shows better turn-off characteristics.

SPE growth proceeds from both ends of the channel and the two growth fronts meet near the middle of the channel, resulting in a low angle grain boundary [Fig. 10 (a)]. With the implant masked such that native oxide is broken up only on one side, crystallization proceeds from one side only, so that the grain boundary in the channel is eliminated from the channel at the cost of an additional lithography step [Fig. 10(b)]. The crystallization step, performed at 550 °C for 12 h, results in lateral solid-phase epitaxial growth to form the channel [Fig. 8(c)], and the range of the lateral SPE is about 0.25 μm.

After the SPE process step, 2 nm of SiO_2 was grown by dry thermal oxidation to form the gate dielectric. This was followed by an *in-situ* n^+ poly-Si deposition, and the poly-Si gate was patterned using electron-beam lithography. The misalignment between the gate and the oxide-wall is typically less than 10 nm. Source and drain extensions were formed by boron ion implantation. Low-temperature deposited SiO_2 was used as the spacer. Self-aligned source and drain regions were then formed by boron ion implantation to give the structure as shown in Fig. 8(d). The dopants were activated by a 800 °C 30 rapid thermal anneal (RTA). Finally, low-temperature oxide passivation, contact-hole etch, metal deposition, and metal patterning steps were performed to complete the device. This device structure is also called the SPE MOSFET (SPEFET) [2] since the thin-body was formed by a lateral solid-phase epitaxy process.

IV. Device Characterization

A. Performance Enhancement From SiGe Heterostructure Channel

In Fig. 11, the output characteristics of the SiGe-channel and the Si-channel thin-body MOSFETs are compared. The drain current $I_{\rm DS}$ versus drain voltage $V_{\rm DS}$ curves are plotted for gate over-drives $(V_{\rm GS} - V_{\rm TH})$ of 0, − 0.6, and −1.2 V. These devices had SPE seeding at the source side only so that the low angle grain boundary is not present in the channel region. An enhancement of 70% in the current drive is observed at $V_{\rm DS} = -1.5$ V, $V_{\rm GS} - V_{\rm TH} = -\ 1.2$ V in the SiGe-channel devices. This is believed to be due to the lower effective mass of holes in $Si_{0.7}Ge_{0.3}$ which could account for a 20% enhancement and probably the existence of biaxial compressive strain in the channel which lifts the degeneracy of the light-hole (LH) and heavy-hole (HH) bands at the Γ point, leading to an even lower in-plane effective mass of the topmost HH band [4], [5]. The strain and defects depth profile of SPE grown SiGe layers on (100) Si has been studied in [21]. In that work, it was found that a fully-strained defect-free 30-nm thick $Si_{0.79}Ge_{0.21}$ layer can be grown by SPE if it is heavily boron-doped. Undoped samples are 80% strained, i.e., partially relaxed, for the same Ge composition [21]. In our SiGe-channel device considered here, the SPE first proceeds vertically from the heavily doped source region, in which full compressive strain is believed to exist in the graded SiGe layer. The SPE then proceeds laterally. One speculation on how strain could be incorporated in the SiGe-channel region is that the elongated lattice constant of SiGe in the vertical direction gets transferred laterally to the channel region during the SPE growth. Although we are not aware of any reports of SPE in which the strained lattice is laterally transferred, this appears to be a plausible mechanism that explains the significant drive current enhancement observed in the SiGe-channel device compared to the Si-channel device. When compared to well-designed bulk MOSFETs, the drive currents of our devices are lower due to the large series resistance in the source and drain regions. A typical dopant activation step for the S/D regions in a CMOS process employs a 1025 °C 5 s rapid thermal anneal, or spike anneal with a higher peak temperature, e.g., 1050 °C. We have used a low and conservative thermal budget (800 °C, 30 s RTA) for the source and drain dopant activation due to concerns about strain relaxation. However, we have demonstrated that a higher thermal budget such as 950 °C 30 s RTA is compatible with a similar strained heterostructure [8]. Further process optimization is required to improve the drive currents of our devices.

B. Unilateral Crystallization of Channel

In Fig. 12(a), the effects of one- and two-sided crystallization on the $I_{\rm DS} - V_{\rm DS}$ characteristics of the SiGe-channel thin-body MOSFETs are shown. The elimination of the grain boundary is seen to give about 80% improvement in the drive current at $V_{\rm DS} = -1.5$ V, $V_{\rm GS} - V_{\rm TH} = -1.2$ V. The $I_{\rm DS} - V_{\rm GS}$ characteristics are plotted in Fig. 12(b) to show the good turn-off behavior of the devices that used one-sided crystallization from

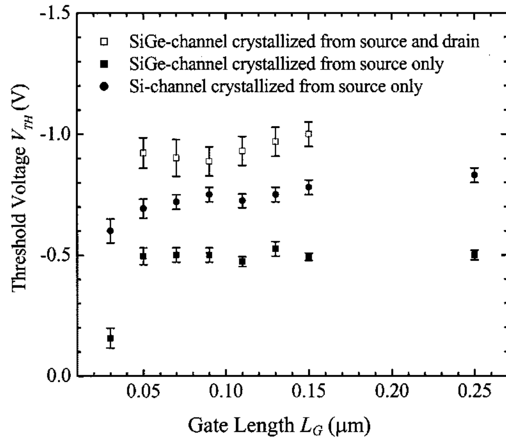

Fig. 13. All thin-body MOSFETs show little V_{TH} roll-off down to $L_G = 50$ nm. Both the existence of a grain boundary in the channels due to seeding at source and drain and the larger band-gap in Si-channel device yield high V_{TH} as expected. The error bars indicate the range of V_{TH} observed at each gate length.

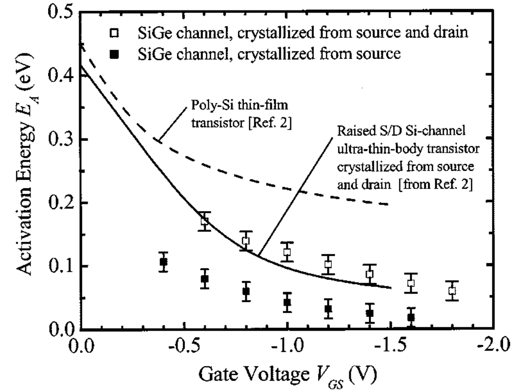

Fig. 14. Crystallization from the source gives a lower drain current activation energy, indicating low or no grain-boundary barrier. The activation energies of the poly-Si thin-film transistor and the raised source/drain thin-body transistor from [2] are also shown for comparison.

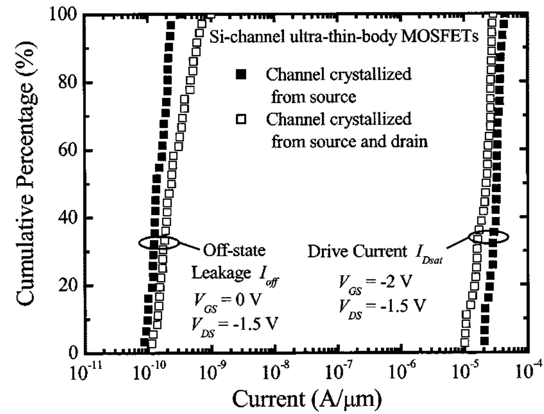

Fig. 15. Distributions of drive current I_{Dsat} and off-state leakage I_{off} for Si-channel thin-body MOSFETs. Devices with the channel crystallized from the source (solid symbols) have a higher drive current and lower off-state leakage compared to devices with the channel crystallized from both the source and drain (open symbols).

the source. With unilateral crystallization of the channel and the elimination of the grain boundary which potentially contains a high trap density, the subthreshold swing as well as the drain-induced barrier lowering (DIBL) are dramatically improved.

Fig. 13 illustrates the excellent control of short-channel effects in the thin-body devices. Negligible V_{TH} roll-off is observed down to a gate length of 50 nm. The high trap density at the grain boundary in devices that had two-sided crystallization degrades the subthreshold swing and also increases the threshold voltage. Fig. 13 also shows that the grain boundary not only increases the threshold voltage, but also causes a wider distribution of the V_{TH} values. The error bars in Fig. 13 indicate the range of V_{th} observed for each gate length. Considering the devices with the channel formed by unilateral crystallization (solid circles and squares in Fig. 13), the threshold voltages of the SiGe-channel devices are about 0.2 V lower than those of the Si-channel devices. This is consistent with the valence band offset between $\mathrm{Si_{0.7}Ge_{0.3}}$ and Si. The valence band offset at the $\mathrm{Si/Si_{0.7}Ge_{0.3}}$ heterostructure results in an earlier onset of inversion in the $\mathrm{Si_{0.7}Ge_{0.3}}$ channel, and therefore a lower threshold voltage.

Further understanding on the differences between the one- and two- sided crystallization can be obtained by studying the activation energy of the barrier at the grain boundary [22]. The grain boundary hinders carrier transport because trapped carriers at the grain boundary causes local band-bending that presents an energy barrier to carriers traveling from the source to the drain. Fig. 14 plots the drain current activation energy of the drain current as a function of the gate bias. For devices with the channel formed by two-sided crystallization, the asymptotic value of the activation energy at high gate bias is representative of the effect of the grain boundary on the carrier mobility [2], [22]. Fig. 14 shows that for all V_{GS}, the drain current activation energy is lower for the channel that is crystallized from one side. This provides further evidence that that the grain boundary is either eliminated or its barrier height much reduced by the masked Si implant.

The distributions of drive current I_{Dsat} and off-state leakage I_{off} for Si-channel thin-body MOSFETs with one-sided as well as two-sided crystallization are shown in Fig. 15. The one-sided crystallization of the channel is very effective in reducing the off-state leakage and increasing the drive current. The off-state leakage is reduced by as much as five times and the drive current is improved by as much as 80%. One-sided crystallization also gives a much tighter distribution of the off-state leakage as well as the drive current. This is another strong indication of the success of the masked Si implant in eliminating the channel grain boundary.

V. Conclusion

In conclusion, we have demonstrated the shortest gate length (50 nm) SiGe-channel heterostructure MOSFET reported to date. The device has a novel structure that employs an undoped thin-body on a SOI substrate to suppress the short-channel effects. The thin body was fabricated by lateral SPE which also provides a convenient way to produce the SiGe/Si heterostructure. A 70% enhancement in the drive current is observed due to the introduction of $\mathrm{Si_{0.7}Ge_{0.3}}$ in the channel. A masked interfacial oxide break-up implant is shown to facilitate unilateral crystallization to eliminate the grain boundary from the channel.

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