Design and Implementation of a Digital PWM Controller for a High-Frequency Switching DC-DC Power Converter

Aleksandar Prodic, Dragan Maksimovic and Robert W. Erickson

Colorado Power Electronics Center
Department of Electrical and Computer Engineering
University of Colorado at Boulder
Boulder, CO 80309-0425, USA
Aleksandar.Prodic@colorado.edu

Abstract **– This paper describes complete design and implementation of a digital controller for a high-frequency switching power supply. Guidelines for the minimum required resolution of the analog-to-digital converter, the pulse-width modulator, and the fixed-point computational unit are derived. A design example based on a buck converter operating at the switching frequency of 1MHz is presented. The controller design is based on direct digital design approach and standard root-locus techniques. Experimental results are shown to validate the design approach and the allocation of resources (resolution) in the implementation.**

I. INTRODUCTION

It can be expected that digital controllers will be increasingly used even in low-to-medium power, high-frequency switching power supplies where conventional analog controllers are currently preferred because of cost and performance reasons [1,2].

This paper addresses practical design and implementation of a digital controller for a power supply that operates at the switching frequency of 1MHz. Attention is given to the digital implementation with limited resources in terms of resolution of A/D and D/A (PWM) blocks and the time available to perform the required computations.

Typical system under consideration is shown in Fig.1.

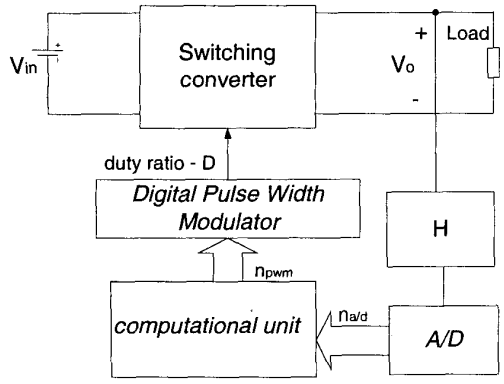

Fig.1. Digital control system for a switching converter

The required resolution of A/D and PWM units is addressed in Section II.

This work was supported by Tyco Electronics Power Systems and National Semiconductor Corp. through the Colorado Power Electronics Center.

Digital controller design approaches are briefly reviewed in Section III from the standpoint of the target converter characteristics and operating modes. A digital controller design example and implementation details are described in Section IV. Experimental results obtained from the 1MHz switching converter with the digital controller are presented in Section V.

II. RESOLUTION OF ANALOG-TO-DIGITAL CONVERTER AND DIGITAL PULSE WIDTH MODULATOR

The system in Fig.1 has an analog-to-digital (A/D) converter to sample the output voltage, a computational unit to determine the value of the switch duty ratio, and a digital pulse-width modulator (DPWM) that outputs a pulsating waveform that controls the switch(es) in the converter at the computed duty ratio. The DPWM serves as a D/A converter in the control loop. It is of interest to examine the required resolution of A/D and DPWM blocks.

A. Resolution of the A/D converter

To satisfy specifications for the output voltage regulation, resolution of the A/D converter has to enable error lower than the allowed variation of the output voltage ΔV_0:

$$\frac{\Delta V_o}{V_o}\cdot H \geq \frac{V_{\max_{a/d}}}{2^{n_{a/d}}\cdot V_o},\quad H=\frac{V_{ref}}{V_o} \tag{1}$$

where:

V_{ref} - is the reference voltage

$V_{max\ a/d}$ - is the full-range voltage of the analog-to-digital converter, assuming unipolar conversion in the range from 0 to $V_{max\ a/d}$

$n_{a/d}$ - is the resolution, i.e. the number of output bits of the A/D converter

H - is the output voltage sensor gain

Rearranging (1) gives the required A/D resolution:

$$n_{a/d}=\text{int}\left[\log_2\frac{V_{\max_{a/d}}}{V_{ref}}\cdot\frac{V_o}{\Delta V_o}\right] \tag{2}$$

where, int[ ] denotes taking the upper rounded integer value of the argument.

Equation (2) gives the minimum number of bits for the A/D converter to meet the design specifications in terms of the output voltage regulation. For example, if 2% variation of the output voltage is allowed, and if Vref is at least 78.2% of the A/D full-range voltage, a 6-bit A/D converter can be used.

The required A/D resolution can also be expressed in terms of the analog equivalent ΔV_q of the A/D least significant bit (LSB),

$$\Delta V_q \le H \cdot \Delta V_o \tag{3}$$

A. Resolution of the digital pulse width modulator

Digital pulse width modulator (DPWM) produces a discrete set of duty ratio values. This means that in steady state only a discrete set of output voltage values can be obtained. If the desired output voltage value doesn't belong to one of these discrete values, the feedback controller will switch among two or more discrete values of the duty ratio. In digital control systems, this type of oscillation is known as the "limit cycle" [3,4]. Figure 2.a illustrates the limit cycle oscillation observed in an experimental buck converter when the DPWM resolution is too low. The switching frequency is 50KHz, the input voltage is 5.6V, the output voltage is regulated at 3.3V, the A/D converter resolution is 7 bits, and Vref is 78.5% of the maximum input analog voltage. The DPWM resolution is 6 bits.

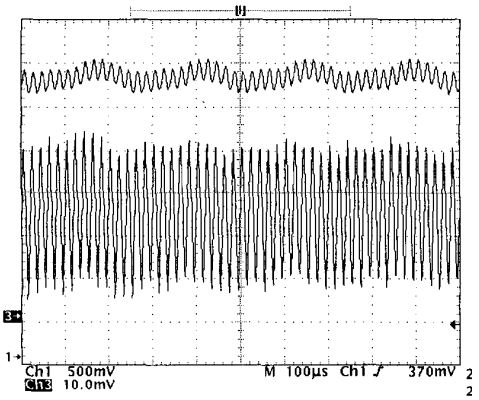

Fig.2.a. Output voltage (top -Ch.1) and inductor current (bottom - Ch3. 0.5Amps/div) oscillations caused by low resolution of DPWM.

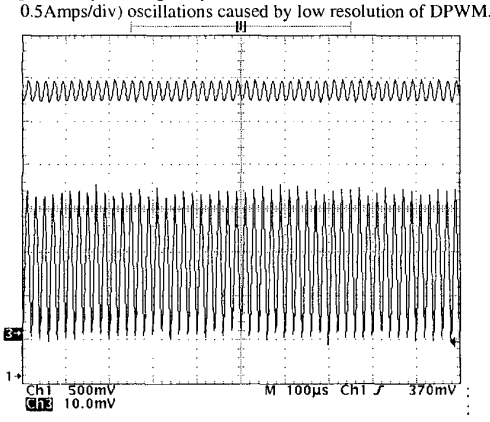

Fig.2.b. Output voltage (top - Ch.1) and inductor current (bottom - Ch3. 0.5Amps/div) for the properly selected resolution of DPWM.

A necessary condition to avoid the limit cycle oscillation is that the change in the output voltage caused by one LSB change in the duty ratio has to be smaller than the analog equivalent of the LSB of the A/D converter:

$$\frac{V_{\max a/d}}{H \cdot 2^{n_{a/d}}} > V_g \cdot \Delta M(D) \quad \text{or} \quad \frac{\Delta V_q}{H} > V_g \cdot \Delta M(D) \tag{4}$$

For example, for the buck converter:

$$M(D) = D, \ \Delta M(D) = \frac{1}{2^{n_{pwm}}} \tag{5}$$

where, n_{pwm} is the DPWM resolution, i.e. the number of bits of the DPWM. Substituting (5) and (2) into (4) gives the required DPWM resolution:

$$n_{pwm} \ge \text{int}\left[n_{a/d} + \log_2\left(\frac{V_{ref}}{V_{\max_{a/d}} \cdot D} \right) \right] \tag{6}$$

From (6) we can see that the minimum resolution of the DPWM depends on steady-state operating conditions in the circuit and the A/D resolution. Table I shows the required DPWM resolution for several typical switching converter configurations.

TABLE I
MINIMUM RESOLUTION OF DPWM FOR TYPICAL CONVERTERS

Type of converter/ Conversion ratio M(D)	**Minimal resolution of DPWM**
Buck M(D)=D	$\text{int}\left[n_{a/d} + \log_2\left(\frac{V_{ref}}{V_{\max_{a/d}} \cdot D} \right) \right]$ $\text{int}\left[\log_2\left(\frac{V_{ref}}{D \cdot \Delta V_q} \right) \right]$
Boost M(D)=1/(1-D)	$\text{int}\left[\log_2\left(\frac{1}{1-D}\left(\frac{V_{ref}}{V_{\max_{a/d}}} \cdot 2^{n_{a/d}} + 1 \right) \right) \right]$ $\text{int}\left[\log_2\left(\frac{1}{1-D}\left(\frac{V_{ref}}{\Delta V_q} + 1 \right) \right) \right]$
Buck-boost, Cuk, sepic M(D)=D/(1-D)	$\text{int}\left[\log_2\left(\frac{1}{1-D}\left(\frac{V_{ref}}{DV_{\max_{a/d}}} \cdot 2^{n_{a/d}} + 1 \right) \right) \right]$ $\text{int}\left[\log_2\left(\frac{1}{1-D}\left(\frac{V_{ref}}{D \cdot \Delta V_q} + 1 \right) \right) \right]$
Flyback M(D)=nD/(1-D)	$\text{int}\left[\log_2\left(\frac{1}{1-D}\left(\frac{V_{ref}}{DV_{\max_{a/d}}} \cdot 2^{n_{a/d}} + 1 \right) \right) \right]$ $\text{int}\left[\log_2\left(\frac{1}{1-D}\left(\frac{V_{ref}}{D \cdot \Delta V_q} + 1 \right) \right) \right]$
Forward M(D)=nD	$\text{int}\left[n_{a/d} + \log_2\left(\frac{V_{ref}}{V_{\max_{a/d}} \cdot D} \right) \right]$ $\text{int}\left[\log_2\left(\frac{V_{ref}}{D \cdot \Delta V_q} \right) \right]$
Watkins-Johnson M(D)=(2D-1)/D	$\text{int}\left[\log_2\left(\frac{1}{D}\left(\frac{V_{\max_{a/d}}}{V_{ref}} \cdot \frac{2^{n_{a/d}}}{2D-1} - 1 \right) \right) \right]$ $\text{int}\left[\log_2\left(\frac{1}{D}\left(\frac{V_{ref}}{(2D-1) \cdot \Delta V_q} - 1 \right) \right) \right]$

Fig. 2(b) shows the experimental waveforms under the same conditions as in Fig. 2(a), except that the DPWM resolution is increased to 8 bits, which is, according to Table I the minimum required DPWM resolution. It can be observed that the limit cycle oscillation is removed.

Design of a high-frequency high-resolution digital pulse width modulator can be a significant problem. Most of today's designs found in DSP chips intended for motor-drive applications or in general-purpose micro-controllers are based on a simple counter approach that requires a high clock frequency of 2^{npwm} f_s, where f_s is the switching frequency. A new DPWM design based on a combination of counter and delay-line approaches has been described in [5]. This approach enables high resolution of 8-bit or more at switching frequencies up to the MHz range. The use of the DPWM chip in our experimental prototype is described in Section IV.

III. DIGITAL REGULATOR DESIGN APPROACHES

There are two basic approaches for digital controller design based on the conventional control theory: digital redesign and direct digital design. Based on comparisons of load transient responses, as well as achievable phase margin and bandwidth in power converter applications, direct digital design has advantages [6,7]. On the other hand, digital redesign enables use of some of the well-known controller design methods previously developed for continuous-time analog implementation.

For the conventional digital controller design, or for applications of any of the methods offered by modern control theory, it is necessary to develop a discrete-time model of the converter (i.e. the plant). One approach is to take into account the switching action in the converter and treat the converter as a sampled-data system that leads naturally to a discrete-time model. Another, simpler approach is to start with a well-known continuous-time, averaged model of the converter and transform the model to a discrete-time equivalent using one of the well known transformation techniques [3].

Selections of the design and transformation method can be based on the system dynamics and constrains caused by limited resources available for implementation.

For the converter configurations where the low-frequency dynamics can be described with a first-order model (such as for converters in discontinuous conduction mode, DCM), a method with good transformation of integral properties can be used (Bilinear transform, Euler or Pole–Zero matching). These methods are also convenient for the case when the digital redesign is used and when a simple PI controller is adequate.

For systems described by second-order dynamics and possibly RHP zeros [8] (such as converters in continuous conduction mode, CCM), methods that provide good transformation of integral and derivative properties (such as Pole-Zero Matching or Euler) give more accurate discrete-time equivalents of the continuous-time model. These methods also give a better transformation of controller properties if a digital redesign method is applied to a PID controller.

IV. DESIGN EXAMPLE

Design of a digital controller for a high-frequency buck converter is described in this section. The example converter is designed to generate the output voltage regulated at 1.8V (with 2% allowed variation) at the output power of 5W, from an input voltage of 4V to 6V.

The test bed used to validate various design approaches is shown in Fig.3. The setup consists of an Analog Devices ADMC-401 DSP development board, the 1MHz, 8-bit DPWM chip [5], and the buck converter power stage.

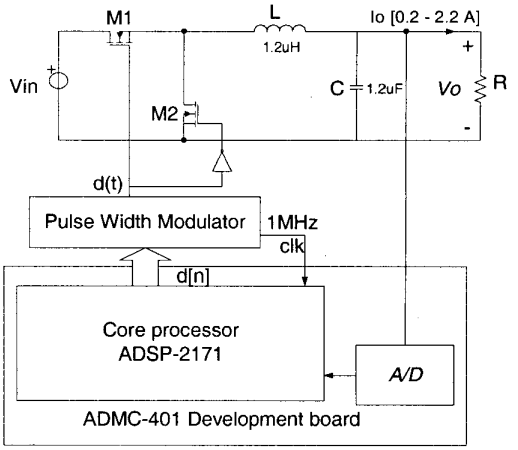

Fig.3. System used for implementation and experimental test of various control approaches

ADMC-401 is a 26 MIPS, 16-bit fixed-point digital signal processor intended for motor control applications. It has a range of peripherals including eight A/D converters, and enables experiments with change of resolution, and with various control algorithms. It should be noted that the built-in PWM units on the ADMC-401 would offer only 2 bits of resolution at the switching frequency of 1MHz, which is why we had to use the external DPWM chip described in [5].

The test bed of Fig.3 has been used to validate a design targeted for a low-cost, stand-alone ASIC.

Based on the criteria presented in Section I, it was found that six-bit resolution of the A/D converter, operating at Vref equal to 90% of Vmax = 2V meets the 2% allowed output voltage variation. From the expressions given in Table I, using the worst case point (maximum value of the input voltage) it was found that the minimum number of bits for the DPWM is eight.

The controller was designed using the direct digital design approach. The system model is shown in Fig 4.

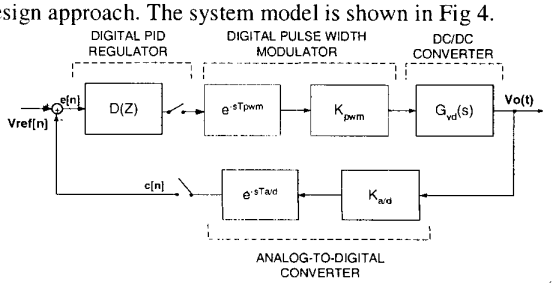

Fig.4. Block diagram of the digital control system

The closed-loop reference-to-output discrete-time transfer function C(z) of this system is:

$$C(z) = \frac{D(z) \cdot Z\{K_{pwm}(s) \cdot Gvd(s)\}}{1 + D(z) \cdot Z\{K_{pwm}(s) \cdot Gvd(s) \cdot K_{a/d}(s)\}} \quad (7)$$

where Gvd(s) is the control-to-output transfer function of the buck converter operating in CCM:

$$G_{vd}(s) = \frac{G_{do}}{1 + \frac{s}{Q\omega_0} + \frac{s^2}{\omega_0^2}} \quad (8)$$

For the selected converter components and the range of operating points, it was found that: Gdo varies from 4V to 6V, the corner frequency (f_0) is 132.7kHz, while the load variation causes the Q factor to vary from 2 to 20.

The transfer function of the DPWM is:

$$K_{pwm}(s) = K_{pwm} \cdot e^{-sTpwm_s}, \quad K_{pwm} = \frac{1}{2^{n_{pwm}} - 1} \quad (9)$$

In this case, K_{pwm} is 1/255 and Tpwm is the delay between the time the DPWM input is updated and the time the switch duty ratio changes.

The transfer function of the A/D is:

$$K_{a/d}(s) = \frac{K_{a/d}}{1 + \frac{s}{\omega_{lp}}} e^{-sT_{a/d}}, \quad K_{a/d} = \frac{1 - 2^{-n_{a/d}}}{V_{\max_{a/d}}} \quad (10)$$

where Ta/d is the delay caused by the conversion time, and the gain of the A/D converter (Ka/d) is 0.498. The pole at f_{LP} =57kHz in the converter characteristic is caused by a low-pass filter which is included on the ADMC-401 board.

The discrete-time transfer function H(z) of the analog plant is:

$$H(z) = Z\{K_{pwm}(s) \cdot Gvd(s) \cdot K_{a/d}(s)\} \quad (11)$$

In this case, the analog plant consists of the switching converter model, the pulse width modulator, and the analog-to-digital converter. The pole-zero matched transformation method was applied to obtain H(z).

The method is simple to apply and the discrete-time model has been shown to reproduce the plant transient responses with good accuracy. The second criterion for the selection of this method is its relatively low sensitivity to coefficient variations. For the plant in (11), the pole-zero matched transformation method is applied as follows [3]:

1. If the continuous time plant H(s) has a continuous plant pole at $s=-\xi_p+j\omega_p$, then the discrete equivalent H(z) has a pole at $z_p=e^{(-\xi_p+j\omega_p)Ts}$, where T_s is the sampling frequency.
2. If H(s) has a zero at $s=-\xi_z+j\omega_z$ then H(z) has a zero at $z=e^{(-\xi_z+j\omega_z)Ts}$.
3. All zeroes at $s=\infty$ are mapped to the point z=-1.
4. A unity delay is represented with z^{-1}.
5. The gain is selected to match the gain of H(s); in most of the cases $H(s)_{s=0}=H(z)_{z=1}$.

Using this method, the pole of H(s) caused by low-pass filter was mapped to 0.669, zero at $s=\infty$ was mapped to z=-1 while the delay was represented according to the rule 4. Poles of the converter and the gain are not constant values and their position in the z-plane depends on the operating point. For the two extreme operating points (maximum input voltage/minimum load, and minimum input voltage/maximum load), the plant transfer function is given by (12) and (13), respectively:

$$H(s) = \frac{11.76e^{-3}}{\left(1 + \frac{s}{358e^3}\right)\left(1 + \frac{s}{7.76e^6} + \frac{s^2}{150.5e^9}\right)} \cdot e^{-sT_s} \quad (12)$$

$$H(s) = \frac{7.846e^{-3}}{\left(1 + \frac{s}{358e^3}\right)\left(1 + \frac{s}{7.76e^6} + \frac{s^2}{150.5e^9}\right)} \cdot e^{-sT_s} \quad (13)$$

For the maximum input voltage and the minimum output load current, the discrete-time equivalent is:

$$H(z) = \frac{1.141 \cdot 10^{-3} \cdot (z+1)}{z \cdot (z - 0.669)(z^2 - 1.331z + 0.9793)} \quad (14)$$

When the load is the heaviest and the input voltage has the minimum value, the discrete-time equivalent becomes:

$$H(z) = \frac{0.761 \cdot 10^{-3} \cdot (z+1)}{z \cdot (z - 0.669)(z^2 - 1.22z + 0.8119)} \quad (15)$$

To achieve a controller suitable for implementation, it was decided to limit the control law to the second order equation. Controller coefficients are determined based on the poles-zeros cancellation approach: the controller zeroes are selected to (approximately) cancel the poles of the discrete transfer function H(z). The coefficients obtained for the pole-zero cancellation at the two extreme operating points are different. As a compromise, the final coefficients of the digital controller are set between the values that correspond to the two extreme cases. Finally, the gain of the controller is found using the root locus method (with the help of the MATLAB rltool [9]). The objective was to place the closed-loop system poles inside the cross section of constant-damping and decrement factor areas inside the z-plane, for all operating points [10]. The decrement factor area determines the minimum response speed, while the constant damping area limits the maximum overshoot in the step transient response. The maximum overshoot was set to 20%, while the minimum response speed was set to 50µs.

The obtained discrete-time control law is given by:

$$d[n] = d[n-1] + 52\left(e[n] - 1.3e[n-1] + 0.8119e[n-2]\right) \quad (16)$$

where d[n] and d[n-1] are the new and one-cycle before values of the duty ratio, respectively, while e[n], e[n-1] and e[n-2] are the new, one-cycle before and two-cycles before values of the error signal.

A. Resolution of the computational unit

Based on the DPWM resolution and the form of the control law, the hardware/software requirements for the computational unit can be found. Figure 5 shows a block diagram of the computational unit and the minimum number of bits needed for various blocks of the computational unit.

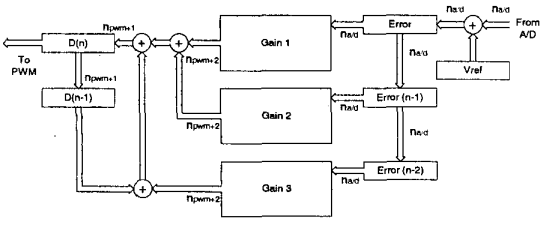

Fig.5. Block diagram of computational unit

Limited resolution of the fixed-point computational unit does not allow exact implementation of the control law. The closest approximation of the designed controller is given by:

$$d[n] = d[n-1] + 49.2\left(e[n] - 1.3e[n-1] + 0.81e[n-2]\right) \quad (17)$$

B. Processing time constrains and controller implementation

The complete real-time controller implementation is interrupt driven. The DPWM chip loads the new value of the duty ratio and at the same time generates an interrupt at the beginning of each switching cycle. Given the switching frequency of 1MHz, the interrupts are 1μs apart. The A/D converter on the ADMC-401 board operates asynchronously, and gives the new value each 250ns. Taking into account the interrupt response time, the time available for the processor to compute the new value of the duty ratio is about 400ns, or 12 instructions.

To reduce the number of multiplications, the control law described by (17) is rewritten in the following form:

$$d[n] = d[n-1] + 64\left(0.769e[n] - e[n-1] + 0.63e[n-2]\right) \quad (18)$$

The multiplication by 64 can be implemented using a shifting operation.

A flow chart of the computation is shown in Fig.6.

After the DPWM interrupt is recognised, the latest sampled value of the output signal (new sample value) is subtracted from the reference and the new value of the error signal is formed. The error is multiplied by the corresponding coefficient (given in Eq. (18)) and that product is added to the value c[n], which was calculated during the previous switching cycle. After the operations of shifting by 6 (equivalent to multiplying by 64) and addition of the value d[n-1] of duty ratio are completed, the new value of the duty ratio is available.

Preprocessing is done to reduce the time needed to perform the computations from the moment when the sample of the output value is taken to the calculation of the new value of the duty ratio. The preprocessing includes updating d[n-1] and calculation of the new value for c[n]. Ones the preprocessing operation is completed, the processor steps out from the DPWM interrupt subroutine and waits until the new interrupt appears. The complete computational process is completed in nine instructions or 297ns.

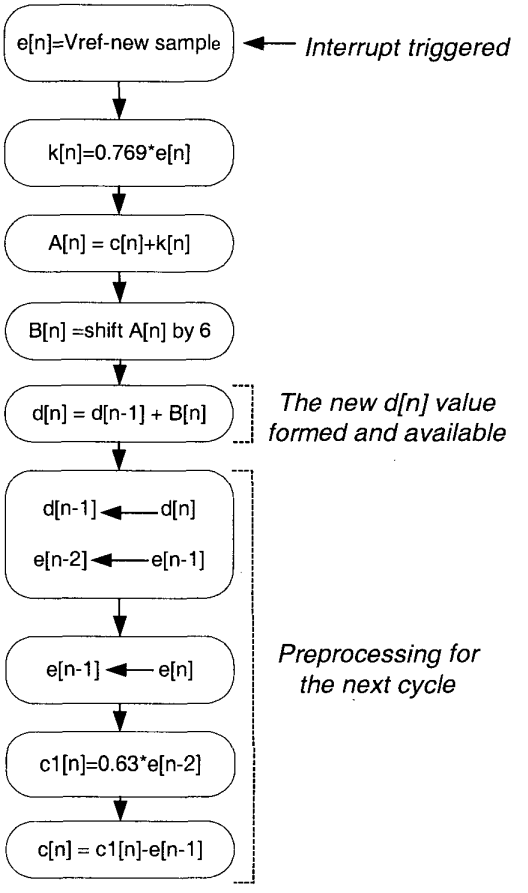

Fig.6. Flow chart of the computations

V. EXPERIMENTAL RESULTS

Figures 7(a) and (b) show load transient responses obtained in the experimental prototype for the load current changes from 2.2A to 0.2A and from 0.2A to 2.2A.

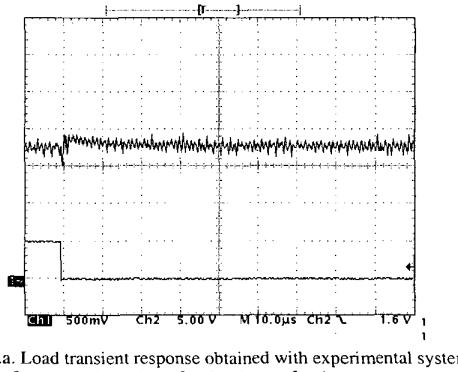

Fig.7.a. Load transient response obtained with experimental system, Change of output voltage (top) for the change for the output current from 2.2A to 0.2A

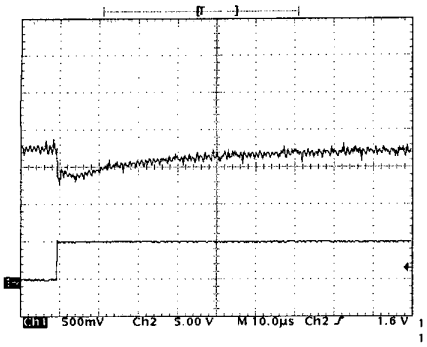

Fig.7.b. Load transient response obtained with experimental system, Change of output voltage (top) for the change for the output current from 0.2A to 2.2A

It can be observed that the load transients take about 30µs to complete.

VI. CONCLUSIONS

This paper describes complete design and implementation of a digital controller for a high-frequency switching power supply. Guidelines for the minimum required resolution of the analog-to-digital converter, the pulse-width modulator, and the fixed-point computational unit are derived. A design example based on a buck converter operating at the switching frequency of 1MHz is presented. The controller design is based on direct digital design approach and standard root-locus techniques. Experimental results are shown to validate the design approach and the allocation of resources in the implementation.

VII. REFERENCES

[1] A.M. Wu, J. Xiao, D. Markovic, S.R. Sanders "Digital PWM Control: Application in Voltage Regulator Models," *IEEE Power Electronics Specialists Conference,* 1997 Record, pp. 77-83.

[2] A. Prodic and D. Maksimovic, "Digital PWM Controller and Current Estimator for a Low-Power Switching Converter," *IEEE Computers in Power Electronics 2000,* pp. 123-128.

[3] G.F. Franklin and J.D. Powell, *Digital Control of Dynamic Systems,* Addison-Wesley Publishing Company, Inc: 1998, p. 440 - 445, 200 –204.

[4] Z. Lu, Z.Qian, Y. Zeng, "Reduction of Digital PWM Limit Ring with Novel Control Algorithm," *IEEE Applied Power Electronics Conference 2001,* vol. 1, 1995, pp. 521-534.

[5] B. Patella, "Implementation of a High Frequency, Low-Power Digital Pulse Width Modulation Controller Chip," M.S. Thesis, University of Colorado at Boulder, 2000.

[6] T.W. Martin and S.S. Ang, "Digital Control of Switching Converters," *IEEE Symposium on Industrial Electronics,* vol. 2, 1995, pp. 480-484.

[7] Y. Duan, H. Jin, "Digital Controller Design for Switch Mode Power Converters," *IEEE Applied Power Electronics Conference,* 1999, Vol.2, pp. 480-484.

[8] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics,* Second Edition, Kluwer Academic Publishers, 2000, pp. 187-264, 409-434.

[9] The Math Works, Inc., Natick, MA. *Control System Toolbox: User's Guide, version 4,* 1998.

[10] Julius T. Tou, *Digital and Sampled Data Control Systems,* McGraw-Hill, pp.491-495