Design and Implementation of a Field Programmable Analogue Array.

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Abstract.

A **F**ield **P**rogrammable **A**nalogue **A**rray (FPAA) is presented based on switched capacitor technology. The chip allows true array programming of undedicated analogue cells. There is provision for internal signal-conditional switching as part of the normal function of the array.

With the presented chip it is possible to implement a very wide range of analogue signal processing functions such as data conversion, linear signal processing and non-linear functions. These functional configurations can be reconfigured and parameterised on the fly during concurrent signal processing.

Very rapid prototyping of switched capacitor circuits is facilitated. The field programmable nature of the chip allows several markets/customers to be targeted simultaneously with obvious benefits in terms of both volume of sales and reduced time to market.

Introduction.

Increasing die sizes are driving the creation of whole systems on a single chip. In parallel with this process, the emergence of the mixed-signal system is allowing a single chip system to interface directly to the real world around it. Reconfigurable analogue circuits allow a small functional block of analogue circuitry to perform many diverse functions, such architectures are well suited to the periphery of a single chip mixed-mode system.

A number of field programmable analogue designs have recently emerged, such as the EPAC device from IMP [1]. The EPAC device contains fixed functionality blocks such as low-pass filters and analogue to digital converters (ADCs) and allows parameterisation of the blocks for cut-off frequency, offset etc.

Toronto University have reported the MADAR array [2], the analogue section of which is based on transconductors and programmable resistors and capacitors. The interconnect between these elements is a configurable array of switches which allows some degree of flexibility.

This paper reports on a FPAA (called DPAD2) which can be programmed for both functionality and be parameterised within that functionality while signal processing takes place. DPAD2 is a true array of identical undedicated analogue cells, it is possible to programme both the functionality of each cell and the interconnect between the cells. As a result a large number of diverse architectures may be implemented.

Many base architectures are possible for an analogue array, such as switched current [3], transconductor-capacitor [4] and MOSFET-capacitor [5], but switched capacitor (SC) [6] technology was chosen for DPAD2 for a number of reasons. There is a large and well established base of design techniques, in particular the use of parasitic insensitive architectures allows arbitrary routing paths within the array with minimal loss of signal integrity. Good matching of proximal capacitors allows precise analogue functions to be generated without trimming or calibration, both of which are expensive and cumbersome. Digital control of FPAA switched capacitor circuits is easily possible via switch control to facilitate a mixed signal environment of digitised analogue functions. Hierarchic design is facilitated by SC circuits due to the small back-coupling of signals from an analogue cell to the previous block, this is very important for system level design.

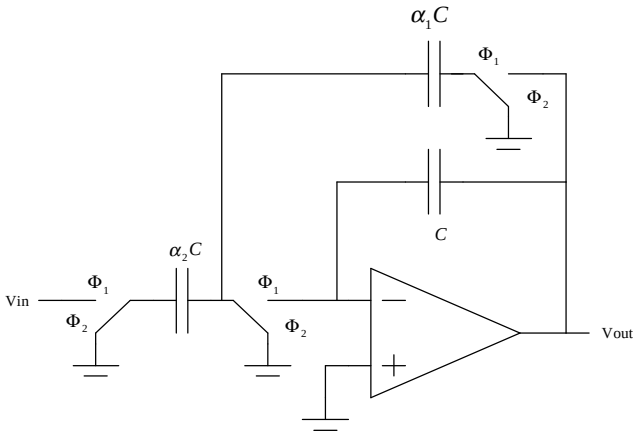

Figure 1. A lossy switched capacitor integrator.

Figure 1 shows a simple SC circuit which performs a lossy integrator function. The transfer function of this circuit maybe be written as,

$$\frac{V_{OUT}}{V_{IN}}(z) = \frac{\frac{\alpha_2}{1+\alpha_1}}{1-\frac{1}{1+\alpha_1}z^{-1}}$$

A major strength of switched capacitor circuits can be seen from this equation, that the function only depends on the ratio of capacitors and not on their absolute values. Capacitor ratios can be controlled to within 0.1% or so on a modern IC fabrication process which gives an accurate gain and pole frequency position. The architecture of Figure 1 is termed parasitic insensitive because parasitic capacitors from each node to ground do not affect the transfer function to first order. Essentially this is because either,

a. a node is driven by a strongly buffered voltage, such as the input and output, so the charge on the parasitic capacitors has little effect.
b. a node remains at a fixed voltage (such as the inverting input of the operational amplifier) and the parasitic capacitors hold a fixed charge as a result.

Parasitic insensitivity is a very valuable feature in an analogue array since the nodes between components may follow different paths depending on the selected architecture and resources.

In defining a programmable analogue architecture it is necessary to consider the implementation in great detail. Unlike some FPGAs, a very fine grained architecture is not desirable because the numerous switches will cause significant signal degradation. However, too coarse an architecture will mean flexibility, and therefore functionality, would be severely limited. A happy compromise is an essential part of a successful FPAA.

The FPAA described here is technologically compatible with PMeL's existing FPGA (available as the Motorola MPA1000 family) to allow the creation of a field programmable mixed-mode array (FPMA) as the ultimate goal of this work. This is an important point, since it is possible to create mixed-mode functions that are not possible in either the digital or analogue domain alone. In addition, the digital section of a FPMA is readily utilised for control of the analogue SC section.

Resource requirements.

Determining the resources necessary for the DPAD2 architecture is a very sensitive process. If major features were missing the functionality would be severely restricted. On the other hand, incorporation of a number of features that were very infrequently used would present a significant overhead leading to unnecessary cost. An example of such a decision is the maximum capacitance load that an operational amplifier might be required to drive with adequate stability. In theory it would be nice to be able to drive all the on chip capacitors from one operational amplifier but in reality this is never required. To drive such a load with a unity gain bandwidth of 10MHz and a 63 degree phase margin would require a DC current of 1.88 amps per amplifier. The resultant total current is in excess of 37.6 amps for the whole array. In this case the maximum safe load was chosen to be 150pF - representing five full capacitor arrays. It was felt that arc welding would probably not be a required function.

It is difficult to provide a hard rule set for resource allocation decisions, other than the intuition of a number of experienced designers. It is expected that as customer feedback becomes available these decisions will be more accurately tailored to one or more applications. In order to initially decide what resources are necessary for the DPAD2 architecture, a number of common switched capacitor cells were analysed in terms of the number of input signal paths per operational amplifier and the switch connectivity and functionality within these branches. A field programmable architecture means that the values of capacitors must be discrete and sufficient bits must be provided, this was also an analysis criterion. In addition to the usual switched capacitor branch functions, some extra flexibility is required for a number of speciality functions such as charge sharing capacitors to produce large time constants [7]. A representative sample of the circuits analysed are detailed in appendix one, these are representative of the major SC functions although by no means do they constitute an exhaustive list.

Array architecture implementation.

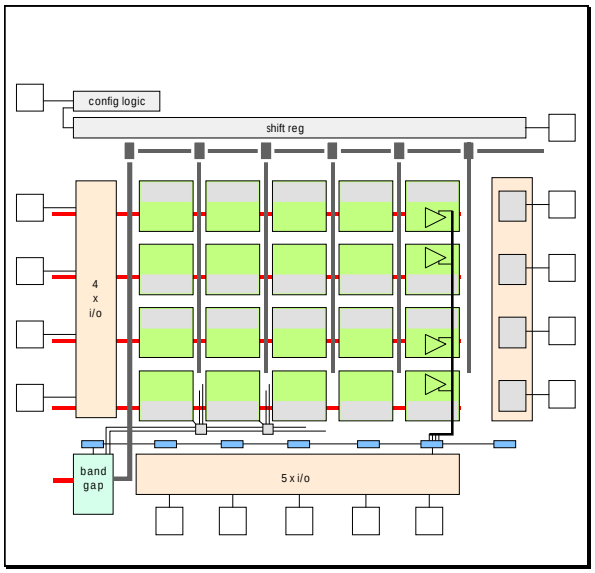

Figure 2. DPAD2 layout overview.

Figure 2 shows a block diagram of the DPAD2 layout architecture and the main functional blocks within it. The principle feature is an array of 4 by 5 programmable analogue cells. To support the analogue core cells there is configuration logic around the upper periphery of the chip which controls connectivity within the array. Some RAM is local to each cell to control the function of the cell. Two busses are provided at the array level, the data transfer bus which carries data for configuration of cells and the transfer control bus which is used for latching of data from the data transfer bus. A bandgap voltage reference is provided on the DPAD2 chip, this has an 8-bit programmable output voltage that is available for each analogue cell. Buffer cells are provided around the periphery of the chip, these may be configured into unity gain buffers or into smoothing/anti-aliasing filters with external components.

Configuration of the full array is done by loading the necessary bits sequentially into a 554 bit wide shift register than runs the full width of the array. Once the shift register is fully loaded, a row of the array is selected and the data is loaded in parallel into that row. The shift register is then loaded with the next data set.

In total there are 10 load operations for a full configuration. Eight are utilised for the core (two per row), one is used for the interface MUX which controls cell to cell connections within the array. The final RAM row is used for programming the internal bandgap reference and I/O functionality. During configuration the internal cells are set to a power-down mode to protect the array against illegal high current modes.

Connections are arranged between the analogue cells on both a local and global level. The local and global interconnect arrangements are shown schematically in Figure 3. Local interconnect output tracks are permanently excited by the operational amplifier that drives them, selection of the appropriate signal for an cell input is performed at the input of that cell. Each input branch of a cell is dedicated to three of the 9 possible inputs as detailed in Figure 3 with the three input branches designated B, C and D. Branch A is reserved for connecting an input of a cell to its own output. It is worth noting that there exists a slight bias in favour of connections that run from left to right. This is implemented because the majority of signal flows are drawn schematically passing in this direction.

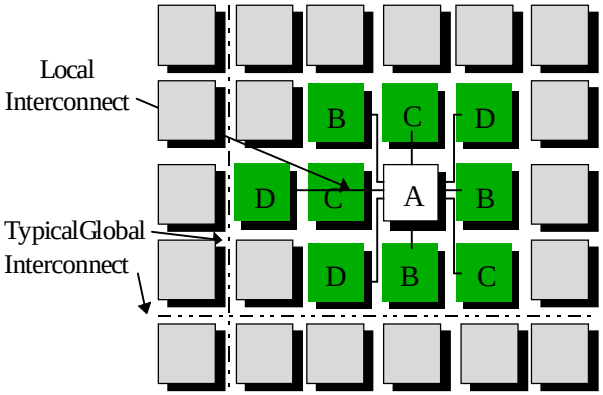

Figure 3. Local and global interconnect pattern.

In the event that local interconnect resource proves inadequate for the required connections there exists a layer of global interconnect. This comprises 2 horizontal and 2 vertical tracks running between all analogue cells for the full length and width of the cell array. At each intersection of the horizontal and vertical interconnect an array of switches allows for cross connections. Local interconnect is the preferred connection medium because it has fewer switches than global interconnect and generally has shorter track lengths.

The broad aspects of this array are referred to in a PMeL patent [8].

Array based performance limitations.

The array nature of the DPAD2 means that the routing of the signals within the array can have an impact on the array performance. Although the recommended SC architectures are parasitic insensitive to first order, some second order effects are important.

1. Each switch connected to a capacitor introduces a small leakage path to the substrate whether the switch is open or closed. Reducing the number of parallel switches is an important point in planning the architecture at an array level.

2. Parasitic resistance of switches combines with various capacitances to form parasitic poles within the array interconnect. Care must be taken to make sure these poles are not present within the frequency regions of interest, they are poorly controlled and may lead to deviant transfer functions or instability in extreme cases.

3. Parasitic insensitive architectures are still sensitive to track to track capacitance. Care must be taken with track routing to avoid this problem occurring even though such capacitances are generally small.

Analogue cell implementation.

Each analogue cell has a patented architecture [9] which is depicted in Figure 4. The configuration data is held in RAM local to the cell and this is then decoded to determine the switching phases within the cell.

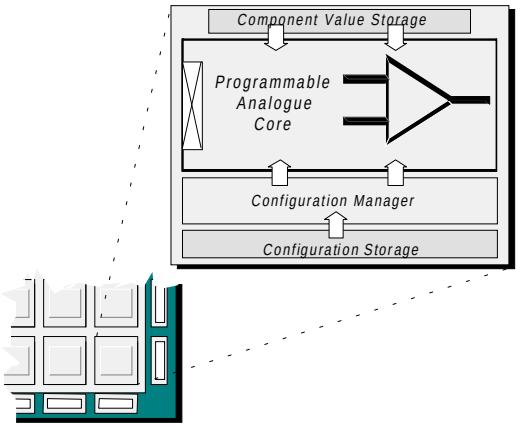

Figure 4. Programmable analogue cell.

There is an operational amplifier within each analogue cell which acts to provide a virtual earth for the switched capacitor functions, it also drives the output voltage of the cell. The operational amplifier has four input branches with individual phasing control. Four was found to be sufficiently flexible while not being excessively so, by consideration of the example SC circuits of appendix one.

All capacitors are eight bit programmable and are local to the analogue cell which uses them. It is possible to share capacitors from one block to the next using local and global interconnect if necessary. Capacitors have their connectivity established by a number of switches which are implemented as complementary MOS pass transistors. The value of a capacitance is initially set at configuration time but may also be dynamically changed during signal processing. Switches are referred to as static or dynamic, the former having their state determined when the chip

is initially configured and the latter toggle between one state and the other, as part of the normal switched capacitor function.

Some example configurations of the more complex single-cell circuit functions are shown in Figure 5.

In some cases it is necessary to provide a switch which is dynamic but has its toggle phase determined by the value of an internal signal. One such application is in the full wave rectifier function which is depicted in Figure 6. In this function the gain stage is switched between inverting and non-inverting gain by appropriate input switch phasing. The output signal is thus an absolute value function of the input. This control is obtained by using a comparator to determine the input signal polarity and the dynamic phase switch unit to control the input switch phasing.

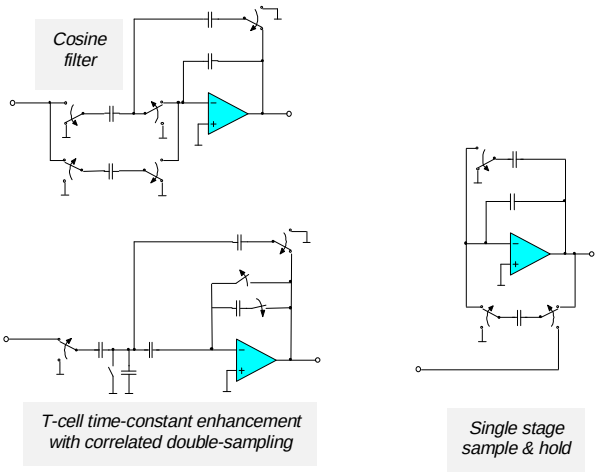

Figure 5. Single-cell example configurations.

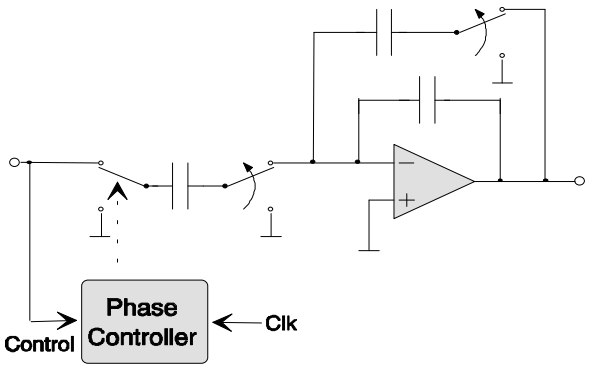

Figure 6. Full wave rectifier.

Dynamic switch control.

Control of the dynamic switches within the analogue cell is accomplished by the use of a patented switch function generator [9], depicted schematically in Figure 7. Each dynamic switch group has one of these controllers dedicated to it. Fundamentally, the switch controller consists of two sections; the first acts on the two phase non-overlapping input clock signals to produce a number of functions and the second section selects which switch(s) in the switch group the function is applied to.

Four primary functions generated from the clock signals are, toggling on either the odd or even phase, permanently open or permanently closed. A summary of the functions is provided in Table 1 where select clock1, select clock2 and select hi are function select inputs and function-a and function-b are the two output functions generated from clock1 and clock2.

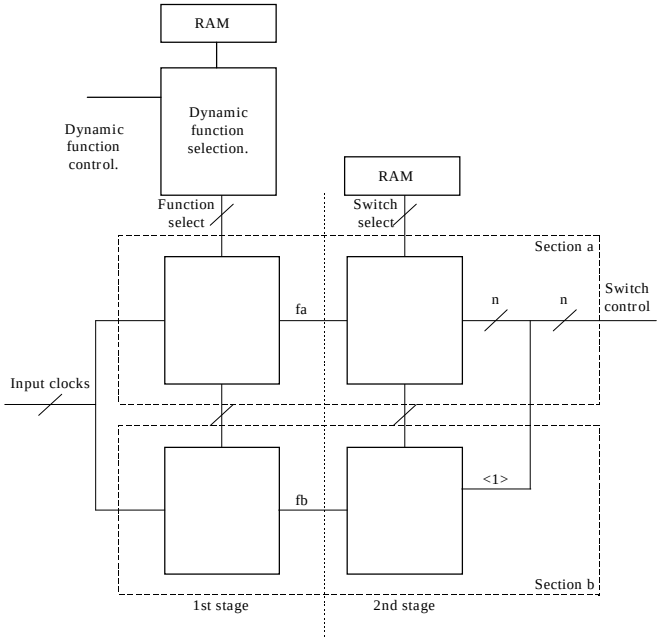

Figure 7. Switch function generator.

select clock1	*select clock2*	*select high*	*function-a*	*function-b*
0	0	1	1	1
0	0	0	0	1
0	1	0	clk2	clk1
1	0	0	clk1	clk2

Table 1. Switch function truth table.

PCM CODEC design.

To give some idea of a larger function implementation on the DPAD2 array a screen shot of a PCM CODEC is shown in Figure 9. The large pale blocks at the top of the array are filter blocks that have been implemented as macro cells. Use of macro-blocks is a powerful feature of the software, allowing the creation of reusable functions within a library and abstracting the user from many of the lower decision levels.

Three cells are shown exploded at the centre bottom of the array, these implement a u-law DAC as one of the sub-circuits within the CODEC. Several uncommitted analogue cells can be seen within the array and several I/O ports are also shown unused.

Results.

The designed performance of DPAD2 is summarised below in Table 2. At the time of writing the DPAD2 chip is still in fabrication but results are available from a test chip that was done as a forerunner of DPAD2. This comprised one programmable analogue cell and some basic programming circuitry. The device was configured as a gain cell and three gains were programmed as it sampled an input waveform. Gains of -1, -2 and -3 were implemented, the input waveform and the resulting output waveforms are shown in Figure 8.

	Evaluation DPAD
Power supply	*0-5v*
No. of analogue cells	*20*
Analogue i/o ports	*13*
Local interconnect connections per cell	*9 cells*
Total number of dynamically programmable / controllable resources	*6 per cell*
Max. no. of dynamically programmable resources per chip.	*8*
Capacitor programming	*8 bits*
Capacitor unit value	*0.12pF*
Voltage reference programming	*8 bits*
Max. clock frequency	*1MHz*
Input signal range	*0-5v*
THD per cell	*0.4%*
Typ. supply current per cell	*1.6mA*
Analogue array configuration time	10ms

Table 2. DPAD2 designed performance.

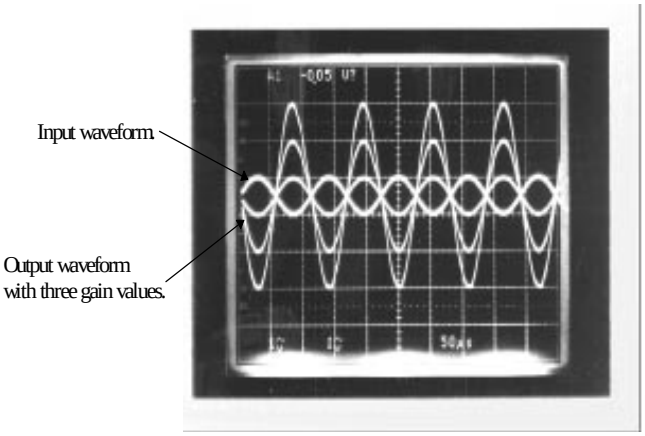

Figure 8. Variable gain stage results.

Conclusions.

A field programmable analogue array (FPAA) has been described which allows the user to easily define both the functionality and parameters of a large number of switched capacitor circuits. Experienced designers may work at component level if they desire while system designers are supported by a library of macro cells that are easily parameterised for a particular application using custom software. The DPAD2 chip may be configured and yield results extremely rapidly which is of benefit in a rapid prototype or a teaching environment.

Careful consideration of the resources necessary for a number of SC circuits has lead to an array that is both very flexible and yet loses little functionality from having a fixed programmable architecture.

Appendix one.

The majority of these circuits are to be found in [6].

* Sample & Hold
* Unity gain buffer
* Unity gain buffer (offset compensated)
* Integrator
* Low Q Cascade Filters
* High Q Cascade Filters
* Ladder filters
* Full wave rectifier
* Relaxation oscillator
* Sine wave oscillator
* Square & Triangle wave generator
* Schmitt Trigger
* u-LAW DAC
* N-path filter
* Large time constant circuits.

References.

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(3) C. Toumazou, J.B. Hughes & N.C. Battersby. ``Switched Currents an analogue technique for digital technology". IEE.

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(7) W. Sansen & P. Van Peteghem, "An area-efficient approach to the design of very-large time constants in switched-capacitor integrators", IEEE Journal of solid-state circuits, Vol. 19, No. 5, October 1984.

(8) UK Patent Application GB 2 246 666. 27/03/1991. Integrated circuit for analog system. US Patent 5,196,740. Mar. 23, 1993. Integrated circuit for analogue system.

(9) UK Patent Application GB 2 275 144 A. 17/08/1994. Programmable switched capacitor circuit.

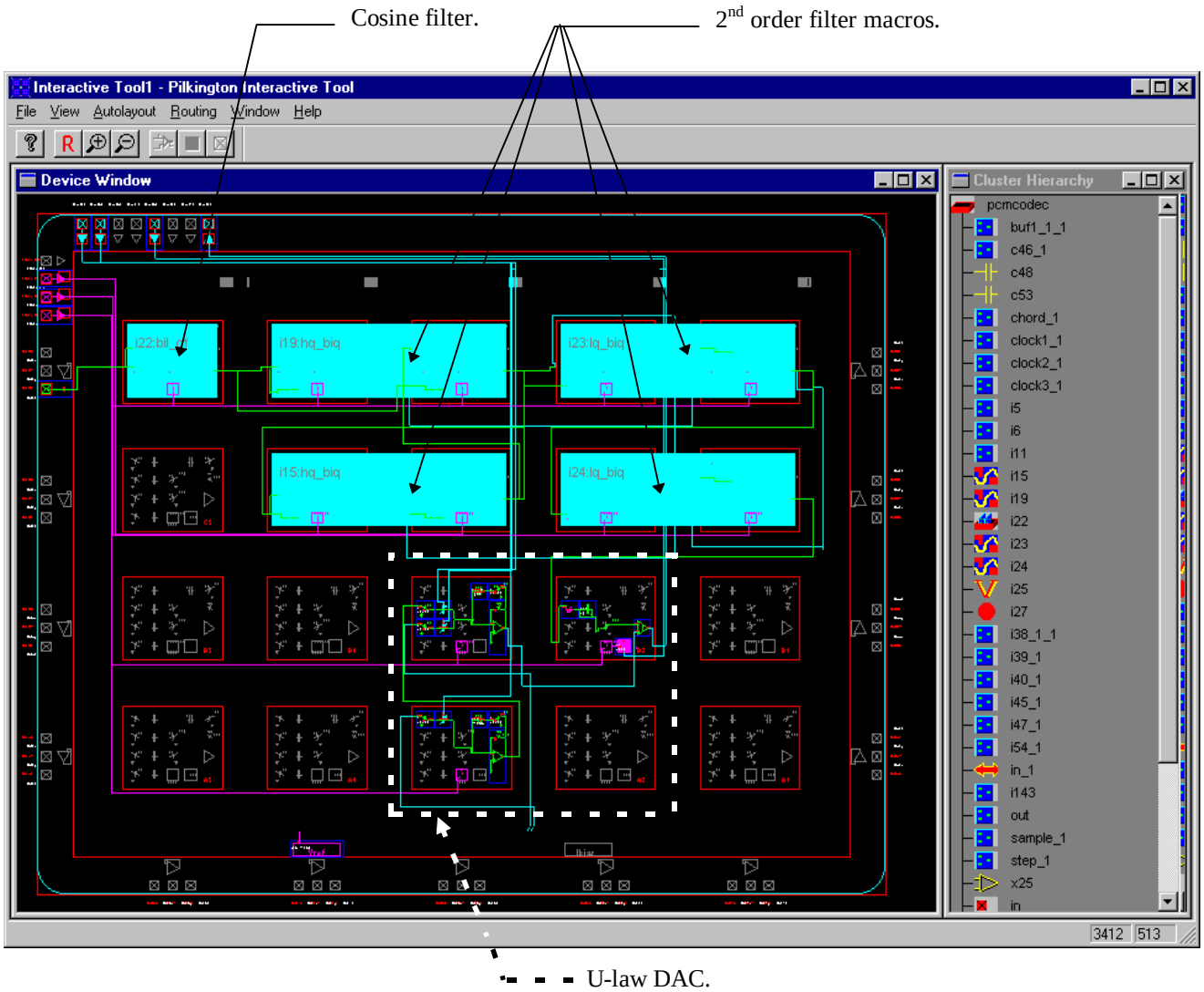

Figure 9. CODEC configured onto DPAD2.