Design and Implementation of a FPGA and DSP Based MIMO Radar Imaging System

Wei WANG[1], Dong LIANG[1], Zhihua WANG[2], Haiyang YU[1], Qi LIU[1]

[1]College of Automation, Harbin Engineering University, Harbin, 150001, China
[2]Beijing Huahang Radio Measurement Institute, Beijing, 100013, China

wangwei407@hrbeu.edu.cn, liangd@hrbeu.edu.cn, sdzjcn@126.com, bigyuhy@126.com, lq_skyven@126.com

Abstract. *The work presented in this paper is aimed at the implementation of a real-time multiple-input multiple-output (MIMO) imaging radar used for area surveillance. In this radar, the equivalent virtual array method and time-division technique are applied to make 16 virtual elements synthesized from the MIMO antenna array. The chirp signal generater is based on a combination of direct digital synthesizer (DDS) and phase locked loop (PLL). A signal conditioning circuit is used to deal with the coupling effect within the array. The signal processing platform is based on an efficient field programmable gates array (FPGA) and digital signal processor (DSP) pipeline where a robust beamforming imaging algorithm is running on. The radar system was evaluated through a real field experiment. Imaging capability and real-time performance shown in the results demonstrate the practical feasibility of the implementation.*

Keywords

Radar imaging, MIMO radar, real-time system, FPGA, DSP.

1. Introduction

Recently, MIMO radar [1], [2] has drawn considerable attention. Benefit from the characteristic that MIMO radar transmits orthogonal waveforms and receives the reflected signals in similar ways, an equivalent virtual array [3] is synthesized to expand the array aperture and many potential advantages (e.g., higher angular resolution, better identifiability, etc.) [4] can be obtained. MIMO radar imaging technology is the combination of equivalent virtual array and imaging process in wideband radar. As a kind of signal form employed in wideband radar, frequency modulated continuous wave (FMCW) signal contributes to a fine capability of ranging and low power consumption [5]. Since the orthogonality between the different transmit signals can be realized through the time division multiple access (TDMA) method [6], switching the array channels to transmit FMCW signal at different time slots became a reliable and popular scheme for MIMO imaging radar [7]-[11].

Accompanied by the emergence of a large number of theoretical results in MIMO radar [12]-[14], the research of engineering application is also in progress. Some MIMO radar systems have been developed for radar system performance analysis and algorithm verification[7]-[11], [15]. In [7], a 77-Ghz FMCW MIMO radar is implemented for 2D target localization using an SiGe single-chip transceiver. In [8], a 2D-MUSIC algorithm for joint estimation of angular and range target locations is applied to the MIMO radar system. As well as imaging resolution and measurement accuracy, real-time performance is also a significant index for an imaging radar. In [9], a through-wall MIMO imaging radar system, which produces real-time imagery of targets at a frame rate of 0.5 Hz, is presented. The system controller and signal processing modules are implemented in LabView [16] running on a PC.

With the purpose to further accelerate the application process of MIMO radar, in this paper, an engineering prototype of MIMO imaging radar is implemented based on a single-board signal processing platform with FPGA and DSP processors . The proposed radar system provides a real-time imaging rate of 1.5625 Hz, featuring low cost and low power consumption.

In order to minimize the error sources from the radar transmitter, a frequency multiplication structure [17], [18] is used as a FMCW signal generator in the radar transceiver to avoid the appearance of image frequencies caused by mixing. Since the coupling effect adversely affects the performance of the imaging radar, a signal conditioning circuit, which consists of switched capacitor filters [19], is applied to inhibit the coupling components of intermediate-frequency (IF) signal. In this radar system, the target ranges are estimated with a discrete Fourier transform (DFT) analysis just like a conventional FMCW range radar, the angle information of the target is then figured out using a beamforming method. The whole signal processing for a continuous measurement takes place on an efficient data pipeline, which is implemented on the singal processing board. The actual performance of the radar system has been verified in the field experiment.

This paper is organized as follows. Section 2 introduces the basic theory of the imaging process. Section 3 describes the design and hardware implementation of the

MIMO radar. Section 4 expatiates the date flow path of the signal processing pipeline. Section 5 describes the field experiment and the corresponding imaging results. Section 6 draws the conclusions.

2. MIMO Imaging Principle

2.1 Antenna Array Architecture

The model is characterized in Fig. 1. A coherent MIMO antenna array is composed by a transmit (TX) linear array of 4 elements and a receive (RX) linear array of 4 elements. In order to reduce the coupling effect within the array, the TX array and RX array are placed in different planes with some vertical offset.
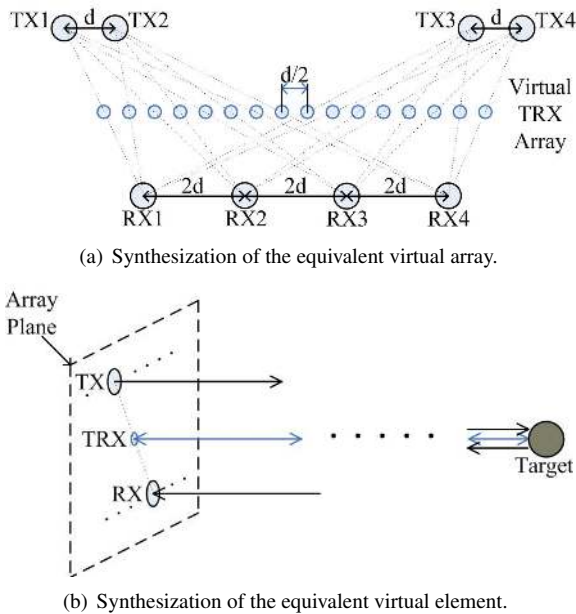

(a) Synthesization of the equivalent virtual array.

(b) Synthesization of the equivalent virtual element.

Fig. 1. MIMO array principle.

The direction of main radiation is perpendicular to the array plane. Referring to a basic TX-RX combination in Fig. 1(b) with the assumption that target is at large distance, it is clear that the TX and RX directions are approximate to be parallel and the TX and RX elements will be the same to the virtual transmit-receive (TRX) element which is placed in the middle of the TX-RX connection line. By extending to every TX-RX combination in the MIMO array, a virtual TRX array with 16 elements is synthesized, as shown in Fig. 1(a).

2.2 FMCW Signal Model

The FMCW signal transmitted by the TX array antenna can be modeled as

$$s(t) = V_T \cos(2\pi f_0 t + \pi \frac{B}{T} t^2 + \phi_0); \quad 0 \le t < T \quad (1)$$

where V_T is the amplitude, f_0 is the start frequency of chirp sweeping, B is the sweeping bandwidth, T is the sweeping duration, and ϕ_0 is the initial phase of the signal. Suppose that frequency of the signal is independent of the propagation path, after traveling a signal delay τ between the antenna and target, the echo signal can be expressed as

$$r(t) = As(t - \tau) \quad (2)$$

where A is the sum of propagation loss and antenna gains. The target echo signal in (2) is processed with a deramp technique, which includes mixing the echo signal with the TX signal (1), followed by a lowpass filtering. Then the IF signal is obtained as

$$u(t) = V \cos[2\pi \frac{B}{T} \tau t + 2\pi f_0 \tau (1 - \frac{\tau B}{2T f_0})] \quad (3)$$

where V is the amplitude of IF signal. Since $f_0 \gg B$ and $T \gg \tau$ in most cases in reality, (3) can be simplified to

$$u(t) = V \cos(2\pi \frac{B}{T} \tau t + 2\pi f_0 \tau). \quad (4)$$

The signal (4) is sampled with a sampling interval T_s for a sweeping duration, the discrete-time series is then generated as the raw data which can be expressed as

$$u(n) = V \cos(2\pi \frac{B}{T} \tau n T_s + 2\pi f_0 \tau); \quad n = 0, 1, 2, ..., N-1 \quad (5)$$

where N is the number of samples and is determined by

$$N = \frac{T}{T_s}. \quad (6)$$

In a conventional FMCW radar, the time τ is usually estimated through a DFT analysis of the raw data in (5). In the result of DFT analysis, a series cycle at the positive side of the abscissa axis can be expressed as

$$U(k) = \frac{1}{2} V e^{j[2\pi f_0 \tau - \frac{N-1}{N}\pi(k - B\tau)]} \frac{\sin[\pi(k - B\tau)]}{\sin[\frac{\pi}{N}(k - B\tau)]}; \quad (7)$$
$$k = 0, 1, 2, ..., N-1.$$

For a FMCW MIMO radar, the estimation of τ contains the measurement of target range and azimuth which can be executed through beamforming method with (7).

2.3 Beamforming Imaging Algorithm

In the virtual TRX array architecture shown in Fig. 2, a range reference point is set at the geometric center with the coordinate of zero.
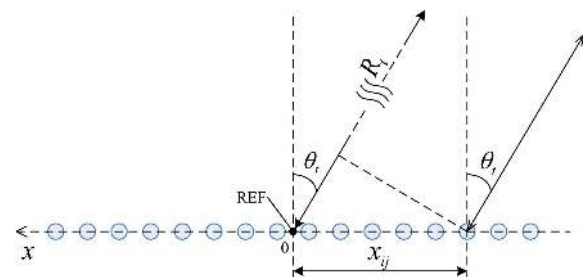

Fig. 2. Target range and azimuth measurement with the virtual array.

The virtual TRX element at x_{ij} is synthesized from the i-th TX element and the j-th RX element. The signal delay between this TRX element and a target from far field at range R_t and angle θ_t can be defined as

$$\tau_{ij} = \frac{2R_t}{c} + \frac{2x_{ij}\sin\theta_t}{c}. \tag{8}$$

Since the TRX element transmit and receive FMCW signal, the time delay τ in (7) should be substituted by (8). However, in the most cases where

$$R_t \gg |x_{ij}|_{max}, \tag{9}$$

there exists the approximately equivalent

$$\tau_{ij} \approx \frac{2R_t}{c}. \tag{10}$$

It should be noted that with the condition $f_0 \gg B$, the term of $2\pi f_0 \tau$ in (7) should not be affected by the approximation in (10) when performing the insertion. Therefore, the expression of the sequence in (7) is reconstructed as

$$U_{ij}(k) = \frac{1}{2}V_{ij}e^{j[2\pi f_0\frac{2x_{ij}\sin\theta_t}{c}+2\pi f_0\frac{2R_t}{c}-\frac{N-1}{N}\pi(k-\frac{2BR_t}{c})]}$$
$$\frac{\sin[\pi(k-\frac{2BR_t}{c})]}{\sin[\frac{\pi}{N}(k-\frac{2BR_t}{c})]}; \quad k = 0,1,2,...,N-1. \tag{11}$$

As can be seen, $U_{ij}(k)$ reaches its peak magnitude when k is nearest to $\frac{2BR_t}{c}$, which means that k can be the range index of the targets in measurement. Therefore, the range information can be retrieved from the series (11), which is so called range time intensity (RTI) data. By referring to the array structure in Fig. 1 and Fig. 2, the beamforming algorithm is applied to (11), the process can be modeled as

$$J(k,\theta) = \left|\frac{1}{16}\sum_{i=1}^{4}\sum_{j=1}^{4}U_{ij}(k)e^{-j(2\pi f_0\frac{2x_{ij}\sin\theta}{c})}\right|^2. \tag{12}$$

Since each k and θ represents a certain range and angle respectively, the process of (12) can be regarded as a searching of a certain location at (k,θ), where the echo signal power is expressed as $J(k,\theta)$. By performing (12) with the ergodic combination of k and θ in the whole imaging area, the image results are figured out.

3. Radar System Implementation

In this section, the hardware implementation of the MIMO imaging radar prototype is described. The block diagram of the radar system is shown in Fig. 3.

The core of this system is a FMCW radar device working at a frequency range from 2.48 GHz to 2.56 GHz. A photograph of the complete radar system is shown in Fig. 4. The antenna array design is based on the virtual array synthesis procedure in reference to Fig. 1. Four transmit antennas and four receive antennas are installed on an acrylic plate and are capable of working as a MIMO system at the S band.
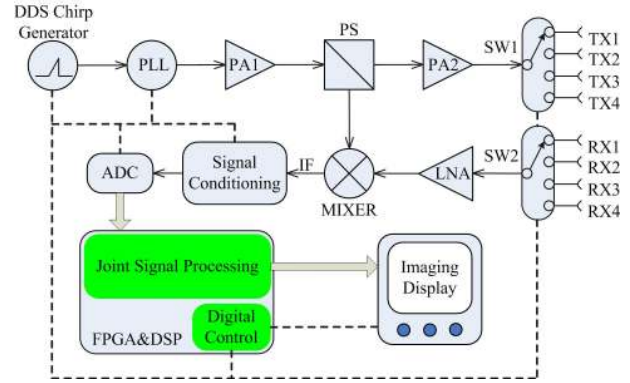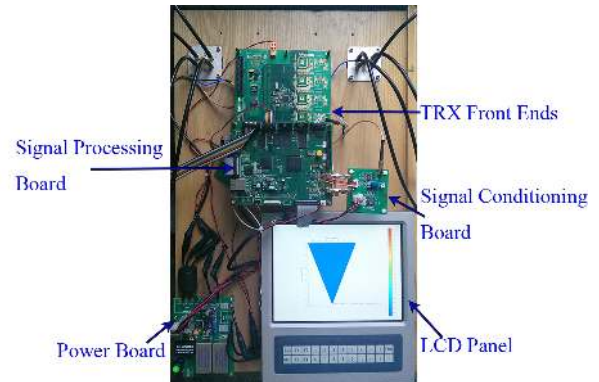

Fig. 3. Block diagram of the TDMA MIMO imaging radar system.

(a) Front view.

(b) Vertical view.

Fig. 4. MIMO radar system.

In Fig.4(b), the main components of the radar are marked out to be seen except the transmitter and receiver front ends, which are shown in Fig. 5. A detailed description of the system contents is as follows.

3.1 TDMA FMCW Signal Transceiver

The photograph of the transmitter and receiver font ends is shown in Fig. 5. In the circuits, a hybrid DDS and PLL structure is applied to generate high quality FMCW signal. Compared with the conventional schematic with a mixer, this signal generator does not produce any image frequencies. Benefit from this, purer spectrum is obtained and the image reject filter is reduced.
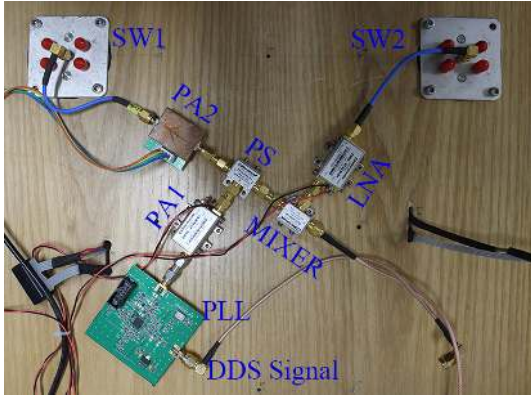
Fig. 5. Transmitter and receiver front ends.

Model	Device	Main Features
DDS	AD9910	1 Gsps, 14 bit.
PLL	HMC820	Phase noise: -105 dBc/Hz.
PA1&LNA	ZX60-272LN+	Gain: 14 dB, IP3: 31.5 dBm, Noise figure: 0.8 dB.
PS	ZX10-2-42+	Total loss: 3.3 dB.
PA2	HMC374	Gain: 9 dB, IP3: 37 dBm.
Mixer	ZX05-43MH+	Conversion loos: 6.1 dB, Passive, IP3: 18 dBm.

Tab. 1. A detailed list of the devices in the front ends.

In addition to a FMCW radar, two SP4T configuration coaxial switches are installed to handle 4 transmit antennas and 4 receive antennas so as to form a MIMO system. In the proposed design, the choice of the 2nd power amplifier (PA2) is based on the required TX power. With the output power of the power splitter (PS) set as 11 dBm and the PA2 gain selected as 9 dB in this radar system, the power of TX signal is determined as about 20 dBm. The devices in the front ends and their main typical features at the used frequency band are listed in Tab. 1.

The features of the low noise amplifier (LNA) and the passive mixer provide the front ends with a wide dynamic range in the receiver. The DDS sweeps from 49.6 MHz to 51.2 MHz with frequency step about 0.93 Hz in a chirp duration of 20.6 ms. The signal is then passed to the PLL. After 50-fold frequency multiplication, FMCW signal at the S band is generated.

The TX signal is measured with a real-time spectrum analyzer at an output port of SW1. The measurement results are shown in Fig. 6. The sweeping spectrum of the signal is sampled with 1000 traces by the analyzer in MaxHold mode. The traces are depicted in Fig. 6(a). For the reason that the analyzer misses some small parts of the sweep, some sharp negative spikes are formed at the missed points within the traces. As can be seen in Fig. 6(a), the FMCW signal is generated with a stable power of 20 dBm sweeping from 2.48 GHz to 2.56 GHz.

In Fig. 6(b), the time-frequency characteristic is measured at the center frequency of 2.52 GHz. For the limitation of the analyzer in real-time mode, the measurement span is set to 15 MHz in maximum, which means that only a part

(a) Spectrum trace with maxhold mode.
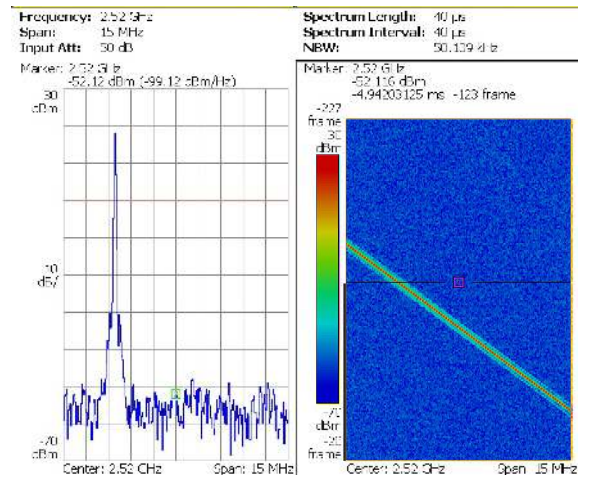
(b) Time-frequency characteristic.

Fig. 6. Spectrum of the FMCW signal.

of the sweeping process is able to be seen. However, this does not affect the excellent chirp linearity and phase noise characteristics of the FMCW signal to be appreciated.

3.2 Signal Conditioning Circuit

Consider an ideal radar with the following signal path: TX antenna - target - RX antenna. The echo signal power is defined as

$$P_r = \frac{P_t G^2 \lambda^2 \delta}{(4\pi)^3 R_t^4} \tag{13}$$

where P_t is the TX signal power, G is the antenna gain and δ is the radar cross-section (RCS) of the target [20]. In Fig. 7 the change curve between P_r and R_t is figured out with the parameters of the proposed radar system where $P_t = 20$ dBm, $G = 14$ dBi, $\lambda = 0.119$ m, and δ is supposed to be 1 m^2.

However, since antennas are distributed in a compact placement in the coherent phased array of MIMO radar, there exists the coupling path from the TX antenna to the RX antenna directly. The corresponding received signal power is the sum of P_t and the antenna isolation I_{ij}. Besides antenna

gain, I_{ij} is mainly determined by the spatial distribution of the transmitter and the receiver. In order to illustrate the issue, with the MIMO array architecture shown in Fig. 1, the minimum isolation I_{21} is measured as -51.3 dB using an S-Parameter network analyzer, and the corresponding received signal power is taken into comparison with the target echo signal in Fig. 7.

As can be seen from Fig. 7, in most of the detection range scope, the power of coupling signal is much higher than the echo signal power, which makes coupling effect to be a prominent example of error sources. Furthermore, the big gap between the power levels leads to a big amplitude difference in time domain of IF signal. As shown in Fig. 10(a), when the IF amplifier gain is set slightly higher, the waveform distortion arise easily. In such a case, the IF amplifier gain is limited and detection dynamic range of the radar is degraded.

From Fig. 8, we know that the coupling signal travels in the shortest path in the whole radar system , their effects only appear in the lowest part of IF signal in the frequency domain according to (4). Therefore, it is possible to implement a range gate to reject the adverse effects of coupling by placing a signal conditioning circuit at the output of the mixer. The signal conditioning circuit, which is shown in Fig. 9, is made up of an 8th order highpass switched capacitor filter, an 8th order lowpass switched capacitor filter and several amplifiers.

The filters are implemented using a filter building blocks chip LTC1068 with the help of the FilterCAD design software. As it is shown in Fig. 9(a), the IF amplifier is divided into two levels. IF signal is sightly amplified by the 1st amplifier to preserve the target signal on the premise of non-clipping. Then, the coupling components within the IF signal are filtered by the highpass filter. Since the output of each filter should be buffered with an amplifier, the 2nd amplifier also acts as an output buffer. Besides providing an upper limit of the range gate, the lowpass filter restrains the noise interference from high frequency band to further improve the quality of the signal. It is noteworthy that the cutoff frequencies of the filters are controlled by the processor with clock signals from FPGA, which means that the cutoff frequencies are tunable and users can easily define the range scope according to their interests by configuring the filters' control parameters. This character produces a big advantage over the analogue filter whose cutoff frequency is unmodifiable after soldering the components on board.

Field measured IF signals are replayed in Fig. 10 with the SignalTap II Logic Analyzer of Quartus II software [21]. These signals were recorded when the TX2 element transmits and the 4 RX elements take turns to receive. The tail of each waveform is deliberately exported as maximal value so that the signals can be distinguished expediently. The waveforms in Fig. 10(a) are measured after an RC analog lowpass filter and an amplifier. In the T2R1 part, the worst case, where no target signal is able to be seen, is presented. Things
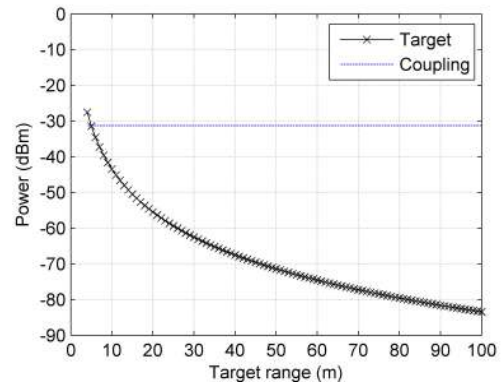

Fig. 7. Comparison between the power of target echo signal and coupling received signal.
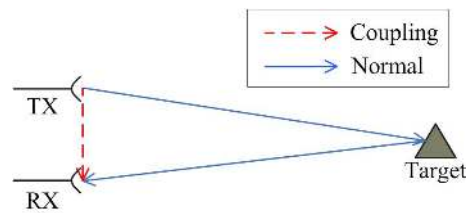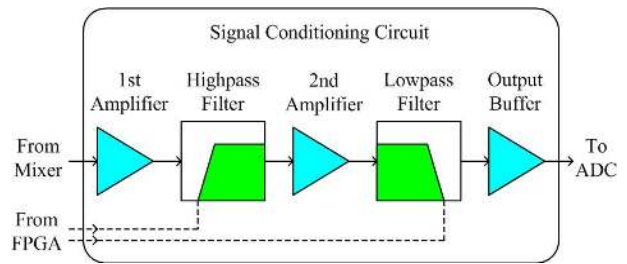

Fig. 8. Normal path and coupling path in a pair of TX and RX antennas.

(a) Scheme of the signal conditioning circuit.

(b) Signal conditioning board.

Fig. 9. Signal conditioning circuit.

get a little better in the rest of the waveforms under such a condition, however, some signals with small amplitudes are still under cover for the limitation of the amplifier gain.
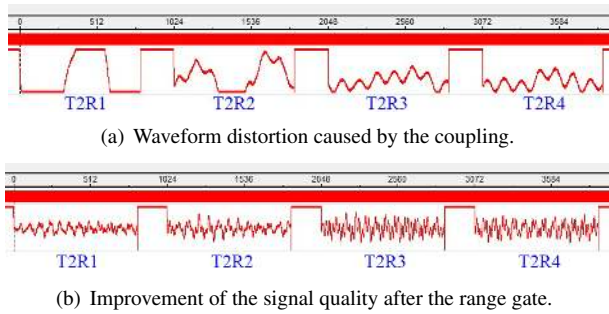
(a) Waveform distortion caused by the coupling.

(b) Improvement of the signal quality after the range gate.

Fig. 10. Comparison of the IF signal waveforms.

By using the proposed signal conditioning circuit with the gain turned to a suitable level, such phenomenon disappears. Signals in Fig. 10(b) are recorded when the circuit is applied and the range gate is set from 20 m to 100 m. As can be seen, compared with the waveforms in Fig. 10(a), more target signals could be identified without waveform distortion even in time domain, which means an improvement of SNR in the radar system.

3.3 Signal Processing Hardware Platform

After sampling through analog-to-digital converter (ADC), the IF signal is processed with a robust digital beamforming (DBF) imaging algorithm. With the purpose to provide imaging results in real-time, a FPGA and DSP based signal processing board, which is shown in Fig. 11, is implemented.

Fig. 11. Photograph of the signal processing board.

A low cost and low power consumption Altera EP3C40 FPGA chip is used as a coprocessor in this structure. The central processor is a high performance fixed/floating-point VLIW DSP TMS320C6747 device. It runs at the clock rate of 300 MHz in this system and is able to achieve a strong operation capability reaching 1800 MFLOPS. Flash storage chips and SDRAM chips are equipped around the processors for data initialization and expanding the on-chip RAM, respectively. The data exchange channel within the processors is a connection between the TMS320C6747 processor's external memory interface A (EMIFA) and the first-in first-out (FIFO) buffers on the FPGA, providing a burst transfer rate of 20 MB/s. The target measurement results are finally displayed on an 1024-by-768-pixel LCD panel, which is actuated by the FPGA at a frame rate of 50 Hz.

4. Real-Time Imaging Algorithm Implementation

4.1 FPGA and DSP Pipeline

This radar resolves targets' range information using fast Fourier transform (FFT), and angular information with a robust digital beamformer. The complete process is shown in Fig. 12.
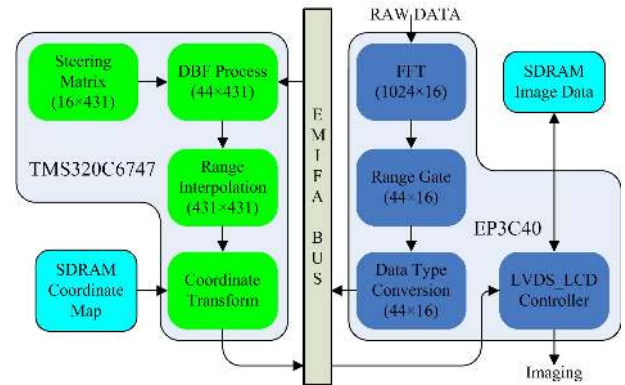

Fig. 12. Imaging process using FPGA and DSP pipeline.

Raw data is provided by the sampling of the IF signal as a real valued matrix of 1024 rows and 16 columns using a 10-bit ADC during one antenna array switching cycle. RTI data is generated from a full output precision 1024-points FFT module which is implemented on the FPGA with the assist of Altera FFT MegaCore function. In order to reduce the amount of data and make a rational use of the hardware resources, a software range gate, whose parameters are determined by users, is applied to the RTI data. According to (11), for the FMCW radar, target range R_t is defined as

$$R_t = \frac{c}{2B} k - R_{\text{sys}}; \quad k = 0, 1, ... N - 1 \tag{14}$$

where R_{sys} is the equivalent system delay that must be taken into consideration when signal travels a long path from power splitter to antenna. R_{sys} is equal to the electrical length of the path, which can be measured through an S-Parameter network analyzer. In this radar system, with $B = 80$ MHz and R_{sys} measured as 1.213 m, the RTI data is selected from $k = 11$ to $k = 54$ corresponding to the range gate (20 m ∼ 100 m) by performing (14). Before moving the selected RTI data from FPGA to DSP, a data type convertor, converting the 21 bit fixed-point data to floating-point data, is applied to maintain precision and make a good use of the DSP's floating-point feature.

It should be noted that a proper memory management based on the computational request is the cornerstone for optimizing the implementation. The C6747 DSP on-chip memory architecture consists of a two-level cache-memory (L1P,

L1D and L2) architecture plus a shared memory. The configurations and usages of the DSP memory resources in this application are shown in Fig. 13.
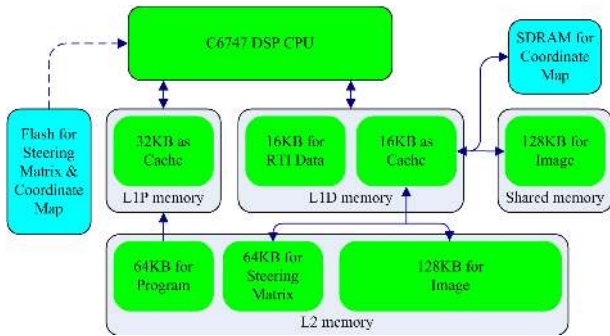

Fig. 13. Memory management for the DSP.

The coordinate map and steering matrix varies from $-21.5°$ to $21.5°$ are pre-computed and stored in a flash memory chip. They are loaded into the SDRAM and L2 memory respectively during initialization. The RTI data is moved from FPGA to the SRAM part of L1D memory, from where the C6747 central processing unit (CPU) can access data directly. The graphical user interface (GUI) provides an area for imaging display on the LCD panel. Since the range gate is set from 20 m to 100 m, pixel to pixel distance is set as 0.2 m in both cross and slant dimension within this display area and the angle between the adjacent pixels at the range of 100 m in the imaging display area can be calculated as about $0.115°$. In order to make a clear display of the radar image, the interval between the steering vectors must be smaller than $0.115°$. Considering unnecessary calculations should be avoided in a real-time system, the value of the interval is set as $0.1°$.

DBF algorithm and some image processes are performed on the DSP. A matrix of 44 rows and 431 columns is obtained as raw image data after computing the complex matrix multiplication of RTI data and steering matrix. For the reason that the radar system displays the relative logarithmic power of the returns from the target scene, a base-10 logarithm of the magnitude squared voltage converts the raw image data to dB relative power. The whole procedure is modeled as

$$\mathbf{J} = 10\log_{10}|\mathbf{S}_R\mathbf{W}|^2 \tag{15}$$

where $\mathbf{S}_R$ is the selected RTI data matrix, $\mathbf{W}$ is the steering matrix and $\mathbf{J}$ is the image data matrix consisting of all the target range and azimuth information lie in the columns and rows respectively.

However, the distance from row to row in $\mathbf{J}$ is dependent on the bandwidth and calculated as 1.875 m according to (14). In order to thin the interval and generate enough imaging points, a linear interpolation is applied to $\mathbf{J}$ in range dimension.

The output of the range interpolation is a matrix of 431 rows and 431 columns in which every element has a certain coordinate of range with azimuth. With the purpose to provide the same scene as a general map, radar image with a Cartesian coordinate system should be figured out from the original range-azimuth coordinate system and a coordinate transformer is needed. In Fig. 12, the coordinate map is a table of mapping relationship between the coordinate systems. With this table, every pixel in the cartesian coordinate system can find its position among the range-azimuth coordinate system. The contents of the table are pre-computed based on the range gate and the GUI. Hence, the only instruction for the DSP is just to move the selected elements from on-chip RAM back to the FPGA, when performing this process.

When the LCD controller receives the image data in the FPGA, it converts the relative power to 16-bit RGB value base on a color bar, and then stores the image to a frame buffer in SDRAM. The last link of the whole pipeline is a low voltage differential signaling (LVDS) controller providing a constant 50 MHz flow of data from the frame buffer to the LCD panel.

4.2 Real-Time Capability

The time consumed by the computation in the DSP can be measured with the profile clock in Code Composer Studio (CCS) software. With the compiler optimization level set as 3 in CCS, the profile clock cycle count for the process that mentioned above is 33105517. Divided by the DSP running clock of 300 MHz, the actual time is calculated to be about 0.11 s.

Considering the beginning part of the pipeline. The chirp duration T_c of the FMCW signal is 20.6 ms. After that a switch operation is executed to change channel, and a delay of 19.4 ms T_d is needed before the next chirp to ensure that the coaxial switch is completely locked. Since the radar provides a constant searching of targets and every searching is an ergodic process of all the channels, the searching cycle T_s is defined as

$$T_s = 16 \times (T_c + T_d) = 0.64 \text{ s.} \tag{16}$$

Benefit from the efficient pipeline architecture, the task of signal processing performs at the same time with data acquisition and image display. The processors finish the task and the image results are generated before the next raw data is ready. Therefore, the longest time T_s became the limiting factor of the radar's real-time capability, determining the image rate to be 1.5625 Hz.

5. Field Experiment Results

This section demonstrates the imaging capabilities of the radar system. A photograph of the test scene is shown in Fig. 14 where the main targets have been highlighted.

The scene is characterized by the presence of a parked car (a), a statue (b), two streetlamps (c), some shrubs (d),

a football goal (e) and a metal fence (f) between the square and the football field. For the measurement, the MIMO radar's antenna array is placed across from the parking lot, facing right ahead. The radar range scope is set from 20 m to 100 m as the box area shown in Fig. 14(b).
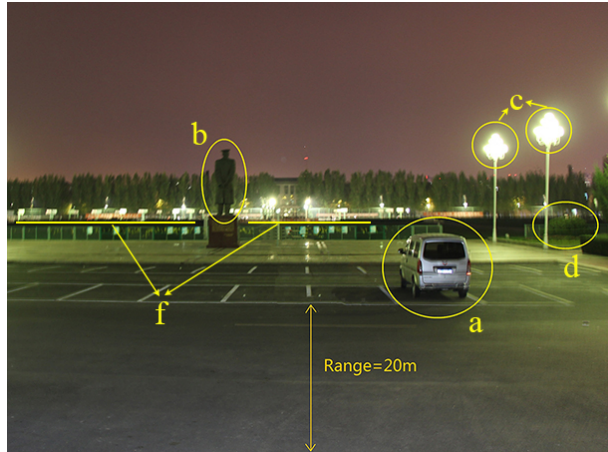
(a) Radar view of the imaged scene.
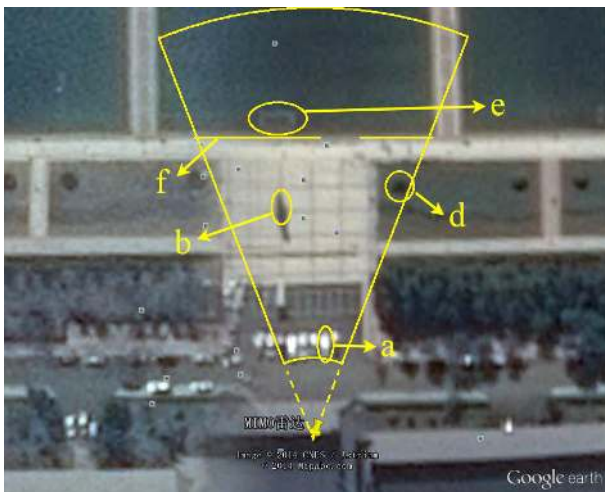
(b) Bird's eye view of the imaged scene.

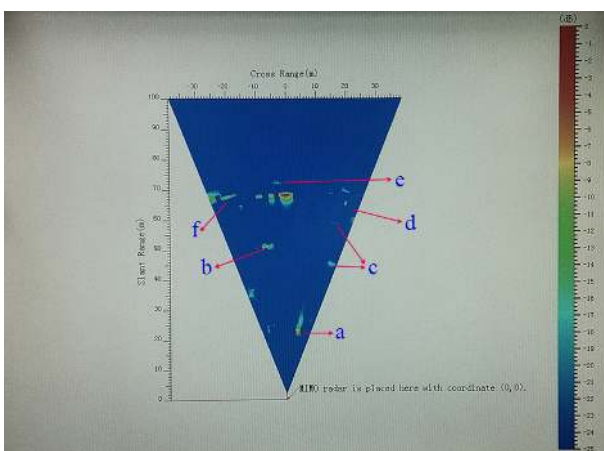**Fig. 14.** Photograph of measurement scene.

Fig. 15. Radar image.

Measurement results on the LCD panel are presented in Fig. 15. The image is displayed in real-time at a rate of 1.5625 Hz. By referring to the imaged scene in Fig. 14, the searching capability provided by the MIMO radar can be appreciated. As can be seen, all the targets that mentioned above are present at the radar image. At about 70 meters away, the empty football field is displayed as a blue area. The depiction of the metal fence is well achieved as a line except that some part of the right half is in the radar shadow behind the car and is absent at the image. Even the football goal is roughly recognized behind the fence. The car and the statue appear at the corresponding location clearly. In the right side of the radar image, two streetlamps and some shrubs are identified. In these imaging results, the spot of the nearer streetlamp is brighter than the one behind it for the reason that the echo signal power of the nearer target is higher than the farther one with the same RCS. Furthermore, in addition to positioning, the separation between these targets is also well realized.

6. Conclusion

In this paper, a MIMO imaging radar using TDMA FMCW signal is described and the initial engineering prototype is implemented. The coupling effect within the coherent antenna array is inhibited by a well-designed signal conditioning circuit in IF signal. The imaging algorithm is operated with an efficient FPGA and DSP pipeline, providing low cost and low power consumption features and a real-time imaging rate of 1.5625 Hz. The performance of multi-target localization of this radar is verified by the demonstrated image quality, which can be seen from the field experiment results. However, the imaging rate of 1.5625 Hz is not qualified in some special applications. Hence, The next step of our work is to reduce the length of a searching cycle by replacing the SW2 switch with 4 parallel de-ramp circuits as well as the corresponding data acquisition pipelines, so that the real-time performance of the radar can be further improved.

References

[1] LI, J., STOICA, P. MIMO radar with colocated antennas. *IEEE Signal Processing Magazine*, 2007, vol. 24, no. 5, p. 106–114. DOI: 10.1109/MSP.2007.904812

[2] HACK, D. E., PATTON, L. K., HIMED, B., SAVILLE, M. A. Detection in passive MIMO radar networks. *IEEE Transactions on Signal Processing*, 2014, vol. 62, no. 11, p. 2999–3012. DOI: 10.1109/TSP.2014.2319776

[3] VEERARALLI, V. V., LIANG, Y., SAYEED, A. M. Correlated MIMO wireless channels: capacity, optimal signaling, and asymptotics. *IEEE Transactions on Information Theory*, 2005, vol. 51, no. 6, p. 2058–2072. DOI: 10.1109/TIT.2005.847724

[4] BROOKNER, E. MIMO radar demystified and where it makes sense to use. In *IEEE Radar Conference*. Cincinnati (USA), 2014, p. 0411–0416. DOI: 10.1109/RADAR.2014.7060413

[5] LIU, Y., DENG, Y. K., WANG, R. Bistatic FMCW SAR signal model and imaging approach. *IEEE Transactions on Aerospace and Electronic Systems*, 2013, vol. 49, no. 3, p. 2017–2028. DOI: 10.1109/TAES.2013.6558035

[6] BELFIORI, F., MASS, N., HOOGEBOOM, P., VAN ROSSUM, W. TDMA X-band FMCW MIMO radar for short range surveillance applications. In *Proceedings of the 5th European Conference on Antennas and Propagation (EUCAP)*. Rome (Italy), 2011, p. 483–487.

[7] FEGER, R., WAGNER, C., SCHUSTER, S., SCHEIBLHOFER, S., JAGER, H., STELZER, A. A 77-GHz FMCW MIMO radar based on an SiGe single-chip transceiver. *IEEE Transactions on Microwave Theory and Techniques*, 2009, vol. 57, no. 5, p. 1020–1035. DOI: 10.1109/TMTT.2009.2017254

[8] BELFIORI, F., VAN ROSSUM, W., HOOGEBOOM, P. 2D-MUSIC technique applied to a coherent FMCW MIMO radar. In *IET International Conference on Radar Systems*. Glasgow (UK), 2012, p. 1–6. DOI: 10.1049/cp.2012.1564

[9] CHARVAT, G. L., KEMPEL, L. C., ROTHWELL, E. J., COLEMAN, C. M., MOKOLE, E. L. A through-dielectric ultrawideband (UWB) switched-antenna-array radar imaging system. *IEEE Transactions on Antennas and Propagation*, 2010, vol. 60, no. 11, p. 5195–5500. DOI: 10.1109/TAP.2012.2207663

[10] KLARE, J., SAALMANN, O., WILDEN, H., BRENNER, A. R. First experimental results with the imaging MIMO radar MIRA-CLE X. In *8th European Conference on Synthetic Aperture Radar (EU-SAR)*. Aachen (Germany), 2010, p. 1–4.

[11] ENDER, J. H. G., KLARE, J. System architectures and algorithms for radar imaging by MIMO-SAR. In *IEEE Radar Conference*. Pasadena (USA), 2009, p. 1–6. DOI: 10.1109/RADAR.2009.4976997

[12] WANG, J., JIANG, S., HE, J., LIU, Z., BAKER, C. J. Adaptive subspace detector for multi-input multi-output radar in the presence of steering vector mismatch. *IET Radar, Sonar & Navigation*, 2009, vol. 5, no. 1, p. 23–31. DOI: 10.1049/iet-rsn.2009.0197

[13] CHEN, H., LI, X., JIANG, W., ZHUANG, Z. MIMO radar sensitivity analysis of antenna position for direction finding. *IEEE Transactions on Signal Processing*, 2012, vol. 60, no. 10, p. 5201–5216. DOI: 10.1109/TSP.2012.2208108

[14] LI, H., HIMED, B. Transmit subaperturing for MIMO radars with co-located antennas. *IEEE Journal of Selected Topics in Signal Processing*, 2010, vol. 4, no. 1, p. 55–65. DOI: 10.1109/JSTSP.2009.2038967

[15] PFEFFER, C., FEGER, R., WAGNER, C., STELZER, A. FMCW MIMO radar system for frequency-division multiple TX-beamforming. *IEEE Transactions on Microwave Theory and Techniques*, 2013, vol. 61, no. 12, p. 4262–4274. DOI: 10.1109/TMTT.2013.2287675

[16] MASON, A., PARKES, S. Using SpaceWire with LabVIEW. In *International SpaceWire Conference*. Athens (Greece), 2014, p. 22–26. DOI: 10.1109/SpaceWire.2014.6936275

[17] ZHAO, Z. Y., LI, X. Y., CHANG, W. G. LFM-CW signal generator based on hybrid DDS-PLL structure. *Electronics Letters*, 2013, vol. 49, no. 6, p. 391–393. DOI: 10.1049/el.2012.2852

[18] BONFANTI, A., AMOROSA, F., SOMORI, C., LACAITA, A. L. A DDS-based PLL for 2.4-GHz frequency synthesis. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal.*, 2003, vol. 50, no. 12, p. 1007–1010. DOI: 10.1109/TCSII.2003.820250

[19] GRILLO, G. J., PEREZ, M. A., FLORENCIAS, A. E. Synchronic filter based on switched capacitor filters for high stability phase-fetectors systems. In *Proceedings of the IEEE Instrumentation and Measurement Technology Conference*. Sorrento (Italy), 2006, p. 1977–1981. DOI: 10.1109/IMTC.2006.328390

[20] HENRIKSEN, S. W. Radar-range equation. *Proceedings of the IEEE*, 1975, vol. 63, no. 5, p. 813–814. DOI: 10.1109/PROC.1975.9829

[21] CUI, Y., CHEN, Q., ZHU, L., GUO, Y. Signal Tap-II based debugging approach for the data acquisition system of multi-joint coordinate measuring machine. In *International Conference on Instrumentation, Measurement, Computer, Communication and Control*. Harbin (China), 2012, p. 1182–1184. DOI: 10.1109/IMCCC.2012.277

About the Authors ...

Wei WANG was born in 1979. He received Ph.D. in Navigation, Guidance and Control from Harbin Engineering University (HEU), Heilongjiang, China, 2005. He was a Postdoctoral Research Associate at Harbin Institute of Technology, China (July 2006 to April 2009), Associate Professor at Harbin Engineering University (August 2008 to August 2010) and Academic Visitor at Loughborough University, UK (January 2010 to December 2010). He has published about 60 refereed journal and conference papers. He is a senior member of the Institute of Electrical and Electronic Engineers (IEEE). His current research interests include signal processing for wireless navigation systems and MIMO radar.

Dong LIANG was born in 1991. He received his B.Sc. from Harbin Engineering University, China, in 2013, and is currently pursuing his M.Sc. in control science and engineering at the School of Harbin Engineering University. His research interests include imaging technology of MIMO radar and high speed real-time signal processing.

Zhihua WANG was born in 1989. He received his B.Sc. and M.Sc. from Harbin Engineering University, China, in 2011 and 2014, respectively. He is currently a engineer at Beijing Huahang Radio Measurement Institute. His research interests include radar signal processing.

Haiyang YU was born in 1990. He received his B.Sc. from Harbin Engineering University, China, in 2014, and is currently pursuing his M.Sc. in control science and engineering at the School of Harbin Engineering University. His research interests include anti-interference technology in phased array.

Qi LIU was born in 1988. He received his B.Sc. from Harbin Engineering University, China, in 2013, and is currently pursuing his M.Sc. in control science and engineering at the School of Harbin Engineering University. His research interests include array signal processing.