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***Abstract*—This paper deals with the design and the implementation of an isolated and highly integrated low voltage, low power microconverter. A dual active-bridge topology is considered as a good candidate for reducing the number of passive elements. The design of a "power die" integrating power inverter legs and their driver circuits is carried out in order to benefit from the high level of integration and to reduce the amount of active components and the volume of the converter. Thus, a microconverter is built for 10 W power supply (5 V/2 A) and is operating at 1 MHz switching frequency. The measured efficiency of the converter is 88% for 6.5 W transferred power and 86% for 8.5 W transferred power without taking into account its control unit. The converter is operating in natural convection, and no cooling system is implemented. Therefore, a power density of 9.9 kW/L is achieved, which is beyond the state of the art of the conventional isolated converters whose power densities are around 1–2 kW/L at the same power level.**

***Index Terms*—CMOS integrated circuits, dc–dc power conversion, power converters.**

I. Introduction

THE power density of power electronics converters has been significantly increased in the last decade thanks to material and technology breakthrough. Nevertheless, at low power, the improvements in power densities, including cooling, are facing great challenges because of discrete implementation, minimum forward voltage drops, and requirement of elements always irrespective of the size and the power level of the converter such as control, for example. Among the major problems of the downsizing of low voltage, low-power converters are the passive elements. In this context, interleaved converters are widely used because they allow an effective sharing of the current flow and of the power losses in each component. Their increased apparent switching frequency offers substantial voltage and significant reduce of the current ripple; hence, the size of their magnetic components is significantly reduced [1], [2]. However, on one hand, they suffer from increased number of active devices such as power switches, gate driver circuits, current sensing, and balancing circuits [3]–[5]. On the other hand, the power consumption of the increased number of active devices penalizes their efficiency for lower power rates. Thus, many works are focused on the development of highly integrated microconverters [6]–[9]. Concepts based on the standard CMOS fabrication processes are exploited in order to optimize the losses and to downsize the active devices of the converters [10]–[12], [33]. Besides, at low-voltage-level application, the forward voltage drop of the diodes is prohibited and the diodes are usually replaced by MOSFETs operating to simulate their behavior. This additional constraint increases the complexity level of low-voltage microconverters. At low voltage level, power integrated circuits in CMOS technologies offer an attractive solution to ease and optimize the implementation of dc/dc converters.

To build an isolation between the power source and the load, isolated dc/dc converters are used. In this case, an implementation of galvanic isolation is mandatory and the price to pay is the increase of the volume and the losses in the transformer. To overcome these drawbacks, isolated low-power converters are mostly based on simple topologies with HF transformers and one active switch such as in flyback or forward converters [13]–[15]. Nevertheless, the design of the magnetic components is usually performed regarding the compactness of the converters, which leads to lower efficiency rates [16], [17]. These converters look simple in terms of active devices and control, but the rating of passive components and the design factor are usually far from being optimal. Furthermore, flyback and forward converters are operating in hard-switching mode where quasi-resonant approaches are usually required in order to overcome the electromagnetic interference (EMI) and design factors of the components.

Prior arts are focused on the realization of highly integrated and isolated microconverters [7], [9], [12], [32], [33]. The proposed solutions deal with the design of custom active and passive components in order to enable high level of integration but the results are not satisfactory in terms of efficiency, power density, cost, and facility of realization [7], [12]. In order to reduce the size of the transformer, topology integrating a coreless transformer is proposed in [32]. Although the realized power supply is highly integrated, the price to pay is low power level and poor efficiency.

Therefore, the main idea of this paper is to synthetize the cutting-edge technologies in order to build one converter beyond the state of the art based on the compromise between efficiency and power density around one selected technology for its high potential for hybrid integration. The design implementation is based on multichip (two chips in our case) approach to enable the use of bulk (low-cost) technology for the active devices and not to manage the galvanic insolation at IC level because single

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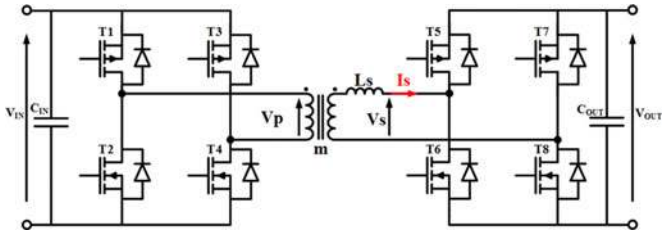

Fig. 1. Structure of a DAB converter.

chip integration can not enable the usual requirement of 1500 V rms galvanic isolation.

This paper deals with the design and the implementation of a microconverter based on the dual active bridge (DAB) topology (see Fig. 1) [18]. This dc/dc isolated topology relies on a reduced number of passive components while the number of the active devices is significantly increased. This kind of converter has the opposite advantages and drawbacks of the simple flyback and forward converter topologies. Active devices are greater in amount and more complex to implement while passive components are all optimized in terms of storage level and rating. The outstanding interests in choosing the DAB converter are as follows:

1) At a low voltage level, rectification diodes are emulated by MOSFETs and CMOS technologies can be used to overcome the complexity thanks to the monolithic integration.
2) Thanks to the CMOS fabrication process, which offers a high level of integration of the inverter legs and of the gate driver circuits, the volume of the active devices is significantly reduced and the reliability is increased compared to hybrid implementation based on discrete packaged components.
3) It offers significant performance improvements allowing the switching cells to operate at high switching frequencies (1 MHz and above) to reduce the size of the transformer and the filters while limiting the switching losses.
4) The symmetry of the DAB converter offers the opportunity to optimize the use of the HF transformer and of its leakage inductance while it downsizes greatly the rms current levels in the input and the output filtering capacitors. Its symmetry allows also a bidirectional energy transfer. Unlike the converter proposed in [7] converter, the output inductor is no more mandatory.
5) The DAB converter has a very specific but optimal design tradeoff. If the ratio between the input and the output voltage (taking into account the transformation ratio) are close, the leakage inductance can be minimized as well as the amount of energy stored in the passive elements. With almost permanent direct power transfer from the primary to the secondary, the DAB converter has an increased dynamic response and is a very good candidate for low-voltage low-power applications.
6) Its ZVS, ZCS natural switching transition completes the benefits of the converter topology to overcome EMI and design factors of all components.

The use of only half bridges does not gain any interest in terms of power density, efficiency, and cost event though it seems to be a less complex approach [31]. The capacitive voltage divider decreases the voltage of the converter, and to reach the same level of transferred energy as the DAB converter, its current has to be doubled. Consequently, the width of the MOSFETs has to be enlarged, and finally, the die will have the same size as the one designed for the DAB converter. Moreover, the copper and the core losses in the transformer will increase as well. To overcome this drawback, a larger core is required in order to implement larger windings but in such a way, the volume of the converter will be penalized without any efficiency improvement.

As mentioned before, the objective of the paper is then to demonstrate that, at low-power low-voltage levels, complex but highly integrated converters are good candidates for high efficiency, high power density, and outstanding EMI and reliability performances. More specifically, it will be shown that the DAB converter is an excellent converter solution with galvanic isolation, especially when the input and output voltages ranges can be considered limited. Moreover, in an optimal operating mode, the input and output currents of the DAB converter are almost continuous. Thus, the required EMI filters for conducting perturbations remain small.

This paper is structured as follows: the next section presents the operating mode of the DAB converter and especially the design opportunity raised with the operation of the converter within a specific range; the optimized design of a power die integrating the power inverter legs and their gate driver circuits fabricated using standard CMOS fabrication process is highlighted in Section III; the design of the transformer, which is fabricated using standard commercial planar core is presented in the Section IV. The last section focuses on the realization, the implementation, and the experimental characterizations of a microconverter built for a 10-W power supply (5 V/2 A). A comparison is proposed to underline the interest of the approach proposed in the paper.

II. Presentation of the DAB Converter

The DAB converter has been studied by many authors [18]–[23], and its general characteristics are well known to the power electronics engineer. It is out of the scope of this paper to recall the wide range of characteristics and specificities of this topology. This section focuses only on its basic characteristics of operation to underline the optimized design considerations.

In normal operating mode, each inverter leg of the DAB converter is driven with a 50% constant duty cycle. The control of this structure is based on the phase shift between the voltages applied on the primary and secondary sides of the transformer. Fig. 2 shows the typical current I_S in the leakage inductance of the transformer and the voltages V_P and V_S, respectively, applied on its primary and secondary sides.

The shape of the current, the output voltage, and the maximum transferred power depend on the phase shift β between the voltages V_P and V_S, on the difference between the input and the output voltage, on the leakage inductance, and on the switching frequency. Therefore, the regulation of the output voltage V_{OUT}

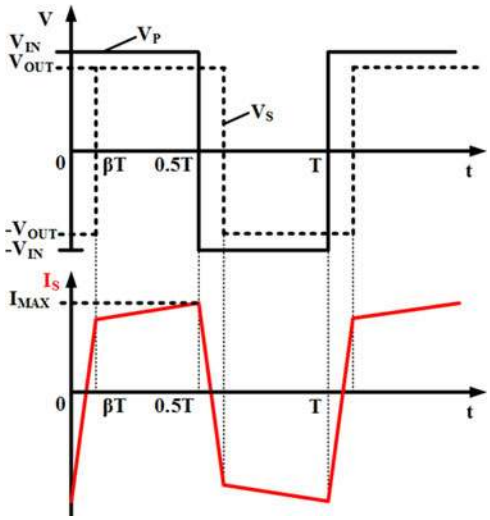

Fig. 2. Current and voltage waveforms.

is given by (1), and the maximum transferred power P_{MAX} is given by (2)

$$V_{\mathrm{OUT}} = \frac{(1-2\cdot\beta)\cdot m\cdot V_{\mathrm{IN}}\cdot R}{f_{\mathrm{sw}} L_S} \tag{1}$$

$$P_{\mathrm{MAX}} = \frac{(1-2\cdot\beta)\cdot m^2\cdot V_{\mathrm{IN}}^2\cdot d\cdot\beta}{f_{\mathrm{sw}} L_S} \tag{2}$$

where *R* is the resistive load, *m* is the transformer ratio, L_S is the leakage inductance of the transformer, f_{sw} is the switching frequency of the converter, and *d* is the ratio between the output and input voltage given by

$$d = \frac{V_{\mathrm{OUT}}}{m\cdot V_{\mathrm{IN}}}. \tag{3}$$

For fixed values of *R*, *m*, L_S, and f_{sw}, the variation of the phase shift can change the transformation ratio of the converter so that it operates in a buck or boost mode. The direction of the energy transfer depends also on the phase shift. For $\beta > 0$, the current flows from V_{IN} to V_{OUT}; and for $\beta < 0$, the current flows from V_{OUT} to V_{IN} [22].

The value of the leakage inductance of the transformer is essential for the level and the shape of the current flowing through the transformer. On one hand, its value has to be as low as possible in order to reach the maximum transferred power P_{MAX} [19] and to minimize its implementation constraints. On the other hand, its value is critical with respect to the magnitude of the current ripple and rms current levels, both related to the losses. If the leakage inductance and the phase shift are fixed, the rms value of the current increases with the difference between V_P and V_S.

Fig. 3 shows analytical result of the transferred power as a function of the value of the leakage inductance for fixed switching frequency and input voltage and load resistance and for different values of the phase shift. The assumed parameters for the following analysis are based on simulated estimations of the parameters of the inverter legs which are built using AMS 5 V 0.35 μm CMOS fabrication process. These values are

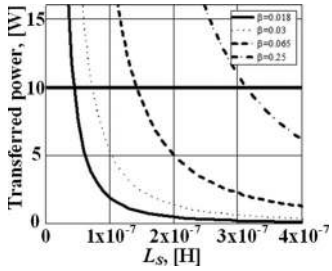

Fig. 3. Transferred power.

TABLE I
ASSUMED PARAMETERS IN THE ANALYTICAL ESTIMATION OF THE LOSSES IN THE CONVERTER AT ROOM TEMPERATURE 25 °C

PMOS on-state resistance ($T = 25$ °C) R_{DSONP}	11 mΩ
NMOS on-state resistance ($T = 25$ °C) R_{DSONN}	9 mΩ
PMOS input gate capacity C_{ISSP}	1000 pF
NMOS input gate capacity C_{ISSN}	345 pF
Transformer winding dc resistance R_{DCW}	15 mΩ
Transformer winding ac resistance (1 MHz) R_{ACW}	35 mΩ

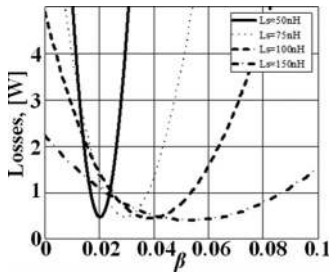

Fig. 4. Total losses ($V_{\mathrm{IN}} = 5$ V, $f_{\mathrm{sw}} = 1$ MHz, and $R = 2.5\ \Omega$).

summarized in Table I. As it can be seen, the phase shift increases with L_S to maintain the transferred power constant until it reaches its maximum value $\beta_{\mathrm{MAX}} = 0.25\ T_{\mathrm{SW}}$. Thus, for 10 W desired transferred power, the maximum value of L_S is limited up to 300 nH.

Fig. 4 shows analytical estimations of losses and of efficiency of the converter as a function of the phase shift β for a fixed switching frequency, input voltage, and load resistance and for different values of the leakage inductance. As it can be observed, for each value of the leakage inductance, there is an optimal phase shift β where the losses are minimized. Moreover, for lower rates of the leakage inductance, the adjustment range of the phase shift is more precise. For example, to keep the efficiency of the converter higher than 90%, the phase shift has to be between $0.18\ T_{\mathrm{SW}}$ and $0.25\ T_{\mathrm{SW}}$, if $L_S = 50$ nH, and between $0.25\ T_{\mathrm{SW}}$ and $0.085\ T_{\mathrm{SW}}$, if $L_S = 150$ nH (T_{SW} is the switching period). As a consequence, at increased frequencies, the minimum value of the leakage inductance will be limited by the resolution of the control module.

According to Fig. 5 and (1), we can conclude that the efficiency is also higher when $d = 1$ ($V_{\mathrm{IN}} = V_{\mathrm{OUT}}$). In this case, the converter will operate at its highest efficiency level. As shown in Fig. 6, it is also possible to find the operation point of the converter with maximal efficiency as a function of the ratio between the maximal current I_{MAX} and the mean output current I_{MEAN}

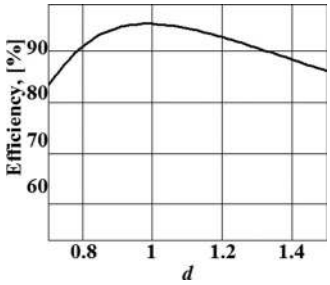

Fig. 5. Efficiency ($V_{\rm IN} = 5$ V, $f_{\rm sw} = 1$ MHz, $L_S = 50$ nH, and $R = 2.5\ \Omega$).

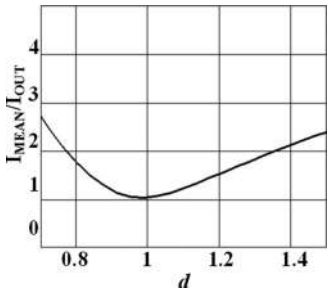

Fig. 6. Ratio $I_{\rm MEAN}/I_{\rm OUT}$ as a function of the ratio *d*.

in steady state [21]. When $d = 1$, the current ripple is lowest and the value of the efficient current is almost equal to the value of the mean output current. Therefore, the losses are reduced as well and the rms currents are minimized in all components at constant power level.

Theoretical studies have been done regarding the operating of the DAB converter in soft switching mode (ZVS) [20]. In this case, the switching losses can be neglected. To achieve ZVS mode, the size of the leakage inductance L_S has to be large enough to discharge the output capacitance $C_{\rm OSS}$ of the MOSFETs. $C_{\rm OSS}$ and L_S create a circuit whose resonant frequency is $L_S C_{\rm OSS}$. In order to apply the ZVS mode, the dead time DT of the MOSFETs during switching has to be optimized with respect to the resonant frequency

$$\mathrm{DT} = \frac{1}{4\sqrt{Lf \cdot C_{\rm OSS}}}. \tag{4}$$

When the converter is operating at lower power levels (lower load value), the $C_{\rm OSS}$ cannot be discharged completely, and thus, the converter is no more running in ZVS mode.

Integration of active devices is mandatory in order to build a highly integrated and compact converter based on the DAB topology. Furthermore, only monolithic integration is able to comply with the constraints of an operation at high frequency with a very low leakage inductance. Indeed, perfect propagation delays are required to switch the transistors under ZVS and ZCS conditions and to insure proper dynamic control and phase shift between the primary and the secondary IC. This requires the use of identical dies for the implementation of the inverter and the rectifier modules. In the next section, the design of the power die is presented.

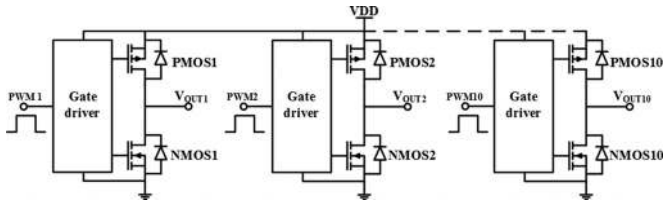

Fig. 7. Structure of the CMOS power die with the elementary inverter legs and dedicated gate drivers.

III. Design of the Power CMOS Die

The power die is designed based on the paralleling of ten elementary CMOS inverter legs with their associated gate drivers. Thus, the parasitic inductances between the drains of the transistors PMOS and NMOS and between the gate driver and the gates of the transistors are eliminated, and the unwanted ringing and the switching losses are reduced. The full-bridge structure has been built by realizing two CMOS power inverter legs, both composed of five independent CMOS inverter legs connected in parallel. As mentioned before, a driver circuitry is dedicated to each elementary inverter leg to provide optimal and tuned propagation delays (see Fig. 7). The command signals can be provided from any external source such as a microcontroller, an FPGA, or another logic circuit. In addition, and this will be underlined later in the packaging section, each elementary inverter leg has its own power pad to limit current flow within the IC tracks. Special care is taken here to overcome the classic limitation of the interconnections at low voltage levels.

The design of each independent inverter leg is based on the standard 0.35 μm 5 V CMOS fabrication process offered by AMS. It is designed for applications up to 2 A, depending on thermal capabilities of the package and the assembly (200 mA mean current per inverter leg). Since a standard CMOS technology process is used, only several characteristics of the MOSFETs such as internal resistances and gate and drain-source capacitances are defined as a function of the gate widths *W* of the MOSFETs [12]. The gate driver circuit used in association with each inverter leg is also optimized with respect to the switching losses of the power MOSFETs and its consumption [10]–[12]. The decoupling capacitor has not been integrated because the CMOS fabrication process allows the integration of only small capacitors (1 fF/μm^2). Thus, the integration of capacitors of several nanofarads would increase the size of the chip, the resistances of the tracks, and the cost of the die.

Integration of active devices does not deal only with the design of one die; the whole design of the converter has to be taken into account with respect to the packaging, the assembly with the substrate and the interconnections between the components, in order to avoid parasitic phenomena and electrical and thermal constraints. Fig. 8 shows a Cadence simulation result of the efficiency of one elementary CMOS inverter leg for different rates of the mean load current while switching at 1 MHz and $V_{\rm DD} = 5$ V. Its parameters are given in Table II. Bump resistances $R_{\rm BUMP}$ and interconnections tracks are also taken into account for each power I/O pad of the inverter leg assuming an elementary series resistance of 5 mΩ [26].

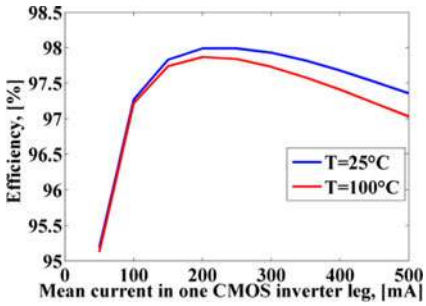

Fig. 8. Efficiency of one CMOS inverter leg as a function of the mean load current ($V_{\mathrm{DD}} = 5$ V, $f_{\mathrm{sw}} = 1$ MHz, and $R_{\mathrm{BUMP}} = 5$ mΩ).

TABLE II
PARAMETERS OF ONE CMOS ELEMENTARY INVERTER LEG

Parameter	NMOS	PMOS
On state resistance ($T = 25$ °C) R_{DSON}	45 mΩ	55 mΩ
Gate input capacitance C_{ISS}	70 pF	200 pF
Rise time	1.4 ns	1.4 ns
Fall time	0.4 ns	0.4 ns

TABLE III
LOSSES IN ONE CMOS ELEMENTARY INVERTER LEG

Conduction Losses	Switching Losses	Driver Losses	Losses in Interconnect Resistances
8.1 mW	5.2 mW	5.2 mW	4 mW

Simulation results show that 97% efficiency can be achieved over a wide current range even for higher power levels; the main limitation in this case being the heat removal capability of the extra losses. It clearly appears that it is mandatory to ensure a good thermal management of the assembly in order to keep the die operating significantly under its maximal operating temperature which is 125 °C [24] while offering a maximum power density level. The power losses are summarized in Table III at nominal current 200 mA and under 5 V.

As it can be seen in Table III, the losses in the bumps are in the same order as the conduction losses, the switching losses, and the driver losses for only 5 mΩ bump resistance per pad. This highlights the need of efficient assembly and the impact of the parasitic resistances on the efficiency of the converter, which is not always as critical at higher voltage applications, for example.

Flip chip and associated assembly technologies allow the connections between the chip's pads and the tracks of the substrate via adhesive paste, stud bumps, copper pillars, or solder bumps instead of bonding wires [25]. The result is a significant downsizing of chip package, reducing the assembly cost and decreasing the parasitic phenomena such as interconnect resistances and inductances [34]. In addition, it reduces the number of thermal interfaces between the chip and the substrate, which operates as the principal heat removal path. Fig. 9 shows an image of the power die designed with respect to the standard PCB design rules for a flip-chip assembly. The design of both the PCB and the CMOS chip is driven by the need to keep the

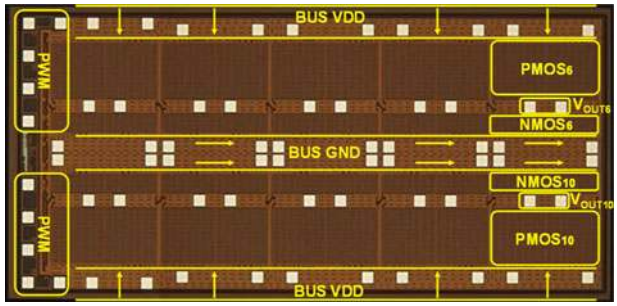

Fig. 9. Image of the power CMOS die.

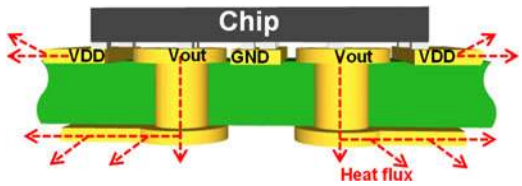

Fig. 10. Layot of the printed circuit board (cross section).

current uniformly spread among all the ten CMOS power inverter legs. The +dc supply terminal is connected to two tracks one on each side of the device. The ground terminal (GND) is in the middle of the chip, between the two rows of CMOS power inverter legs. This configuration allows maximal reduction of the resistances of the power tracks in the die since the power NMOSFET and PMOSFET are vertically flattened. Besides, it allows to uniformly spread the pads over most of the surface of the die. The number of pads is determined with respect to their maximal current density given in DRM of the technology [24] so that the equivalent bump resistances of each power terminal of the inverter legs are significantly reduced in comparison to the characteristics of the device. Thus, the surface of the die is 9.9 mm^2 (4.5 mm length and 2.2 mm width) and it contains 70 pads. Ten pads are dedicated to the command, 20 pads in parallel are dedicated to the GND (two pads in parallel per inverter leg), 20 pads in parallel are dedicated to the V_{DD} (two pads per inverter leg), and 20 pads are dedicated to the middle points, two per inverter leg. In such a way, each inverter leg is closely connected to six pads for maximum heat removal while giving the opportunity to reduce the equivalent series resistance of each power terminal as well as the current density on each pad. Also, the MOS devices being quite large, the use of two pads for each contact minimize the current circulation in the conductive layers of the die. The position of each pad is optimized to reduce this current circulation at die level.

The PCB has been designed with standard two layers technology and material FR4 with the objective to ensure optimal thermal management of the assembly (see Fig. 10). The output pads of each inverter leg are placed on vias in order to get a direct access to the outputs on the backside of the PCB. In this way, the heat can be also drained through the bumps to the copper tracks on the bottom layer. In order to achieve such PCB design, the shape of each power transistor has been optimized to enable the placement of the vias. V_{DD} and GND tracks of the PCB serve as heat spreaders as well.

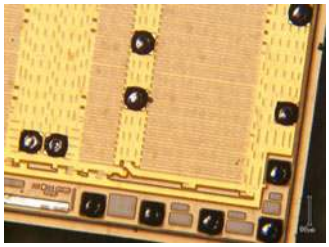

Fig. 11. Solder bumps on the pads of the CMOS circuit.

Solder bump bonding has been used to make the flip-chip assembly of this die with 70 pads and complex substrate pattering. This technology deals with the soldering of bumps composed of different alloys such as SnPb, SnAgCu, SnAg, SnCu, etc., directly on the chip pads [27]. Fig. 11 shows a photograph of solder bumps of SnAgCu alloy with 90 μm diameter soldered on the chip pads. The chip is then aligned to the PCB substrate, and the joints are built by welding the bumps during a reflow process. Afterward, an underfilling process has been carried out in order to enhance the mechanical strength of the flip-chip assembly. Thus, high reliability of the assembly of the active devices is expected.

IV. Design of the Transformer

The transformer has to be designed according to the compromise between the losses and the volume of the converter. The magnetic inductance has to be high enough to reduce the magnetic current in the core in order to minimize the value of the magnetic induction and the core losses. The leakage inductance has to be optimized with respect to the maximal transferred power [see (2)]. The windings have to be optimized so that their resistances are highly reduced and skin and proximity effects are minimized. Moreover, the volume of the transformer has to be scaled down in order to build a converter with a higher power density. Indeed, in order to limit the maximum magnetizing current of the transformer, the value of the magnetizing inductance must be greater than 3.7 μH. With this value, for a half period of 1 μs and a 5 V symmetrical square voltage applied to the primary side of the transformer, the maximum current ripple ΔI is limited to 0.8 A. Therefore, the peak current in the magnetizing inductor is around 0.4 A compared to the 2 A nominal current under an input/output voltage mismatch of 20% max. The value of the leakage inductance has to be as high as possible due to the resolution constraint of the control and lower than 300 nH in order to obtain the maximum power transfer greater than the nominal power transfer of micropower converter (10 W).

The planar technology is a solution for designing low-profile transformers with good thermal characteristics, high power density, an ease of manufacturability, and cost reduction. It is also a master choice when predictable parasitics are required, which is our case since we want to integrate the DAB inductor within the HF transformer as being its leakage inductance [28]. A planar transformer has been designed using finite elements software, which allows the choice of the optimal magnetic core and the routing of the windings to control and optimize the value of the leakage inductance. Thus, it has been designed using one commercially available half-core ER9.5 and one fabricated I core,

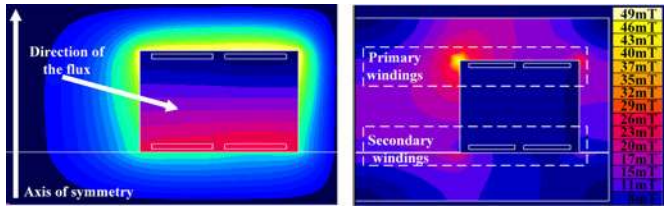

Fig. 12. Finite element analysis for the planar transformer. (a) Direction of the magnetic flux. (b) Induction in the magnetic core.

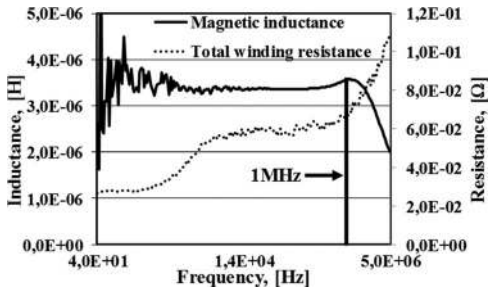

Fig. 13. Characteristics of the planar transformer with 3F3 material.

both made of 3F3 material. Since a resolution of 125 μm is used to create the land pattern of the die, the maximum thickness of the copper given by the manufacturer is 35 μm. This thickness has a significant impact on the resistance of the windings and, consequently, on the losses in the transformer. Nevertheless, the PCB resolution is dictated by a compromise at power level. If larger PCB tracks would be used to enable the use of thicker copper tracks, this would give an impact on the optimization of the die itself, with the constraints on pad location becoming larger.

The primary and the secondary windings have two turns, which are printed on the top and the bottom layers of the PCB. As shown in Fig. 12, the turns of each winding are placed around the central leg of the transformer. The direction of the magnetic flux is in parallel regarding the conductors and the skin effect is oriented toward the thickness of the conductor. The width of the conductor is designed as large as possible (700 μm) according to the size of the wire window in order to reduce its series resistance. The distance between the primary and the secondary windings is defined so that there is a sufficient leakage inductance to control the transferred power. This is made possible within the limits of the winding window and as a function of PCB thicknesses constraints.

As presented in Fig. 13, at a switching frequency of 1 MHz, the operating point of the converter is close to the resonance of the magnetic core because the 3F3 material is appropriate for use at frequencies of 0.2–0.7 MHz. It is also possible to use the same ER9.5 magnetic core with 3F4 material, which is appropriate for use at frequencies of 1–2 MHz, but its permeability is lower ($\mu_{3\mathrm{F3}} = 1130$; $\mu_{3\mathrm{F4}} = 700$). As a result, the magnetic inductance would be decreased around 1.6 times, and consequently, the values of the magnetic current and the corresponding losses would be increased. Therefore, the core and the winding losses of the transformer with 3F4 material would be higher than these of the transformer built with 3F3 material. The parasitic capacitances of the transformer winding to

TABLE IV
PARAMETERS OF THE PLANAR TRANSFORMER

DC resistance (one winding) R_{dc}	15 mΩ
AC resistance at 1 MHz (one winding) R_{ac}	35 mΩ
Magnetic inductance L_m	3.75 μH
Leakage inductance (1 MHz) L_s	60 nH

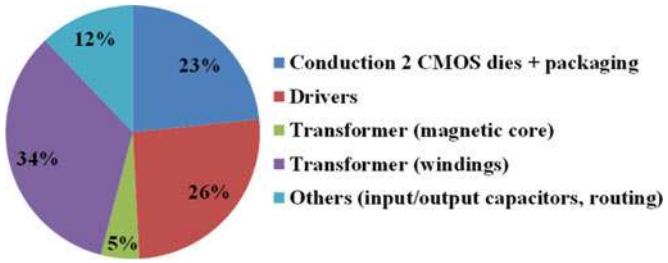

Fig. 14. Loss breakdown of the converter ($V_{\mathrm{IN}} = V_{\mathrm{OUT}} = 5$ V, $I_{\mathrm{OUT}} = 1.7$ A, and $f_{\mathrm{sw}} = 1$ MHz).

winding, turn to turn, and layer to layer are very low and can be neglected because, on one hand, the distance between the primary and the secondary windings of the transformer is too large, and on the other hand, there are only two turns per winding implemented on the same layer of the PCB. Therefore, the first resonance of the transformer is the resonance of the magnetic core (see Fig. 13). Finally, the parameters of the designed transformer are shown in Fig. 13 and summarized in Table IV.

For a 10 W transferred power, these values give 340 mW conduction losses due to R_{AC} and 40 mW core losses due to 49 mT maximum magnetic induction (see Fig. 12). Therefore, the estimated efficiency of the transformer is around 96% at the full-power level. The obtained value of the leakage inductance is 60 nH, and its value is especially stable at 1 MHz.

Fig. 14 shows the loss breakdown of the converter at 8.5 W transferred power. In our design, the windings of the transformer are the source of highest losses; hence, future works will be focused on its optimization. The global efficiency of the converter is from a simulation and theoretical point of view around 90%.

V. EXPERIMENTAL RESULTS

The first prototype of the converter is built in open-loop mode, and the phase shift is adjusted manually. For this purpose, an external microcontroller (dsPIC) is used. Fig. 15 shows a picture of the realized converter. Its size has been highly reduced (length 23 mm, width 11 mm, and height 3.4 mm). The surface of the PCB has been optimized to operate the converter in natural convection mode, without any external cooling system. During the experiments, no EMI filters have been added to the testing circuit since in the optimal operating mode, the input and output currents of the DAB converter are almost continuous. Fig. 16 shows the waveform of the current on the primary side of the transformer and the voltages (V_P and V_S) on its primary and secondary sides for an output current level $I_{\mathrm{OUT}} = 1.7$ A, input and output voltages $V_{\mathrm{IN}} = V_{\mathrm{OUT}} = 5$ V, and a switching frequency $f_{\mathrm{sw}} = 1$ MHz. The phase shift angle between V_P and V_S has been adjusted manually observing the input and the output

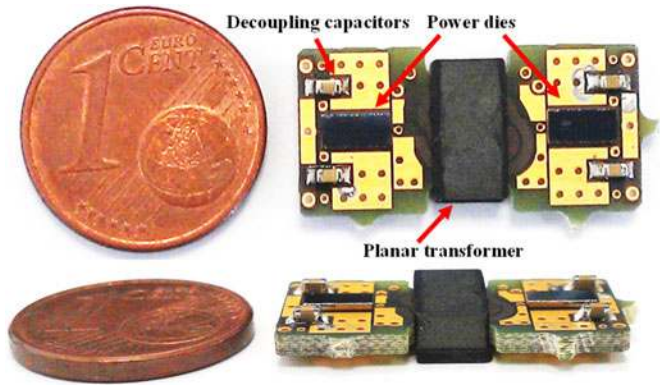

Fig. 15. First prototype of the DAB converter.

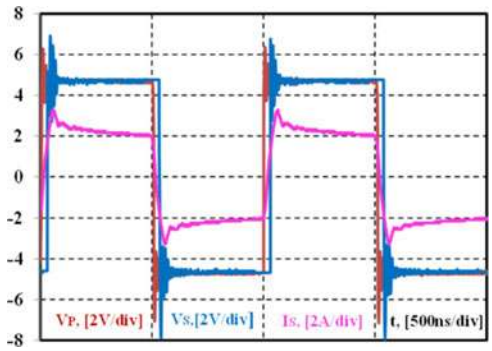

Fig. 16. Current *Is* in the leakage inductance of the transformer ($V_{\mathrm{IN}} = V_{\mathrm{OUT}} = 5$ V $I_{\mathrm{OUT}} = 1.7$ A and $f_{\mathrm{sw}} = 1$ MHz).

voltages, which are measured with a four-terminal sensing method. The current waveform is the characteristic, which can validate the proper operation of the converter. As it can be observed, there is no distortion of the current waveform; hence, we can conclude that the converter is operating correctly. A capacitor has been added in series with the winding of the transformer in order to filter a potential voltage offset (due to the different values of the voltage drops over the transistors PMOS and NMOS since the values of their R_{DSON} are a bit different), which could cause its saturation. Its value being a bit lower, creates a small voltage variation that causes an initial exponential decay in the current waveform.

Fig. 17 shows an image taken with an IR camera in order to observe the thermal constraints of the converter. As it can be seen, the windings of the transformer are the source of high losses and they heat the magnetic core as well. Their temperature rises up to 100 °C for an output current $I_{\mathrm{OUT}} = 1.7$ A or 8.5 W transferred power. The temperature of both dies is around 75–80 °C, and the heat is well evacuated thanks to the copper planes

As shown in Fig. 18(a), the efficiency analysis of the converter has been performed with $V_{\mathrm{IN}} = V_{\mathrm{OUT}} = 5$ V, under a switching frequency $f_{\mathrm{sw}} = 1$ MHz and for different power rates. Without taking into account the consumption of the control unit, an efficiency of 88% is reached for output current $I_{\mathrm{OUT}} = 1.3$ A or transferred power $P_{\mathrm{OUT}} = 6.5$ W. Then the efficiency decreases to 86% for output current $I_{\mathrm{OUT}} = 1.7$ A or transferred

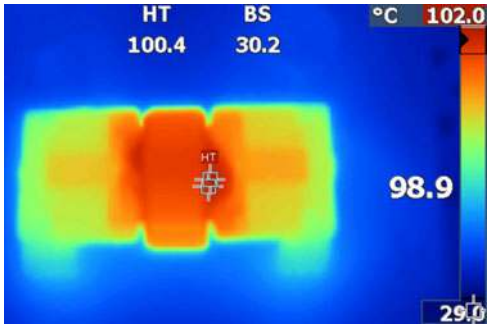

Fig. 17. Thermal image of the DAB converter ($V_{\mathrm{DD}} = 5$ V, $V_{\mathrm{OUT}} = 5$ V, $I_{\mathrm{OUT}} = 1.7$ A, and $f_{\mathrm{sw}} = 1$ MHz).

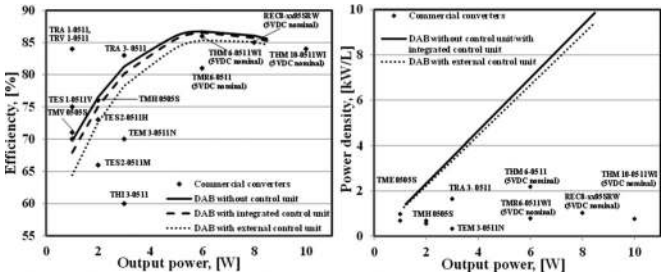

Fig. 18. Comparison of the DAB converter and commercial converters with integrated/external control unit (projected). (a) Efficiency versus output power. (b) Power density versus output power.

power $P_{\mathrm{OUT}} = 8.5$ W due to the losses in the windings of the transformer. The external microcontroller consumes 90 mW power but future works will be focused on the integration of low consumption voltage sensing and pulsewidth-modulated (PWM) generator in the same die with the power inverter legs and the gate drivers without increasing its volume. In this case, the consumption of the control unit is estimated 30 mW maximum.

The DAB converter represents a galvanic isolation with fixed input and output voltages. Therefore, the maximal voltage range on its input and output tolerated by the converter so that it achieves a maximum efficiency is 10% (4.5–5 V). To make a better comparison with the state of the art in terms of efficiency and power density, commercial isolated converters are also selected with fixed input and output voltages of 5 V $\pm$ 10%. As shown in Fig. 18(a) and (b), the efficiency and power density of the DAB converter are greater than those of the commercially available low-power supplies [29], [30].

Comparative analysis shows that the DAB converter has greater performance for transferred power more than 2 W. The DAB converter is designed for one optimal operating point, which in our case is 10 W transferred power. At lower power rates (low load), the losses of the gate drivers remain the same and the switching losses appear since the converter is not running in ZVS mode anymore. Meanwhile, its conventional opponents shown in the graph are optimized, especially for the respective power levels. The comparison of the power density highlights the reached gain of the design factor of DAB converter. A very high power density of 9.9 kW/L at 8.5 W transferred power is achieved in comparison to the commercial converters whose power density is generally around 1–2 kW/L at this power level.

VI. Conclusion

In this paper, the design and the implementation of a highly integrated DAB microconverter for low-voltage low-power applications incorporating a galvanic isolation has been presented. This structure has a reduced number and optimal design ratings of the passive components while compensating the complexity of the active part thanks to the monolithic integration. A power IC containing inverter legs and their driver circuits has been designed based on a standard AMS 5 V 0.35 μm CMOS fabrication process. Its design has been realized with respect to the standard PCB design rules and constraints in order to reduce the volume of the assembly, to ease the heat evacuation and to offer the possibility to reduce the parasitic resistances of the contacts thanks to the flip-chip assembly process. Then a planar transformer has been designed. Experimental results validate the operation of the microconverter, and 88% efficiency has been achieved at 6.5 W transferred power, whereas 86% efficiency was reached for 8.5 W. This is beyond the state of the art of the conventional isolated converters whose power densities are around 1–2 kW/L at the same power level.

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