Design and Implementation of a Low-Complexity RAKE Receiver and Channel Estimator for DS-UWB

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***Abstract*—In this paper, the design and implementation of a low complexity Direct Sequence Ultra-Wideband (DS-UWB) receiver subsystem which incorporates a Channel Estimator (CE) and a novel hybrid Partial/Selective (HPS) RAKE Receiver (RR) using maximal ratio combining (MRC) is presented. The proposed architecture demonstrates the tradeoff between energy capture, performance and receiver complexity by combining the benefits of both partial and selective RAKE receiver algorithms. We focus our work on a highly parallel, modular, synthesizable design which is based on FPGA technology and it is optimized for high performance.**

I. INTRODUCTION

Since its regulation in 2002, UWB technology has drawn considerable attention, emerging as an attractive solution for short-range, low-power, high data rate wireless communications, with application in wireless personal area networks (WPANs) and wireless sensor networks (WSNs) [1]. IEEE 802.15.3a task group for standardization (before its disbandment in January 2006) and various industry groups have considered two alternative physical layers for WPANs based on UWB technology: direct-sequence spread spectrum UWB (DS-UWB) systems [2], which we consider in this work, and multiband orthogonal frequency-division multiplexing UWB (MB-OFDM UWB) systems.

The main characteristic of a UWB system is its wide bandwidth (in the order of several GHz), which leads to highly frequency selective channels and received signals composed of a significant number of resolvable multipath components with different delays in the order of nanosecond. A DS-SS UWB system [3] with a RAKE receiver can exploit multipath diversity by constructive summation of the desired signal energy which is dispersed over the various multipath components, helping to mitigate fading and thus improving performance. However, the low energy of the resulting paths combined with the high resolvability, result in a RAKE receiver that must employ a large number of multipath components in order to optimize the received SNR. Previous studies showed that a RAKE receiver operating in a typical modern office building requires about 50 different RAKE fingers to capture a sufficient amount of the total energy of the received signal [4]. This fact poses significant challenges in the design and implementation of a RAKE receiver aiming to achieve a high performance gain in a low complexity and power efficient structure. The most common methods proposed towards this aim are the Selective RAKE (SRake) and Partial RAKE (PRake) schemes [5]. The first one combines the L_S strongest multipath components among the L_{TOT} available at the receiver input using MRC scheme. Despite the reduction in the number of RAKE fingers, the selection procedure requires efficient channel estimation in order to keep track of the value of all multipath components at each time instant. The second method combines the first L_P arriving multipath components using MRC and it is a less complex solution, as it does not have to carry out any selection among the multipath components. It is clear, that SRake performs better than PRake since the latter combines paths that may not contribute to increasing the collected energy. However, in cases where the stronger multipath components are located in the beginning of the channel impulse response the performance gap decreases.

So far, several other complex types of RAKE architectures have been proposed for UWB systems. Comparison between PRake and SRake for pulse position modulation showed that the simpler one, PRake, is almost as good as SRake with a small number of fingers in a Nakagami fading channel [5]. Fractionally-spaced (FS) RAKE receivers for single user DS-UWB systems employing Gaussian monocycles have been studied in [6]. It is shown there that the FS RAKE receiver outperforms chip- and symbol-spaced RAKE receivers at the cost of higher complexity, since it can compensate better for channel distortion. Although, combined RAKE-equalization techniques have been examined in order to alleviate inter-symbol interference (ISI) [7] [8], it was shown that in a UWB system of a single user link, the performance limiting factor in the SNR range of interest is energy capture rather than ISI [9], [10]. In [11], new algorithms for finger assignment are developed which use different selection criteria for assigning the RAKE fingers to reduce the effect of pulse shaping and pulse position modulation in the RAKE receiver performance.

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These algorithms allow the channel paths to be spaced closely, thus improving multipath resolvability. Finally, other RAKE schemes with low complexity combining algorithms include generalized selection combining (GSC) receivers [12], such as absolute threshold GSC (AT-GSC) and normalized threshold GSC (NT-GSC) where the combined paths are determined by the SNR of each individual path. Also, minimum selection GSC (MS-GSC), output threshold GSC (OT-GSC) and minimum estimation and combining GSC (MEC-GSC) schemes have been proposed where the combined paths are determined by the combiner's output SNR [13], [14], [15]. In [16], a low complexity RAKE receiver with group decision general selection combining (GD-GSC) for UWB systems is introduced. This algorithm is based on group sorting and decision tree theory, which divides candidate paths into several groups and selects the best ones from each group.

Despite the aforementioned work in this area, the proposed architectures and algorithms are mostly evaluated using Monte Carlo simulations and theoretical performance studies. In recent literature very few works deal with the architecture and implementation of a RAKE receiver for DS-UWB [17], [18].

In this paper, we propose and implement an efficient architecture for a chip-spaced DS-UWB RAKE receiver subsystem that consists of four parts: the Channel Estimator (CE), the Selection Subsystem (hybrid Partial/Selective - HPSS), the RAKE Receiver (RR) and the RAKE Control (RC). Our method, after performing complete channel estimation (as in SRake), introduces the HPS method to reduce the RAKE receiver fingers by selecting the strongest multipath rays. The proposed algorithm running in the HPS subsystem combines the benefits of both SRake and PRake methods in order to further reduce its complexity. The whole DS-UWB RAKE system is implemented by the use of VHDL language techniques, and it is fully synthesizable, targeting a platform that employs a Xilinx Virtex-4 FPGA [19]. The structure of our design is highly parallel and modular, is optimized for high performance and achieves a clock frequency of over 200 MHz in order to operate at the desired chip rate.

The remainder of the paper is organized as follows: In Section II the transmission model of our system is analyzed, in Section III we describe the architecture of the proposed DS-UWB RAKE and in Section IV we present numerical results on the complexity and hardware utilization of our implementation. Furthermore we give system performance curves and a comparison between three different RAKE implementations. Finally, conclusions are given in Section V.

II. DS-UWB SYSTEM MODEL

In this section the transmission model of the DS-UWB system (Figure 1) is presented in order to better understand the challenges of the architecture of the proposed system.

A. Transmitter

The information bits to be transmitted are generated randomly by a Binary Source at a symbol rate of $1/T_b$ bits/sec, where T_b is the duration of a BPSK symbol. The binary sequence (at point A) is represented by a vector $\boldsymbol{b}$, with elements $\{b_m, m \in (-\infty,+\infty)\}$. After BPSK modulation it becomes $\boldsymbol{d}\{d_m = 1-2b_m, m = \lfloor j/N_c \rfloor \in (-\infty,+\infty)\}$ (at point B) and it is spread by a PN sequence $\boldsymbol{pn}\{pn_n, n = mod(j,N_c) \in [0,N_c-1]\}$ composed of ± 1's, where N_c is the length of the PN code. After spreading, $\boldsymbol{d}$ is transformed to a vector $\boldsymbol{c}\{c_j = d_m \cdot pn_n,\ j \stackrel{\text{def}}{=} (m,n) \in (-\infty,+\infty)\}$, which is generated at a chip rate of $1/T_c = N_c/T_b$ chips/sec (at point C). The spread spectrum processing gain is T_b/T_c.

After the Pulse Shaper filter with impulse response $p_T(t)$ we get a signal (at point D):

$$s(t) = \sum_{j=-\infty}^{+\infty} c_j \cdot p_T(t - j \cdot T_c) = \\ = \sum_{m=-\infty}^{+\infty} d_k \sum_{n=0}^{N_c-1} pn_n \cdot p_T(t - m \cdot T_b - n \cdot T_c) \quad (1)$$

where $p_T(t)$ is the transmitted shaping pulse form with duration T_p and energy E_p.

B. Multipath Channel

The signal $s(t)$ passes through a multipath channel. In this paper we use the high frequency channel model that has been established by the IEEE 802.15.3a standardization group for the evaluation of the performance of different physical layers for high-data rate UWB systems [20]. This model is based on a modified Saleh-Valenzuela channel model [21] for indoor multipath propagation which adopts a cluster-based approach for the multipaths arriving at the receiver. The channel impulse response is expressed as

$$h_i(t) = X_i \cdot \sum_{l=0}^{L} \sum_{k=0}^{K(l)} \alpha_{k,l}^i \cdot \delta\left(t - T_l^i - \tau_{k,l}^i\right) \quad (2)$$

where X_i is a lognormal random variable which represents shadowing, L is the number of observed clusters, $K(l)$ is the number of multipath rays within each cluster, $\alpha_{k,l}^i$ is the gain coefficient of the kth ray of the lth cluster, $\tau_{k,l}^i$ is the delay of the kth ray within the lth cluster, T_l^i is the arrival time of the lth cluster and i refers to the ith realization. The cluster arrival time and the ray arrival time within each cluster are modeled as a Poisson process whereas the coefficients $\alpha_{k,l}$ are assumed log-normally distributed. IEEE 802.15.3a group has suggested four sets of parameters to fit measurement data by considering

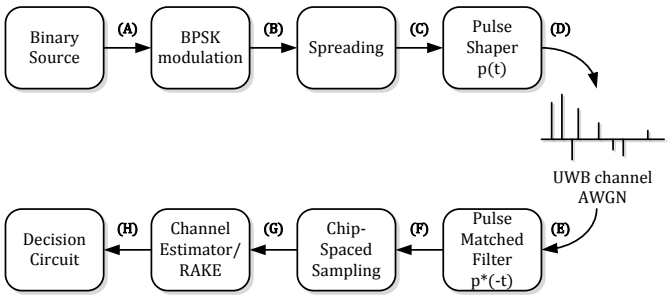

Figure 1. DS-UWB Transmission Model

four channel models (CM) representing different environmental scenarios: CM1 (0-4m, Line of Sight (LOS), CM2 (0-4m, non-LOS (NLOS)), CM3 (4-10m, NLOS) and CM4 (extreme NLOS).

C. Receiver

After passing through the channel, the multipath affected received signal $r(t)$ can be expressed as follows (at point E):

$$r(t) = s(t) * h(t) + n(t) = \\ = X \sum_{j=-\infty}^{+\infty} \sum_{l=0}^{L} \sum_{k=0}^{K(l)} \alpha_{k,l} c_j p_T\left(t - jT_c - T_l - \tau_{k,l}\right) + n(t) \quad (3)$$

where $n(t)$ represents the additive white Gaussian noise (AWGN) at the receiver input, with two-sided power spectral density $N_0/2$ and $*$ denotes convolution.

The received signal goes through a pulse matched filter $p_R(t) = p_T^*(-t)$, $((\cdot)^*$ denotes complex conjugation) (at point F) and after sampling with chip rate $1/T_c$, we get the discrete-time signal (at point G):

$$r_M[\kappa] = \sum_{j=-\infty}^{+\infty} c_j \cdot h_M[\kappa - j] + n_M[\kappa] \quad (4)$$

where $h_M[\kappa] = h_M(\kappa T_c)$ and $n_M[\kappa] = n_M(\kappa T_c)$. Function $h_M(t) = p_T(t) * h(t) * p_R(t)$ includes the effects of the transmitter and receiver filters and the multipath channel impulse response, and $n_M(t) = n(t) * p_R(t)$ is the filtered AWGN. In [8] it has been proven that chip-matched filtering and chip-rate sampling provide close-to-optimum performance.

Signal $r_M[\kappa]$ inputs the RAKE receiver subsystem, where it is delayed by each finger z at u_z chip intervals, it is de-spread and then the selected N_{HPS} taps are combined according to the MRC method. The output of this subsystem is the signal $\hat{d}[m]$ (H):

$$\hat{d}[m] = \sum_{v=-\infty}^{+\infty} d_v \cdot \hat{h}[m - v] + \hat{n}[m] \quad (5)$$

where $\hat{n}[m]$ is the noise sequence at the output of the RAKE receiver and $\hat{h}[m]$ is the symbol time impulse response, given by:

$$\hat{h}[m] = \\ = \frac{1}{N_c} \sum_{z=1}^{N_{HPS}} \tilde{h}_M[u_z] \sum_{n=0}^{N_c-1} \sum_{\rho=0}^{N_c-1} pn_n pn_p h_M[mN_c + u_z + \\ + \rho - n] \quad (6)$$

where N_{HPS} is the number of RAKE fingers assigned to the resolvable multipath rays of $h_M[\kappa]$ which are selected by the HPS algorithm and $\tilde{h}_M$ are the coefficients produced by the channel estimator. Throughout this analysis we assumed perfect timing synchronization.

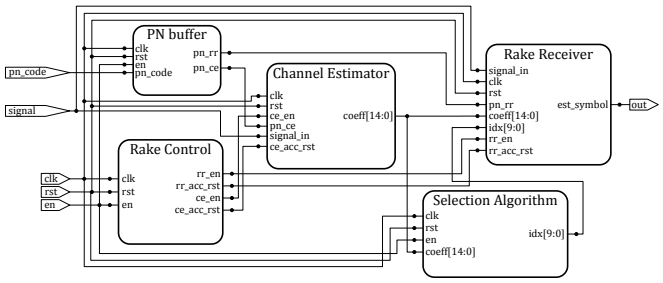

Figure 2. Block diagram of the proposed system architecture

III. System Architecture

The proposed overall architecture of the DS-UWB receiver subsystem is presented in Figure 2. It consists of four different main parts: the RAKE Control (RC), the Channel Estimator (CE), the component that implements the Selection Algorithm (HPSS) and finally the RAKE Receiver (RR). The PN buffer component contains the PN sequence which is fed into the CE and RR. The role of the RC is to synchronize the CE and RR subsystems and determine the exact time of operation for each of them. The complete architecture is entirely designed and implemented using VHDL language techniques in the programming environment of the Xilinx ISE Design Suite 9.2. The design targets a platform that hosts a Xilinx Virtex-4 SX (XC4VSX35) FPGA [19]. For the signal representation we have chosen an accuracy of 8 bits, which is adequate for our application [17].

In the following subsections the three main components of our system are described.

A. Channel Estimator

The CE subsystem produces estimates of the channel impulse response coefficients which are fed into the HPS subsystem. Channel Estimation is performed by using a data-aided approach, in which we assume that each packet begins with N_e known pilot bits. Each of these pilot bits, is chosen to be the PN sequence with the desirable characteristics (low cross-correlation, high auto-correlation values). The CE subsystem correlates the received pilot bits with the local PN sequence and calculates the estimates of the channel coefficients. This sub-optimal but low-complexity algorithm is known as Sliding Window (SW) algorithm and it can be

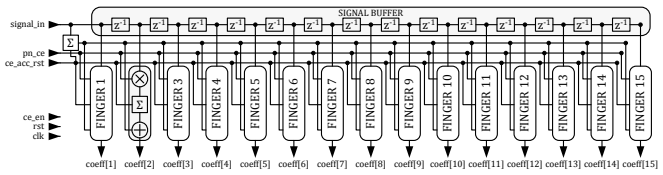

Figure 3. Channel Estimator Subsystem

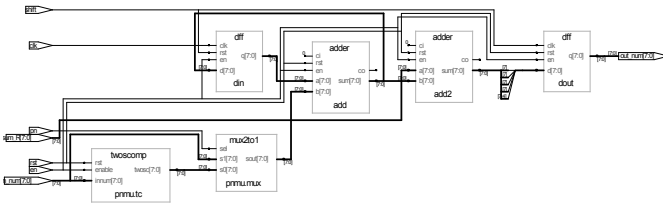

Figure 4. Channel Estimator Finger Implementation

optimum (in the maximum likelihood-ML sense) if the shifted versions of the signal are mutually orthogonal [6]. The channel is assumed to remain constant for the duration of the data packet and the estimated channel coefficients are used for the whole detection process of the data packet. The block diagram for the CE architecture is given in Figure 3. It consists of 15 fingers which compute a corresponding number of estimates. The RTL schematic for the implementation of each CE finger is presented in Figure 4. The PN multiplier is implemented by the use of a multiplexer which selects between the incoming signal and its two's complement. This is followed by an accumulator consisting of an adder and two registers which are synchronized appropriately by the RC component. The adder that follows uses information that comes from an accumulator of the input signal in order to normalize the final output which is the exported estimate of a certain channel coefficient.

B. *RAKE Receiver*

The corresponding block diagram and the RTL schematic of the finger implementation for the RAKE Receiver are shown in Figures 5 and 6, respectively. In Figure 5, we see the full RAKE case where the selection algorithm is not implemented and all of the 15 RAKE fingers are used for the MRC scheme. When the selection algorithm is employed, the RR takes the form of the block diagram shown in Figure 7 which is the proposed HPS implementation. In this case, only 9 of the 15 fingers are implemented in hardware, combining the selected coefficient estimates and the corresponding signals from the Signal Buffer. The information on which signals from the Signal Buffer are chosen, comes from the HPS subsystem in the form of indices that drive certain multiplexers. For example, in Figure 7, fingers 1, 2, 3, 5, 6 and 10 were not selected to participate in the MR combining scheme.

Each RR finger consists of a PN multiplier, an accumulator and a coefficient multiplier. The first two are implemented in the same manner as described above for the CE finger. The final multiplier multiplies the output of the

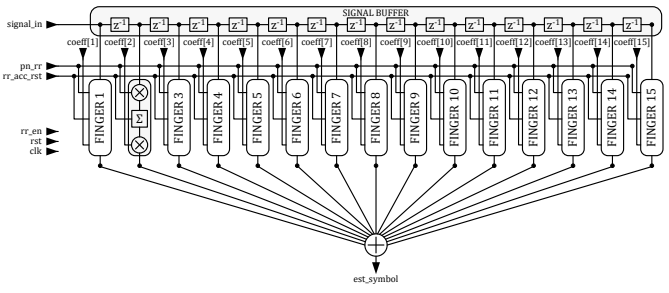

Figure 5. RAKE Receiver Subsystem

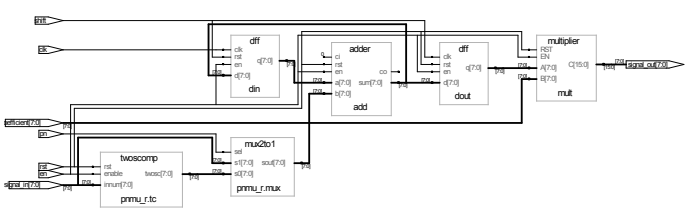

Figure 6. RAKE Receiver Finger Implementation

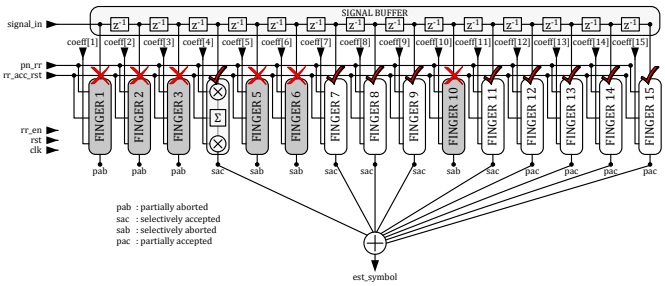

Figure 7. Hybrid Partial/Selective RAKE Receiver Subsystem (example)

accumulator with the corresponding coefficient in order to implement the MRC scheme. The outputs of all RR fingers are summed to obtain the final estimated symbol.

C. *Hybrid Partial/Selective Sybsystem*

The HPS subsystem employs the CE coefficient estimates and selects the strongest of them. The proposed HPS algorithm minimizes the complexity by reducing the channel coefficients' estimates that participate in the selection process. This algorithm exploits the fact that, with great certainty the first multipath components will be strong enough to be selected by the sorting algorithm, while the multipath components at the tail of the channel impulse response are so weak that the probability of being selected is very low. This assumption can be adopted owing to the fact that the channel model has a power delay profile (PDP) that is exponentially decaying. For that reason, we partially select a number of the channel coefficients' estimates that correspond to the first arriving multipath components of the channel and partially abort the estimates that correspond to the latest arriving multipath components. An example of this procedure is shown in Figure 7, where four channel estimates were partially accepted and three of them were partially aborted. Consequently, eight of the CE exported estimates participate in the selection process, among which five are finally selected (selectively accepted) and three are aborted (selectively aborted). That way, the Selection Subsystem's complexity can be reduced significantly as it will be shown numerically in the next section.

The implementation of the proposed Selection Subsystem (HPSS) is based on a modified version of the bubble sorting algorithm written in VHDL language. This algorithm suits well in our application because we do not desire full sorting of the input coefficients but only a certain number of the strongest coefficients. Thus, in our example, the main loop of the algorithm runs only five times, instead of eight, leading to a very low complexity implementation. The synthesis tool translates optimally the algorithm into a set of comparators and multiplexers. The RTL schematic is not shown here because of its visual complexity.

The HPS subsystem exports the indices of the nine partially and selectively accepted estimates that are used by the RR subsystem, which is now implemented by employing only nine fingers instead of fifteen.

TABLE I. RESOURCE UTILIZATION

Resource Utilization Virtex 4 (XC4VSX35)							
Feature	***Available***	***Full RAKE***	***%***	***SRake 9 fingers***	***%***	***HPS RAKE***	***%***
Slices	15360	1181	7	2701	17	1349	8
Flip Flops	30720	1799	5	1463	4	1463	4
4 input LUTs	30720	1416	4	4494	14	2284	7
IOBs	428	159	35	195	43	195	43
GCKLs	32	5	15	5	15	5	15
DSP48s	192	15	7	9	4	9	4

IV. NUMERICAL RESULTS

Table I summarizes the resource utilization for three cases. The first case is the full RAKE where 15 fingers are used in the MRC combining without any selection process. We can see that 15 DSP48s, which contain multipliers, are necessary in this case. In the second system, a selective RAKE (SRake) which chooses 9 out of 15 fingers is evaluated. The selection algorithm acts upon 15 inputs and outputs the 9 best of them. In this case the number of DSP48s is reduced to 9 since only 9 RAKE fingers are implemented in hardware, but the number of slices and LUTs is increased because of the subsystem that implements the selection algorithm. In the third case, we have the proposed hybrid PS RAKE system. The number of DSP48s is 9 again but with this compact method, the number of slices and LUTs is comparable to the full RAKE case. All of the three systems have a maximum clock frequency of over 200 MHz which is the target chip rate.

Figure 8 shows the simulation results for the performance of our system. It is proven that the performance of the HPS RAKE is comparable to that of the Full RAKE with 15 fingers and the simple Selective RAKE (SRake) with 9 fingers, so it can be claimed that the proposed HPS algorithm provides a good alternative to a Selective or Partial RAKE receiver structure achieving a compact implementation without compromising on the performance. The rest of the curves represent the performance of a Selective RAKE (SRake) receiver that chooses the strongest 12, 6 or 2 out of the 15 available estimates of the channel coefficients. All simulations were run for the channel model CM4 which is the extreme NLOS environmental scenario. In this point it should be noted that for a RAKE system with much more fingers it is expected that the proposed HPS algorithm will provide a much better tradeoff between hardware complexity and full RAKE performance.

V. CONCLUSION

In this paper, the design and implementation of a DS-UWB RAKE receiver employing a Channel Estimator and a Selection Subsystem is presented. The Selection Subsystem is based on the proposed hybrid Partial/Selective RAKE algorithm that combines the benefits of both Partial and Selective RAKE schemes. The objective of the proposed architecture is to reduce the number of RAKE fingers and consequently hardware complexity without sacrificing the performance of the receiver. The structure of the implemented system is highly parallel and modular, and optimized for high performance. The VHDL implementation of the proposed system compared to those of different architectures such as Full RAKE or Selective RAKE appears to provide compact hardware utilization. Furthermore, BER curves are provided demonstrating a performance which is very similar to the Full RAKE scheme.

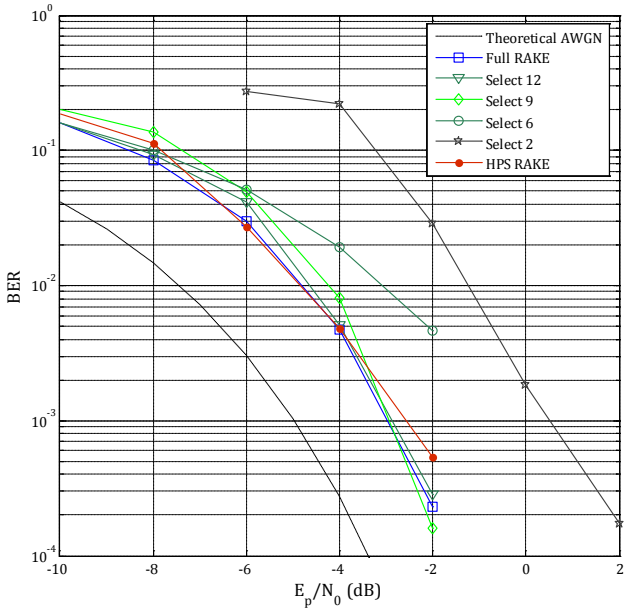

Figure 8. BER performance of the proposed HPS RAKE receiver

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