Design and Implementation of High Speed Sense Amplifier for SRAM

PULLAREDDY. A, G.SREENIVASULU
Dept of Electronics and Communication Engineering
Sri Venkateswara University College of Engineering
Tirupati, Andhra Pradesh, INDIA

Abstract: The Sense amplifier's sense delay is one important parameter to measure the speed of SRAM memory cell. The sense delay depends on the amplifier reaction time. This delay parameter is more vulnerable to device variations, temperature and supply voltage variations. A latch type voltage controlled sense amplifier considered among all the offered current and voltage sense amplifier types for data sensing from the SRAM cell. The modified conventional latch type voltage controlled coupling capacitor based sense amplifier is implemented to improve the performance of the memory cell. The proposed circuit scheme will provide the reasonable negative voltage at the sense amplifier virtual ground, then the driving capability of the pull down (NMOS) transistors is increased, hence it made the sense amplifier faster. The conventional sense amplifier is compared with proposed coupling capacitor sense amplifier. From the experimental results, it is observed that coupling capacitor based sense amplifier circuit scheme will decrease the sense amplifier reaction time and access the data fast. The result shows, the proposed scheme provides the improvement of sense delay reduction of 198ps at SS/-40^{o}C/1.2v and 18ps at FF/127^{o}C/1.2v process corners at the cost of power consumption.

Keywords: Coupling Capacitor, SRAM cell, Offset, Reaction time.

1. Introduction

In present day microprocessors are having more than 50% of the chip size is used for cache memory. The design of on-chip caches with faster and larger size continues to be increasingly essential for high-speed processors. Sense delay indicates the overall latency of the caches. So, the schemes which are improving the sense delay of the circuit is crucial in the design of high-performance caches. Due to the high array efficiency and robustness design, traditional small data sensing schemes are widely used for static memory designs. As the technology scaling increases continuously, it has become hard for on chip memories to maintain the tendency of the delay reduction with the speed of present processors logic. The cache memories are static random access memories (SRAM). The larger memory design is built by the small SRAM memory blocks [1]. But the structure of SRAM cell is fixed due to the limitation of technological level, so the performance improvement of the SRAM mainly depends on peripheral circuits [2].

The sense amplifier circuit is one part of SRAM memory and its design has the benefits of low power consumption, fast data access, robust design and is now broadly used in portable devices [3-4] too. The sense amplifier will play an important role during the memory read operation. It is utilized to get the data from the selected SRAM cell of the memory array by sensing and amplifying the small differential voltage or current is developed among the bit lines. Due to the large cell resistance and bit line capacitance these differential voltage or currents are small [5]. Hence, small output energy levels of the cell at read operation. Therefore the use of sense amplifier will provide the required voltage or current output logic levels and also improves the speed of the memory. During the operation of the sense amplifier, the content of cell node data should not disturb. However, due to the time variation of bit line charging and discharging and large capacitive loads, the design of the high-speed sense amplifier is most important for high-performance SRAM memory designs [6]. Optimum bit line differential voltage may play an important role, building bit line differential voltage takes a large time to discharge due to

the huge bit line capacitance. Considering less differential voltage leads to speed up memory, but may cause a problem during the read operation, so optimal value should be taken.

Technology scaling reduces chip cost, but increases uncontrollable device variations. Sometimes variations in device significantly decrease the worst case read current and increase the worst case sense amplified differential requirement for successful sensing of the data without penalizing cycle time. The proposed capacitive coupling based circuit scheme, which compensates the loss of the differential because of the device variations and/or because of the relative mismatch between the timing of the SAE (sense amplifier enable) signal and the generation of the required differential on the bit-lines and subsequently on the internal nodes of sense amplifier across the PVT (Process, Voltage and Temperature) corners.

The remaining sections are organized as follows. Section II: deals with the conventional sense amplifier. Section III: provides the proposed new sense amplifier circuit technique. Section IV: Discusses the simulation results carried out using the Cadence virtuoso tool.

2. SRAM Architecture

SRAM memory contains an array of SRAM cell (6T SRAM) and peripheral circuits. A typical column of the SRAM array contains the following circuits [7]: 6T SRAM cells, row and column decoder circuits, write driver, sense amplifier and pre-charge circuit as shown in Fig. 1. The SRAM cell is the main part of the memory array, it is composed of two back to back connected inverters (N1-P1,N2-P2) with two access transistors (N3, N4) connected to paired bit-lines (BL, BLB) as shown in Fig. 2. Both N3 and N4 MOS transistors are directly connected to the word line to perform the access write and read operations through the bit lines.

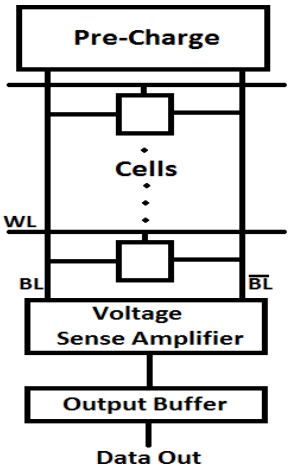

Figure 1. Column circuit of SRAM Array

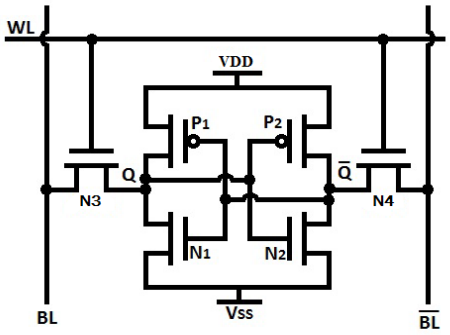

Figure 2. 6T SRAM cell

With the pre-charge circuitry the bit lines (BL, BLB) are pre-charged to the equal voltage levels before each read and write cycles. When 'pre' goes to low then the bit lines are pre-charged to VDD levels as shown in the Fig. 3. The transistor P3 provides the same voltage levels to the both BL and BLB.

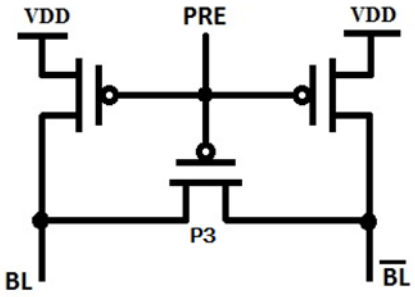

Figure 3. Bit line precharge circuit

The write driver circuit is used to write a data value to the SRAM cell and it is directly connected to the bit lines. The row and column decoder circuits are used to select a memory

location which is to be read/write. The functionality of the sense amplifier circuit is to amplify small signals to full swing [8]. In the coming sections will explain the classification of sense amplifiers with respect to their mode of operation and significance of their role in the SRAM read operation.

2.1 Conventional sense amplifiers

Sense amplifiers are mainly classified into two categories. Differential and non-differential sense amplifiers, these differential sense amplifiers can be also known as voltage mode, current mode and charge transfer sense amplifier [9]. The voltage mode sense amplifiers are having both static designs and dynamic designs. Static designs are latch based and it measures the differential voltage between the bit lines and sense that output. Dynamic designs are constantly monitoring the difference between the bit lines and set their output accordingly [10]. In SRAMs, the latch type sense amplifiers are chosen because as they achieve fast sensing because of the presence of strong positive feedback [11]. In the memory read operation the SRAM cell nodes are directly connected to the bit lines. Due to the cell node voltages one of the bit lines start to discharge through bit cell, so some differential voltage will produce across the bit lines and it will determine the output logic value. This differential voltage strongly affected by the bit line capacitance (C_{bit}), supply voltage and the process variations. The performance of the sense amplifier will depend on the differential voltage [12]. If it is too large then the required differential voltage can't be generated for enabling the sense amplifier, so it leads to readability failure.

A conventional latch-type sense amplifier is shown in Fig. 4. It consists of two cross couple inverter pairs (M1-P1, M2-P2) with positive feedback connection to amplify the differential voltage developed by the bit lines [13]. The basic variation of the latch based sense amplifier involves the addition of decoupled pass transistors (DC-PMOS) i.e. DCL and DCR transistors depicts in the Fig.4. The advantage of adding pass transistor is it effectively decouples the amplifier inputs and outputs from the bit lines. When the SRAM cell in the read mode, both the bit lines are pre-charged, if we supply the sense amplifier enable signal to low (SAEN is low), then both DCL and DCR pass transistors are switched ON and M3 is OFF, due to this some differential voltage is established across the bit lines, at the same time the sense amplifier output nodes are charged to bit line voltages. When required differential voltage is reached, then SAEN signal goes to high and transistors M3 switched ON and transistors DCL and DCR are OFF, the functionality of the sense amplifier will start. Because of the pass transistors (DCL, DCR) are OFF the bit lines are decoupled from the sense amplifier nodes, so any changes in bit line voltage will not affect the read operation. The read outputs are measured at sense amplifier nodes, i.e. SO_0 or SOB_0. It can be observed in experimental waveform as shown in the Fig 7. Due to process variation [14], a possible scenario has been occurring, when the SRAM cell being in read mode, the worst, i.e. least read current, so the slowest discharge rate of the bit-lines, SAEN path happens to be fast, with respect to differential voltage generation on bit-lines going to sense amplifier and sense amplifier happens to be the worst i.e. having maximum differential voltage (offset) requirement. This implies, effective differential of the sense amplifier internal nodes is very less. This increases the sense amplifier reaction time. The cause of increasing the reaction time is the driving capability of the MOS transistors M1 and M2 is very less when low differential voltage is applied to the sense amplifier internal nodes from the bit line.

3. Proposed Sense Amplifier

In order to reduce the sense amplifier reaction time, a modified conventional type sense amplifier is being proposed as shown in Fig.5. The sense amplifier virtual ground is represented as VS1, which is responsible for the enhancement of sense amplifier reaction time. The unique feature of the design approach is: (1) capacitive coupling based transient negative VS1 voltage generation circuit. (2) Easy to integrate with available sense amplifier circuit. Here we inserted the odd number of inverters for delaying the signal from SAEN to coupling capacitor one end node.

To gain a substantial amount of dip at VS1 node, the negative coupling at the VS1 node should occur when VS1 node has already reached to the minimum possible level. To

achieve the stated requirement, a chain of an odd number of inverters and a capacitor has been put between SAEN and VS1 nodes. The inverter chain delays the SAEN signal to reach one end of the coupling capacitor node and improves the coupling voltage. The circuit operation illustrated in Fig. 5 is when SAEN going high, the sense amplifier virtual ground node VS1 starts discharging and reaches to minimum voltage. Due to inverter delay, one end of the capacitor goes low with high ramp and couples with VS1 provides extra drive for NMOS transistors M1 and M2, i.e. the gate to source voltage of NMOS transistors increases, which decreases the sense amplifier reaction time and makes the sense amplifier faster [15].This will leads to a small differential voltage is required between the bit lines for quick operation of the sense amplifier. This capacitive coupling based circuit scheme, which compensates the loss of the differential because of the device variations and/or because of the relative mismatch between the timing of the sense amplifier enable signal and the generation of the required differential voltage on the bit-lines and subsequently on the internal nodes of sense amplifier across the PVT corners.

4. Results and Discussion

The 6T SRAM cell write operation simulation waveform as shown in the Fig 6. When the wordline is enabled the data from/to the cell is accessed for read/write operation through the bit lines. If write enable (WE) is high, then the data input (Din) is written into the memory cell.

The simulation waveform of SRAM cell read operation as shown in the Fig 7. It illustrates the sense amplifier reaction time improvement of the SRAM in the read operation. Before the read operation begins, the bit lines are pre-charged to VDD. During read operation the word line (WL) goes to high, according to data available at cell nodes one of the bit line (BL_1/BLB_1) starts discharging, Therefore, some differential voltage developed across the bit lines, when required differential voltage is reached it will turn on the sense amplifier (SAEN goes high).Therefore the data is identified at the sense amplifier nodes. From the Fig 7, the sense amplifier output signals are denoted as SO/SOB (SO_0-conventional, SO_1-proposed) and virtual grounds are VS/VS1 (VS-conventional, VS1-proposed).

When SAEN going high, VS and VS1 nodes starts discharging, due to coupling capacitor effect the VS1 nodes quickly reaches to below the ground (negative voltage), this will provide the extra drive to NMOS transistors (N1,N2) which makes the sense amplifier faster.

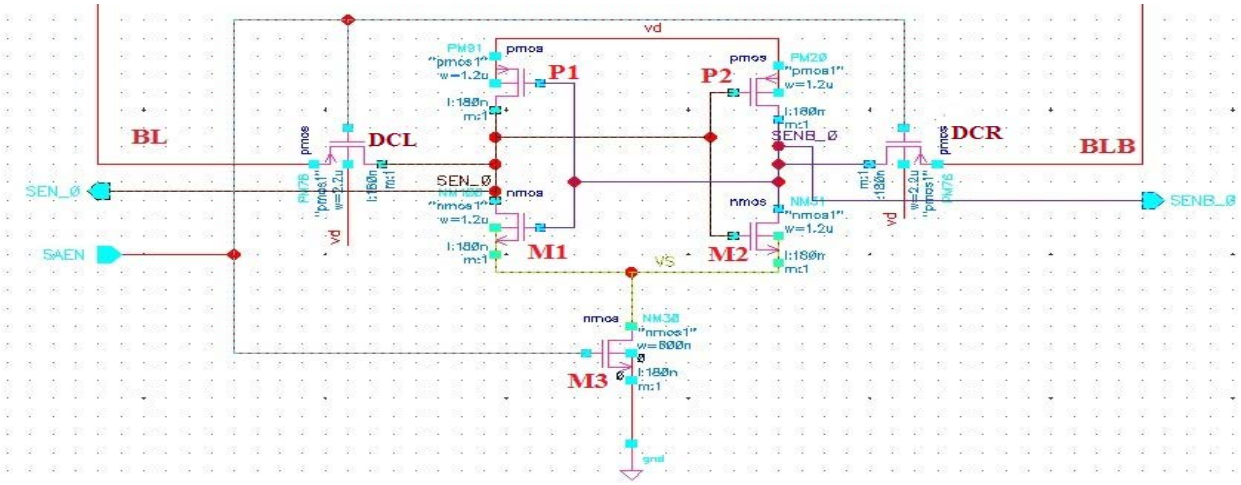

Figure 4. Conventional Sense Amplifier Circuit

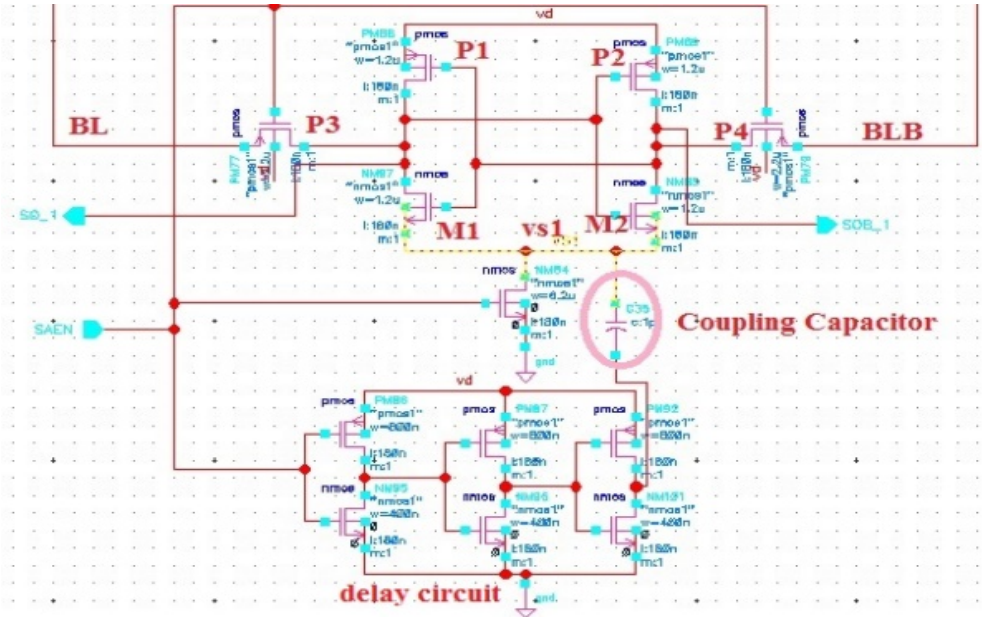

Figure 5. Coupling capacitor based sense amplifier

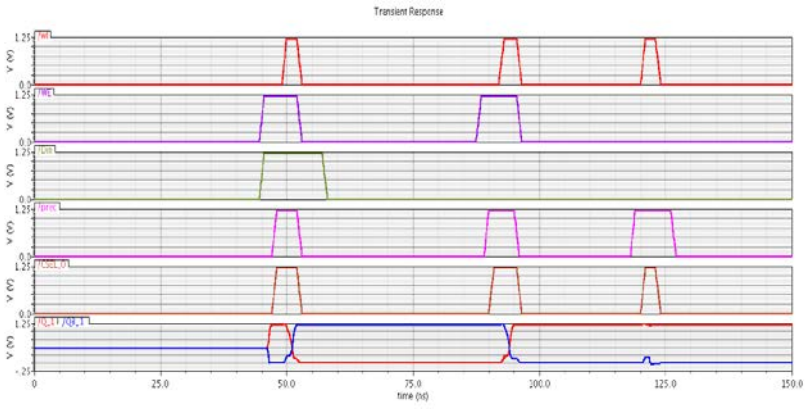

Figure 6. Simulation waveform of SRAM cell write operation

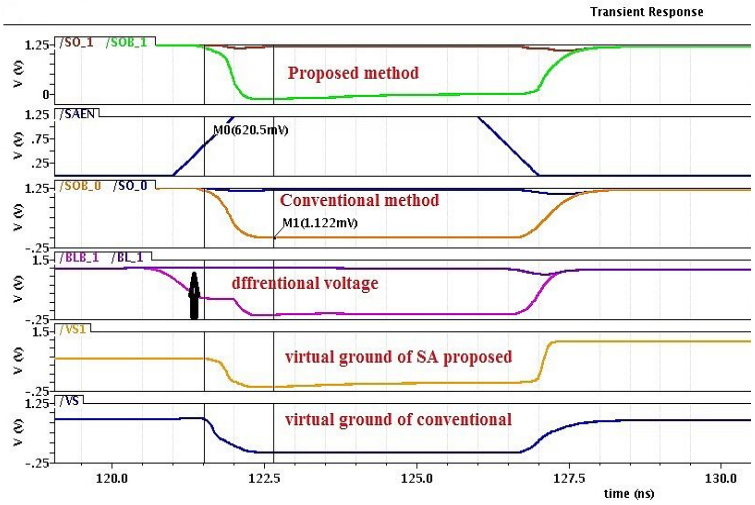

Figure 7. The simulation waveform for proposed and conventional sense amplifier read operation

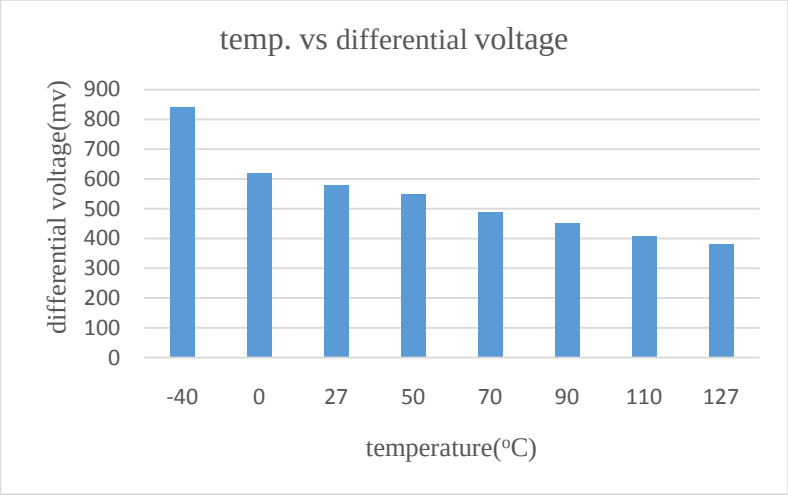

Figure 8. Temperature impact on bit line differential voltage

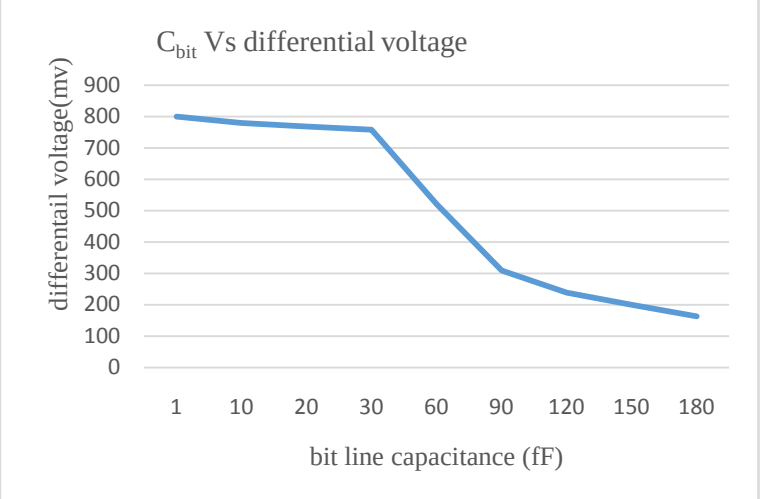

Figure 9. Impact of bit line capacitance on generation of differential voltage

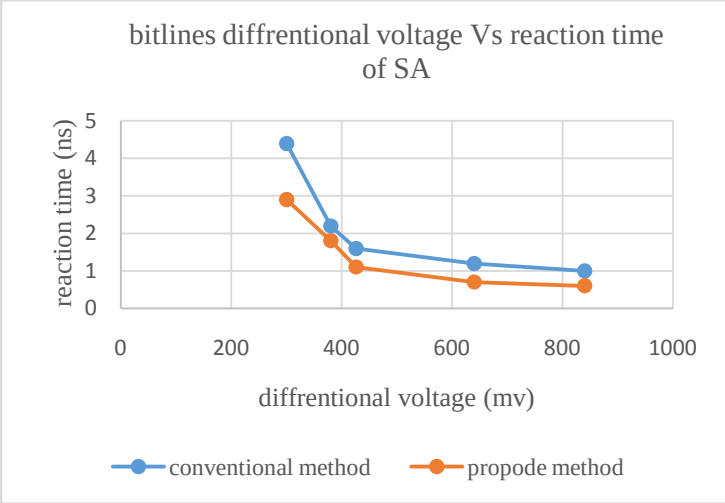

Figure 10. Comparison graph of the convention and proposed SA read operation

4.1 Effect of temperature on sense delay

Fig. 8 depicts the impact of temperature on differential voltage built by the bit lines. It shows that as the temperature increases the differential voltage rapidly decreases and the data sensing delay of the sense amplifier is increases this will leads to decrease the performance of the SRAM memory cell.

4.2 Effect of bit line capacitance on sense delay

In the SRAM cell read operation the bitline capacitance will also showan important role and it defines the access delay. As the bit line capacitance increases, then the differential voltage developed between the bit lines is decreased, it is observed in the Fig. 9. Hencethe speed the memory cell is decreased. The impact of bit line capacitance on the sense delay is observed at 1.2v supply voltage and it was found that sense delay is proportional to the bitline capacitance.

The sense amplifier reaction time at various bit line differential voltages are measured and drawn as shown in the Fig. 10, it is observed that the proposed coupling capacitor based sense amplifier provided the fast reaction time compared to conventional type sense amplifier. As the bit lines differential voltage decreases the sense amplifier reaction time will increase, it leads to slow read operation.It is also found that the coupling capacitor based sense amplifier circuit provides the better improvement, even at small differential voltage is produced across the bit lines. The comparison of SRAM cell read delaywith different supply voltages is summarized in Table 1, (See Table 1 in the APPENDIX at the end of the article). The result shows, the proposed scheme providesthe gain of delay reduction of 3.4psat 1.2v, 148ps at 0.9v of supply voltage.

The memory cell read delay is examinedand summarised in Table 2 , (See Table 2 in the APPENDIX at the end of the article). at the SS (Slow PMOS, Slow NMOS) and FF (Fast PMOS, Fast NMOS) process corners. It is observed that coupling capacitor sense amplifier in the SS model at -40°C and FF model at 127°C operated at 1.2v provides faster data access compared to a traditional sense amplifier.

5. Conclusion

This paper presented a new design of coupling capacitor based sense amplifier for the improvement of sense amplifier reaction time in SRAM read operation. During the memory read operation the proposed circuit scheme provided the required negative voltage at the sense amplifier virtual ground, then the driving capability of the sense amplifier's pull down

NMOS transistors is increased, hence it reduces the reaction time and it made memory faster. The impact of temperature on differential voltage is analysed and plotted the graph. The dependency of the sense amplifier reaction time on bit line differential voltage is observed. We compared the proposed circuit scheme with conventional method, therefore,the proposed scheme provides the improvement of delay reduction of 198ps at SS/-40°C/1.2v and 18ps at FF/127^{o}C/1.2v process corners at the cost of power consumption of the SRAM cell in the read operation. The experimental results are measured across the PVT.

References

[1] Rakesh Oayaramji Chandankhede, et al., "Design of High Speed Sense Amplifier for SRAM", IEEE International Conference on Advanced Communication Control and Computing Technologies (ICACCCT), 2014, pp.340-343.

[2] T. seki, E. Itoh, C. Furukawa, I. Maeno, T. Ozawa, and H. Sano, "A 6-ns 1-Mb CMOS SRAM with Latched Sense Amplifier", IEEE Journal of Solid-State Circuits, vol. 28, pp. 478-483, 1993.

[3] Manoj Sinha, et al., "High Performance and Low Voltage Sense Amplifier Techniques for sub 90nm SRAM", SOC Conference Proceedings. IEEE International, 2003, pp.113-116.

[4] Chow H C and Chang S H, "High Performance Sense Amplifier Circuit for Low Power SRAM Applications", IEEE ISCAS, 2004, pp.741-744.

[5] Anil Kumar Gundu, Mohammad S. Hashmi and Anuj Grover ,"A New Sense Amplifier Topology with Improved Performance for High Speed SRAM Applications", 29th International Conference on VLSI Design (VLSID), 2016, pp.185-190.

[6] Taehui Na, S. Woo, J. Kim, H. Jeong, and S. Jung, "Comparative Study of Various Latch-Type Sense Amplifiers", IEEE Transactions on VLSI Systems, vol. 22, no. 2, pp. 425-429, Feb. 2014.

[7] Y. Tsiatouhas, A. Chrisanthopoulus, G.Kamoulakos, and T. Haniotakis, "New Memory Sense Amplifier Designs in CMOS Technology", IEEE International Conference in Electronics and Circuits System, Feb. 2000, pp. 19–22.

[8] R. Singh and N. Bhat, "An Offset Compensation Technique for Latch type Sense Amplifiers in High-Speed Low-Power SRAMs", IEEE Transactions on Very Large Scale Integration (VLSI) Systems., vol. 12, no. 6, pp. 652–657,Jun. 2004.

[9] B. Mohammad, P. Dadabhoy, K. Lin, and P. Bassett, "Comparative Study of Current Mode and Voltage Mode Sense Amplifier Used for 28nm SRAM", 24th International Conference in Microelectronics (ICM), 2012, pp.1-6.

[10] B. Wicht, "Current Sense Amplifiers for Embedded SRAM in High-Performance System-on-a-Chip Designs", Springer Series in Advanced Microelectronics. Springer, vol. 12, 2003.

[11] Bhupendra sing Reniwal, et al., "Ultra-Fast Current Mode Sense Amplifier for Small ICELL SRAM in FinFET with Improved Offset Tolerance", International Journal of circuits and syst. signal process,Springer, vol.35,2016.

[12] WA. J. Bhavnagrwala, X. Tang, and J.D. Meindl, "The Impact of Intrinsic Device Fluctuations on CMOS SRAM cell Stability," IEEE Journal of Solid-State Circuits, vol. 36, no. 4, pp. 658–665, Apr. 2001.

[13] Mahmut E. Sinangilc, et al., "A 28 nm 2 Mbit 6 T SRAM With Highly Configurable Low-Voltage Write-Ability Assist Implementation and Capacitor-Based Sense-Amplifier Input Offset Compensation", IEEE Journal of Solid-State Circuits, vol. 51, Issue:2, pp.1-11, 2015.

[14] W. David, "Sense Amplifier having Reduced Vt Mismatch in Input Matched Differential Pair," U.S. Patent 6445 216, Sep. 3, 2002.

[15] M. J. M. Pelgrom, A.C. J.Duinmaijer, and A. P. G. Welbers, "Matching Properties of MOS Transistors," IEEE Journal of Solid-State Circuits, vol. 24, no. 5, pp. 1433–1440, Oct. 1989.

APPENDIX

Table 1. Comparison table of memory cell read delay

Technique	Read delay (ps)		
	Vdd=1.2v	Vdd=1v	Vdd=0.9v
Conventional Method	224.8	484.4	682.4
Proposed Method	221.4	364.4	534.0

Table 2. Comparison table of memory cell read delay at process corners

Process Corner	Read delay(ps)	
	Conventional Method	**Proposed Method**
SS/-40°C/1.2V	611.4	413.7
FF/127°C/1.2V	161.1	143.5