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Design and implementation of multiple output forward converter with Mag-amp and LDO as post regulators for space application

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Abstract

Linear power supplies are commonly used power supplies for many applications. They have some drawbacks such as low efficiency, difficulty in thermal management and also in regulation of the output voltage. Some of these drawbacks can be overcome by Switch Mode Power Supplies (SMPS). One of the best-suited applications of SMPS is for space applications that require power supplies which are lighter, smaller, more efficient and highly reliable. Multiple-output DC-DC converters are an important topology of SMPS that can be used for space applications. But, in multiple output converters usually, only the master output is regulated and the other outputs are left unregulated and this can result in cross-regulation. In this paper, post regulators such as Magnetic amplifiers (Mag-amp) and Low DropOut regulator (LDO) are proposed to regulate each output and also to improve load regulation. In addition to this, the input voltage feed-forward control technique is proposed to control the duty cycle of the switch, which is dynamically faster and provides better line regulation when compared to the voltage feedback controller. Besides, over current protection circuit for the converter is discussed in detail.

Keywords: Cross regulation effect, Mag-amp and LDO, multiple output forward converter, output over current protection, voltage feed forward control.

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1. Introduction

In space missions power electronic circuits are widely used in areas of power management, power conditioning, and control systems. The power supply systems for deep space missions are to be designed such that they are reliable and operate efficiently under extreme temperatures. The power supply is an interface between electric power and electric load, which are usually classified as linear power supplies and switched-mode power supplies. There are many basic topologies used in power supply design (Hart, 2010). Among various isolated converters, the Forward converter has many advantages over other topologies because it is more energy-efficient and used in applications requiring comparatively higher output power. The proposed converter consists of three outputs, wherein one output will be master output, that is, the highest output voltage among the three outputs. The closed-loop is provided to the master output and hence its voltage is maintained constant under varying line and load regulations. But the other two outputs are slave outputs and are in open loop and left uncontrolled. The variation of slave outputs in open-loop

due to the changes in master output or due to changes in the slave circuits is called cross-regulation effect (Cash, 1991). This can be overcome by the use of post regulators like Mag-amp and LDO regulator, where the selection of post regulators will be based on the output current. If the output current is less than 1.5A the linear regulators like LDO regulators are used as post regulators and if the current is more than 1.5A then Mag- amps are used as post regulators (Nabeshima *et al*., 1985; Cash, 1991).

The PWM technique for the proposed converter is the voltage feedforward control technique (CS51220 datasheet, 2002). Conventional Voltage mode control includes feedback and possesses a poor line transient response. Current mode control technique has better transient response but it is complex to design due to the presence of two loops. Also, exclusively post regulated output with voltage feed-forward control gives more reliable performance (Bhat *et al*., 2016).

Protection circuits are the most important parts of the power supply unit. In the proposed converter the output overcurrent protection is provided in addition to input under-voltage and output over-voltage protection. If the output current exceeds 125% of the desired output current, then the protection circuit gets activated thus the converter gets shutdown and protects the power supply unit from major failure. The Mag-amps works on the principle of core saturation. These are saturable inductors; when the core reaches the saturation level the complete voltage appears across the mag-amp coil and drops to zero and carries the total current. When unsaturated, the coil blocks the full voltage and no current flows through it. Magnetic amplifiers as post regulators are very effective to regulate the output voltage on the secondary side and are easy to use (McLyman, 1993). An LDO regulator is a simple and cost-effective voltage regulator to obtain a regulated output voltage from a higher input voltage. LDO takes in a variable input voltage and provides a continuously controlled, steady, low-noise DC output voltage.

The sudden spikes in the output voltage due to input line voltage changes can be reduced. To achieve better line regulation, the PWM controller should be made to respond to input line voltage instantaneously and vary the duty cycle following the input voltage. This can be obtained by voltage feed-forward technique. In this technique whose slope varies following the input voltage is implemented instead of fixed slope ramp. This provides great line regulation and excellent response. The output overcurrent protection is required to protect the converter components and load, from an abnormal condition that lead to a large current. The fundamental principle of overcurrent protection is that the current is sensed by a current sensing element like a resistor and subsequently it is compared with the reference current. If the sensed output current is more than the reference current, then the turn OFF command is sent to the PWM IC and the converter gets shutdown.

This paper proposes Mag-amp and LDO post regulators for a forward converter designed to provide three outputs as per the specifications. The input voltage feedforward technique is used to improve the line regulation. The details about the proposed regulators and the results obtained are discussed in the following sections. The paper is organized as follows: In Section 2, the circuit and specifications of the forward converter are provided. Section 3 discusses the Low Dropout Regulators and Section 4 discusses Mag-amp as post regulator. In Section 5, the design details of hardware implementation are shown. Section 6 briefs about the voltage feed-forward network with certain equations. In section 7, overcurrent protection circuit is discussed. Section 8 discusses the simulation results and in Section 9, the experimental results are presented. Finally, the conclusion is made in Section 10.

2. 2. Circuit and Specifications of Forward Converter

The block diagram of the proposed converter is as shown in Figure 1, and the specifications of the same are as shown in Table 1. The expected voltage and current outputs and also the limit for the line regulation, load and cross regulations are listed in Table 1. In the circuit, isolation is provided between the primary and secondary winding through the transformer. When an input voltage is applied across the primary winding of the transformer and the switch (Q) is closed, the primary current begins to flow. A voltage appears across the secondary winding due to the dot polarity of the transformer and energy is transferred from primary to secondary. The diode D1 becomes forward biased when the switch is ON and the transformer secondary voltage develops across the low pass filter constituted by L1 and C1, and the output is delivered to the load. The Diode D2 is turned OFF during this period.

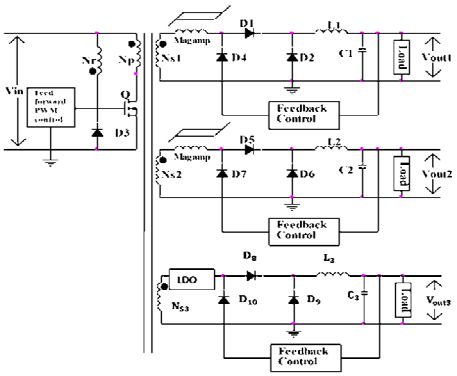

Figure 1. Proposed three output forward converter with post regulators

Table 1. Specifications of the designed converter

Parameters	Range
Minimum Input voltage $V_{in_{\min}}$	24V
Nominal Input voltage $V_{in_{nom}}$	28V
Maximum Input voltage $V_{in_{\max}}$	36V
Number of outputs	3
Output-	5.3V/12A
Output-	5.4V/4.5A
Output-	-5V/0.7A
Total output power P_{out}	92.6watt
Efficiency	≥70%
Line regulation	1%
Load and cross regulation	2%
Switching frequency F_{sw}	140kHz
Input under-voltage protection	< 22.6V
Output over-voltage protection	110% of the output voltage
Output over-current protection	125% of the output current
D_{max}	0.4

As the input power is carried to the load, this mode is stated as powering mode of the Forward converter. Diode D3 is reverse biased and remains OFF due to its opposite dot polarity. The freewheeling mode begins during the OFF condition of switch Q. The continuous current is maintained by the filter inductor on the secondary side and it supplies to the load through the freewheeling diode D2. The forward diode D1 remains OFF during this mode and the Diode D3 conducts due to the opposite dot polarity of reset winding(Nr) and primary winding(Np) as shown in Figure 1. Hence the magnetizing current flows in the reverse direction and resets the core.

3. Low Dropout Regulator (LDO)

Low Dropout Regulators are used as linear post regulators that can regulate even when the supply is close to the output. The circuit of the Linear Drop Out regulator is shown in Figure 2. The desired output can be found by using the Equation (1).

$$V_{OUT} = V_{IN} - V_{DROP} \tag{1}$$

where V_{OUT} is the desired output, V_{IN} is the input voltage and V_{DROP} is the dropout voltage

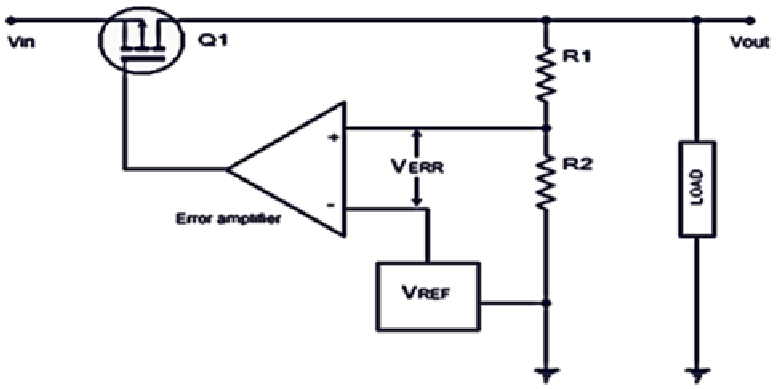

Figure 2. Low dropout regulator

A low dropout regulator consists of an error amplifier and PMOS transistor between V_{IN} and V_{OUT}. The output voltage V_{OUT} is scaled down by the voltage divider R1, R2 and compared to the reference voltage V_{REF}. The minimum potential difference necessary to achieve stable transistor operation is called the dropout voltage. In this case $V_{OUT} + V_{DROP}$ is the minimum operating voltage. In this proposed work, Output-□ of the Forward converter as specified in Table 1 is derived from a LDO regulator and is obtained practically by reversing the voltage measurement terminals on the load side of the converter and is calculated by using Equation (2).

$$-5\ V = -5.4\ V + 0.4\ V \tag{2}$$

4. Mag-amp regulators

In this proposed work, Mag-amp is proposed as post regulator for Output-□ and Output-□ of Forward converter as specified in Table 1. Mag-amp is actually a saturable inductor. The principle and operation of Mag-amp can be discussed using a simple LR circuit as shown in Figure 3 (Bhat et al., 2016).

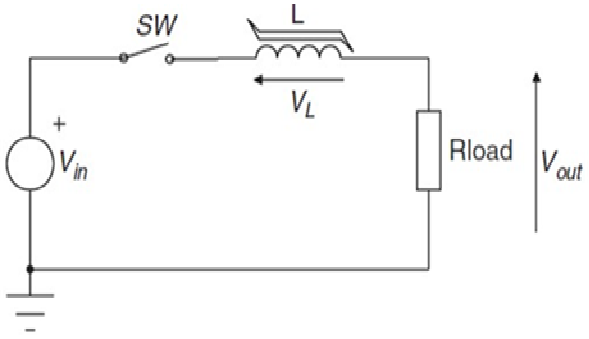

Figure 3. Mag-amp equivalent circuit

Mag-amp works on the principle of core saturation. It operates in two modes: during mode 1 the switch is open, hence, no saturation current flows through the circuit due to which the does not get saturated and it offers maximum inductance. Hence full resistance is offered to the load, thus, no current flows to the output. Similarly, during mode 2 the switch is closed, hence the full saturation current flows through the core which leads to the core saturation and makes the inductance zero. Hence, the inductance coil just acts as a short circuit and no resistance is offered to the load therefore full current flows to the output.

5. Design details for Hardware implementation

The following sections discuss the design details corresponding to Output I of the Forward converter as specified in Table 1. For the other two outputs (Output II and Output III) the same design procedure is followed.

5.1 Design equations and Filter Design for Output-□ (McLyman, 1993)

The duty cycle range and the expected input current drawn by the converter is calculated by considering maximum duty cycle (D_{max}) and minimum obtainable efficiency, η equal to 70% as specified in the Table 1. The values for all other parameters in Equations (3) to (11) are specified in Table 1. The minimum duty cycle is calculated by using output voltage gain equation as below.

$$D_{\min} = D_{\max} \times \left[\frac{V_{in_{\min}}}{V_{in_{\max}}} \right] = 0.266 \tag{3}$$

The input flat topped pulsed current is calculated by Equation (4).

$$I_{pdf} = \frac{P_{out}}{V_{in_{\min}} \times \eta \times D_{\max}} = 13.77\,Amp \tag{4}$$

The average input current is given by Equation (5).

$$I_{ave} = \frac{P_{out}}{\eta \times V_{in_{\min}}} = 5.51Amp \tag{5}$$

The output filter section consists of an inductor in series for current smoothening and capacitor in parallel to decrease the output ripple voltage. The inductor value is designed by suitable output inductor current ripple and is calculated by Equation (6).

$$\text{Inductor L} = \frac{V_{out1} \times (1 - D_{\min}) \times T_S}{\Delta iL} = 7.097\mu H \quad \text{for 33\% current ripple} \tag{6}$$

where where I_{out1} is considered to be 130% of output current for the safer operation of the circuit. The output filter capacitor is calculated by assuming suitable output voltage ripple and is given by Equation (7).

$$\text{Capacitor C} = \frac{I_{out1} K_1}{8 F_{sw} \Delta v_1} = 178\mu F \quad \text{for 2\% voltage ripple} \tag{7}$$

where I_{out1} is considered to be 130% of output voltage for the safer operation of the circuit, K_1 is the ripple factor i.e. 0.25. The filter capacitor connected at the output side in the hardware implementation should be five times more than the calculated value is connected which will decrease the total ESR value and reduces the maximum peak to peak ripple voltage.

5.2 Design of transformer (McLyman,1993)

The initial design of the transformer is done by calculating the area product required by the magnetic core for the designed converter specification. The area product for the forward converter is given by Equation (8).

$$A_p = \frac{\sqrt{D_{\max}} \times P_{out} (1 + \frac{1}{Efficiency})}{K_W J \times 10^{-6} B_m F_{SW}} = 3.979 \times 10^3 \text{ mm}^4 \tag{8}$$

where K_w: Window Utilization Factor = 0.4, J: Current Density = 6 Amp/mm^2, B_m: Flux Density = 0.12 Tesla and P_{out}: Output Power = 92.6 Watts

The selected core should have an area product greater than the calculated area product value. The core that is selected is 0R43019UG, material: R, AL: 6680nH/1000T. The turns ratio for the Output - □ of the transformer is calculated by using the output voltage gain equation including the diode drop at the output side and this is given by Equation (9).

$$T_{ration1} = \frac{N_{s1}}{N_p} = \frac{V_{out1} - V_D}{N_p} = 1.119 \tag{9}$$

where V_D = 0.68V is the diode drop voltage .

The primary turns are calculated using Faraday's law as Equation (10).

$$N_p = \frac{V_{in_{\min}} \times D_{\max}}{B_m A_C \times 10^{-6} F_{SW}} = 2.88 \text{ Turns} \tag{10}$$

where A_c = 136 mm^2; N_p = 2.801 Turns considered as Np = 5 Turns;

The secondary turns are calculated by using the turns ratio and primary turns calculated above using the relation in Equation (11).

$$\text{Secondary turns} = N_p \times T_{ratio1} = 5.59 = 7 \text{ Turns} \quad (11)$$

The primary and secondary turns is wounded to the core by selecting suitable number of copper strands of 28AWG wire to sufficiently carry primary and secondary current. The designed values of the proposed converter are shown in Table 2 (McLyman, 1993). The other design values for Output-□ remain to be same as Output-□ as shown in Table 2.

Table 2. Designed values of the proposed converter

Output-I	**5.3V/12A**
Primary winding inductance L1	167uH
Secondary winding inductance L2	327uH
Magnetizing Inductance L4	284uH
Output Inductance L3	7uH
Output capacitance C1	178uF
Load R1	0.48ohm
Output-□	**5.4V/4.5A**
Secondary winding inductance L5	327uH
Output Inductance L6	19.28uH
Output capacitance C2	66.78uF

6. Voltage feed forward Control

One of the common techniques to control the duty cycle of the switch is Voltage feedback technique. But this technique is found to be dynamically slow and also results in poor line regulation (Bhat et al., 2016). This can be overcome by the use of input voltage feed forward control. The block diagram of the voltage feed forward control circuit for the converter is shown in Figure 4.

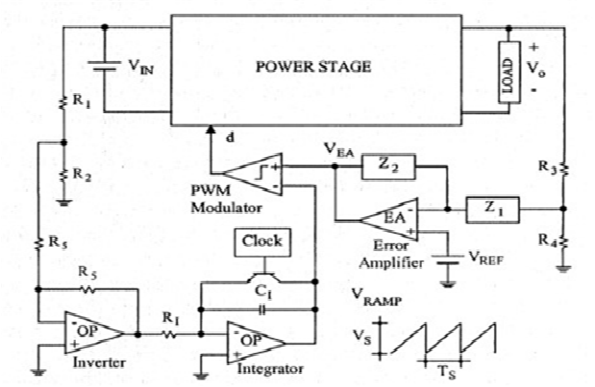

Figure 4. Block diagram of voltage feed forward control

The design details and its operation can be described by following equations (Bhat et al., 2016). In this approach, a ramp whose slope varies in proportion with the input voltage variation is utilized at the PWM modulator input instead of a fixed slope saw tooth ramp (Equations (12) and (13)).

$$V_s = \left(\frac{V_{in}}{K}\right) \quad (12)$$

$$D = \left(\frac{T_{on}}{T}\right) = \frac{V_C}{V_S} = \frac{KV_C}{V_{in}} \quad (13)$$

where D: Duty ratio; K: constant: V_{in}: Input voltage; V_S: Peak-Peak Saw Tooth Voltage; V_C: Control Voltage

7. Over current protection (OCP)

Protection circuits are the crucial part of the power supply unit. The schematic of the output over current protection circuit for the converter is shown in Figure 5.

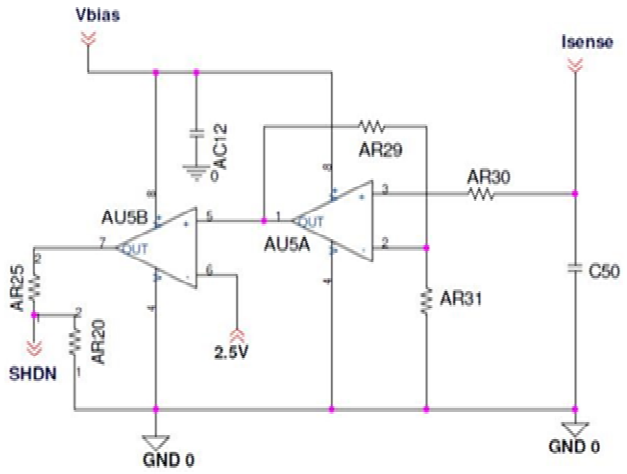

Figure 5. Over current protection circuit

The schematic of the output over current protection circuit is shown in Figure 5. The ramp current I_{sense} flows through a resistor to produce a ramp voltage. The signal strength is very low and hence it is amplified with an op-amp AU5A, this amplified signal is compared with 2.5V that is always maintained at the inverting terminal of AU5B. When the current exceeds 125% of the rated secondary current the output of AU5A goes beyond 2.5V. Hence the output of AU5B goes HIGH. This HIGH signal will be sent to the shutdown pin of the PWM IC (SHDN) as shown in Figure 5. Hence the converter shuts down and thus the converter is protected against overcurrent.

8. Simulation results

The simulation model developed using LT spice for proposed converter is shown in Figure 6. The simulation results obtained are presented. In the simulation, Output-□ and Output-□ are obtained by varying the input from 24V to 36V with Mag-amp as post regulator on the secondary side as shown in Figure 6. Output-□□ is derived from a Low dropout regulator as post regulator shown in Figure 13. Linear regulator is used to drop the raw voltage across the secondary of the transformer from 5.4V to -5V where 0.4V is dropped due to LDO. The output current of the third output (Output-III) is 0.6A which is very small and hence LDO is used as post regulator (Bhat et al., 2016). The output results are shown in Figure 7 to Figure 16.

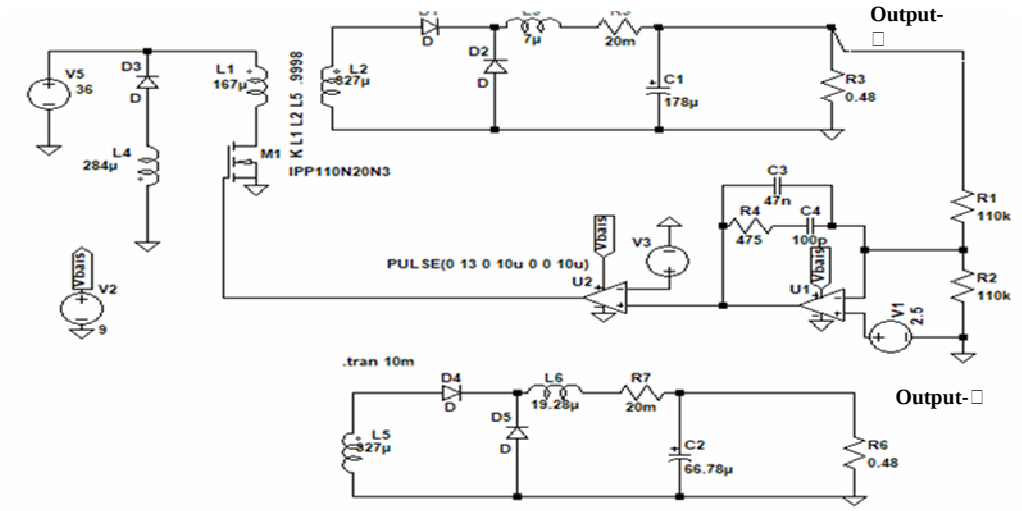

Figure 6. Closed loop Forward converter with multiple output

Figure 7 shows Output-□, which is obtained as 5.3V with an input voltage of 24V.

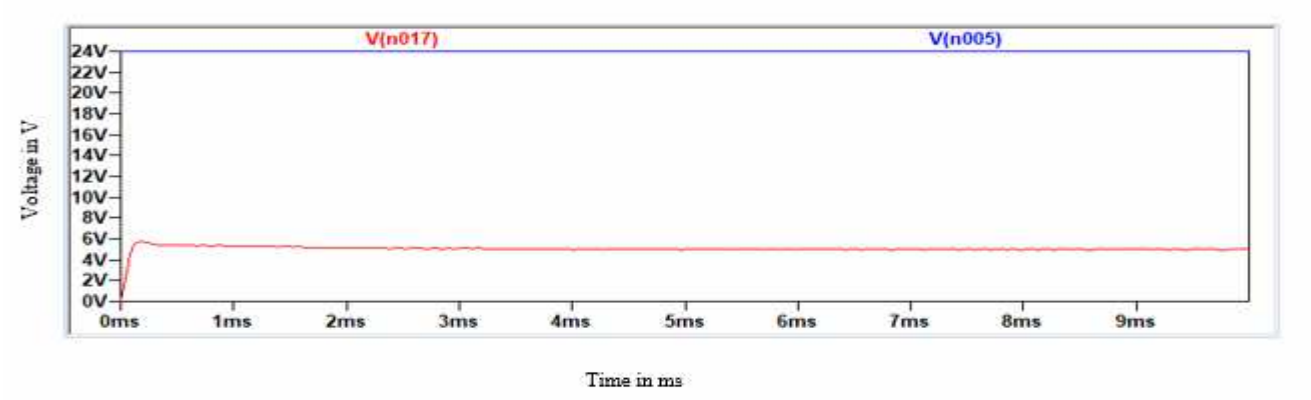

Figure 7. 5.3V output with 24V input

Figure 8 shows Output-□, which is obtained as 5.3V with an input voltage of 28V.

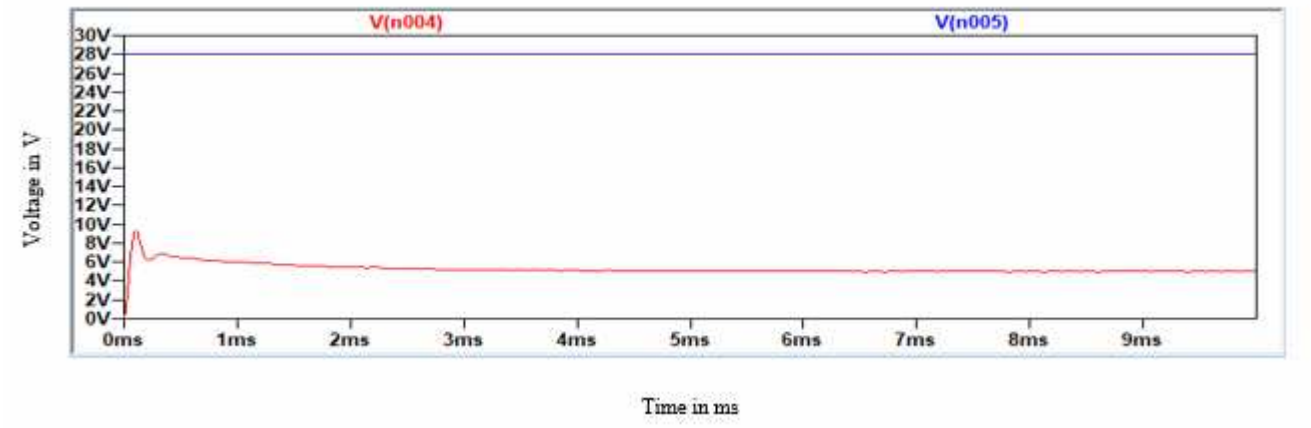

Figure 8. 5.3V output with 28V input

Figure 9 shows Output-□, which is obtained as 5.3V with an input voltage of 36V.

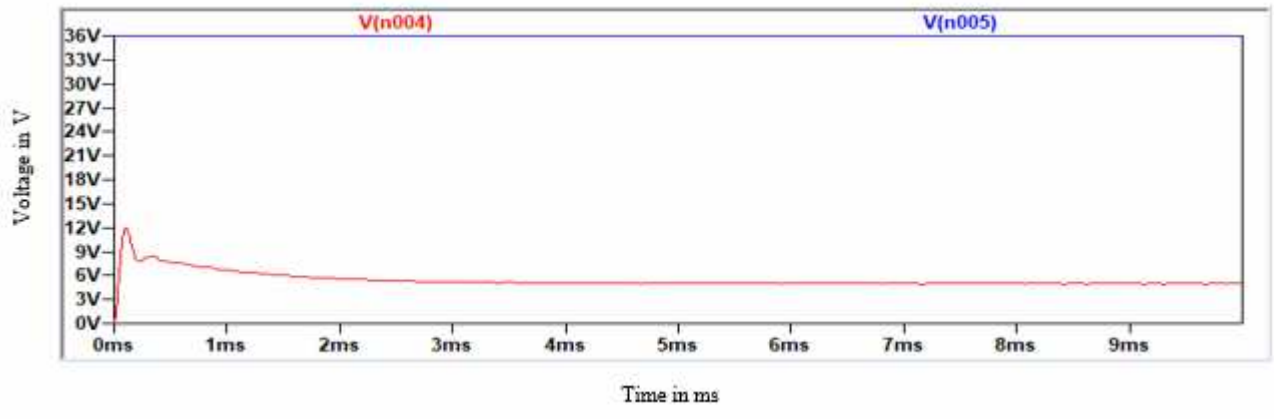

Figure 9. 5.3V output with 36V input

It is observed that, with variation of input voltage as 24V, 28V and 36V, the output remains constant at 5.3V for Output I.

Figure 10 shows Output-□, which is obtained as 5.4V with an input voltage of 24V.

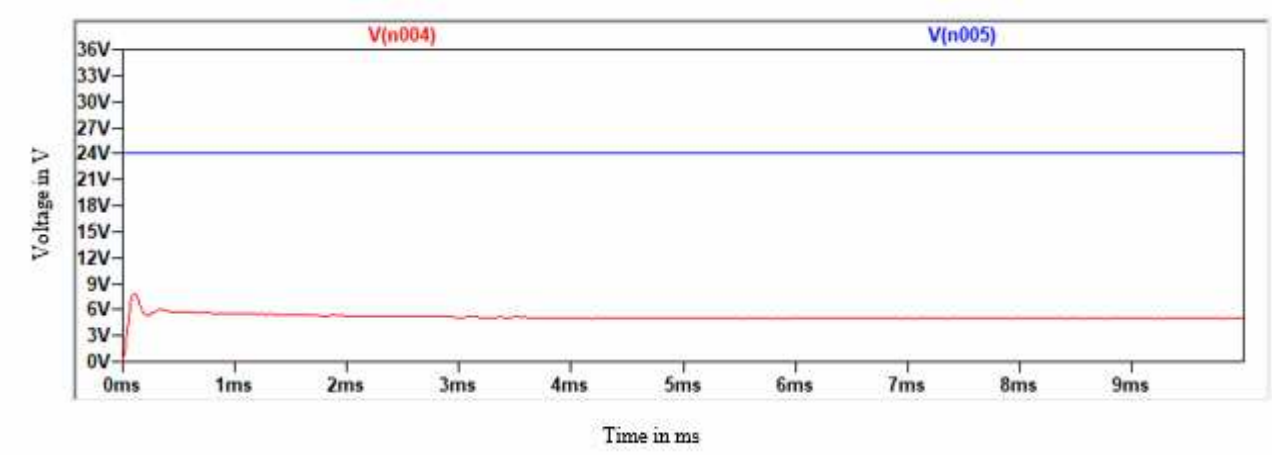

Figure 10. 5.4V output with 24V input

Figure 11shows Output-□, which is obtained as 5.4V with an input voltage of 28V.

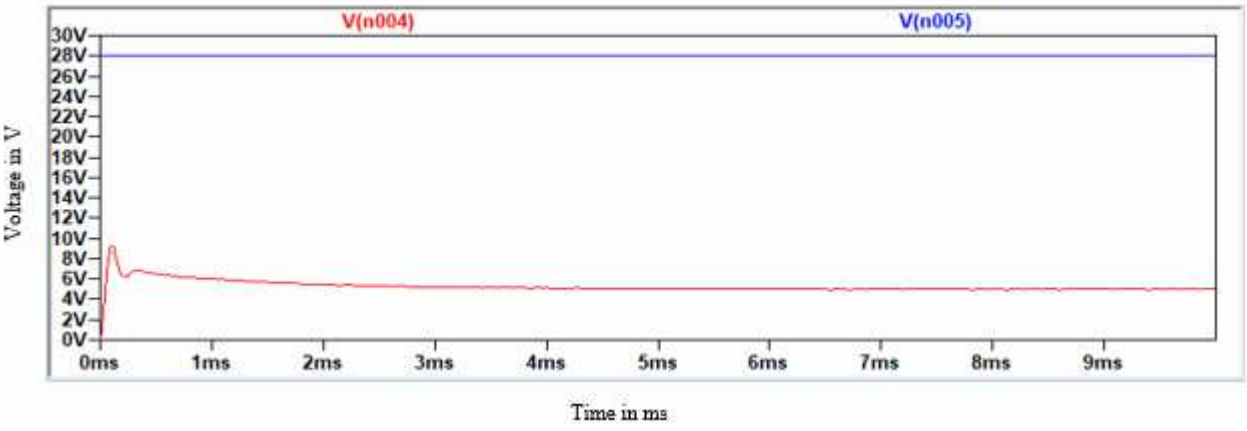

Figure 11. 5.4V output with 28V input

Figure 12 shows Output-□, which is obtained as 5.4V with an input voltage of 36V.

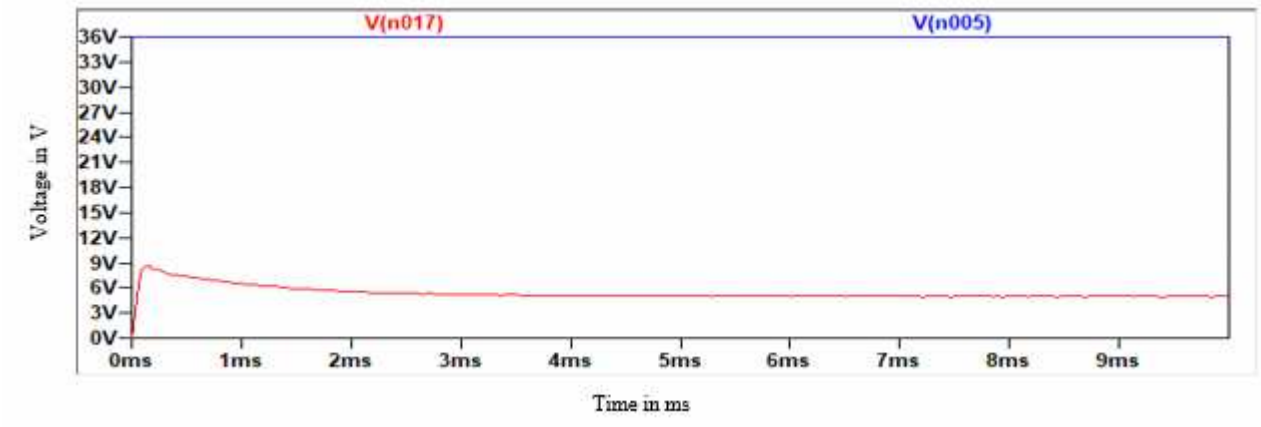

Figure 12. 5.4V output with 36V input

It is observed that, with variation of input voltage as 24V, 28V and 36V, the output remains constant at 5.4V for Output II.

Output-□ for the Forward converter is obtained by using LDO regulator as post regulator on the secondary side (Figure 13). The -ve value is obtained by reversing the voltage measurement terminals on the output side.

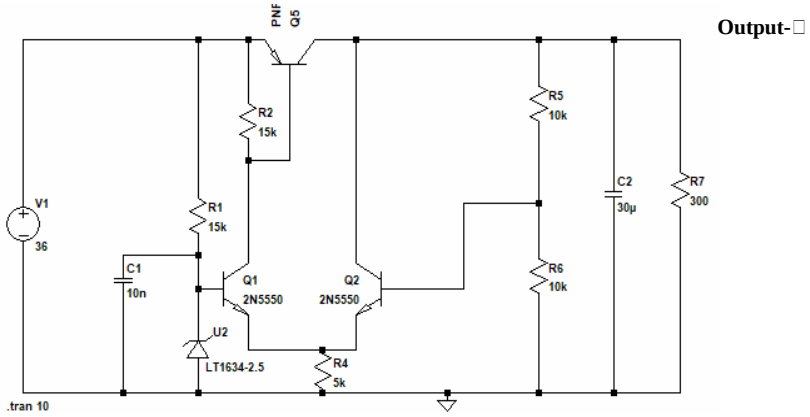

Figure 13. LDO regulator

Figure 14 shows Output-□, which is obtained as -5V with an input voltage of 24V.

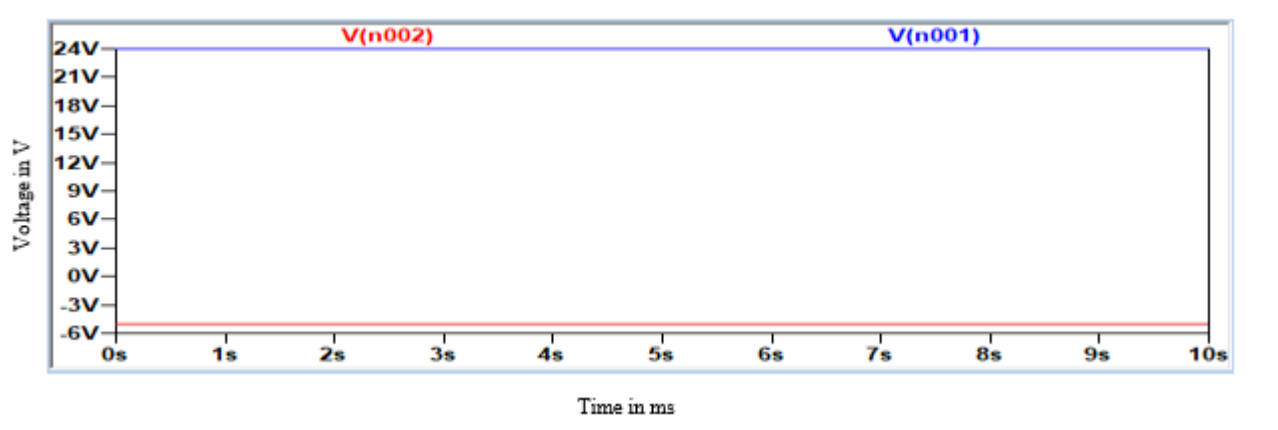

Figure 14. -5V output with 24V input

Figure 15 shows Output-□, which is obtained as -5Vwith an input voltage of 28V.

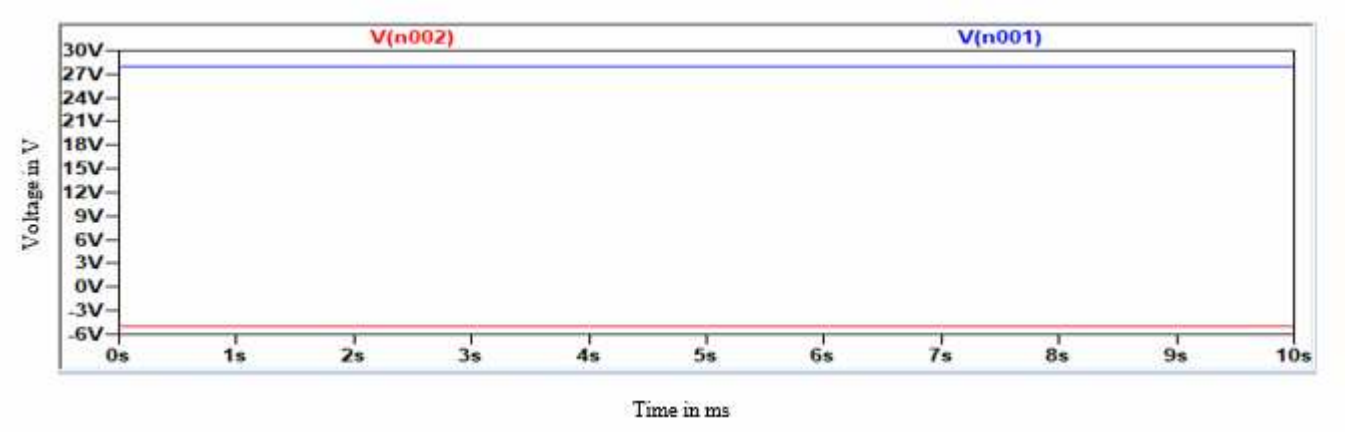

Figure 15. -5V output with 28V input

Figure 16 shows Output-□, which is obtained as -5V with an input voltage of 36V.

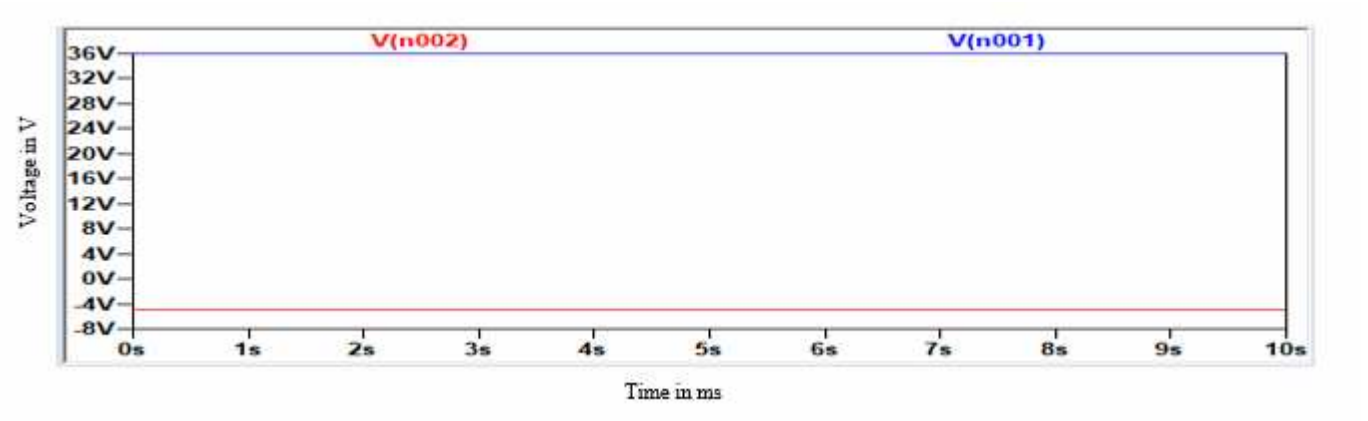

Figure 16. -5Voutput with 36V input

From the results obtained, it is observed that, with variation of input voltage as 24V, 28V and 36V, the output remains constant at -5 V for Output III.

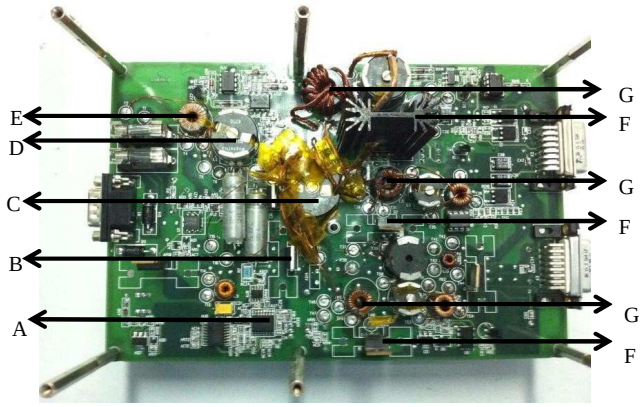

Figure 17. Top view

Figure 18. Rear view

A - PWM IC; B – MOSFET; C – Transformer; D - Differential mode inductor; E - Common mode inductor; F - Mag-amps; G - Output diode; H – LDO

9. Experimental Results

The hardware implementation of multiple output Forward converter is shown in Figures 17 and 18. The various components of hardware implemented are as listed. Following results are obtained from the hardware implementation of the circuit and are shown in Table 3. An ideal value of 0% is obtained as % regulation in some of the cases, as accuracy for the application under consideration is considered to be satisfactory upto two decimal points. The percentage load regulation for Output-□ is calculated for different input voltages and different levels of loads and tabulated in Table 3.

Table 3. Output voltages at +5.3V output at various load conditions with % line and load regulation

Vin (V)	Output Voltage (V)			% Load Regulation
	Minimum Load	Nominal Load	Maximum Load	
24	5.28	5.27	5.25	0.19
28	5.28	5.27	5.25	0.18
36	5.28	5.27	5.25	-0.19
% Line Regulation	0	0	0	

It is observed that, % load regulation is in the range -0.19 to +0.19 and %line regulation is an ideal value of 0%. These are well within the specifications of line regulation which should be less than ± 1% and load regulation which should be less than ± 2%. The percentage load regulation for Output-□ is calculated for different input voltages and different levels of loads and tabulated in Table 4.

Table 4. Output voltages at +5.4V output at various load conditions with % line and load regulation

Vin (V)	Output Voltage (V)			% Load Regulation
	Minimum Load	Nominal Load	Maximum Load	
24	5.47	5.46	5.45	0.18
28	5.47	5.46	5.45	0.18
36	5.47	5.46	5.45	-0.18
% Line Regulation	0	0	0	

It is observed that % load regulation is in the range -0.18 to +0.18 and %line regulation is an ideal value of 0%. These are well within the specifications of line regulation less than 1% and load regulation less than 2%. The percentage load regulation for output-□ is calculated for different input voltages and different levels of loads and tabulated in Table 5.

Table 5. Output voltages at -5V output at various load conditions with line and % load regulation

Vin (V)	Output Voltage (V)			% Load Regulation
	Minimum Load	Nominal Load	Maximum Load	
24	-5.02	-5.02	-5.004	0.318
28	-5.02	-5.01	-5.01	0.199
36	-5.02	-5.01	-5.01	0.199
% Line Regulation	0	-0.199	+0.199	

It is observed that %load regulation is in the range of 0.199 to 0.318 and %line regulation is in the range of -0.19 to +0.19. These are well within the specifications of line regulation less than ± 1% and load regulation less than ± 2%. The percentage cross regulation of the three outputs is calculated for different input voltages and tabulated in Table 6.

Table 6. Cross regulation obtained at various conditions with different input voltage condition

Vin (V)	Output Voltage (V)		
	5.3V/12A	5.4V/4.5A	-5V/0.7A
24	-0.189	0	-0.199
28	0	0	0
36	-0.189	0	0.199

From the experimental results it is observed that maximum cross regulation is 0.19%. Thus the converter meets the specifications of cross regulation less than ± 2% for all outputs. Figure 19 to Figure 21 shows the gate voltage, stress across the main switch and voltage across the mag-amp coil. The Y- axis represents the voltage in V and X-axis represents the time in ms.

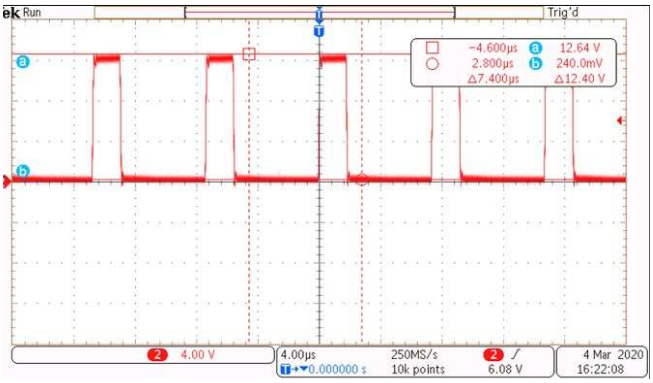

Figure 19. Gate Voltage (20V/div) of the MOSFET at 36V input and maximum load. (Time scale 2gs/div).

The gate voltage of the MOSFET (V_{GS}) is as shown in the Figure 19 and is found to be equal to 12V. Hence the minimum gate voltage of 12V required to switch on the MOSFET is obtained.

The voltage stress across the MOSFET (V_{DS}) is shown in the Figure 20, and is found to be equal to 128V

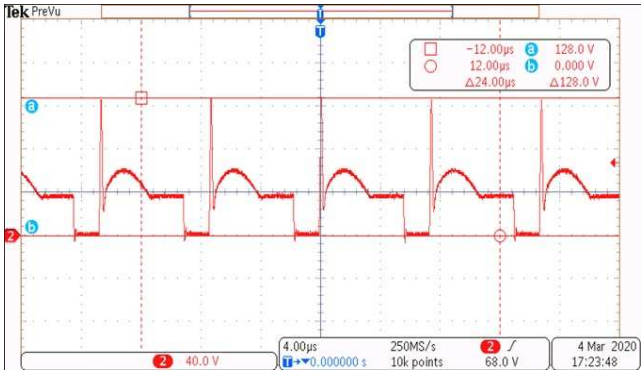

Figure 20. Voltage stress (20V/div) across the MOSFET at 36V input and maximum load. (Time scale 2gs/div)

The $\mathbf{V_{DS}}$ of the selected MOSFET is 200V, hence the observed voltage stress is 128V and is well within in the specifications of the MOSFET.

The voltage across the mag-amp coil is shown in the Figure 21

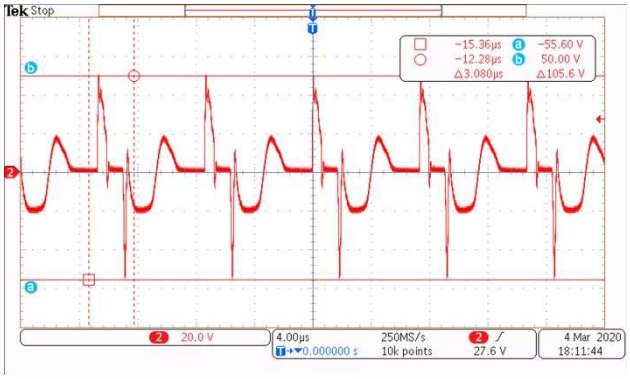

Figure 21. Voltage (20V/div) across the mag-amp coil at 36V input and maximum load (Time scale 2gs/div)

The voltage across the mag-amp coil at maximum voltage of 36V with maximum load is observed to be 105.6 V.

10. Conclusion

This paper presents the design and implementation of a three output Forward Converter with Mag-amp and LDO as post regulators for Space Application. Design details of the converter and regulators are discussed in detail. The voltage feed forward control technique is applied to improve the line regulation of the converter. Simulation and hardware implementation of the converter is carried out. From the results obtained, it is found that, the performance of the Mag- amp and LDO regulators is found to be satisfactory in regulating individual outputs and achieving good load and cross regulation that are well within the required specifications. It can also be concluded that, the implementation of voltage feed forward technique has improved the line regulation.

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