Design and Implementation of Three-Phase Voltage Flicker Calculation Based on FPGA

Shu-Chen Wang, Yu-Jen Chen, and Chi-Jui Wu

Abstract—This study proposes a method for computing equivalent three-phase voltage flicker using field-programmable gate array (FPGA)-based integrated circuit (IC) to measure the instantaneous voltage vectors. The very high-speed integrated-circuit hardware description language (VHDL) is used to design scheme, which provides high flexibility and technology independence. The instantaneous voltage vector module, management module, and quantification modules are developed to simulate the entire system. Some novel IP (intellectual property) cores, such as CORDIC and FFT, are introduced and adopted. Then the chip based on these IP cores is designed for voltage flicker calculation and is realized by using a signal FPGA (XC3S1500), which can be adopted as a coprocessor with a general-purpose microprocessor. Simulation results of waveforms and field-measured waveforms with voltage flicker disturbances are presented to show the validity of the flicker components obtained in designed IC.

Keywords—Electric power quality, voltage flicker, Field programmable gate array, instantaneous voltage vector, fast Fourier transform.

I. INTRODUCTION

Voltage flicker means the fluctuations in the envelope of the 50/60 Hz supply voltage that is frequently caused by heavy fluctuating loads [1]-[3]. It may be generally divided into cyclic flicker and stochastic flicker. The former is repetitive and caused by periodic operation loads such as compressors or arc welders. The latter flicker refers to occasional behaviors and is caused by arc furnaces or ac choppers. Several definitions and calculation methods had been proposed and developed [4]-[6]. These methods include the short-term severity P_{st} and the 10-Hz equivalent voltage flicker value ΔV_{10}. The P_{st} is the IEC standard and was established by the Union for Electro-heat (UIE). The Central Research Institute of the Electric Power Industry (CRIEPI) of Japan proposed using the ΔV_{10} as the standard for assessing voltage flicker. The Taiwan Power Company (TPC) also uses ΔV_{10}, and then it is considered in this study. The frequencies of flicker components between 0.1 Hz to 30 Hz are extremely important owing to being visually irritating. Numerous reports have established that a small voltage flicker, ranging from 0.3% to 0.5% in the frequency range of 6-10 Hz could cause visible incandescent flickering and human discomfort [7], [8]. Persistent voltage flicker problems have long existed in several distribution areas of TPC [9], [10]. Field measurements are always required.

The usage and performance of FPGA has risen significantly in recent years for its reconfiguration and flexibility. The FPGA has been applied to analyzing and controlling a power system [11], [12]. The major difference between FPGA and DSP-based solutions is that FPGA enables simultaneous execution of all control subroutines, which allows high performance and novel control methods [13]. While conventional designs are based on functions, FPGA is based on the reuse of IP or the function assembly. When a large system is constructed from a number of macro-modules, IP cores can be used to represent those modules. Several particular functional IP cores such as CORDIC and FFT cores could be developed. VHDL was also employed to model a digital control system at many levels [14]. VHDL can be considered as a combination of sequential, concurrent, net-list, timing specification, and waveform generation languages. It utilizes the top/down design methodology and can be used to model a complete digital electronic system. The design benefits include easy error correction and technology independence. The same algorithm can be synthesized into any other FPGA.

This investigation develops an FPGA-based control IC for computing the equivalent three-phase voltage flicker. Usually each phase of a three-phase circuit has different flicker components. This design approach gives the representative equivalent values of the three phases. The voltage waveforms of three phases are sampled at a specified sampling frequency and stored in a ROM. The instantaneous voltage vector module is adopted to determine the real and imaginary magnitudes of the instantaneous voltage vectors. A 1024-point FFT core is applied to obtain the real and imaginary magnitudes of the voltage flicker components. Finally, the flicker component magnitudes, in the range of 0~30 Hz, are calculated by the quantification module. The study results show that the proposed method gives a precise three-voltage calculation scheme. Each phase of three-phase circuits may have different

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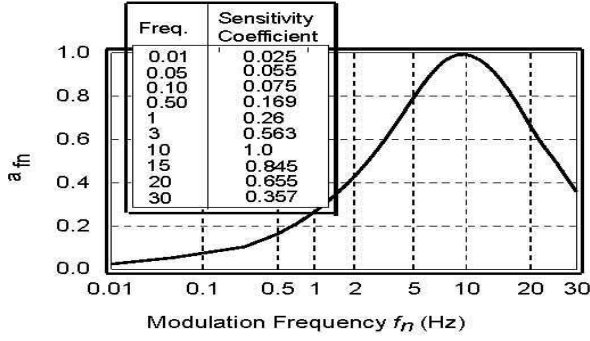
flicker components.

Fig. 1. Flicker sensitivity coefficient curve.

II. DEFINITION OF VOLTAGE FLICKER

Voltage flicker means the fluctuation in the amplitude of voltage waveforms typically at a frequency lower than the power frequency. The behaviors of voltage flicker can be either cyclic or stochastic. However, in a short period, the voltage flicker can be appropriately modeled as an amplitude modulation waveform.

Let ΔV_{fn} denote the degree of difference between the maximum and minimum amplitude at the modulation frequency f_n for a voltage waveform with the RMS value V_{rms}. Consequently, the flicker component is

$$v_f(t) = \frac{1}{2}\Delta V_{fn}\cos(2\pi f_n t)\sqrt{2}V_{rms}\cos(2\pi f_{sys}t) \tag{1}$$

The total voltage waveform with several flicker components can be expressed as

$$v(t) = \sqrt{2}V_{rms}\left[1 + \frac{1}{2}\sum_n \Delta V_{fn}\cos(2\pi f_n t)\right]\cos(2\pi f_{sys}t) \tag{2}$$

Generally, the components of modulation frequencies in the range 0.25~30 Hz must be considered for specifying the limitations on voltage flicker. The voltage fluctuation is defined as

$$\Delta V = \sqrt{\sum(\Delta V_{fn})^2} \tag{3}$$

Moreover, the 10-Hz equivalent voltage flicker value is define d as,

$$\Delta V_{10} = \sqrt{\sum(a_{fn}\Delta V_{fn})^2} \tag{4}$$

Where a_{fn} denotes the flicker sensitivity coefficient corresponding to the modulation frequency f_n component. Figure 1 plots the distribution curve of the sensitivity coefficients, which snows the sensitivity of the human eye-brain system to illumination flicker. The frequency to which it is most sensitive is 10 Hz, at which the visual sensitivity coefficient is one. When the frequency is below 0.25 Hz or over 30 Hz, the sensitivity coefficients are so small that they can be ignored. In the TPC, the limit of ΔV_{10} is set as 0.45%. This value was determined through various filed experiments.

III. THREE-PHASE VOLTAGE FLICKER CALCULATION METHOD

The instantaneous voltage vectors can be used to obtain the equivalent three-phase voltage envelopes. For a three-phase circuit, the magnitude of the instantaneous voltage vector is defined as

$$|v_i(t)| = \left|\frac{\sqrt{2}}{3}[v_R(t) + v_S(t)(\frac{-1}{2} + j\frac{\sqrt{3}}{2}) + v_T(t)(\frac{-1}{2} - j\frac{\sqrt{3}}{2})]\right| \tag{5}$$

Where v_R, v_S and v_T are instantaneous voltages of the corresponding phases. The real and imaginary magnitudes of the instantaneous voltage vector are respectively given by

$$\text{Re}(v_i(t)) = \frac{\sqrt{2}}{3}[v_R(t) - \frac{1}{2}v_S(t) - \frac{1}{2}v_T(t)] \tag{6}$$

$$\text{Im}(v_i(t)) = \frac{1}{\sqrt{6}}[v_S(t) - v_T(t)] \tag{7}$$

Usually each phase could have different flicker components. The equivalent three-phase flicker components can be obtained from $v_i(t)$.

In order to explain the method to obtain voltage flicker components from the instantaneous voltage vectors, let phase-R have a single voltage flicker component and the other two phases be purely sinusoidal.

$$v_R(t) = \sqrt{2}V_{rms}\left[1 + \frac{1}{2}\Delta V_{fn}\cos(2\pi f_n t)\right]\cos(2\pi f_{sys}t) \tag{8}$$

$$v_S(t) = \sqrt{2}V_{rms}\cos(2\pi f_{sys}t - \frac{2\pi}{3}) \tag{9}$$

$$v_T(t) = \sqrt{2}V_{rms}\cos(2\pi f_{sys}t + \frac{2\pi}{3}) \tag{10}$$

From (5), (8), (9), and (10), the magnitude of instantaneous voltage vector is given by

$$|v_i(t)| = \frac{2V_{rms}}{3}\left| \begin{array}{l} \left[1 + \frac{1}{2}\Delta V_{fn}\cos(2\pi f_n t)\right](\frac{e^{j2\pi f_{sys}t} + e^{-j2\pi f_{sys}t}}{2}) \\ +[\frac{e^{j(2\pi f_{sys}t - \frac{2}{3}\pi)} + e^{-j(2\pi f_{sys}t - \frac{2}{3}\pi)}}{2}](\frac{-1}{2} + j\frac{\sqrt{3}}{2}) \\ +[\frac{e^{j(2\pi f_{sys}t + \frac{2}{3}\pi)} + e^{-j(2\pi f_{sys}t + \frac{2}{3}\pi)}}{2}](\frac{-1}{2} - j\frac{\sqrt{3}}{2}) \end{array} \right| \tag{11}$$

After some algebraic manipulations, it can be obtained that

$$|v_i(t)| \cong V_{rms}[1 + \frac{1}{3}\frac{\Delta V_{fn}}{2}\cos(2\pi f_n t) + \frac{1}{3}\frac{\Delta V_{fn}}{2}\cos(2\pi f_n t)\cos(2\pi f_{sys}t)] \tag{12}$$

The frequency spectrum of (12) has four components. The first term is the DC component. The second contains the useful

information to obtain the corresponding flicker component. The last term represents two higher frequency components, and

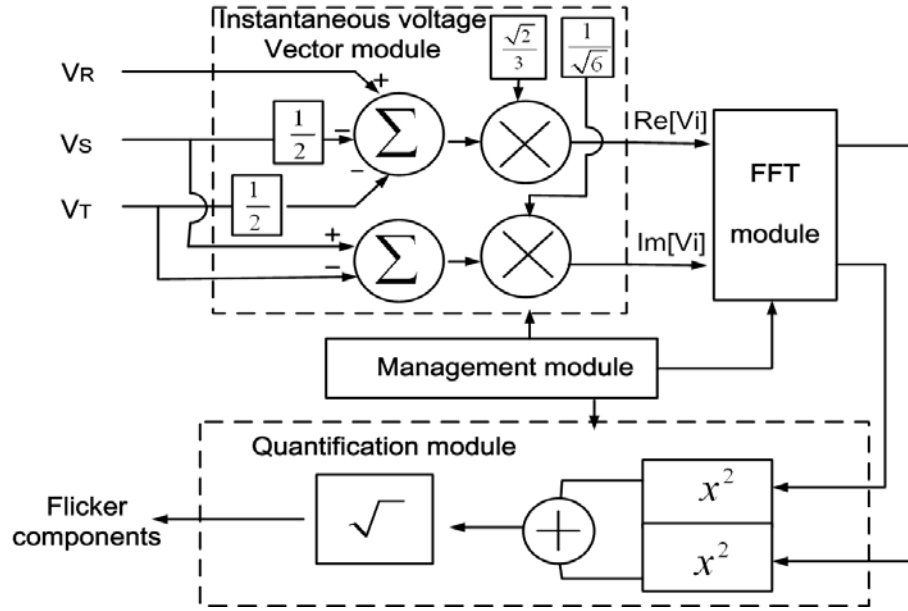could be filtered out since $f_{sys} \pm f_n$ is much larger than f_n.

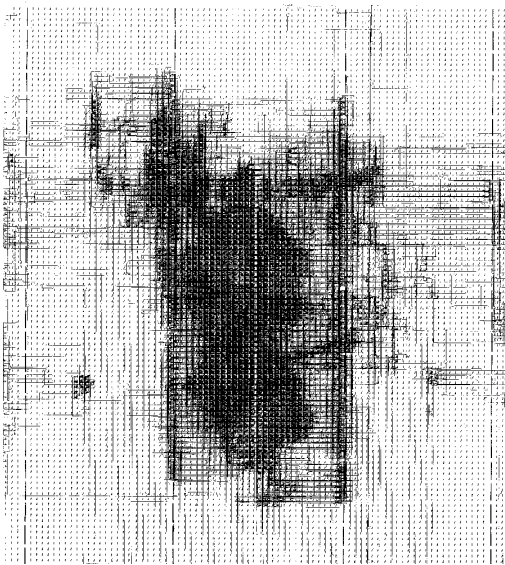Fig. 2. Functional module diagram of the designed IC
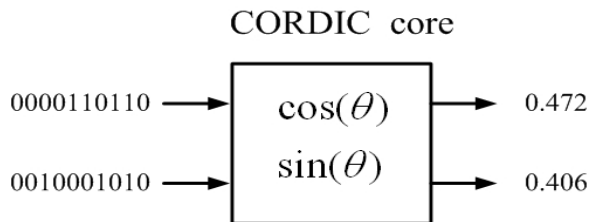

Fig. 3. FPGA routing diagram

Fig. 5. Structure diagram of radix-4 FFT core
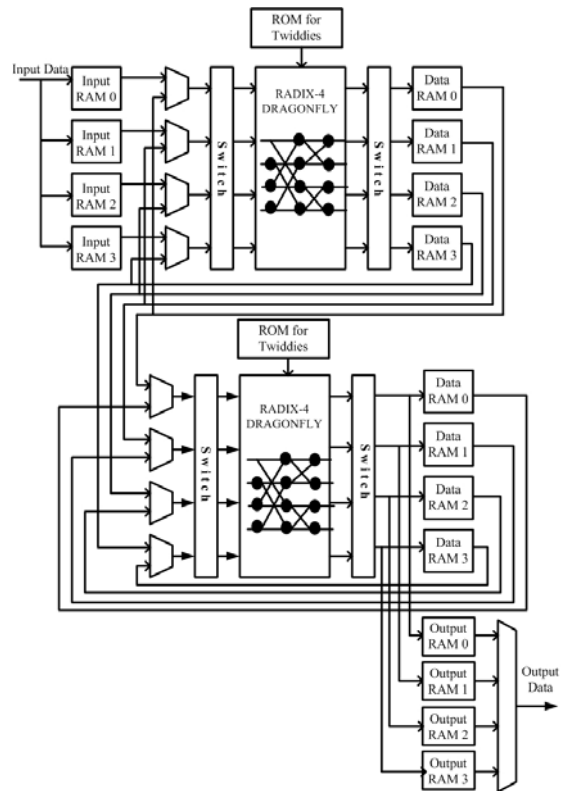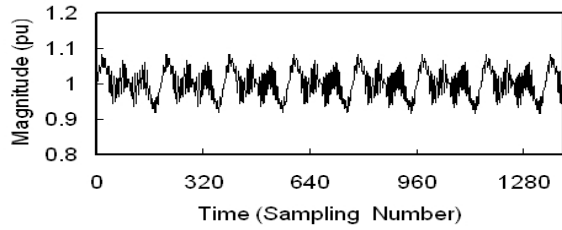

Fig. 4. CORDIC core structure

Fig. 6. Instantaneous voltage vector magnitudes of Case 12

TABLE I
FLICKER COMPONENT CALCULATION RESULTS OF GIVEN CASES

	Given flicker components ΔV_{fn} (pu/Hz)	Calculated flicker components ΔV_{fn} (pu/Hz)	
		Matlab	FPGA
CASE 1	v_R : 0.1/10 v_S : --- v_T : ---	0.0333/10	0.0334/10
CASE 2	v_R : 0.1/5,0.1/10 v_S : --- v_T : ---	0.0333/5 0.0333/10	0.0335/5 0.0335/10
CASE 3	v_R : 0.15/5,0.1/10 v_S : --- v_T : ---	0.05/5 0.0333/10	0.05/5 0.0333/10
CASE 4	v_R : 0.1/10 v_S : 0.1/10 v_T : ---	0.0667/10	0.0667/10
CASE 5	v_R : 0.1/5 v_S : 0.1/10 v_T : ---	0.0333/5 0.0333/10	0.0335/5 0.0331/10
CASE 6	v_R : 0.1/10 v_S : 0.15/10 v_T : ---	0.0833/10	0.0833/10
CASE 7	v_R : 0.1/5 v_S : 0.15/10 v_T : ---	0.0333/5 0.05/10	0.0334/5 0.0449/10
CASE 8	v_R : 0.1/5 v_S : --- v_T : 0.1/10	0.0333/5 0.0333/10	0.0335/5 0.0331/10
CASE 9	v_R : 0.1/10 v_S : 0.1/10 v_T : 0.1/10	0.1/10	0.0993/10
CASE 10	v_R : 0.1/5 v_S : 0.1/10 v_T : 0.1/15	0.0333/5 0.0333/10 0.0333/15	0.0336/5 0.0332/10 0.0332/15
CASE 11	v_R : 0.1/10 v_S : 0.15/10 v_T : 0.2/10	0.05/10	0.0499/10
CASE 12	v_R : 0.1/5 v_S : 0.15/10 v_T : 0.2/15	0.0333/5 0.05/10 0.0667/15	0.0333/5 0.0498/10 0.0665/15

IV. DESIGN OF FPGA-BASED CALCULATION IC

The most important issue in designing the calculation IC is the choice of numerical data processing schemes. A floating-point arithmetic method has the advantage of a wide dynamic range, but its hardware realization is very complicated. A fixed-point arithmetic scheme is a more practical solution to most industrial applications with simple circuit realization. The proper numerical data scaling plays a significant role in synthesizing an integer controller. In this study, numerical variables and parameters must be transformed into approximate integers with finite word lengths. Figure 2 illustrates the functional module diagram of the designed three-phase voltage flicker calculation IC. The three-phase voltage waveforms are sampled with a specified sampling frequency and transformed to digital data, which act as the data source of the instantaneous voltage vector module. Figure 3 reveals the integrated routing diagram of calculation modules. Each module of the designed circuit is described as follows.

A. Management module

This module is a task scheduler to generate an internal clock and to coordinate works of each module, such as giving corresponding data to each block in a definite order, and recording the sequential operation events.

B. Instantaneous voltage vector module

From (6) and (7), the real and imaginary part of the instantaneous voltage vector are determined. The powers of $1/2$ are implemented using the shifter. The $\sqrt{2}/3$ and $1/\sqrt{6}$ are implemented using the generalized coordinated rotational digital computer (CORDIC) algorithm. The CORDIC core was initially developed to iteratively solve trigonometric equations [15], and later generalized to solve a broader range of equations [16], including the hyperbolic and square root equations. The CORDIC algorithm introduces a scale factor to the results, and provides the option of automatically compensating for scale factor. If the *Sin* and *Cos* functional configuration is selected, the unit vector is rotated, using the CORDIC algorithm and the input angle, θ , to generate the output vector $\cos(\theta)$ and $\sin(\theta)$. Figure 4 illustrates the CORDIC structure. The CORDIC core generates, respectively, 0.472 and 0.406, which are close to $\sqrt{2}/3$ and $1/\sqrt{6}$. The errors are about 0.13% and 0.55%, respectively. They are acceptable in this application.

C. FFT module

The Fast Fourier Transform (FFT) is a computationally efficient algorithm for deriving the Discrete Fourier Transform (DFT). The FFT core developed by Xilinx can compute an *N*-point forward DFT or inverse DFT (IDFT) where $N = 2^m$, $m = 4 \sim 14$. The FFT core applies the Cooley-Tukey decimation-in-time (DIT) algorithm to determine the DFT. It utilizes two radix-4 butterfly-processing engines, and offers continuous data processing using input memory, output memory, and intermediate memory banks. Figure 5 illustrates the structure of a radix-4 FFT. When using radix-4, the FFT

consists of $\log_4(N)$ stages, with each stage including $N/4$ radix-4 butterflies. This core can simultaneously perform transform computations on the current data frame, load the input data for the next data frame, and unload the results of the previous frame of data. All memory is on-chip using either block RAM or distributed RAM. The radix-4 1024-point DIF method was adopted as process 2-channel data. From the results of FFT, the 2nd to 30th flicker components can be obtained.

TABLE II
DEVICE UTILIZATION OF XC3S1500

	Used	Available	Usage ratio
Silices	4441	13312	33%
Silices Flip Flops	5913	26624	22%
4 Input LUTs	6593	26624	24%
Iuput/Output Blocks (IOB)	258	487	52%
BRAMs	27	32	84%
MULT18x18s	26	32	81%
GCLKs	1	8	12%

TABLE III
THREE-PHASE VOLTAGE FLICKER CALCULATION RESULT OF DC
FURNACE MEASUREMENT DATA

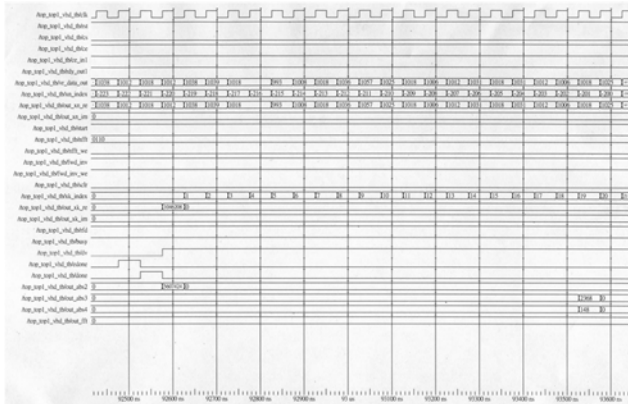|	Calculation Method	
	Matlab	FPGA
ΔV (pu)	0.0262	0.0265
ΔV_{10} (pu)	0.0203	0.0205

Fig. 7. Timing simulation of the calculation IC

D. *Quantification module*

The FFT module outputs 16-bit frequency domain data samples, where both the real and imaginary components are fed into this module. That picks out the complex pair corresponding to a target frequency. The square root operation is also implemented using the simplified CORDIC algorithm. The flicker components are then computed.

V.   GIVEN WAVEFORM TEST

This investigation presents a novel digital circuit design methodology, in which all modules were described by using VHDL, and a synthesis tool, ISE 6.2, was adopted to map these designed codes directly onto FPGA. A design implementation software application, Modelsim, was utilized to obtain results. The logic and timing simulation softwares are (especially OR particularly) important for the design of complicated digital circuits to resolve problems during the early design stage. The Xilinx's XC3S1500 was applied to implement this design. Table I lists 12 given cases in which the equivalent
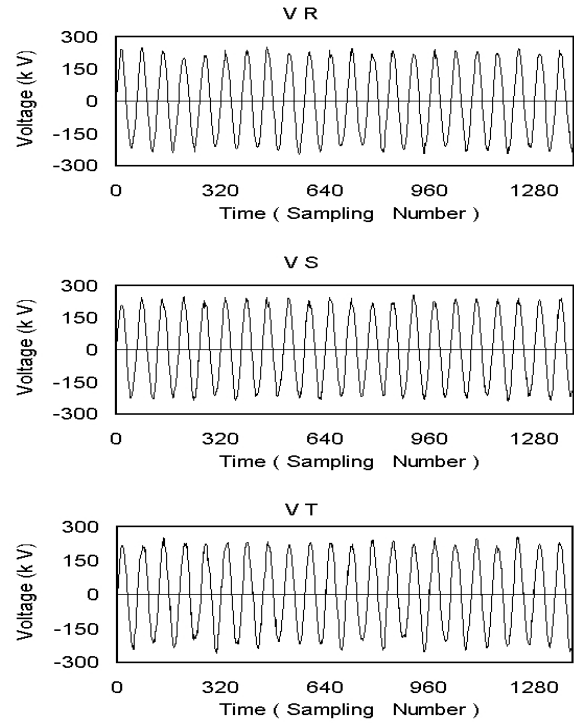

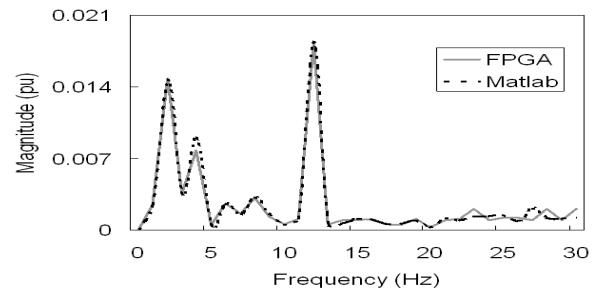Fig. 8. DC arc furnace voltage waveform

Fig. 9. Flicker components of the DC arc furnace measurement data

three-phase voltage flicker values are calculated using Matlab and FPGA methods. The flicker components obtained from FPGA are approximately equal to those obtained from Matlab.

It can be observed from Table I that if only one phase has a flicker component, the equivalent three-phase flicker will be 1/3 of the given value. And if two phases have the same flicker component, the equivalent flicker will be 2/3 of the given value. Only when all three phases have the same flicker component, the equivalent flicker will be the same value. Figure 6 shows

the instantaneous voltage vector magnitudes of Case 12. Figure 7 illustrates the timing simulation results of the develop calculation IC. Table II displays the chip resource usage. Optimizing the storage structure and FFT module can attain further performance improvement.

VI. EXPERIMENTAL TEST RESULTS

The three-phase measurement data from the 161-kV feeder of an 82-MVA DC arc furnace was adopted to confirm the design of the above methods to practical cases. Figure 8 illustrates the three-phase voltage waveforms. The sampling rate is 32 samples per power cycle. Table III presents the equivalent three-phase voltage flicker calculation results of the measurement data. Figure 9 depicts the distribution of flicker components. The major flicker components of this arc furnace locate at lower frequencies. The calculation results of flicker components using FPGA are approximately equal to these using Matlab.

VII. CONCLUSION

This study has presented an FPGA-based calculation IC for obtaining the equivalent three-phase voltage flicker values using the instantaneous voltage vectors. The design scheme has advantages of concurrent operation, small hardware requirement, and easy and fast circuit modification. Adopting VHDL provides sufficient flexibility and speed to construct the design circuits by some IP cores. All modules were designed and integrated to others. The major benefit of the proposed approach is that it executes all logics continuously and simultaneously. The simulated and experimental results confirm that the instantaneous voltage vectors are effective to obtain the three-phase voltage flicker values. The designed FPGA-based system can calculate precise flicker components. The developed scheme in this paper is a favorable choice for power quality calculation.

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